TOSHIBA CDMOS Integrated Circuit Silicon Monolithic

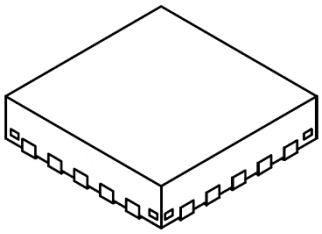
TC78B043FTG/FNG

Sine Wave PWM Drive Controller for Three-phase Brushless Motor

1. Outline

The TC78B043FTG/FNG are Sine Wave PWM drive controllers for 3-phase brushless motors.
The TC78B043FTG is encapsulated in a WQFN20 package, and the TC78B043FNG is encapsulated in a HTSSOP28 package. And, they have built-in non-volatile memory (NVM), allowing various settings according to the characteristics and usage of the motor to be written to the NVM via SPI communication.
Additionally, the NVM in the TC78B043FNG has initial settings suitable for common motors, allowing driving a motor without writing via SPI communication. Furthermore, it is equipped with four pins: FGC pin, LATYPE pin, LAOFS pin, and LA pin. The voltage settings of these pins also allow adjustments of some parameters, such as motor lead angle control.
TC78B043FTG has no four pins: FGC pin, LATYPE pin, LAOFS pin, and LA pin. The NVM has no initial settings for motor control. Therefore, to control the motor, it is necessary to write settings to the NVM via SPI communication.

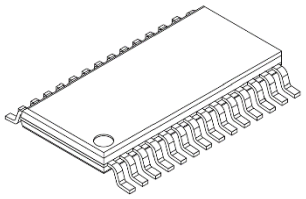
TC78B043FTG



P-WQFN20-0303-0.50-002

Weight: 0.02 g (typ.)

TC78B043FNG



P-HTSSOP28-0510-0.65-001

Weight: 0.10 g (typ.)

2. Applications

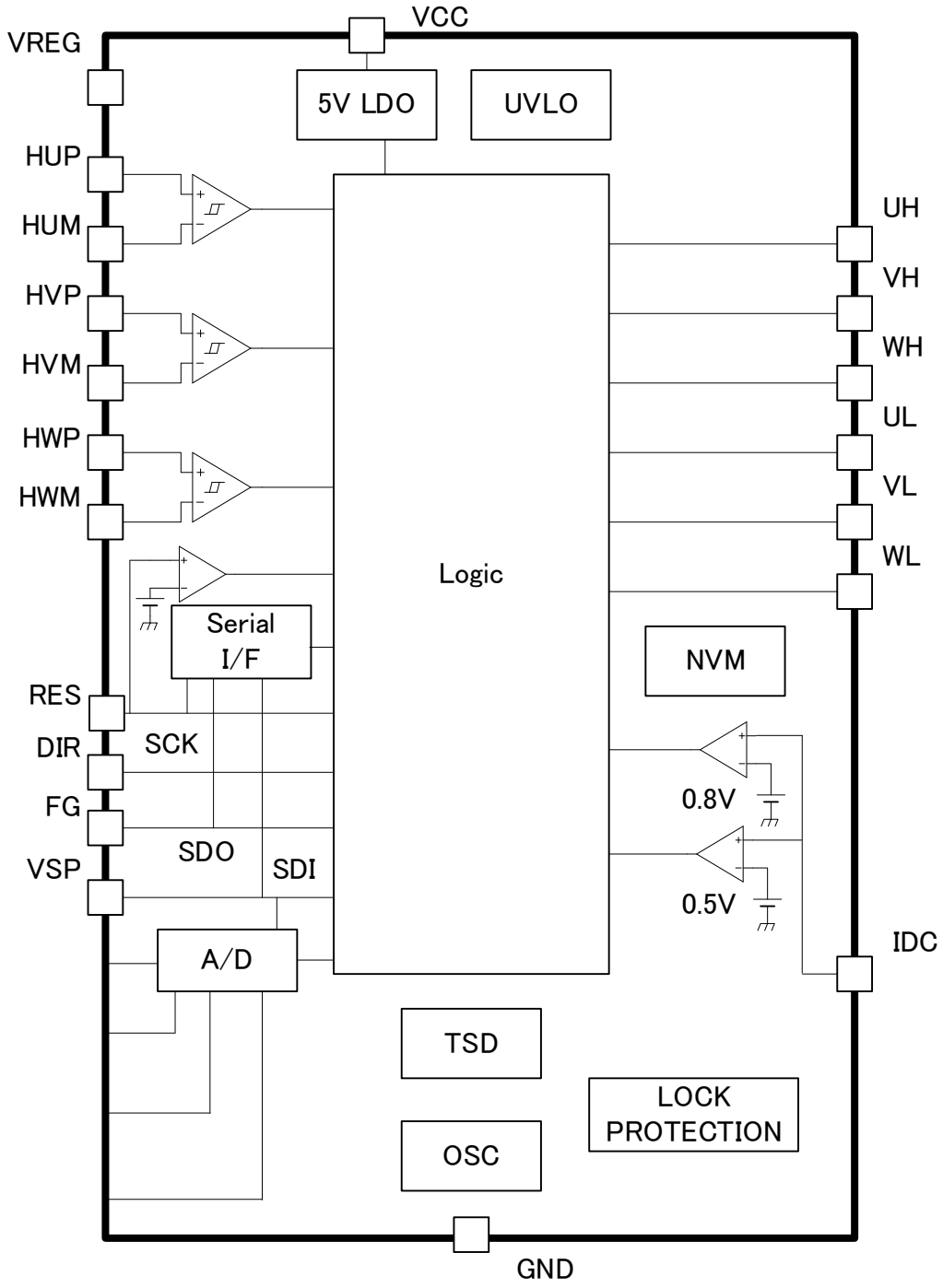
Air conditioner fan motors
Air cleaner fan motors

3. Features

- Sine Wave PWM Drive
- The Operational Supply Voltage Range: VCC=6~ 23V (Absolute Maximum Rating is 25 V)
- Various settings are available owing to NVM (Nonvolatile Memory) and SPI communication
- Automatic Lead Angle Control or Fixed Lead Angle Control is selectable.
- Hall element Input or Hall IC Input is selectable.
- Forward Rotation and Reverse Rotation can be switched.
- Speed Control Input with Analog Voltage, PWM Duty, or SPI is selectable.
- Number of pulses for Rotation Pulse Signal Output is selectable.
- Built-in Regulator Circuit (VREG= 5 V (typ.), 35 mA (max.))
- Thermal Shut Down Function (TSD)
- Power Supply Low Voltage Detection (UVLO)
- Current Limiting Function
- Output Over-current Detection (ISD)
- Lock Protection Function

Start of mass production
2025-09

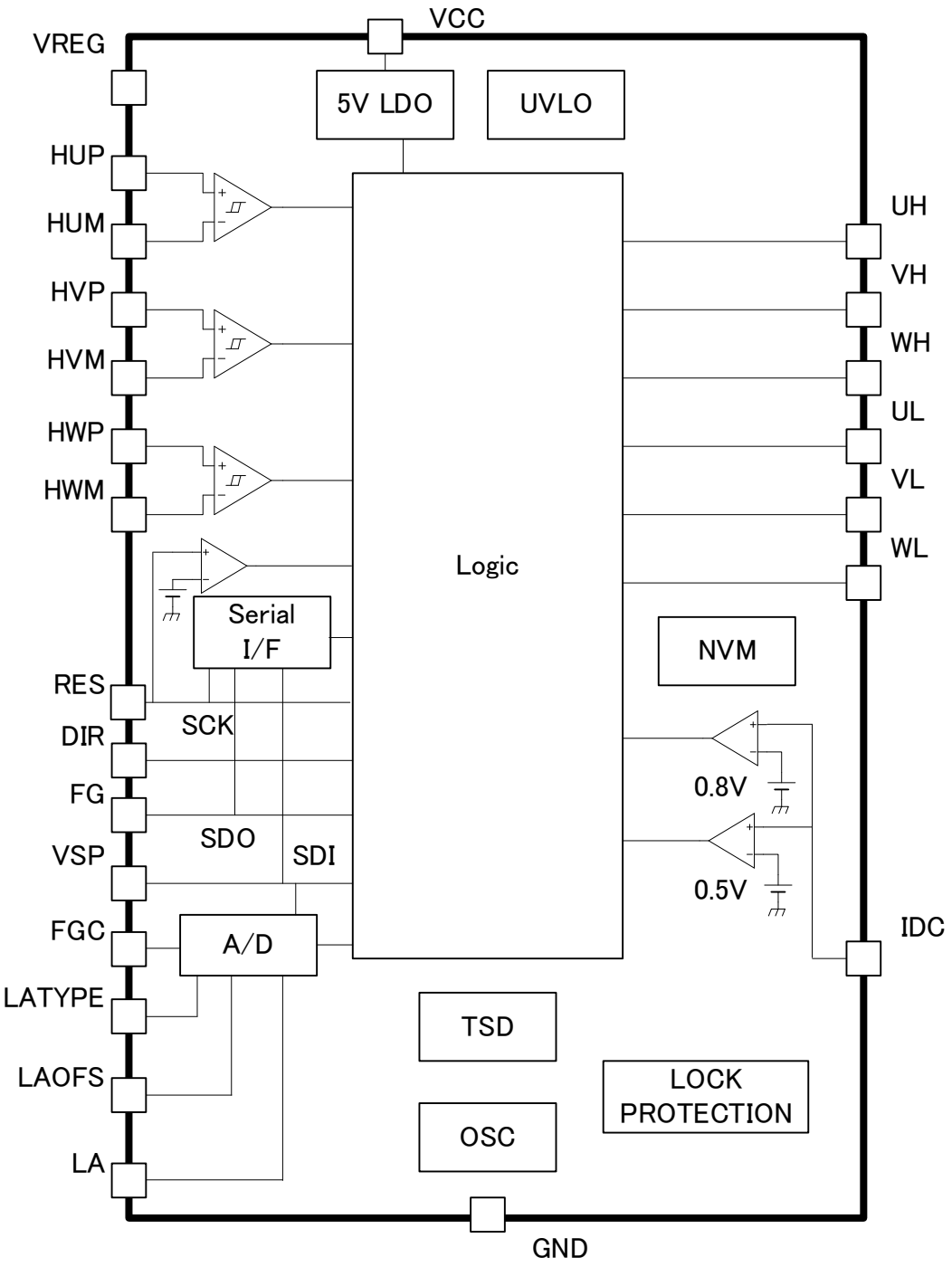
4. Block Diagram: TC78B043FTG (WQFN20)



Note: Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Fig.4 Block Diagram

5. Block Diagram: TC78B043FNG (HTSSOP28)



Note: Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Fig.5 Block Diagram

6. Pin Assignment: TC78B043FTG (WQFN20)

<Top view>

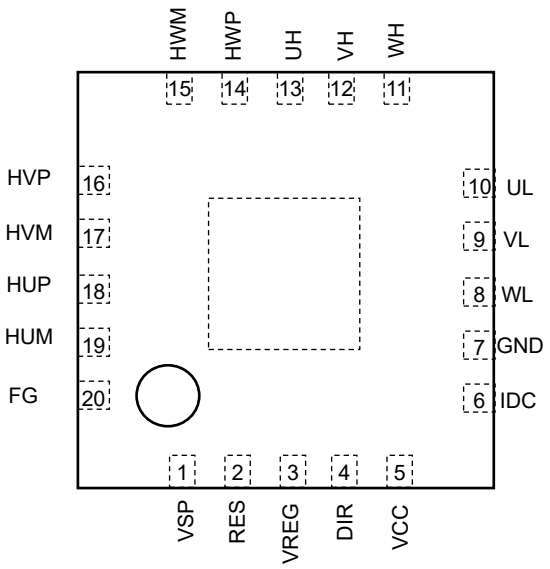


Fig.6 Pin Assignment

7. Pin Assignment: TC78B043FNG (HTSSOP28)

<Top view>

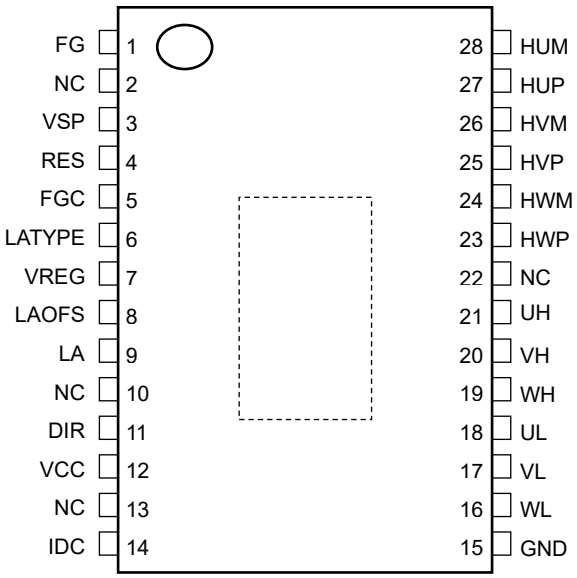


Fig.7 Pin Assignment

8. Pin Description

Table 8 Pin Description

TC78B043FTG (WQFN20) Pin number	TC78B043FNG (HTSSOP28) Pin number	Name	Input Output	Pin Description
1	3	VSP	Input	Dual use of Speed Control Input and Data-in for SPI Communication
2	4	RES	Input	Dual use of Failure Detection (Over-voltage Detection) Input and Clock signal for SPI Communication
3	7	VREG	Output	5 V Reference Voltage Output
4	11	DIR	Input	Forward/Reverse switching Input / Short Brake Input / Failure Detection Input
5	12	VCC	Power	Power Supply Voltage
6	14	IDC	Input	Current Limiting Input / Over-current Detection Input
7	15	GND	Ground	Ground
8	16	WL	Output	W-phase Low-side Commutation Signal Output
9	17	VL	Output	V-phase Low-side Commutation Signal Output
10	18	UL	Output	U-phase Low-side Commutation Signal Output
11	19	WH	Output	W-phase High-side Commutation Signal Output
12	20	VH	Output	V-phase High-side Commutation Signal Output
13	21	UH	Output	U-phase High-side Commutation Signal Output
14	23	HWP	Input	W-phase Hall Signal (+) Input
15	24	HWM	Input	W-phase Hall Signal (-) Input
16	25	HVP	Input	V-phase Hall Signal (+) Input
17	26	HVM	Input	V-phase Hall Signal (-) Input
18	27	HUP	Input	U-phase Hall Signal (+) Input
19	28	HUM	Input	U-phase Hall Signa (-) Input
20	1	FG	Output	Dual use of Rotation Pulse Output and Data out for SPI Communication
—	5	FGC	Input	Input for setting Rotation pulse / Sine Wave Reset method
—	6	LATYPE	Input	Input for setting Lead Angle Control type / with or without Stop Sequence
—	8	LAOFS	Input	Input for setting Lead Angle value / SPD value offset
—	9	LA	Input	Input for setting Maximum Lead Angle value / Fixed Lead Angle value
—	2	NC	-	Non Connection
—	10	NC	-	Non Connection
—	13	NC	-	Non Connection
—	22	NC	-	Non Connection

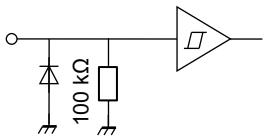
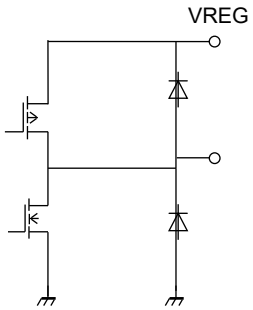
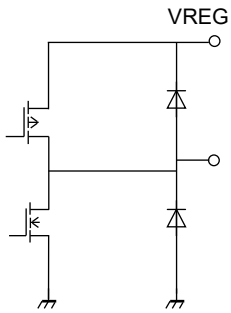
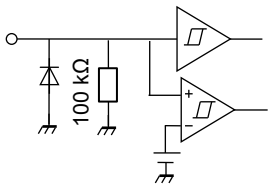
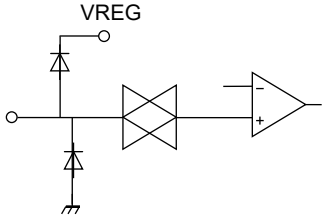
Note: The absolute maximum rating of the RES pin is 6 V, however, the RES pin is designed not to be destroyed by the VSP voltage even though the RES pin is shorted to the adjacent VSP pin.

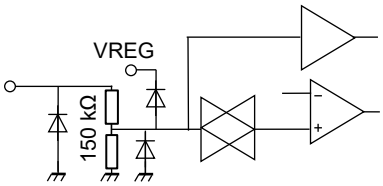
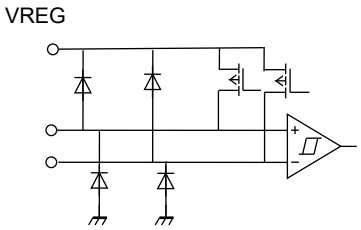
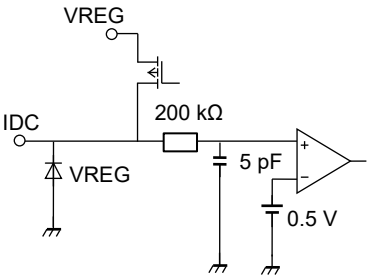
Note: The absolute maximum rating of the DIR pin is 6 V, however, the DIR pin is designed not to be destroyed by the VCC voltage even though the DIR pin is shorted to the adjacent VCC pin.

9. I/O Equivalent Circuit

The equivalent circuit diagram may be omitted or simplified for explanatory purposes.

Table 9 I/O Equivalent Circuit

Pin name	Remarks	I/O Internal Circuit
DIR	Digital Filter for Input Signals:18/fosc	
FG		
UH VH WH UL VL WL		
RES	Digital Filter for Input Signals:18/fosc	
LA FGC LATYPE LAOFS	Pins for TC78B043FNG（HTSSOP28） Be sure to input voltage to each pin before use, otherwise the input is undefined.	

Pin name	Remarks	I/O Internal Circuit
VSP		
HUP HUM HVP HVM HWP HWM	Digital Filter for Input Signals:18/fosc	
IDC	Digital Filter for Input Signals:18/fosc	

10. Functional Description

10.1. Settings of Driving Waveform

For the startup of this device, either from the Forced Commutation of the Sin Wave Drive (180°Commutation) or from the Square Wave Drive (120°Commutation) can be selected.
In case of the Sine Wave Drive Startup, the motor is started to rotate by the Forced Commutation 1 Hz of the Sine Wave Drive, and when the rotation frequency exceeds the set value for switching, the driving waveform is switched to the Sine Wave Drive for Normal Rotation.
For the Square Wave Drive Startup, the driving waveform is switched to the Squire Wave Drive for Normal Rotation when the Hall Signal exceeds the Rotation Frequency of f = 1Hz. The Lead Angle value below the Rotation Frequency 1Hz is 0 °. And when the frequency exceeds 1Hz and the driving waveform is shifted to Normal Rotation, the Lead Angle value is shifted to the value set by the Lead Angle Function.

Also in Normal Rotation, either the Sine Wave Drive or the Square Wave Drive can be selected.
For the Sine Wave Drive during Normal Rotation, the Reset Method of the Hall Signal which generates the Sine Wave can be selected from 60 ° Reset, 360 ° Reset, 180 ° Reset, and 60 °/120 ° Reset. The reset method is starts from the 60 ° Reset Method and shifted to the selected method when the Rotation Speed Fluctuation is settled within the set value.
When the Rotation Frequency Fluctuation exceeds the set value or falls below 1 Hz, the method is returned to the 60 ° Reset method.
For the Sine Wave Drive during Normal Rotation, by setting the number of averaging times, the Rotation Frequency Fluctuation is reduced, because the period of Hall Signal Input is averaged by that number of times with the set width.
For the Square Wave Drive, either 120 ° Commutation or 150 ° Commutation can be selected. And in 120 ° Commutation, the Lead Angle Control Valid/Invalid can be selected.

Table10.1.1 Settings of Driving Waveform

<table>
<tr><th>Register settings
2[15:12]
PWM_MODE
[3:0]</th><th>Inverted Hall Signal Input
(Note)</th><th>At Rotation Startup</th><th>In Normal Rotation
Non-inverted Hall Signal Input (Note)</th><th>Reset Method of Sine Wave Generation</th></tr>
<tr><td>0000</td><td rowspan="16">Square Wave Drive
120°Commutation
(Lead Angle = 0°
/with Refresh Operation)</td><td rowspan="2">Forced Commutation
Sine Wave Drive: 60°
Reset (Lead Angle=0°)</td><td rowspan="8">Sine Wave Drive
(Lead Angle: Lead Angle setting)</td><td>60° Reset</td></tr>
<tr><td>0001</td><td>60°⇔360° Reset</td></tr>
<tr><td>0010</td><td rowspan="14">Square Wave Drive
120° Commutation
(Lead Angle = 0°
/with Refresh Operation</td><td>60°⇔180° Reset</td></tr>
<tr><td>0011</td><td>60°⇔60° / 120° Reset</td></tr>
<tr><td>0100</td><td>60 ° Reset</td></tr>
<tr><td>0101</td><td>60 °⇔360° Reset</td></tr>
<tr><td>0110</td><td>60 °⇔180° Reset</td></tr>
<tr><td>0111</td><td>60°⇔60° / 120° Reset</td></tr>
<tr><td>1000</td><td>Square Wave Drive150° Commutation
(Lead Angle: Lead Angle setting / with no Refresh Operation)</td><td>-</td></tr>
<tr><td>1001</td><td>Square Wave Drive 120° Commutation
(Lead Angle:
Lead Angle setting /
with no Refresh Operation)</td><td>-</td></tr>
<tr><td>1010</td><td rowspan="6">Square Wave Drive 120° Commutation
(Lead Angle control Invalid, Lead Angle = 0°/ with Refresh Operation)</td><td>-</td></tr>
<tr><td>1011</td><td>-</td></tr>
<tr><td>1100</td><td>-</td></tr>
<tr><td>1101</td><td>-</td></tr>
<tr><td>1110</td><td>-</td></tr>
<tr><td>1111</td><td>-</td></tr>
</table>

Note: When the rotation direction is set to Forward Rotation and Hall Signals are input in the correct order, it is defined as the Non-inverted Hall Signal Input, and the motor is driven in Normal Rotation according to the setting. On the other hand, when the Hall Signals are input in the opposite order due to reverse wind, etc., this is defined as the Inverted Hall Signal Input, and in this case, the motor is driven in the Square Wave Drive 120° Commutation.
And when the rotation direction is set to Reverse Rotation, the motor is driven in Normal Rotation when Hall Signals are input in the reverse order, and the motor is driven in the Square Wave Drive 120° Commutation when Hall Signals are input in the positive order.
The Refresh Operation is to turn ON the Low-side Commutation Signals at a fixed cycle (carrier cycle). The ON duty is approximately 8%.

Table10.1.2 Settings of Rotation Frequency to switch from Forced Commutation

Resister settings 6[1:0] START_FREQ [1:0]	Rotation Frequency to switch from Forced Commutation［Hz］
00	2
01	4
10	5
11	8

Table10.1.3 Settings of Rotation Frequency Fluctuation Figure to switch Sine Wave Reset Method

Resister settings 6[3:2] SIN_SW_RATIO[1:0]	Rotation Frequency Fluctuation Figure to switch Sine Wave Reset method ［%］
00	6.25
01	12.5
10	25
11	37.5

Table10.1.4 Settings of Averaging Times Number in Sine Wave Drive

Resister settings 6[5:4] AVE_SEL[1:0]	Averaging Times Number ［times］
00	2
01	4
10	8
11	Invalid

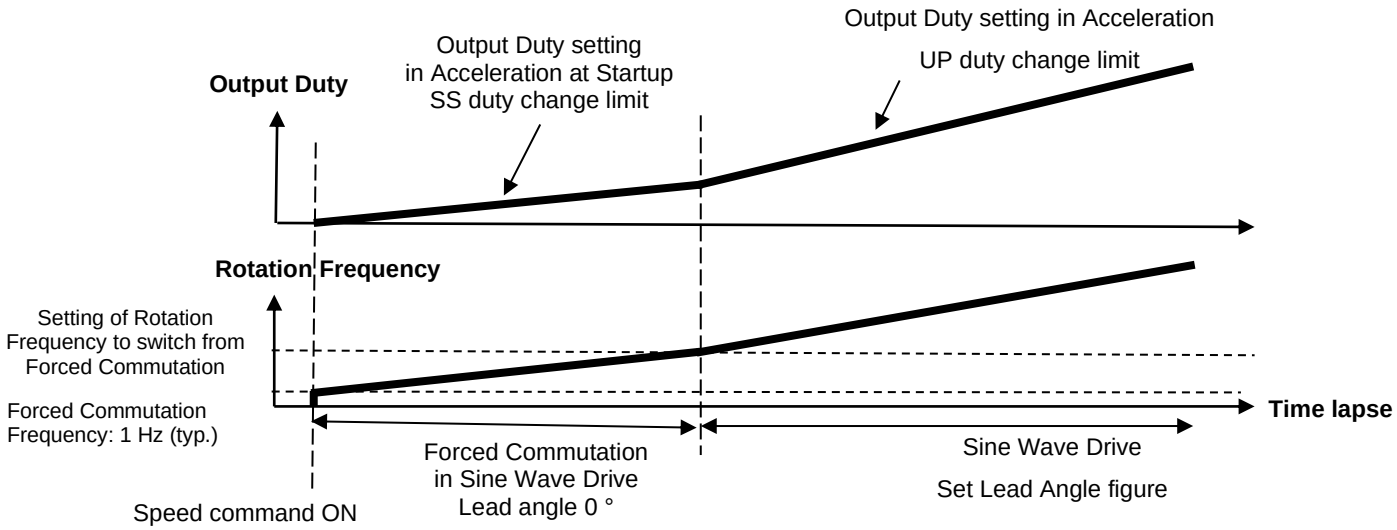


Fig.10.1.1 Settings of Forced Commutation in Sine Wave Drive at Startup

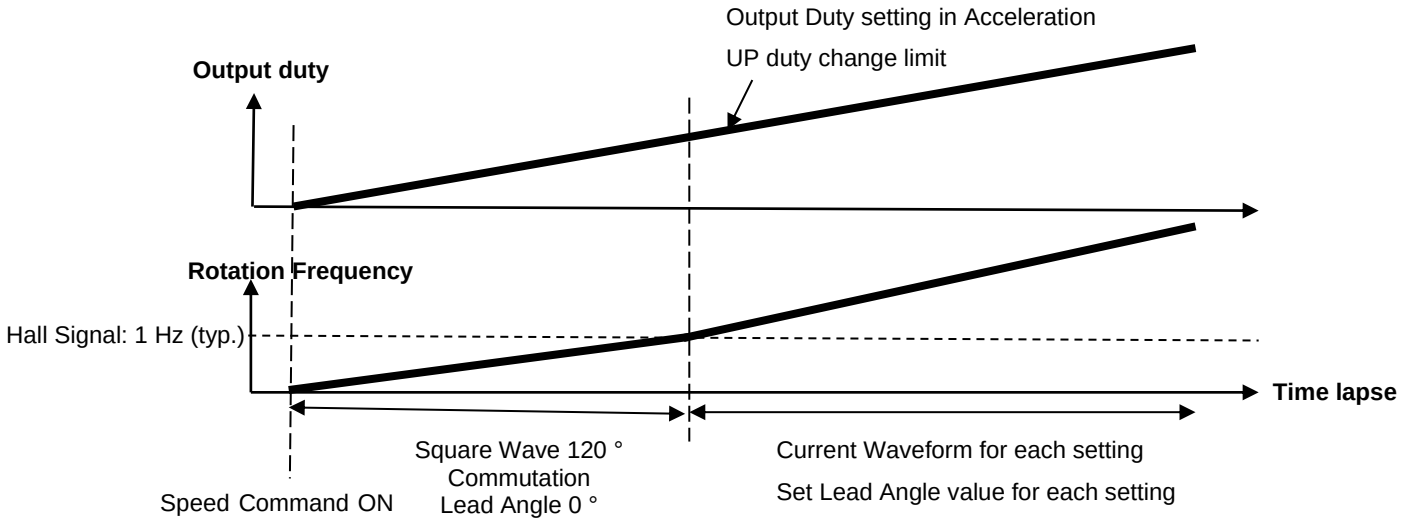


Fig.10.1.2 Settings of Square Wave 120 ° Commutation at Startup

10.2. Operating Waveforms

(1) Sine Wave Drive: Settings of Forward Rotation, Non-inverted Hall Signal Input, Lead Angle 0°, and 3 ppr at FG pin

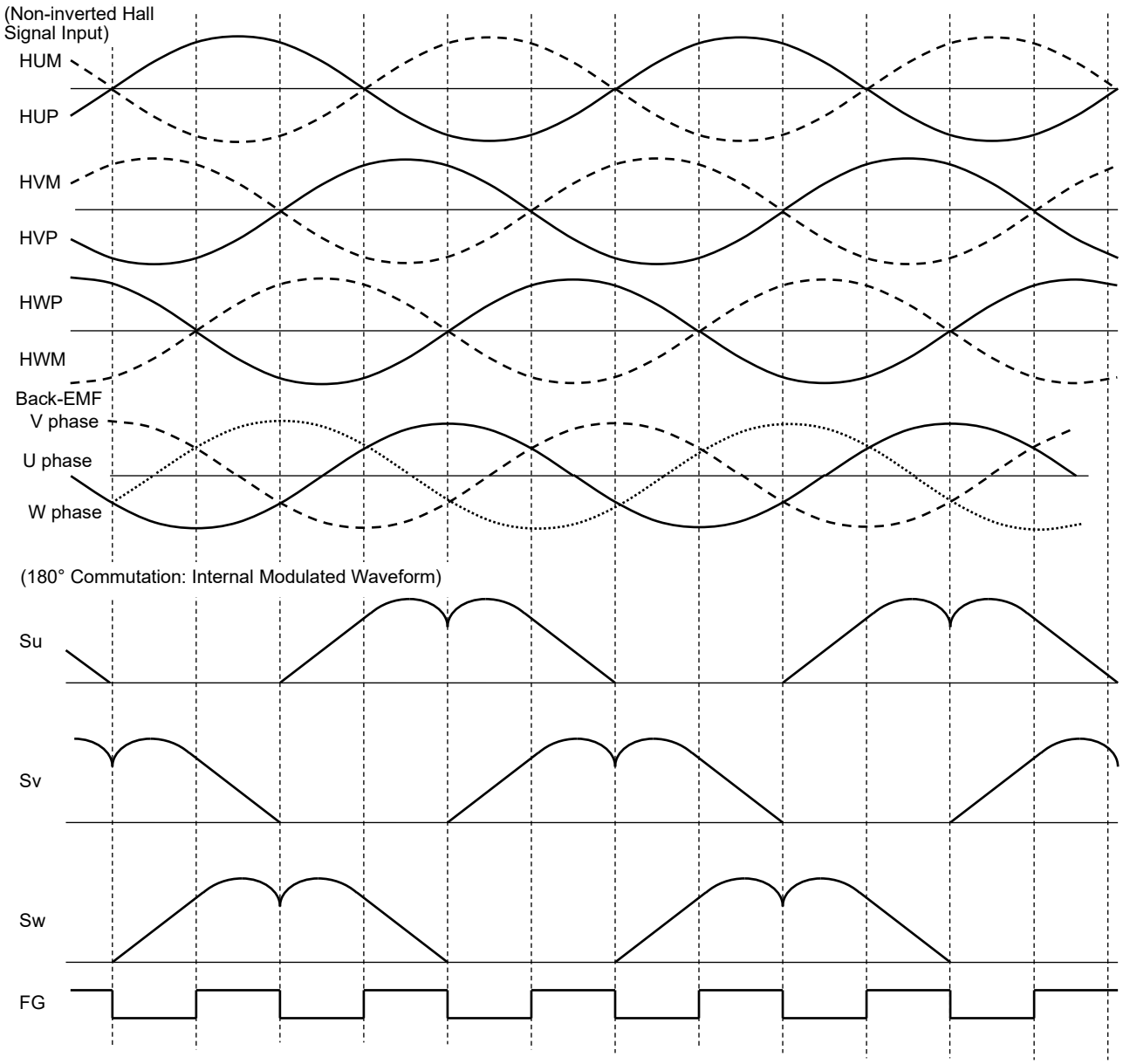


Fig.10.2.1 Sine Wave Drive: Settings of Forward Rotation, Non-inverted Hall Signal Input, Lead Angle 0°, and 3 ppr at FG pin

Note: The Timing Chart is simplified for explanatory purposes.

(2) Square Wave Drive in 120° Commutation: Settings of Forward Rotation, Inverted Hall Signal Input, and 3 ppr at FG pin

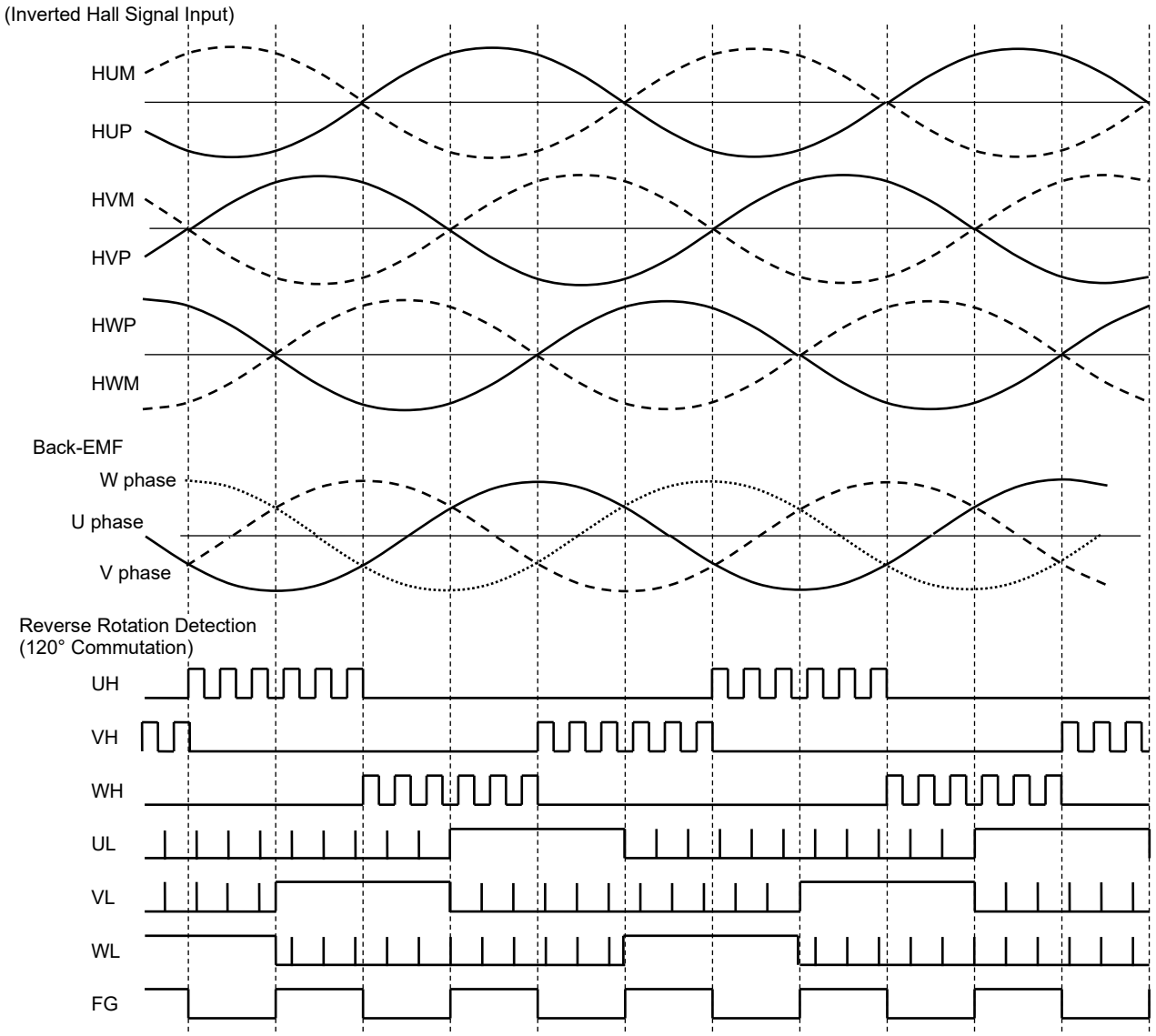


Fig.10.2.2 Square Wave Drive in 120° Commutation: Settings of Forward Rotation, Inverted Hall Signal Input, and 3 ppr at FG pin

Note: In case of the Inverted Hall Signal Input, the motor is driven in 120 ° Commutation with 0° Lead Angle. (Reverse Rotation Operation)

(3) Sine Wave Drive: Settings of Reverse Rotation, Inverted Hall Signal Input, Lead Angle 0°, and 3 ppr at FG pin

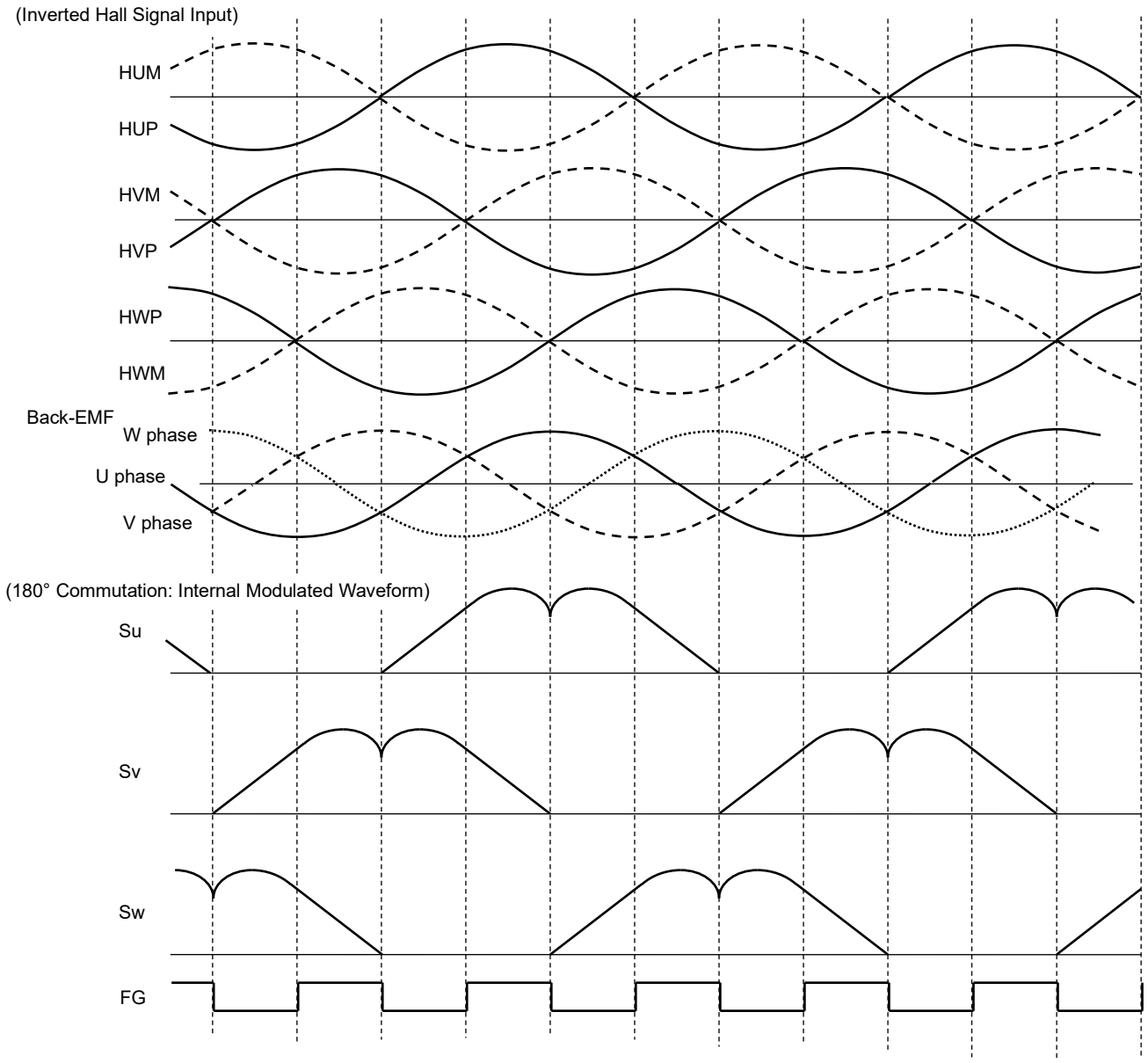


Fig.10.2.3 Sine Wave Drive: Settings of Reverse Rotation, Inverted Hall Signal Input, Lead Angle 0°, and 3 ppr at FG pin

(4) Square Wave Drive in 120° Commutation: Settings of Reverse Rotation, Non-inverted Hall Signal Input, and 3 ppr at FG pin

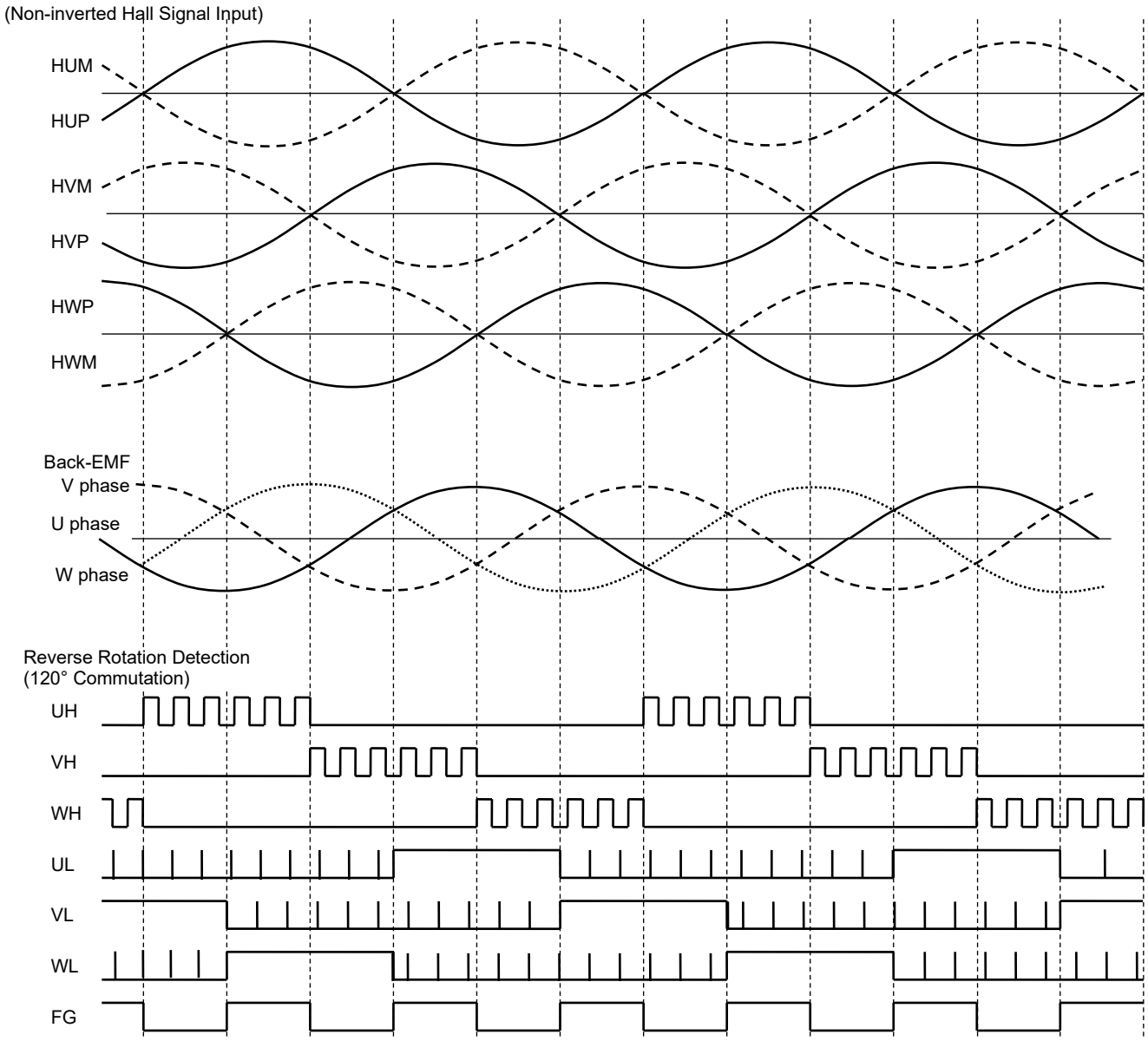


Fig.10.2.4 **Square Wave Drive in 120° Commutation: Settings of Reverse Rotation, Non-inverted Hall Signal Input, and 3 ppr at FG pin**

Note: In case of the Non-inverted Hall Signal Input, the motor is driven in 120 ° Commutation with 0° Lead Angle. (Reverse Rotation Operation)

(5) Square Wave Drive 120 ° /150 ° Commutation: Settings of Forward Rotation, Non-inverted Hall Signal Input, and 3 ppr at FG pin

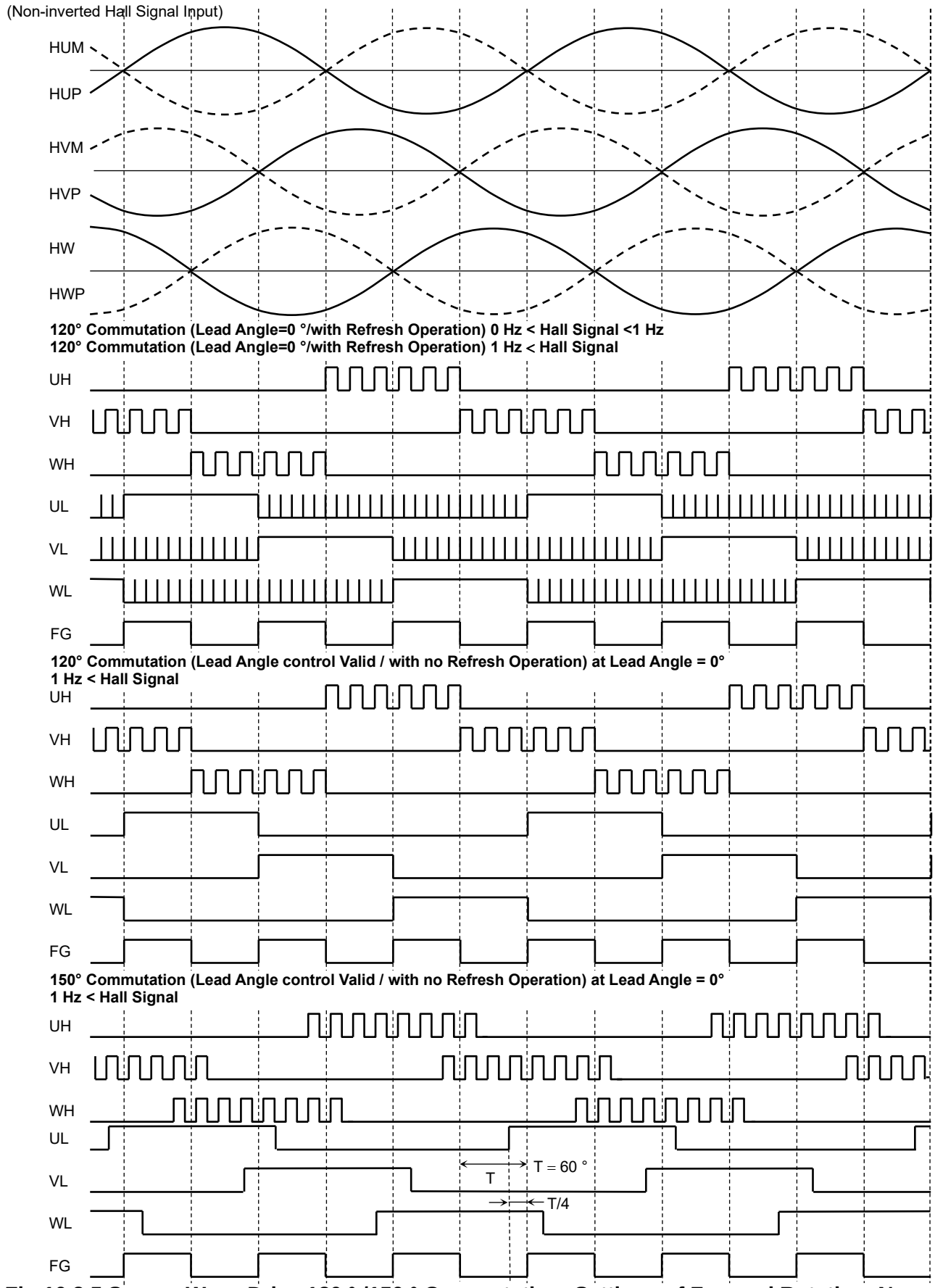


Fig.10.2.5 Square Wave Drive 120 ° /150 ° Commutation: Settings of Forward Rotation, Non-inverted Hall Signal Input, and 3 ppr at FG pin

(6) Square Wave Drive 120 ° /150 ° Commutation: Settings of Reverse Rotation, Inverted Hall Signal Input, and 3 ppr at FG pin

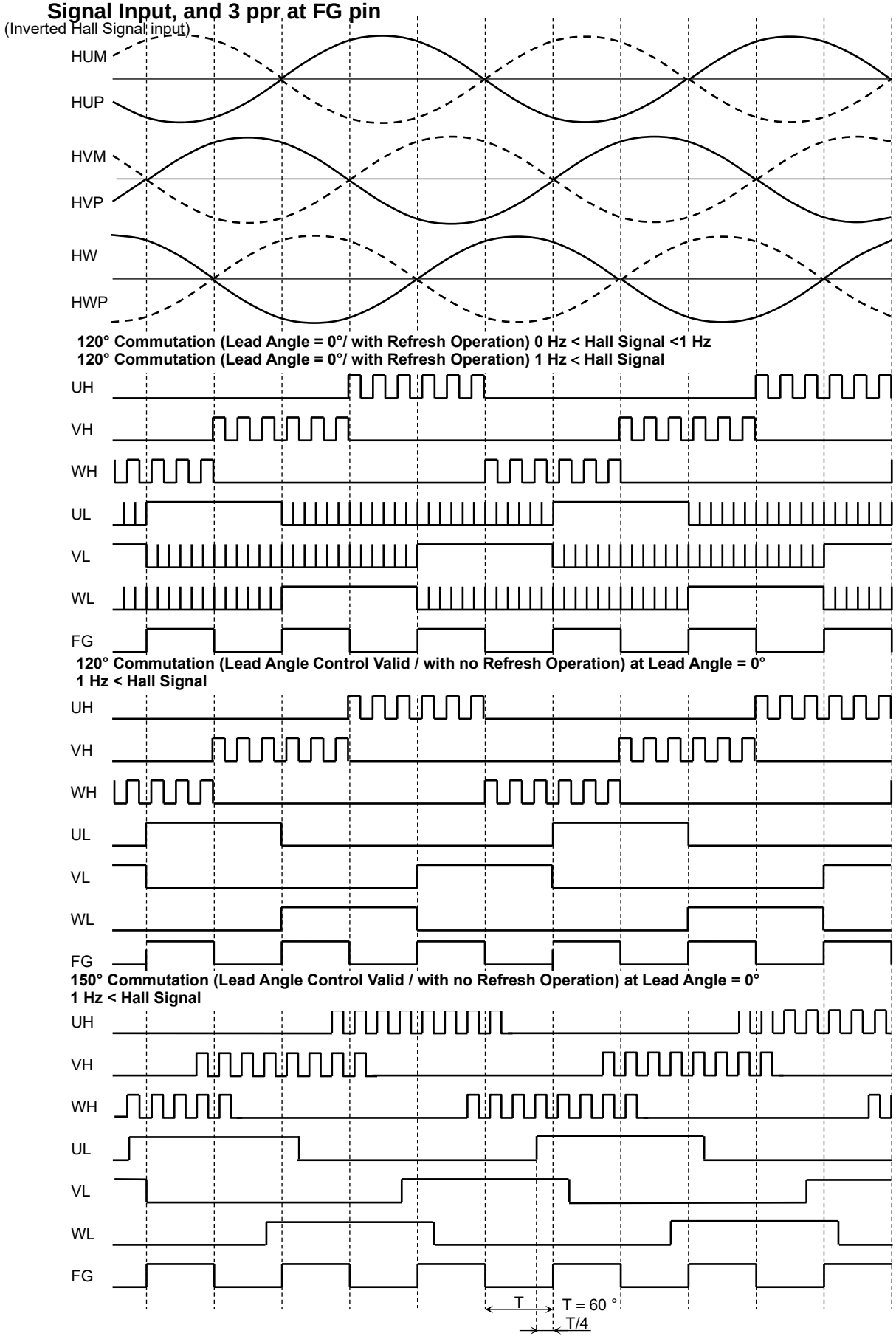


Fig.10.2.6 Square Wave Drive 120 ° /150 ° Commutation: Settings of Reverse Rotation, Inverted Hall Signal Input, and 3 ppr at FG pin

10.2.1. Operating Waveforms of Square Wave PWM Drive in 120° Commutation (with Refresh Operation)

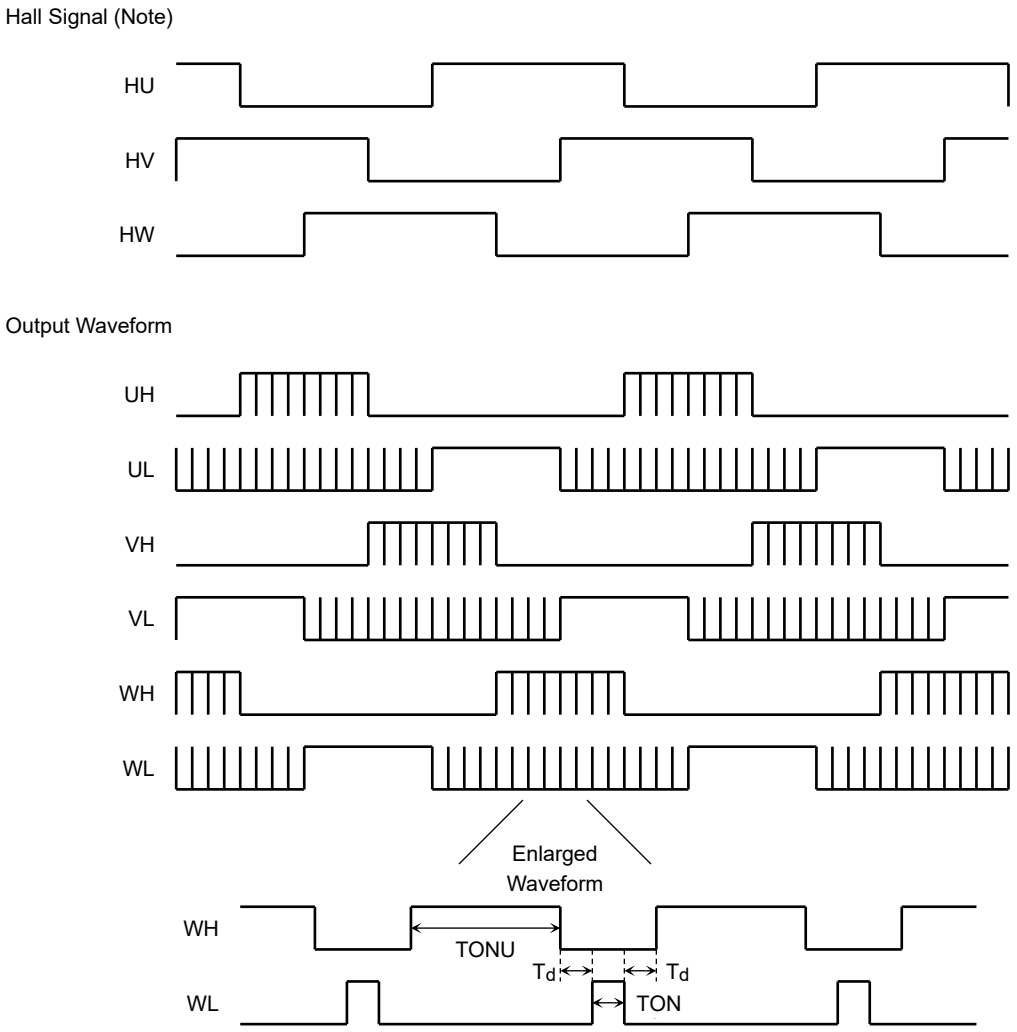


Fig.10.2.1.1. Operating Waveforms of Square Wave PWM Drive in 120° Commutation (with Refresh Operation)

Note: As for the Hall Signal, Square Wave is used to simplify the chart.

To ensure the bootstrap voltage, the Low-side UL, VL, and WL Outputs are always ON in the carrier cycle even during the OFF period. At this time, the High-side UH, VH, and WH Outputs are turned off with a dead time at the timing when the Low-side of each phase is turned on, as shown in the enlarged waveform in the chart above.

TONL = carrier period × 8 % (s) (constant regardless of VSP Input)

Speed change during Square Wave Drive is determined by the Speed Command, and Acceleration/Deceleration is performed by ON duty of TONU.

10.2.2 Operating Waveforms of Sine Wave PWM Drive

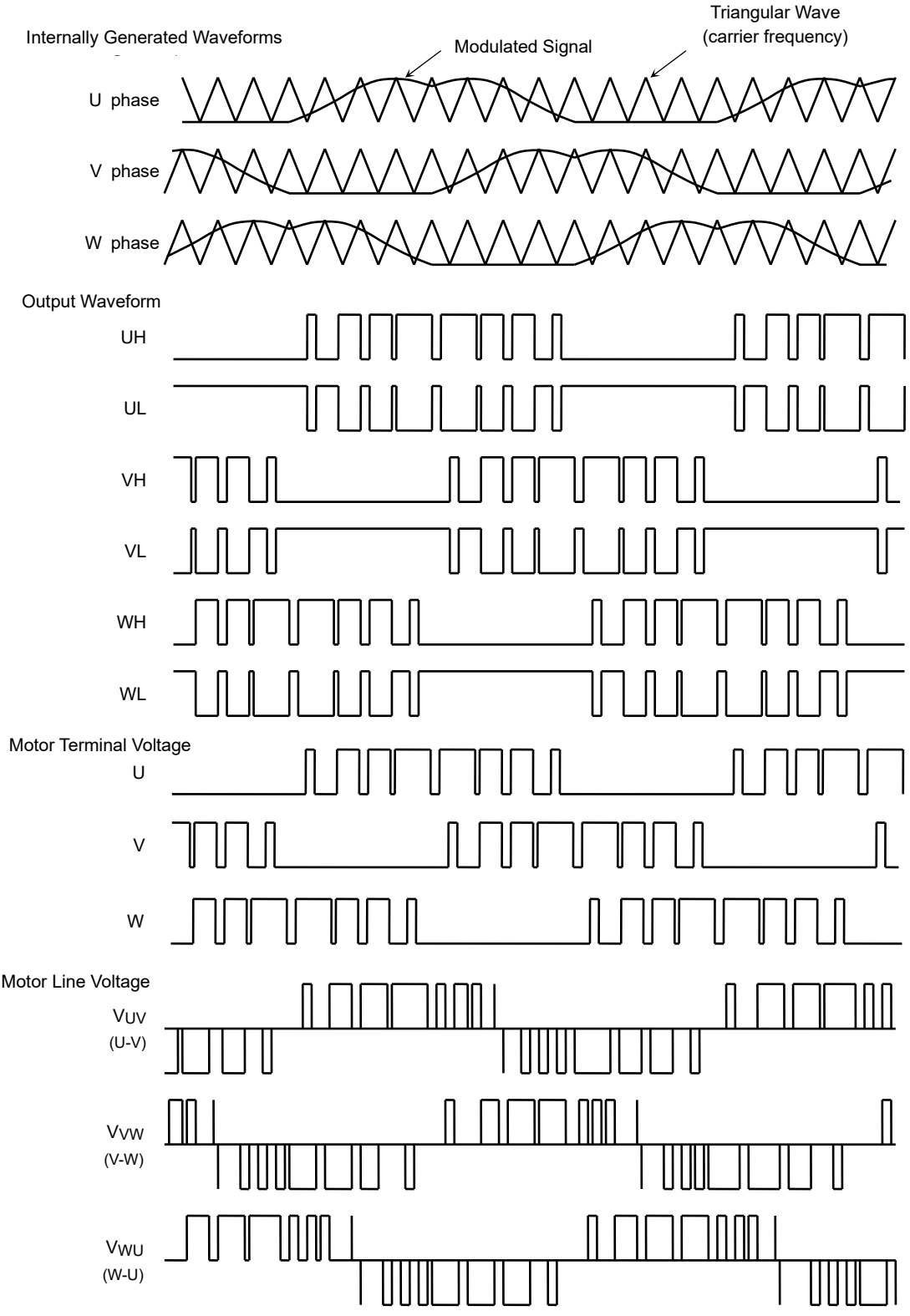


Fig.10.2.2.1 Operating Waveforms of Sine Wave PWM Drive

Note: As for speed change in Sine Wave Drive, the amplitude of the modulation signal changes with the Speed Command, and Acceleration/Deceleration is performed by the ON duty of the Output Waveform.

10.3. Sine Wave PWM Generation Method

(1) Settings of Sine Wave 60° Reset Method

The Sine Wave PWM Signal is generated by creating a modulated waveform from a Hall Signal and comparing this modulated waveform with a Triangular Waveform. The period of time (Electrical Angle: 60°) between the up edge (down edge) of the three Hall Signals and the next down edge (up edge) is counted, and this period is used as the data for the next 60° phase portion in the modulation waveform. The 60° phase portion in the modulation waveform consists of 128 data, and the time width of one data is 1/128 of the time width of the previous 60° phase, and the modulation waveform advances in this width.

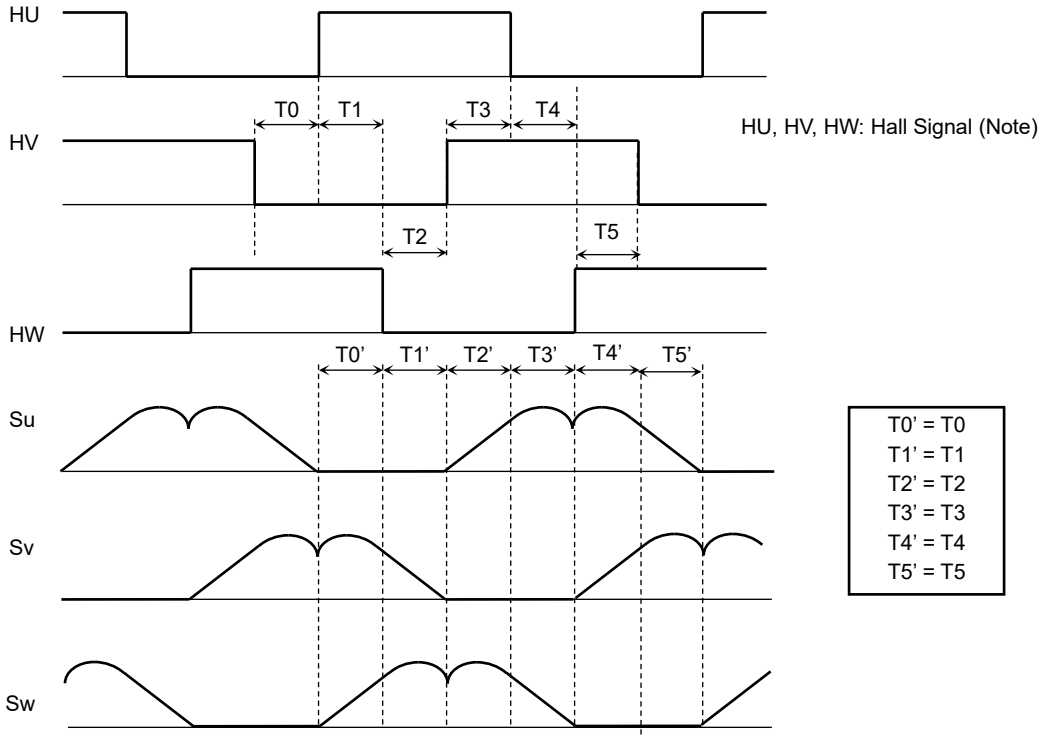


Fig.10.3.1 Settings of Sine Wave 60° Reset

In the above Figure, the T1' data of the modulation waveform advances within a time width of 1/128 of the period T1 from the HU (up edge) to the HW (down edge), and likewise, the T2' data advances within a time width of 1/128 of the period T2 from the HW (down edge) to the HV (up edge). When the next edge does not come even after 128 data arrives, the 128th data is retained as it is. (In the case of Forced Commutation in Sin Wave Drive, when the next edge does not come even after 128 data arrives, the next 128 data advances in the same time width until the next edge arrives.) Every 60° Electrical Angle, the modulation waveform is reset in synchronization with the up/down edges of the Hall Signals. Therefore, the modulation waveform is made discontinuous at each resetting when the Hall Signal is out of position or during Acceleration/Deceleration.

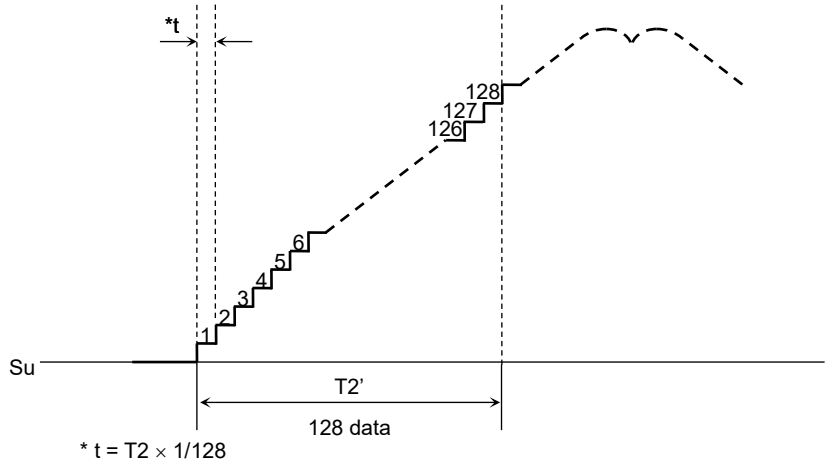


Fig.10.3.2 Timing Chart

Note: As for the Hall Signal, Square Wave is used to simplify the figure.

(2) Settings of Sine Wave 360° Reset Method

The Sine Wave PWM signal is generated by creating a modulated waveform from a Hall Signal and comparing this modulated waveform with a triangular waveform.
The period of time (electrical angle: 360°) between the down edge of the HU signal and the next down edge is counted, and this period is used as the data for the 360° phase portion in the next modulation waveform.
The 360° phase portion in the modulation waveform consists of 128 x 6 data, and the time width of one data is 1/(128 x 6) of the time width of the previous 360° phase, and the modulation waveform is generated in this width.

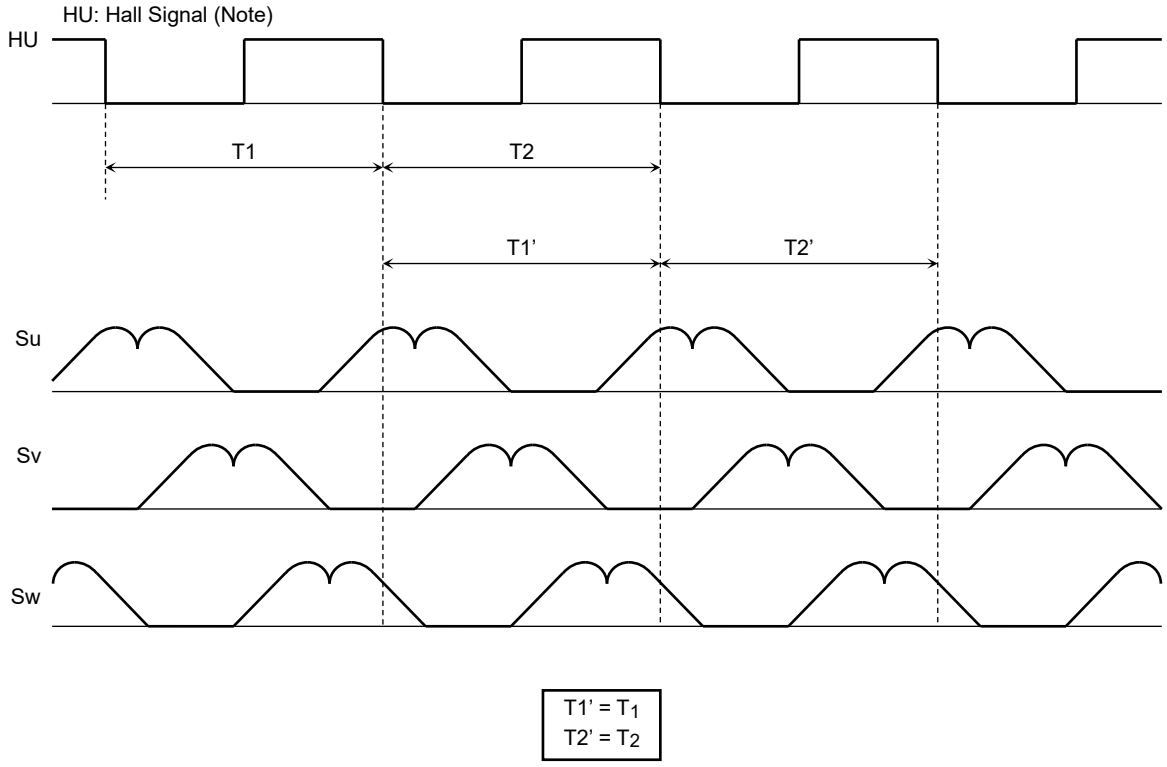


Fig.10.3.3 Timing Chart

In the above chart, the T1' data of the modulation waveform advances within a time width of the period T1 from the HU (down edge) to the next HU (down edge). When the next HU edge does not come even after T1' data ends, the data is retained as it is.
The modulation waveform is reset synchronously with the down-edge of each 360° electric angle of the HU Hall Signal.
During motor Acceleration/Deceleration, the modulation waveform is made discontinuous at each reset.

Note: As for the Hall Signal, Square Wave is used to simplify the chart.

(3) Settings of Sine Wave 180° Reset Method

The Sine Wave PWM signal is generated by creating a modulated waveform from a Hall Signal and comparing this modulated waveform with a triangular waveform.
The period of time (electrical angle: 180°) between the down edge of the HU signal and the next down edge is counted, and this period is used as the data for the 180° phase portion in the next modulation waveform.
The 180° phase portion in the modulation waveform consists of 128 x 3 data, and the time width of one data is 1/(128 x 3) of the time width of the previous 180° phase, and the modulation waveform is generated in this width.

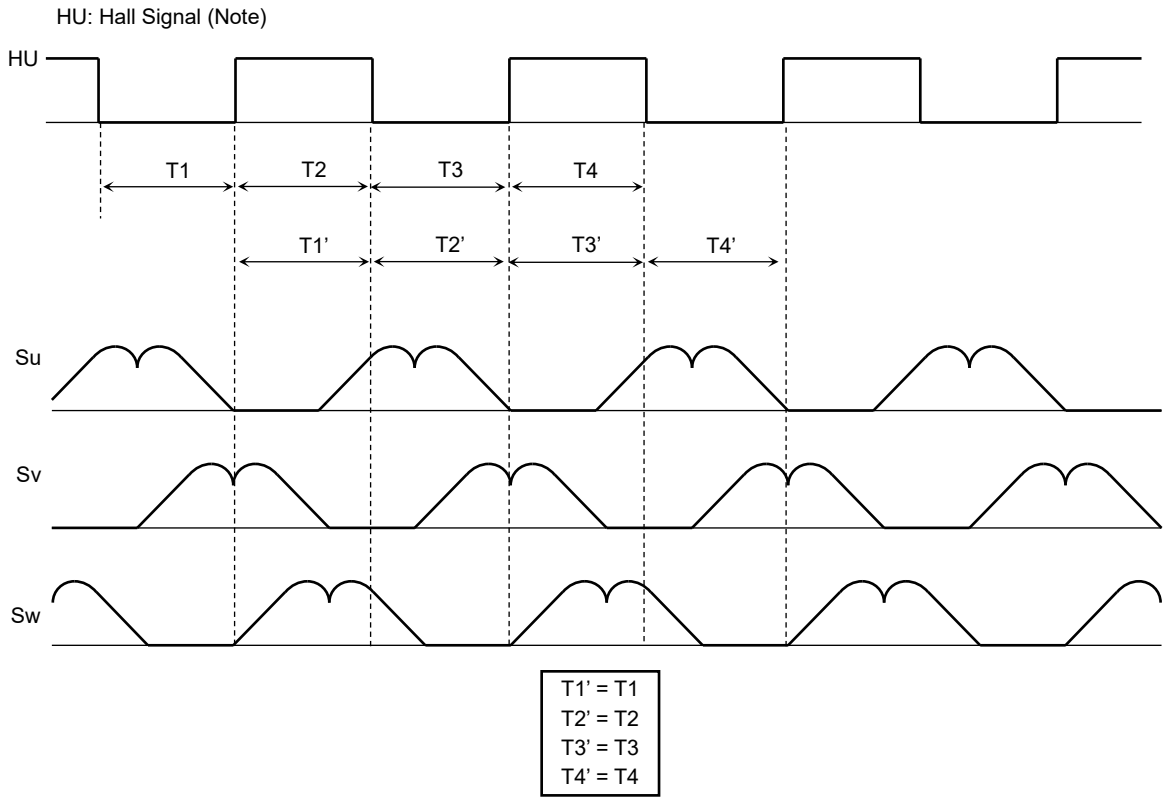


Fig.10.3.4 Timing Chart

In the above figure, the T1' data of the modulation waveform advances within a time width of the period T1 from the HU (down edge) to the next HU (up edge). When the next HU down edge does not come even after T1' data ends, the data is retained as it is.
The modulation waveform is reset synchronously with the down edge of each 360° electric angle of the HU Hall Signal.
During motor acceleration/deceleration, the modulation waveform is made discontinuous at each reset.

Note: As for the Hall Signal, Square Wave is used to simplify the chart.

(4) Settings of Sine Wave 60°/120° Reset Method

The Sine Wave PWM signal is generated by creating a modulated waveform from a Hall Signal and comparing this modulated waveform with a triangular waveform.
The period of time (electrical angle: 60°/120°) between the edge of the HU/HV signals and the next edge is counted, and this period is used as the data for the 60°/120° phase of the next modulation waveform.
The 60° phase portion in the modulation waveform consists of 128 data, and the time width of one data is 1/128 of the time width of the previous 60° phase, and the modulation waveform is generated in this width.
The 120° phase portion in the modulation waveform consists of 128 x 2 data, and the time width of one data is 1/(128 x 2) of the time width of the previous 120° phase, and the modulation waveform is generated in this width.

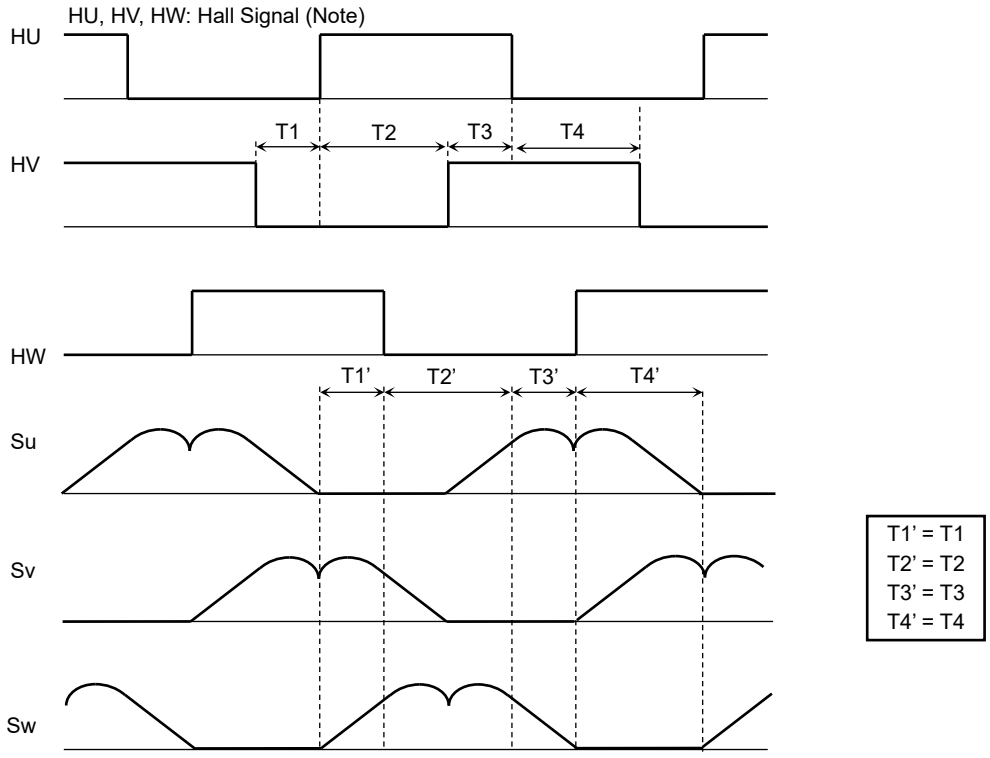


Fig10.3.5 Timming Chart

In the above figure, the T1' data of the modulation waveform advances within a time width of the period T1 from the HV (down edge) to the HU (up edge). When the next HV down edge does not come even after T1' data ends, the data is retained as it is.
The modulation waveform is reset synchronously with the down-edge/up-edge of each 60°/120° electric angle of the HU/HV Hall Signals.
During motor acceleration/deceleration, the modulation waveform is made discontinuous at each reset.

Note: As for the Hall Signal, Square Wave is used to simplify the chart.

10.4. Settings of Acceleration/Deceleration/Stopping Sequence

The Output Duty Change Ratio for Acceleration at startup, Acceleration/Deceleration in Steady State, and Stopping can be set, those are changed every 3.2 msec.

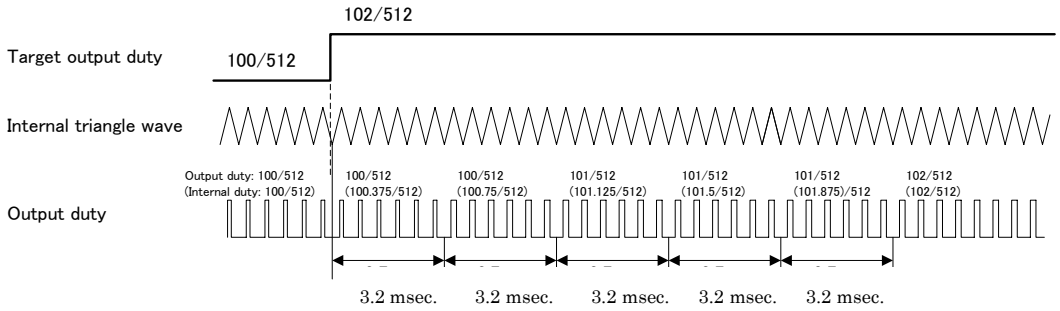


Fig.10.4.1 Example: In case of Setting Duty Change Limit = 3/8 during Acceleration

10.4.1. Settings of Output Duty for Acceleration at Startup

The settings of Output Duty for Acceleration at Startup are shown below.
The Output Duty is increased with the set ratio of “SS duty change limit”.

Table 10.4.1.1 Settings of Duty for Acceleration at Startup

Resister settings 5[3:0] SS_DUTY_CHANGE_LIMIT[3:0]	SS Duty Change Limit
0000	Immediate Input Figure = Output Figure
0001	1/8×1/8
0010	2/8×1/8
0011	3/8×1/8
0100	4/8×1/8
0101	6/8×1/8
0110	10/8×1/8
0111	20/8×1/8
1000	1/8
1001	2/8
1010	3/8
1011	4/8
1100	6/8
1101	10/8
1110	20/8
1111	56/8

10.4.2. Settings of Output Duty for Acceleration in Steady State

The settings of Output Duty for Acceleration in Steady State are shown below.
The Output Duty is increased with the set ratio of "UP duty change limit".

Table10.4.2.1 Settings of Duty for Acceleration in Steady state

Register settings 5[7:4] UP_DUTY_CHANGE_LIMIT[3:0]	UP Duty Change Limit
0000	Immediate Input Figure = Output Figure
0001	1/8×1/8
0010	2/8×1/8
0011	3/8×1/8
0100	4/8×1/8
0101	6/8×1/8
0110	10/8×1/8
0111	20/8×1/8
1000	1/8
1001	2/8
1010	3/8
1011	4/8
1100	6/8
1101	10/8
1110	20/8
1111	56/8

10.4.3. Settings of Output Duty for Deceleration and Stopping Sequence

The settings of Output Duty for Deceleration and Stop Sequence are shown below.
(The Output Duty is reduced with the set ratio of "DWN duty change limit".

Table10.4.3.1 Settings of Duty for Deceleration and Stopping Sequence

Register settings 5[11:8] DWN_DUTY_CHANGE_LIMIT[3:0]	DWN Duty Change Limit
0000	Immediate Input Figure = Output Figure
0001	1/8×1/8
0010	2/8×1/8
0011	3/8×1/8
0100	4/8×1/8
0101	6/8×1/8
0110	10/8×1/8
0111	20/8×1/8
1000	1/8
1001	2/8
1010	3/8
1011	4/8
1100	6/8
1101	10/8
1110	20/8
1111	56/8

10.4.4. Settings of Stopping Sequence

Stopping Sequence Valid or Invalid is selectable.
In case of Stop Sequence Invalid, the Motor Output is immediately turned off with a stopping signal (Commutation Signal Output = all Low).
And in case of Stop Sequence Valid, when a stopping signal in Speed Command is input, the Output Duty is lowered according to the setting of "DWN duty change limit", and the Output Duty is turned to 0 %.
When the Hall Signal is no longer switched, the Motor Output is turned OFF (Commutation signal output = all Low) after the TON period. And after Output Duty = 0 %, when the TOFF period is past, the Motor Output is turned OFF (Commutation Signal Output = all Low), because TOFF is the maximum value.

Table10.4.4.1 Setting of Stop Sequence Valid/Invalid

Register settings 5[15] STOP_SEQ	Stopping Sequence
0	Valid
1	Invalid

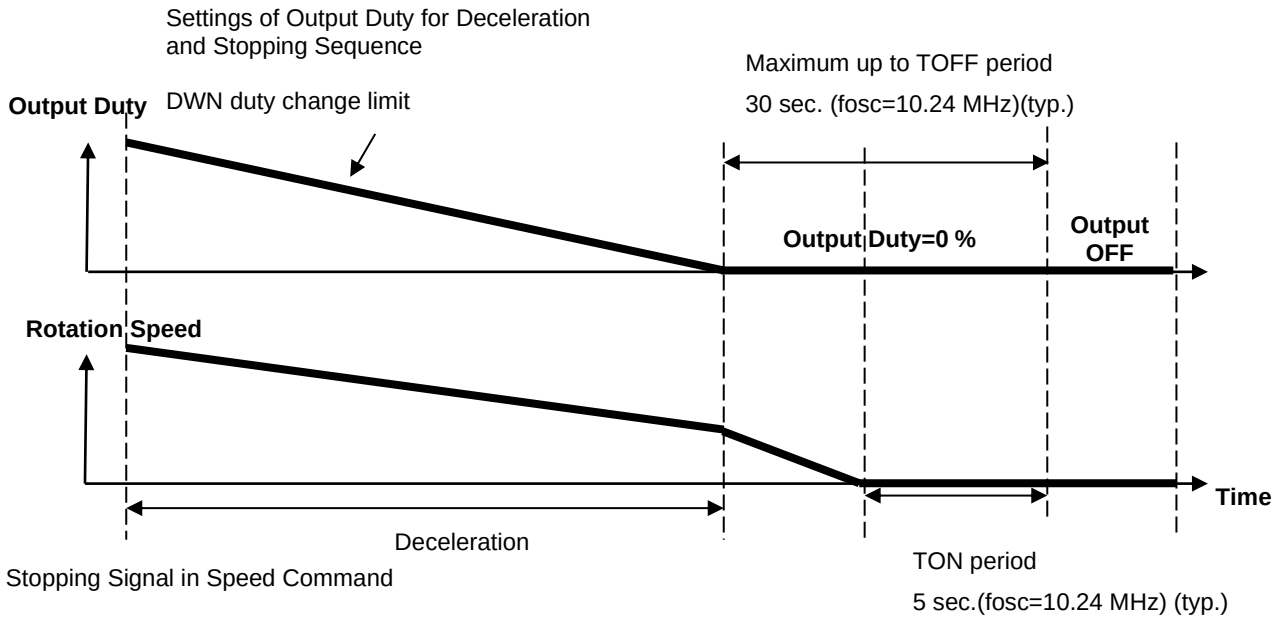


Fig. 10.4.4.1 Stopping Sequence

10.5. Settings of Initial Output Duty in returning from Idle Rotation

When the motor is returned from idle rotation, the Initial Output Duty Cycle is determined based on the set reference frequency, and the motor starts rotating. Thereafter, the Output Duty is increased or decreased according to the settings of Acceleration/Deceleration with the Speed Command Input Figure.

Example: 250 Hz setting, 125 Hz at idle rotation
The idle rotation starts with the Output Duty = 125 Hz/250 Hz = 50%, and the Output Duty is increased or decreased according to the settings of Acceleration/Deceleration with the Speed Command Input.

Table10.5.1 Settings of Reference Frequency of Initial Output Duty in returning from Idle Rotation

Register settings 6[7:6] HZ_RANGE[1:0]	Reference frequency	Example: Reference rpm in case of 8-pole motor	Example: Reference rpm in case of 10-pole motor
00	Invalid (Immediate Input Figure = Output Figure)	Invalid (Immediate Input Figure = Output Figure)	Invalid (Immediate Input Figure = Output Figure)
01	166.7 Hz	2500 rpm	2000 rpm
10	250 Hz	3750 rpm	3000 rpm
11	416.7 Hz	6250 rpm	5000 rpm

10.6. Settings of Speed Command

The setting of Speed Command is selected from the settings in the table below.

Table 10.6.1 10.6. Settings of Speed Command

Register settings 6[15:13] TRQ_SEL[2:0]	Settings of Speed Command
000	Analog Voltage Input to VSP pin: A Mode
001	Analog Voltage Input to VSP pin: B Mode
010	Analog Voltage Input to VSP pin: Velocity Curve Mode
011	PWM Duty Input VSP pin: Low active Velocity Curve Mode
100	PWM Duty Input (High active) to VSP pin: Velocity Curve Mode
101	SPI Communication Input: Velocity Curve Mode
110	-
111	-

10.6.1. High-voltage Input to VSP pin Operation Mode

When the Input Voltage to the VSP pin is set to 7.75 V < VSP ≦ 10 V, “High-voltage Input to VSP pin Operation Mode” is selected, and the Motor Outgoing Test Mode or the Commutation Output Low can be selected with the register. (When the Input Voltage exceed 10 V, what is outside range of the VSP Operating Input Voltage, “High-voltage Input to VSP pin Operation Mode” is selected.)

In the Motor Outgoing Test Mode, the Sine Wave Drive operates with zero Lead Angle and the Output ON Duty is maintained at the maximum value. Even though the Sine Wave Generation Method is changed to another reset method, the Sine Wave 60° Reset remains set.

"High-voltage Input to VSP pin Operation Mode" Valid or Invalid can also be selected with the register. The register can also be used to select "High-voltage Input to VSP pin Operation Mode" Valid or Invalid. When the register is set to Invalid, the maximum value in the Speed Command is maintained. The settings of the Lead Angle and the Sine Wave Generation Method are kept unchanged.

Table10.6.1.1 Settings of High-voltage Input to VSP pin Operation Mode

Register settings 11[5] SHIP_CHG	High-voltage Input to VSP pin Operation Mode
0	Motor Outgoing Test Mode ・Sine Wave 60° Reset ・Zero Lead Angle ・Output ON Duty maximum value
1	Commutation Output all Low (Motor Output OFF)

Table10.6.1.2 Settings of High-voltage Input to VSP pin Operation Mode Valid/Invalid

Register settings 11[6] SHIP_MASK	High-voltage Input to VSP pin Operation Mode
0	Valid
1	Invalid

10.6.2. Settings of Speed Command: A Mode of Analog Voltage Input to VSP pin

When the speed command is set to “A Mode of Analog Voltage Input to VSP pin”, by inputting analog voltage to the VSP pin, the Output can be controlled and the Motor Speed is controlled as shown below.

1. When the Command Input Voltage (VSP) is VSP ≦ 1.0 V,
   the Commutation Output is turned OFF. (for protection of Gate block)

2. When the Command Input Voltage is 1.0 V ＜ VSP ≦ 2.1 V (Refresh Operation),
   the Low-side Commutation Signal is turned ON at a fixed cycle (carrier cycle).
   ON duty= approx. 8 %

3. When Command Input Voltage is 2.1 V ＜VSP ≦ 7.75 V,
   the Output ON Duy changes with 512 resolution, and when 5.4 V (typical) ≦ VSP, the Output ON Duty maintains the maximum value.
   In case of Square Wave Drive, the Low-side Commutation Signal is forced ON at a fixed cycle (carrier cycle). ON duty= 8 %
   In the Stop State, when VSP = 2.1 V or more is input, the Driving Signal is output after a Refresh Operation 1.5 msec. is completed.
   And in the Rotation State, when VSP = 2.1 V or more is input, the Driving Signal is output immediately.

4. When Command Input Voltage is 7.75 V ＜VSP ≦ 10 V, “High-voltage Input to VSP pin Operation Mode” is set.

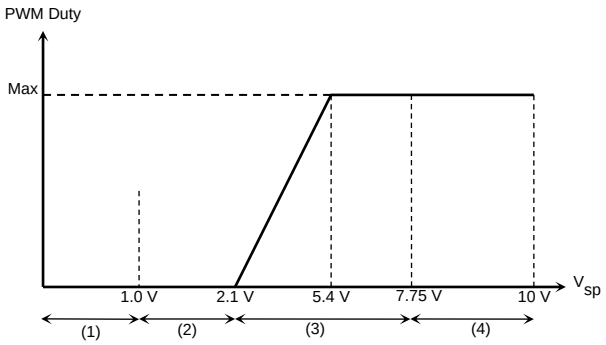


Fig.10.6.2.1 A Mode of Analog Voltage Input to VSP pin

10.6.3. Settings of Speed Command: B Mode of Analog Voltage Input to VSP pin

When the Speed Command is set to the “B Mode of Analog Voltage Input to VSP pin”, by inputting analog voltage to the VSP pin, the output can be controlled and the motor speed is controlled as shown below.

1. When the Command Input Voltage (VSP) is VSP ≦ 0.2 V (Refresh Operation),
   the Low-side Commutation Signal is turned ON at a fixed cycle (carrier cycle).
   ON duty= approx. 8 %

2. When the Command Input Voltage is 0.2 V ＜VSP ≦ 7.75 V,
   the Output ON duty changes with 512 resolutions.
   And when 5.0 V (typ.) ≦ VSP, the Output ON Duty maintains the maximum value.
   In case of Square Wave Drive, the Low-side Commutation Signal is forced ON at a fixed cycle (carrier cycle). ON duty= 8 %
   In the Stop State, when VSP = 0.2 V or more is input, the Drive Signal is output after a Refresh Operation 1.5msec. is completed.
   And in the Rotation State, when VSP = 0.2 V or more is input, the Drive Signal is output immediately.

3. When the Command Input voltage is 7.75 V ＜VSP ≦ 10 V, “High-voltage Input to VSP pin Operation Mode” is set.

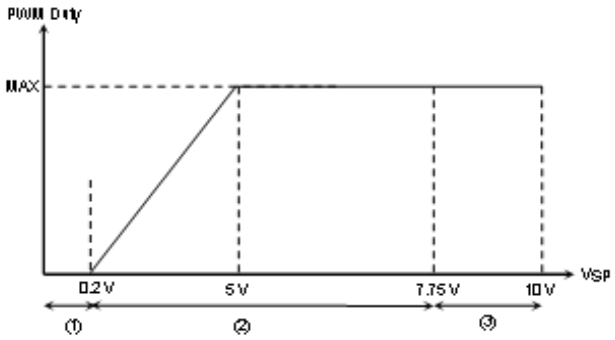


Fig.10.6.3.1 B Mode of Analog Voltage Input to VSP pin

10.6.4. Settings of Speed Command: Velocity Curve Mode of Analog Voltage Input to VSP pin

When the Speed Command is set to "Velocity Curve Mode of Analog Voltage Input to VSP pin", after setting the Speed Curve, the Output can be controlled by inputting an analog voltage within the range of 0.2 V to 5.4 V to the VSP pin as shown below, and then the motor speed is controlled.

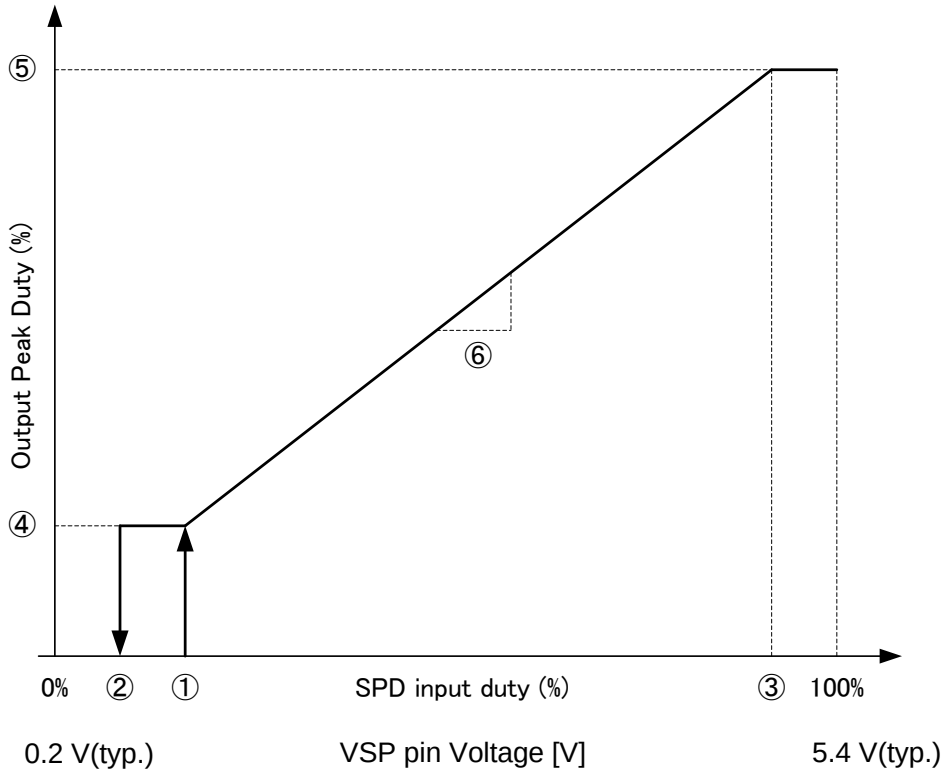


Fig.10.6.4.1 Velocity Curve of Analog Voltage Input Mode at VSP pin

Note: When the Command Input Voltage is 7.75 V ＜VSP ≦ 10 V, “High-voltage Input to VSP pin Operation Mode” is set.

Table10.6.4.1 10.6.4. Settings of Velocity Curve

Item	Setting Range	Setting Method	Setting Resolution	Resister
①Startup Duty (Start Duty)	0 to 49.8 %	STARTDUTY / 512	0.2 %	1[7:0] STARTDUTY[7:0]
②Stopping Duty (Stop Duty)	0 to 49.6 %	STOPDUTY × 2 / 512	0.4 %	1[14:8] STOPDUTY[6:0]
③Maximum Duty (Max Duty)	50.2 to 100 %	(MAXDUTY + 257) / 512	0.2 %	2[7:0] MAXDUTY[7:0]
④Minimum Output Duty (Min Output)	0 to 49.8 %	STARTOUTDUTY / 512	0.2 %	3[7:0] STARTOUTDUTY[7:0]
⑤Maximum Duty (Max Output)	Depending on①③⑥	N/A	N/A	N/A
⑥Acceleration Slope (Speed Slope)	0 to 16 Output%/Input%	DUTYSLOPE/ 1024	1/1024 Output%/Input%	4[13:0] DUTYSLOPE[13:0]

10.6.5. Settings of Speed Command: Velocity Curve Mode of PWM Duty Input to VSP pin

When the Speed Command is set to " Velocity Curve Mode of PWM Duty Input to VSP pin", the Output is controlled with the ratio of the High and Low duty of the PWM Duty Input Signal to the VSP pin. and then the motor speed is controlled.
High active and Low active for the PWM Duty Input Signal is selectable.
The frequency range of the PWM Duty Input Signal is from 1 kHz to 100 kHz, and the recognizable duty resolution of the PWM Duty Input Signal is determined by the formula of (Oscillation Frequency fosc)/(Frequency of the PWM Duty Input Signal), and the upper limit of resolution is 512.

For example, under the setting of the Oscillation Frequency fosc = 10.24 MHz (typ.),
when the PWM Duty Input Signal Frequency = 100 kHz, the Resolution = 10.24 MHz/100 kHz = 102,
when the PWM Duty input signal Frequency = 20 kHz, the Resolution = 10.24 MHz/20 kHz = 512,
when the PWM Duty input signal Frequency = 1 kHz, the recognizable duty resolution is calculated 10.24k from the formular of 10.24 MHz/1 kHz, however, it results in 512 because of the upper limit.

Table10.6.5.1 PWM Duty Input

Settings	State
PWM Duty Input (High active)	When the PWM Duty Input is set to High, the motor output is turned ON, and when set to Low, the Motor Output is turned OFF.
PWM Duty input (Low active)	When the PWM Duty Input is set to Low, the motor output is turned ON, and when set to High, the Motor Output is turned OFF.

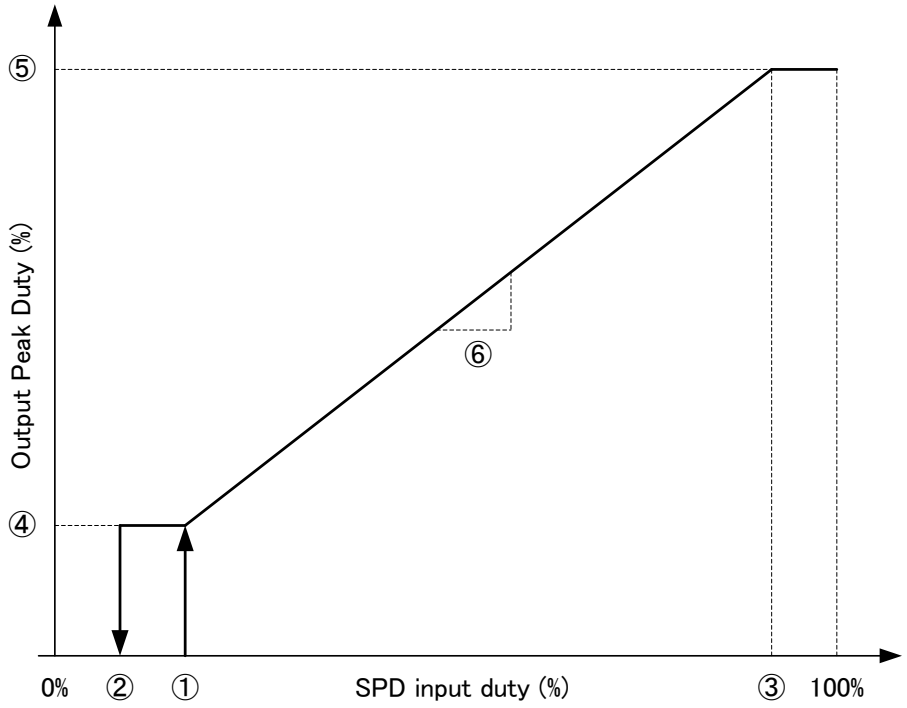


Fig. 10.6.5.1 Velocity Curve Mode of PWM Duty Input to VSP pin

Note: When the Command Input Voltage is 7.75 V < VSP ≦ 10 V, "High-voltage Input to VSP pin Operation Mode" is set.

Table10.6.5.2 Settings of Velocity Curve

Item	Setting Range	Setting Method	Setting Resolution	Resister
①Startup Duty (Start Duty)	0 to 49.8 %	STARTDUTY / 512	0.2 %	1[7:0] STARTDUTY [7:0]
②Stopping Duty (Stop Duty)	0 to 49.6 %	STOPDUTY × 2 / 512	0.4 %	1[14:8] STOPDUTY [6:0]
③Maximum Duty (Max Duty)	50.2 to 100 %	(MAXDUTY + 257) / 512	0.2 %	2[7:0] MAXDUTY [7:0]
④Minimum Output Duty (Min Output)	0 to 49.8 %	STARTOUTDUTY / 512	0.2 %	3[7:0] STARTOUTDUTY [7:0]
⑤Maximum Duty (Max Output)	Depending on ①③⑥	N/A	N/A	N/A
⑥Acceleration Slope (Speed Slope)	0 to 16 Output%/Input%	DUTYSLOPE/ 1024	1/1024 Output%/Input%	4[13:0] DUTYSLOPE [13:0]

10.6.6. Settings of Speed Command: Velocity Curve Mode of SPI Communication Input

When the Speed Command is set to "Velocity Curve Mode of SPI Communication Input", after setting the Speed Curve as shown below, the Output Duty is controlled by inputting command of 0 to 512 (513 or more also is judged as 512.) to the Speed Command register 13[15:6]TRQ_DUTY[9:0] via SPI Communication, and then the Motor Speed is controlled.

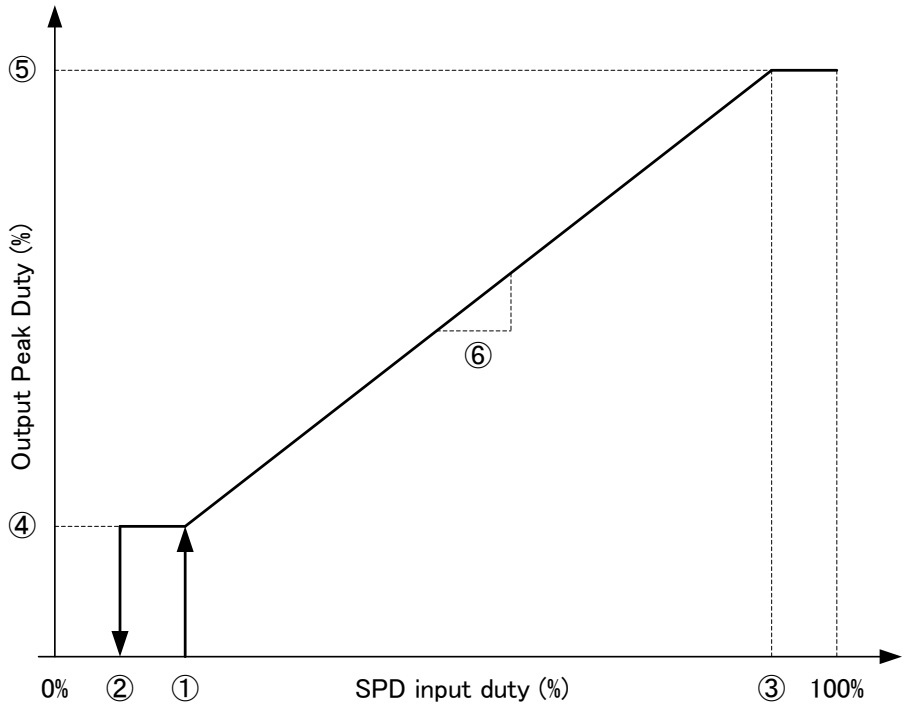


Fig.10.6.6.1 Velocity Curve Mode of SPI Communication Input

Table10.2.6.1 Settings of Velocity Curve

Item	Setting Range	Setting Method	Setting Resolution	Resister
①Startup Duty (Start Duty)	0 to 49.8 %	STARTDUTY / 512	0.2 %	1[7:0] STARTDUTY [7:0]
②Stopping Duty (Stop Duty)	0 to 49.6 %	STOPDUTY × 2 / 512	0.4 %	1[14:8] STOPDUTY [6:0]
③Maximum Duty (Max Duty)	50.2 to 100 %	(MAXDUTY + 257) / 512	0.2 %	2[7:0] MAXDUTY [7:0]
④Minimum Output Duty (Min Output)	0 to 49.8 %	STARTOUTDUTY / 512	0.2 %	3[7:0] STARTOUTDUTY [7:0]
⑤Maximum Duty (Max Output)	Depending on ①③⑥	N/A	N/A	N/A
⑥Acceleration Slope (Speed Slope)	0 to 16 Output%/Input%	DUTYSLOPE / 1024	1/1024 Output%/Input%	4[13:0] DUTYSLOPE [13:0]

The Refresh Operation Valid or Invalid can be set with the register.
Refresh Operation: To turn the Low-side Commutation Signal ON at a fixed cycle (carrier cycle).
ON duty is approx. 8 %.

Table10.6.6.2 Refresh Operation Valid/Invalid

Register settings 10[7] BOOT_ON	Refresh Operation
0	Invalid
1	Valid

High-voltage Input to VSP pin Operation Mode Valid or Invalid is set with the register.

Table 10.6.6.3 High-voltage Input to VSP pin Operation Mode Valid/Invalid

Register settings 13[0] SHIP_MODE	High-voltage Input to VSP pin Operation Mode
0	Invalid
1	Valid

10.7. Settings of Lead Angle Function

The Lead Angle Value can be selected as shown below.
The Lead Angle Value is determined by the Speed Command Figure (SPD: Internal Speed Command Figure), which is controlled by the Acceleration/Deceleration setting (Duty_Chg _Limit). And the Lead Angle value is changed every 1 STEP at the reset timing of the Sine Wave Reset Method to be the set Lead Angle value.

Table 10.7.1 Settings of Lead Angle Function

Register settings 7[15:13] LA_TYPE[2:0]	Settings of Lead Angle Function
000	Linear Curve Lead Angle: LAoffset Valid
001	Linear Curve Lead Angle: Doffset Valid
010	Quadratic Curve Lead Angle: LAoffset Valid
011	Quadratic Curve Lead Angle: SPDoffset Valid
100	Lead Angle of Quadratic Curve with Inflection Point
101	Fixed Lead Angle
110	Lead Angle 0°
111	Lead Angle 0°

Table10.7.2 Settings of Lead Angle Function

Resister name	No	Contents of Settings	Input range	Range of Setting Figure	Resolution
[6:0] LA [6:0]	①	Maximum Lead Angle value / Fixed Lead Angle value	0 to 127	0 to 59.5 °	60/128
8[7:0] MAX_SPD [7:0]	②	SPD value of maximum Lead Angle	0 to 255	256 to 511	1/512
9[15:8] CHG_SPD [7:0]	③	SPD value of Quadratic Curve with Inflection Point	0 to 255	0 to 510	2/512
8[15:8] LA_OFF/SPD_OFF [7:0]	④	LA offset	0 to 63	0 to 29.5 °	60/128
	⑤	SPD offset	0 to 255	0 to 255	1/512

10.7.1. Linear Curve Lead Angle: LA offset Valid

When " Lead angle of primary curve: LA offset valid" is selected, the Lead Angle indicates the behavior of a linear curve with respect to the Speed Command SPD (Internal Speed Command Figure) and can be set as shown below.

①The Maximum Lead Angle value is determined with the setting of LA x Resolution (60/128).
Example: when the setting of LA = 100,
the Maximum Lead Angle is 100 x 60 / 128 = 46.9 °

②The SPD figure of maximum Lead Angle is determined with the setting of max_spd setting + 256.
Example: when the setting of max_spd/chg_spd = 100,
the SPD value of Maximum Lead Angle is 100 + 256 = 356

④The LA offset is determined with the setting of la_off/spd_off x resolution (60/128).
Example: when the setting of la_off/spd_off is 30,
the LA offset is 30 x 60 / 128 = 14.1°.

Example: The Lead Angle when SPD=200 at the above settings is as follows.
Lead Angle [°] = [{(LA-la_off/spd_off) / (max_spd / chg_spd+256) × SPD} + la_off/spd_off]
× (60 / 128)
Lead Angle [°] = [{(100-30) / (100 + 256) × 200} + 30] × (60 / 128)
Lead Angle [°] = 32.5
When LA < la_off/spd_off, LA-la_off/spd_off is 0.

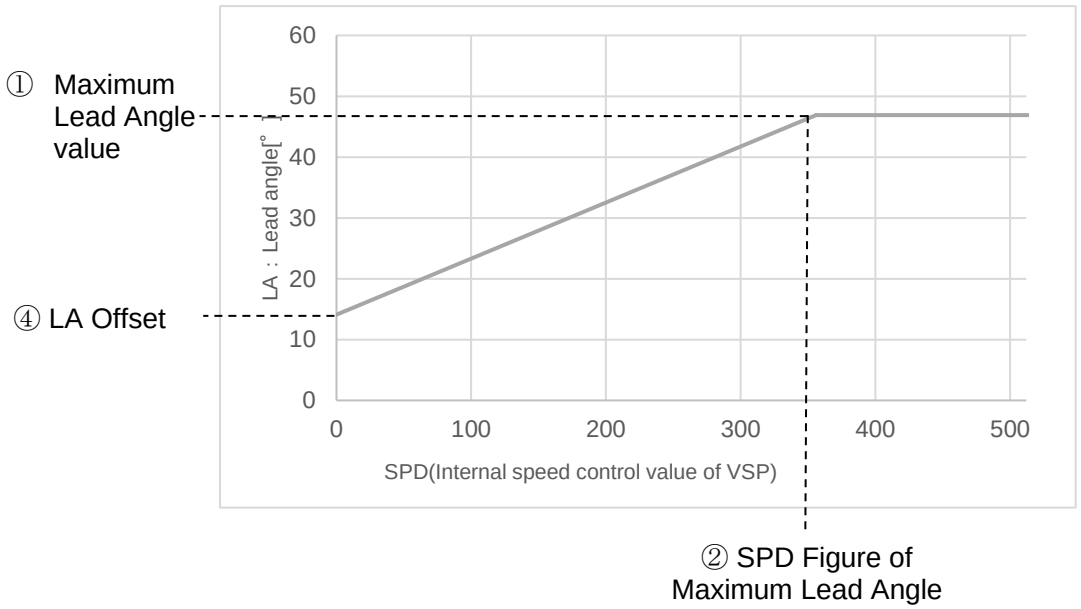


Fig.10.7.1.1 Linear Curve Lead Angle: Settings of LA offset Valid

10.7.2. Linear Curve Lead Angle: SPD offset Valid

When the " Linear curve Lead angle: SPD offset valid" is selected, the lead angle indicates the behavior of a linear curve with respect to the Speed Command SPD (Internal Speed Command Figure) and can be set as shown below.

①The Maximum Lead Angle value is determined with the setting of LA x Resolution (60 / 128).
Example: when the setting of LA = 100,
the Maximum Lead Angle is 100 x 60 / 128 = 46.9 °

②The SPD figure of Maximum Lead Angle is determined with the setting of max_spd setting + 256.
Example: when the setting of max_spd / chg_spd = 100,
the SPD value of Maximum Lead Angle is 100 + 256 = 356

⑤The SPD offset is determined with the setting of la_off/spd_off.
Example: when the setting of la_off/spd_off is 100,
SPD offset is 100.

Example: The Lead Angle when SPD = 200 at the above settings is as follows.
Lead Angle [°] = LA × (SPD-la_off/spd_off) / (max_spd / chg_spd+256-la_off/spd_off) × (60 / 128)
Lead Angle [°] = 100 × (200 - 100) / (100 + 256 -100) × (60 / 128)
Lead Angle [°] = 18.3
When SPD < la_off/spd_off, Lead Angle [°] is 0.

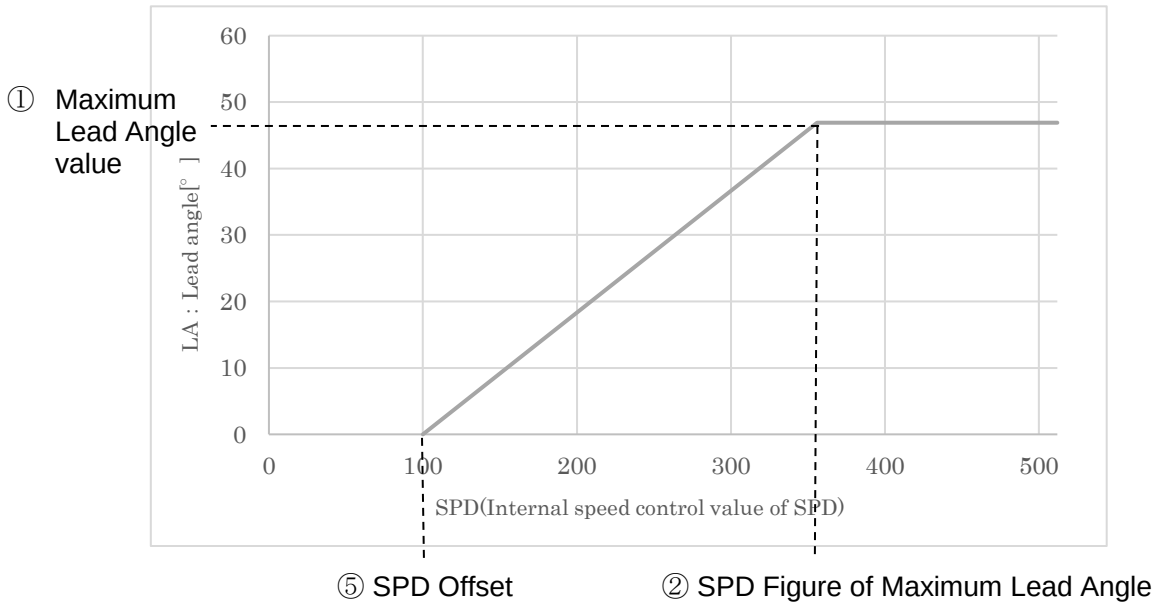


Fig.10.7.2.1 Linear Curve Lead Angle: Settings of SPD offset Valid

10.7.3. Quadratic Curve Lead Angle: LAoffset Valid

When the "Quadratic curve Lead Angle: LAoffset valid" is selected, the lead angle indicates the behavior of a quadratic curve with respect to the Speed Command SPD (Internal Speed Command Figure) and can be set as follows.

①The Maximum Lead Angle value is determined with the setting of LA x Resolution (60/128).
Example: when the setting of LA = 100,
the Maximum Lead Angle is 100 x 60 / 128 = 46.9 °

②The SPD figure of Maximum Lead Angle is determined with the setting of max_spd setting + 256.
Example: when the setting of max_spd / chg_spd = 100,
the SPD value of maximum Lead Angle is 100 + 256 = 356

④The LA offset is determined with the setting of la_off/spd_off x Resolution (60/128).
Example: when the setting of la_off/spd_off is 30,
the LA offset is 30 x 60/128 = 14.1°.

Example: The Lead Angle when SPD=200 at the above settings is as follows.
Lead Angle [°] = [{(LA-la_off/spd_off) / (max_spd / chg_spd + 256) ^2 x SPD^2} + la_off/spd_off]
x (60 /1 28)
Lead Angle [°] = [{(100 - 30) / (100 + 256)^2 x 200^2} + 30] x (60 / 128)
Lead Angle [°] = 22.9
When LA < la_off/spd_off, LA-la_off/spd_off is 0.

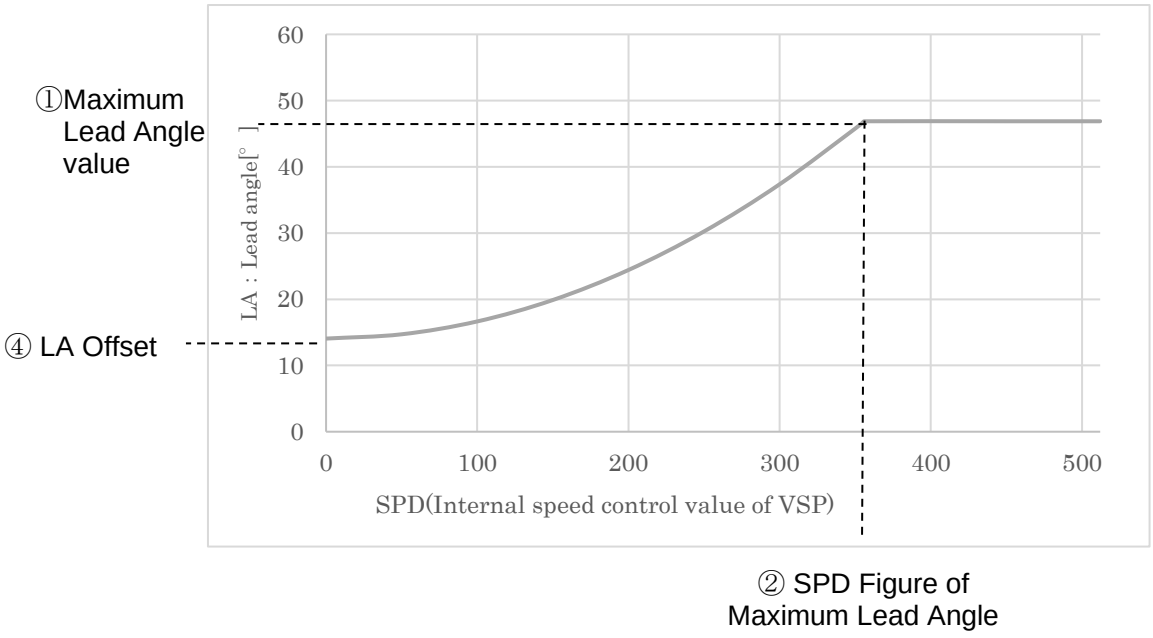


Fig 10.7.3.1 Quadratic Curve Lead Angle: Settings of LAoffset Valid

10.7.4. Quadratic Curve Lead angle: SPD offset Valid

When the "Quadratic curve Lead Angle: SPD offset valid" is selected, the lead angle indicates the behavior of a quadratic curve with respect to the Speed Command SPD (Internal Speed Command value) and can be set as shown below.

①The Maximum Lead Angle value is determined with the setting of LA x Resolution (60 / 128).
Example: when the setting of LA = 100,
the Maximum Lead angle is 100 x 60 / 128 = 46.9 °

②The SPD Figure of Maximum Lead Angle is determined with the setting of max_spd setting + 256.
Example: when the setting of max_spd / chg_spd = 100,
the SPD value of maximum Lead angle is 100 + 256 = 356

⑤The SPD offset is determined with the setting of la_off/spd_off.
Example: when the setting of la_off/spd_off is 100,
SPD offset is 100.

Example: The Lead Angle when SPD=200 at the above settings is as follows.
Lead Angle [°] = LA × (SPD-la_off/spd_off) ^2 / (max_spd / chg_spd + 256 - la_off/spd_off)^2 × (60 / 128)
Lead Angle [°] = 100 × (200-100)^2 / (100 + 256 - 100)^2 × (60 / 128)
Lead Angle [°] = 7.2
When SPD < la_off/spd_off, Lead Angle [°] is 0.

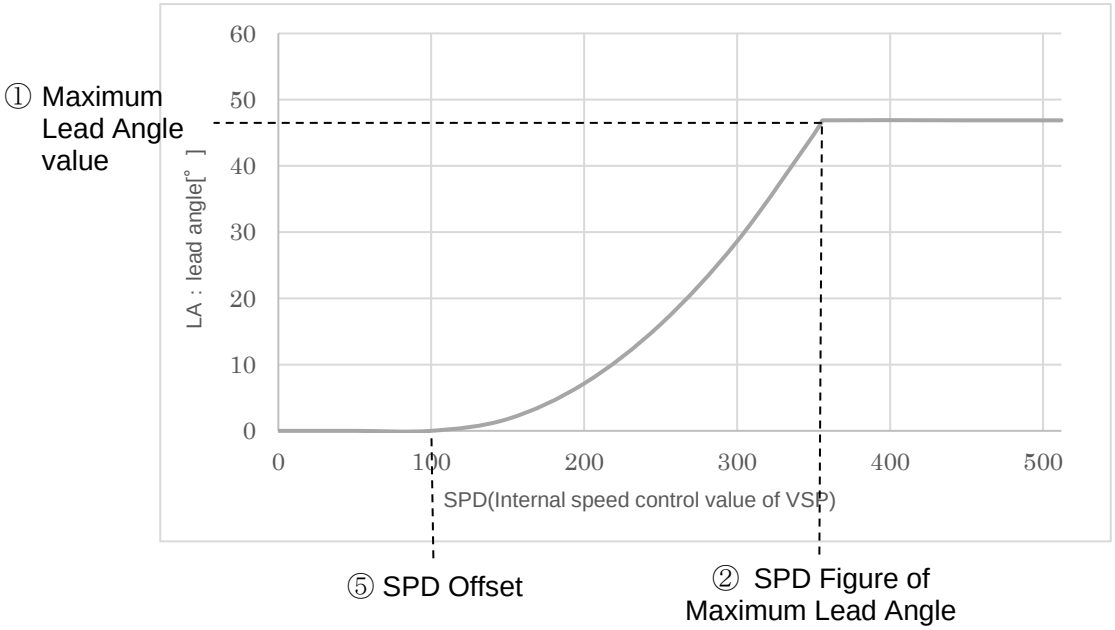


Fig10.7.4.1 Settings of Quadratic Curve Lead Angle: SPD offset Valid

10.7.5. 2 Lead Angle of Quadratic Curve with Inflection Point

When the "Lead Angle of Quadratic Curve with Inflection Point" is selected, the Lead Angle indicates the behavior of a quadratic curve with respect to the Speed Command SPD (Internal Speed Command value) and can be set as show below.

①The Maximum Lead Angle value is determined with the setting of LA x Resolution (60 / 128).
Example: when the setting of LA = 100,
the Maximum Lead Angle is 100 x 60 / 128 = 46.9 °

③The SPD Figure of Quadratic Curve with Inflection Point is determined with the setting of chg_spd x 2.
Example: when the setting of max_spd/chg_spd = 100,
the SPD value of Quadratic Curve with Inflection point is 100 x 2 = 200

Example: The Lead Angle when SPD=200 at the above settings is as follows.
When the inflection point > SPD,
Lead Angle [°] = LA × SPD^2 / {2 × (2 × max_spd / chg_spd)^2} × (60 / 128)
Lead Angle [°] = 100 × 100^2 / {2 × (2 × 100)^2} × (60 / 128)
Lead Angle [°] = 5.9

Example: The Lead Angle when SPD=300 at the above settings is as follows.
When the inflection point≦SP,
Lead Angle [°] = (LA - [{LA × (512 - SPD)^2)} / {2 × (512 - 2 × max_spd / chg_spd)^2}]) × (60 / 128)
Lead Angle [°] = (100 - [{100 × (512 - 300)^2)} / {2 × (512 - 2 × 100)^2}]) × (60 / 128)
Lead Angle [°] = 36.1

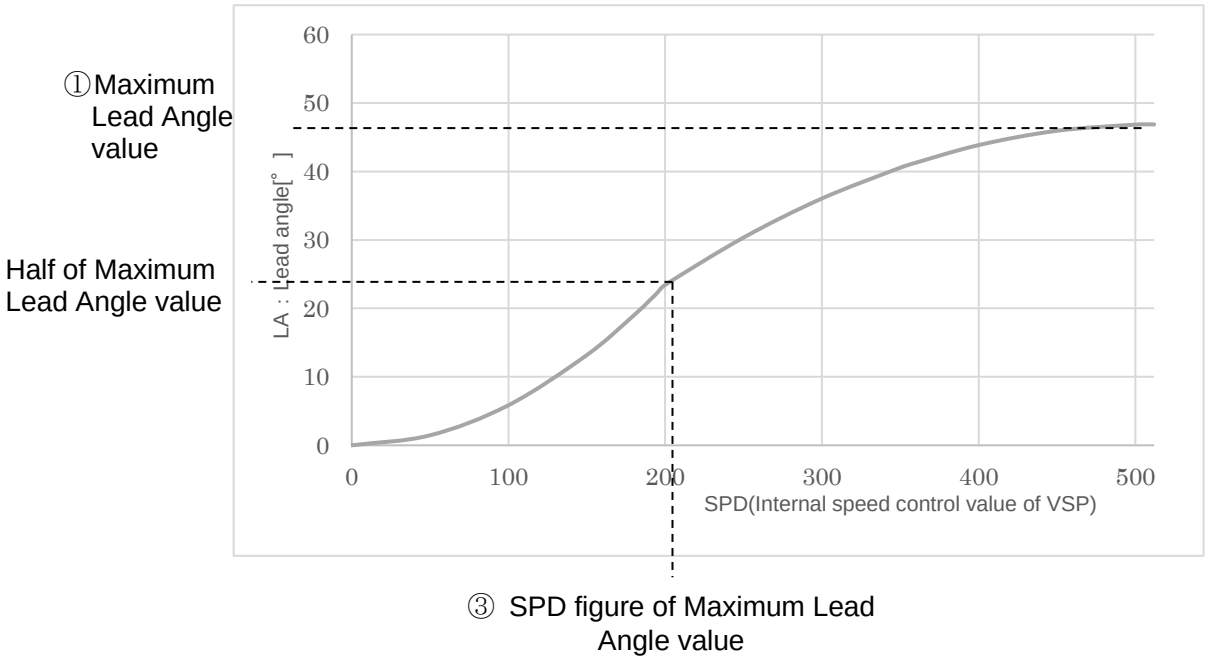


Fig. 10.7.5.1 Settings of Lead Angle of Quadratic Curve with Inflection Point

10.7.6. Fixed Lead Angle

When the "Fixed Lead Angle" is selected, the Lead Angle is constant with respect to the Speed Command SPD (Internal Speed Command value) and can be set as follows.

①Fixed Lead Angle is determined with the setting of LA x resolution (60 / 128).
Example: When LA setting = 100,
the Maximum Lead Angle is 100 x 60 / 128 = 46.9°.

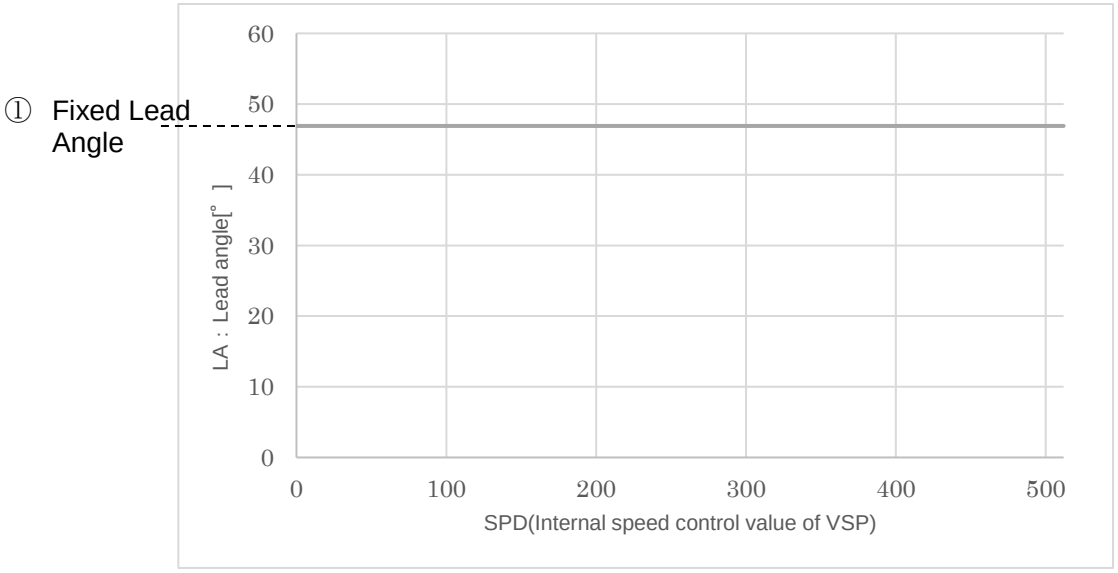


Fig.10.7.6.1 Settings of Fixed Lead Angle

10.7.7. Lead Angle 0°

When the “Lead Angle 0°” is selected, the Lead Angle remains 0° for any Speed Command SPD (Internal Speed Command Value).

10.8. Settings at FG pin

The Output Signal at the FG pin can be selected as shown below.
The Output Structure at the FG pin can also be selected.
The FG pin also plays the role of SDO for Serial Communication, but it can be selected to output the FG Function Signal even during the Serial Communication with the register settings.

Note: ・As for the FG function, no Rotation Pulse Signal is output for rotation below 1 Hz, except for the 3 ppr and 1 ppr settings.
・When the FG pin is set as an open drain output and a pull-up resistor is connected to a separate external power supply without using the VREG pin, voltage may be supplied from the separate external power supply to the power supply of this device via the FG pin. Even though a voltage is supplied from the FG pin, this device is not abnormally controlled as long as the FG pin is used within the specification range. But please note that this phenomenon may occur.

Table10.8.1 1 Selection of Output Signal Functions in Serial Communication at FG pin

Register settings 1[15] SR_FG	Output Signal at FG pin
0	SDO Function
1	FG Function

Table10.8.2 Selection of Output Structure at FG pin

Register settings 11[4] FG_OD	Selection of Output Structure at FG pin
0	Push-pull Output
1	Open Drain Output

Table10.8.3 Settings of Functions at FG pin

Register settings 10[3:0] FG_SEL	Poles	2	4	6	8	10	12	14	16
	Pole pairs	1	2	3	4	5	6	7	8
	ppr	Pulse per revolution							
0000	3.00	3.00	6.00	9.00	**12.00**	15.00	18.00	21.00	24.00
0001	2.40	2.40	4.80	7.20	9.60	**12.00**	14.40	16.80	19.20
0010	2.00	2.00	4.00	6.00	8.00	10.00	**12.00**	14.00	16.00
0011	1.71	1.71	3.43	5.14	6.86	8.57	10.29	**12.00**	13.71
0100	1.50	1.50	3.00	4.50	6.00	7.50	9.00	10.50	**12.00**
0101	1.00	1.00	2.00	3.00	**4.00**	5.00	6.00	7.00	8.00
0110	0.80	0.80	1.60	2.40	3.20	**4.00**	4.80	5.60	6.40
0111	0.67	0.67	1.33	2.00	2.67	3.33	**4.00**	4.67	5.33
1000	0.57	0.57	1.14	1.71	2.29	2.86	3.43	**4.00**	4.57
1001	0.50	0.50	1.00	1.50	2.00	2.50	3.00	3.50	**4.00**
1010	Failure Detection Signal								
1011									
1100									
1101									
1110									
1111									

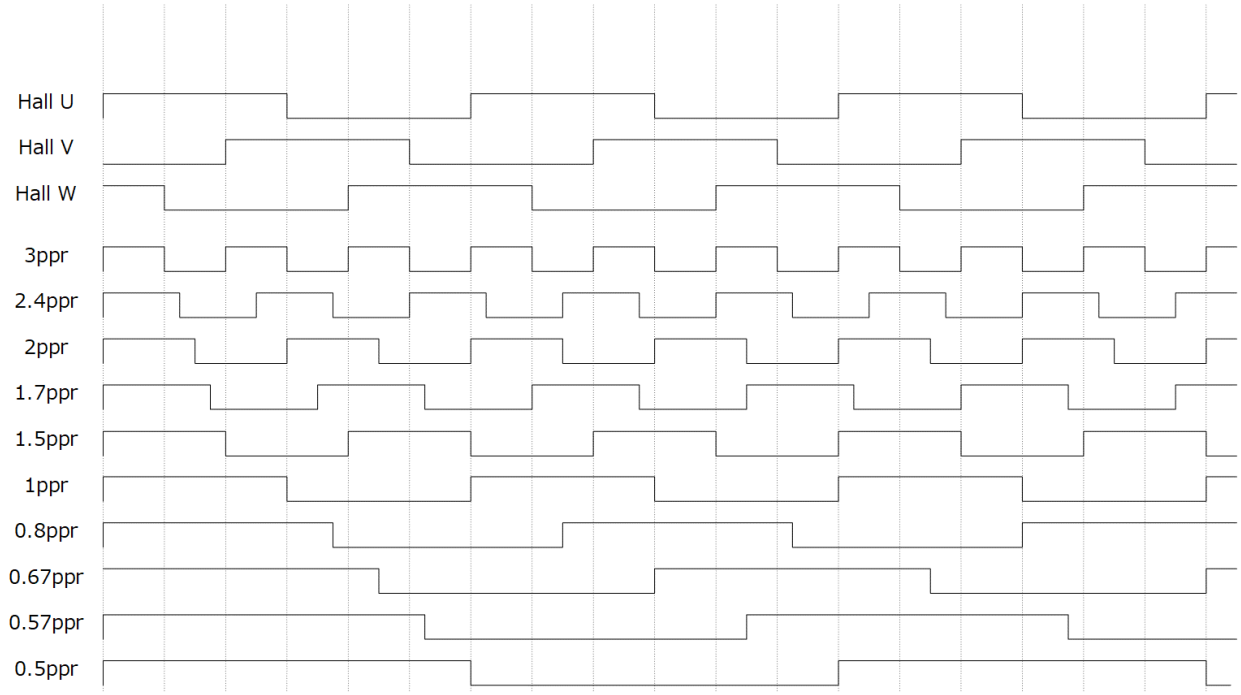


Fig.10.8.1 Timing Chart of Rotation Pulse Signal at FG pin

10.9. Settings at DIR pin

By setting the registers, the DIR pin can be switched to the following functional pin.
The forward/reverse rotation can be set with the rotation direction input.
The short brake can be set with the short brake input.
As for the Failure Detection Input, the Failure Stare and the Normal Operation can be switched in the same way as the RES pin.
(However, the timing for releasing the Failure State is not the carrier frequency timing as with the RES Pin does, but an immediate release to the Normal operation.)
The Rotation Direction Input, the Short Brake input, and the Failure Detection Input can also be set with the registers.

Note: ・Do not set the voltage to the DIR pin to 6.5 V or higher, which is outside range of the Operating Input Voltage, because the device is switched to the Test Mode.
・During short brake state, the short brake condition is prioritized over SPD=0 and Refresh Operation.

Fig.10.9.1 Setting of Functions at DIR pin

Register settings		Settings of input operation at DIR pin	Input voltage to DIR pin	State of Operation
12[2:1] DIR_SEL[1:0]	12[0] DIR_INV			
00	0	Non-inverted Input of Rotation Direction	HIGH	Reverse Rotation
			LOW/OPEN	Forward Rotation
	1	Inverted Input of Rotation Direction	HIGH	Forward Rotation
			LOW/OPEN	Reverse Rotation
01	0	Non-inverted Input of Forward Rotation	HIGH	Forward Rotation
			LOW/OPEN	Normal Operation
	1	Inverted Input of Short Brake	HIGH	Normal Operation
			LOW/OPEN	Forward Rotation
10	0	Non-inverted Input of Failure Detection	HIGH	Failure State: Motor Output OFF (Commutation Output = All Low)
			LOW/OPEN	Normal Operation
	1	Inverted Input of Failure Detection	HIGH	Normal Operation
			LOW/OPEN	Failure State: Motor Output OFF (Commutation Output = All Low)
11	0	Register Settings	-	Note
	1			

Note: The functions of the rotation direction input and short brake input that are not specified in the input operation settings at the DIR pin are the register settings.
As for the Failure Detection Input, either the register settings or the Failure Detection Input at the RES pin can be used to switch to the Failure State.

Table10.9.2 Register Settings of Rotation Direction Input

Register 12[4] DIR	Rotation Direction
0	Forward Rotation
1	Reverse Rotation

Table10.9.3 Register Settings of Short Break Input

Register 12[3] BRK_ON	Short Break
0	Normal Operation
1	Short Break

Table10.9.4 Register Settings of Failure Detection Input at DIR pin

Register 12[5] RES	Failure Detection Input
0	Normal Operation
1	Failure State

10.10. Setting pins for TC78B043FNG (Settings for HTSSOP28)

In the TC78B043FNG, the control that enables a specific motor to rotate has already been written to NVM as the initial setting. And by adjusting each register setting from the 4 pins (LA, FGC, LATYPE, LAOFS), the motor can be rotated by this Initial Setting without setting registers via SPI Communication. When the default setting is insufficient to rotate the motor and a readjustment of the register setting is required, the readjustment can be performed via SPI Communication.
Note: In the case of the TC78B043FTG (WQFN20), the registers of the four pins (LA pin, FGC pin, LATYPE pin, and LAOFS pin) are set Invalid. Please do not set them Valid, because the setting state is undefined when they set Valid.

10.11. Settings at LA pin

By inputting voltage to the LA pin, the setting of the register LA (maximum Lead value and fixed Lead value) is performed.
And by setting the register Valid or Invalid, the LA pin setting or the Register: LA setting is selectable.
For noise suppression, this device is designed as the settings do not change even though the input voltage fluctuates by ±2 LSB.

Table10.11.1 Setting at LA pin

Voltage to LA pin	Register name	Contents of Settings	Input range	Range of Setting Figure	Resolution
0 to 5 V	7[6:0] LA[6:0]	Maximum Lead Angle value /Fixed Lead Angle	0 to 127	0 to 59.5 °	60/128

Table10.11.2 Settings of LA pin and Register: LA Valid/Invalid

Register settings 11[1] VIN_MODE1	LA pin	Register 7[6:0] LA [6:0]
0	Invalid	Valid
1	Valid	Invalid

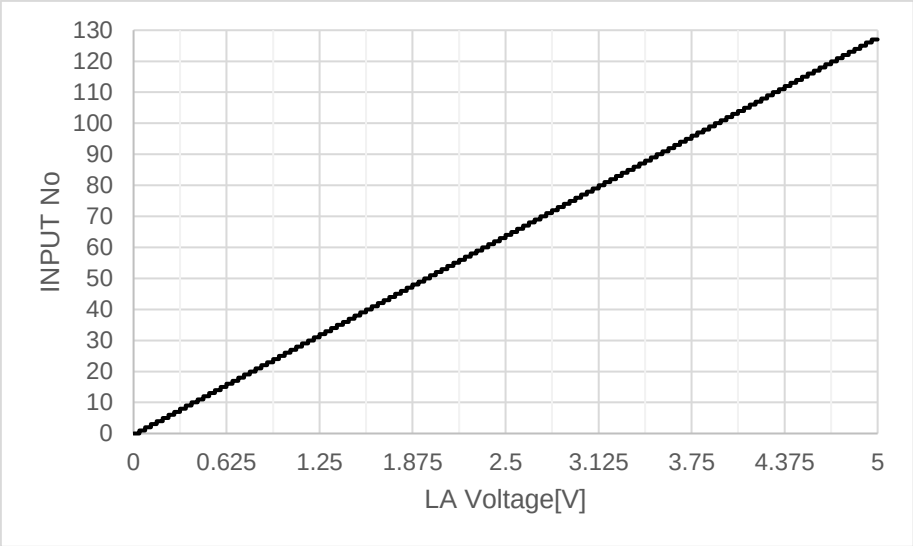


Fig.10.11.1 Setting of LA Voltage at LA pin

10.12. Setting at FGC pin

By inputting a voltage to the FGC pin, the registers for the number of pulses to the FG pin and for the Sine Wave reset method can be set. At startup, the forced Commutation of Sine Wave (60° reset method) is set.
And by setting the register Valid or Invalid, the setting of Pulse Number to the FG pin or the Register Setting is selectable.

Table10.12.1 Settings at FGC pin

No	Voltage to FGC pin	Pulses Number to FG pin	Sine Wave Reset Method
7	4.375V to 5V	3 ppr	60 °
6	3.75V to 4.375V	3 ppr	60 °⇔360 °
5	3.125V to 3.75V		
4	2.5.V to 3.125V	2.4 ppr	60 °⇔360 °
3	1.875V to 2.5V		
2	1.25V to 1.875V	2.4 ppr	60 °
1	0.625V to 1.25V		
0	0V to 0.625	2.4 ppr	60 °⇔60 °/ 120 °

Table10.12.2 Settings of FGC pin and Register Valid/Invalid

Register settings 11[0] VIN_MODE0	Settings at FGC pin	Register 10[3:0] FG_SEL[3:0]	Register 2[15:12] PWM_MODE[3:0]
0	Invalid	Valid	
1	Valid	Invalid	

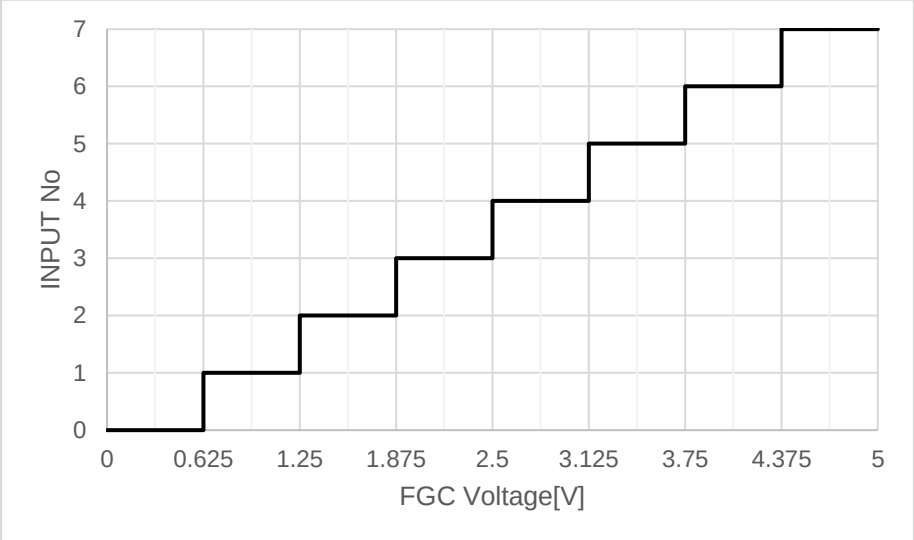


Fig.10.12.1 Settings of FGC Voltage at FGC pin

10.13. Setting at LATYPE pin

By inputting a voltage to the LATYPE pin, the Lead Angle Function and for the stop sequence can be set. And by setting the register Valid or Invalid, setting at LATYPELA pin or the register setting is selectable. For noise suppression, this device is designed as the settings do not change even though the input voltage fluctuates by ±1 LSB.

Table10.13.1 Settings at LATYPE pin

No	Voltage to LATYPE pin	Lead Angle Function	Stopping Sequence
63	4.92	Lead Angle in Quadratic Curve: LAoffset Valid	Valid
62	4.84		
61	4.77	Lead Angle in Quadratic Curve: SPDoffset Valid	
60	4.69		
59	4.61		
58	4.53		
57	4.45		
56	4.38		
55	4.30	Lead Angle in Linear Curve: LAoffset Valid	
54	4.22		
53	4.14		
52	4.06		
51	3.98		
50	3.91		
49	3.83	Lead Angle in Linear Curve: SPDoffset Valid	
48	3.75		
47	3.67		
46	3.59		
45	3.52		
44	3.44		
43	3.36	Lead Angle in Quadratic Curve with inflection point	
42	3.28		
41	3.20		
40	3.13		
39	3.05		
38	2.97		
37	2.89	Fixed Lead Angle	
36	2.81		
35	2.73		
34	2.66		
33	2.58		
32	2.50		
31	2.42	Fixed Lead Angle	Invalid
30	2.34		
29	2.27		
28	2.19		
27	2.11		
26	2.03		
25	1.95	Lead Angle in Quadratic Curve with Inflection point	
24	1.88		
23	1.80		
22	1.72		
21	1.64		
20	1.56		
19	1.48	Lead Angle in Linear Curve: SPDoffset Valid	
18	1.41		
17	1.33		
16	1.25		
15	1.17		
14	1.09		
13	1.02	Lead Angle in Linear Curve: LAoffset Valid	
12	0.94		
11	0.86		
10	0.78		
9	0.70		
8	0.63		
7	0.55	Lead Angle in Quadratic Curve: SPDoffset Valid	
6	0.47		
5	0.39		
4	0.31		
3	0.23		
2	0.16		
1	0.08	Lead Angle in Quadratic Curve: LAoffset Valid	
0	0.00		

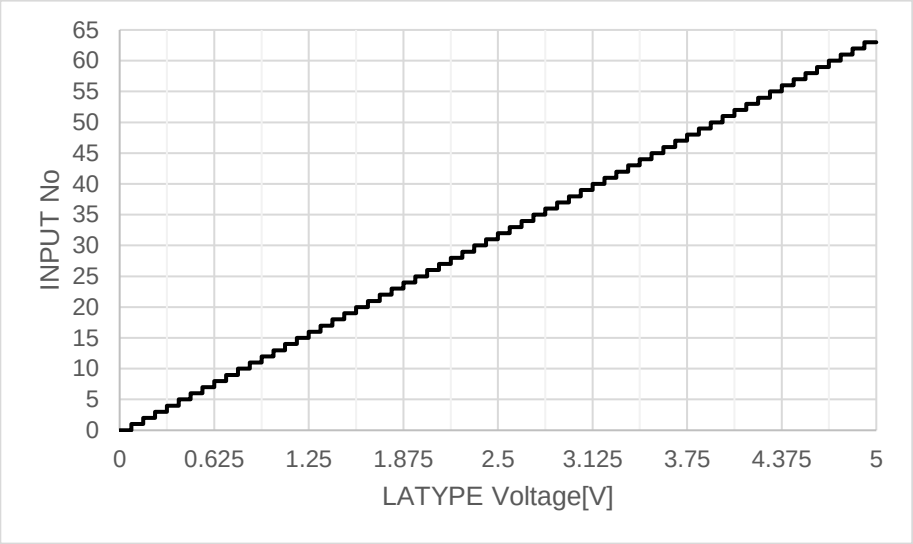


Fig. 10.13.1 Setting of LATYPE Voltage at LATYPE pin

Table 10.13.2 Settings of LATYPE pin and Register Valid/Invalid

Register settings 11[2] VIN_MODE2	Settings at the LATYPE pin	Register 7[15:13] LA_TYPE	Register 5[15] STOP_SEQ
0	Invalid	Valid	
1	Valid	Invalid	

10.14. Settings at LAOFS pin

By inputting voltage to the LAOFS pin, the registers for register “chg_spd” and “la_off/spd_off” can be set.
And by setting the register valid/invalid, the LAOFS pin setting or the register setting is selectable.
In the setting of the Lead Angle Function at the LATYPE pin, the LA offset can be set by inputting voltage to the LAOFS pin under the setting of "Lead Angle in Linear Curve: LA offset Valid" or "Lead Angle in Quadratic Curve: LA offset Valid".
The SPD offset can be set by inputting voltage to the LAOFS pin under the setting of “Lead angle in Linear curve SPD offset Valid” or “Lead angle in Quadratic Curve: SPD offset Valid”.
In case of the setting of the Lead Angle in a Quadratic Curve with Inflection Point, by inputting voltage to the LAOFS pin, the SPD value in Quadratic Curve with Inflection Point can be set.
For noise suppression, this device is designed as the settings do not change even though the Input Voltage fluctuates by ±2 LSB.
The SPD Value for the maximum Lead Angle value (register name: 8[7:0]MAX_SPD[7:0]) is set the Initial Value of 511.

Table10.14.1 Settings at LAOFS pin

Register name	Contents of Settings	Input Range	Range of Setting Figure	Resolution
9[15:8] CHG_SPD [7:0]	SPD Value in Quadratic Curve with Inflection Point	0 to 255	0 to 510	2/512
8[15:8] LA_OFF/SPD_OFF [7:0]	LA offset	0 to 63	0 to 29.5 °	60/128
	SPD offset	0 to 255	0 to 255	1/512

Table10.14.2 Settings of LAOFS pin and Register Valid/Invalid

Register settings 11[3] VIN_MODE3	Settings at LAOFS pin	Register 9[15:8] CHG_SPD[7:0]	Register 8[15:8] LA_OFF/SPD_OFF[7:0]
0	Invalid	Valid	
1	Valid	Invalid	

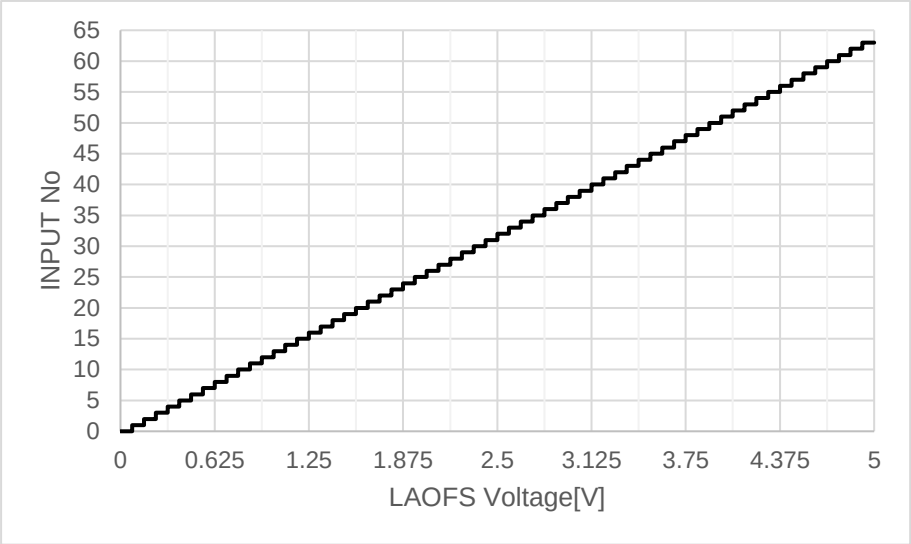


Fig10.14.1 Setting of LA Offset Voltage at LAOFS pin
(Refer to Table10.14.1 Settings at LAOFS pin)

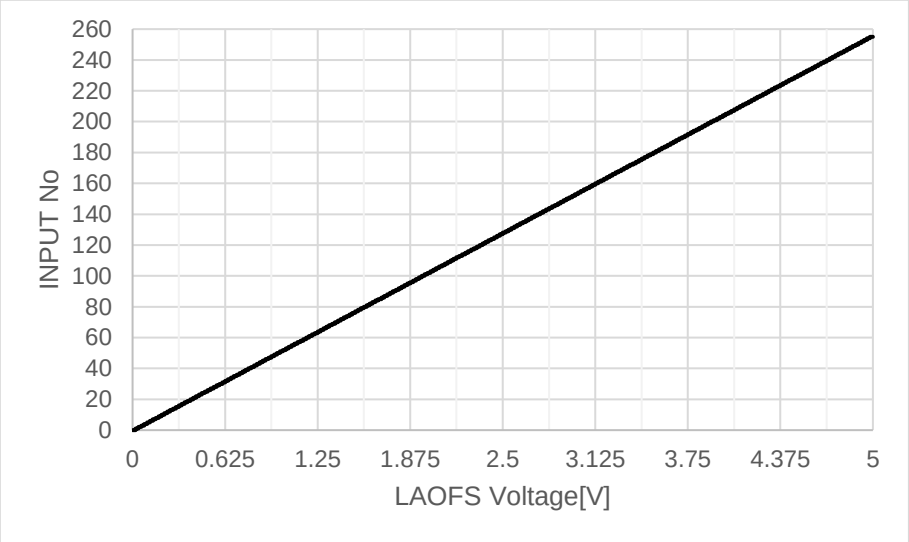


Fig.10.14.2 Settings at LAOFS pin: SPD Offset Voltage and SPD value in Quadratic Curve with Inflection point
(Refer to Table10.14.1 Settings at LAOFS pin)

10.15. Failure Detection Function

Each Failure Detection Function is built-in as shown below.
By setting the register, the Output Signal of the Failure Detection at the FG pin can be selected.
And the polarity of the Output Signal is also selectable.
In addition, after the Failure Detection is operated, the Failure Detection Output Signal continues to output the Failure State until the Failure Status is released, regardless of the Latch Mode or Automatic Recovery Mode.

Table10.15.1 Settings of Polarity of Output Signal for Failure Detection

Register settings 10[12] DET_INV	Normal Operation	Failure State
0	Low	High
1	High	Low

Table10.15.2 Settings of Output Signal for Failure Detection

Register settings 10[11:8] DET_SEL[3:0]	Output signal
0000	Composite signal of the following failures (all the Failure Detection) Current Limiting Function Over-current Detection Thermal Shutdown Detection Failure Detection Input Function Position Detection Signal Failure Function Lead Angle Limiting at High RPM Function Motor Lock Protection Function
0001	Composite signal of the following failures (except for Current Limiting Function) Over-current Detection Thermal Shutdown Detection Failure Detection Input Function Position Detection Signal Failure Function Lead Angle Limiting at high RPM Function Motor Lock Protection Function
0010	Current Limiting Function
0011	Over-current Detection
0100	Thermal Shutdown Detection
0101	Failure Detection Input Function
0110	Position Detection Signal Failure Function
0111	Lead Angle Limiting at High RPM Function
1000	Motor Lock Protection Function
1001	-
1010	-
1011	-
1100	-
1101	-
1110	-
1111	-

10.15.1. Current Limiting Function (at IDC pin)

The Current Limiting Function Valid or Invalid is selectable.
In the Sine Wave Drive, when the IDC pin voltage exceeds the Internal Reference Voltage of 0.5 V (typ.), either the setting of all the Commutation Signal Outputs turned Low, or the setting that the Driving Signals in the Low-side phase Outputs (UL, VL, WL) are output according to the Hall Signals as shown in the Timing Chart after all the High-side phase Outputs (UH, VH, WH) are turned Low can be selected. The current limit function is released at each carrier frequency.
And in case of the Square Wave Drive, the High-side phase Outputs (UH, VH, WH) are set to Low, when the IDC pin voltage exceeds the Internal Reference Voltage of 0.5 V (typ.).
The Low-side phase Outputs (UL, VL, WL) output driving signals according to the Hall Signal as shown in the Timing Chart and the Current Limiting Function is released at each carrier frequency. And during the Short Brake State the Current Limiting Function at the IDC pin is Invalid.

Table10.15.1.1 Settings of Sine Wave Drive Operation in Current Limiting Function

Register settings 10[13] IDC_SEL	Current Limiting Function
0	High-side Output (UH, VH, WH) set Low Low-side Phase Outputs (UL, VL, WL) output Driving Signals according to the Hall Signals as shown in the Timing Chart.
1	All the Commutation Output ＝Low

Table10.15.1.2 Settings of Current Limiting Function Valid/Invalid

Register settings 11[8] IDC_MASK	Current Limiting Function
0	Valid
1	Invalid

10.15.2. Over-current Detection (at IDC pin)

The Over-current Detection can be selected Valid/Invalid.
When the IDC pin voltage exceeds the Internal Reference Voltage of 0.8 V (typ.), all the Commutation Signal Outputs are turned Low.
For releasing this detection, the Automatic Recovery Mode or the Latch Mode is selectable.

Table10.15.2.1 Settings of Over-current Detection Valid/Invalid

Register settings 11[9] ISD_MASK	Over-current Detection
0	Valid
1	Invalid

Table10.15.2.2 Settings of Over-current detection Release

Register settings 11[10] ISD_LATCH	Mode	Settings of Releasing Over-current Detection
0	Automatic Recovery Mode	Automatic Recovery after 10 msec. Releasing by the Speed Command = 0, or by inputting Refresh Operation
1	Latch Mode	Releasing by the Speed Command = 0, or by inputting Refresh Operation

10.15.3. Thermal Shutdown Detection (TSD)

The Thermal Shutdown Detection can be selected Valid/Invalid.
The TSD is to turn all the Commutation Signal Outputs Low, when the junction temperature inside the device exceeds 165°C (typ.).
For releasing this detection, the Automatic Recovery Mode or the Latch Mode is selectable.

Table 10.15.3.1 Settings of Thermal Shutdown Valid/Invalid

Register settings 11[11] TSD_MASK	Thermal Shutdown
0	Valid
1	Invalid

Table10.15.3.1 Settings of Releasing Thermal Shutdown

Register settings 11[12] TSD_LATCH	Mode	Settings of releasing TSD
0	Automatic Recovery Mode	Automatic Recovery after dropping to the TSD releasing temperature 135°C (typ.)
1	Latch Mode	After dropping to the TSD releasing temperature 135°C (typ.), released by the Speed Command = 0 or by inputting Refresh Operation

10.15.4. Failure Detection Input Function (Reset Signal Input: the RES pin)

When the Input Signal level RES = High, the Commutation Signal Outputs are set to Low, and after setting RES = Low it is released for each carrier frequency to restarts. The polarity of the input can also be switched. When a Speed Command is input in Stop State, after 1.5 msec. of Refresh Operation driving signals are output to restart.
On the other hand, when a Speed Command is input in Rotation State, immediate driving signals are output to restart.
As the Internal Counter is still operating during the reset input, the FG signal is kept outputting.
And the RES pin can be used for monitoring the Motor Power Supply Voltage by attenuating the motor power supply voltage with a resistor divider and inputting it to this pin.
In addition, the RES pin is used as a role of the SCK for the Serial Interface Communication.
The Failure Detection Input Function can be turned ON/OFF by setting the register.

Table10.15.4.1 Setting of Polarity at RES pin

Register settings 10[5] RES_INV	Settings of Input at RES pin	Failure State All Commutation Output = Low	Normal Operation
0	Non-inverted Input	High	Low (OPEN)
1	Inverted Input	Low (OPEN)	High

Table10.15.4.2 Settings of Failure Detection Input Function Valid/Invalid

Settings of register 10[4] RES_ON	State
0	Normal Operation
1	Failure State All Commutation Output = Low

10.15.5. Position Detection Signal Failure Function

When the Position Detection Signal (the Internal Hall Amplifier Outputs) is H-H-H or L-L-L-L, all the Commutation Signal Outputs are set to Low (for the Gate Block protection), and the motor is restarted with any other signal combinations.
And when all the position input signals (HUP, HUM, HVP, HVM, HWP, HWM) are Open, all the Commutation Signal Outputs are also set to Low (for the Gate Block protection) and restarted with any other signal combinations.
In addition, the position detection signal (the internal Hall amplifier output) of the Sine Wave PWM Drive is configured a latch type, and the previous state is retained, when the position detection signal is different from the expected logic value. Therefore, the device is configured to avoid malfunction by minor noise or chattering.
The Position Detection Signal Failure Function can be selected Valid/Invalid.

Table 10.15.5.1 Settings of Position Detection Signal Failure Function Valid/Invalid

Register settings 11[13] HA_ERR_MASK	Position Detection Signal Failure
0	Valid
1	Invalid

10.15.6. Settings of Lead Angle Limiting at High RPM Function

When the rotation speed exceeds the high rotation detection frequency set by the register, the lead angle value is set to 0° or the motor outputs are turned off (all the Commutation Outputs = Low) according to the register setting of the limit function at high RPM. When the lead angle value is set to 0°, the lead angle is controlled to reduce to 0° at every 1-step after a high RPM is detected. And the releasing method is performed by the register setting to release the Lead Angle Limiting at High RPM Function.

Table 10.15.6.1 Settings and Releasing of Lead Angle Limiting at High RPM Function

Register settings 9[5:4]MAX_HZ_DECT [1:0]	High RPM frequency [Hz]	Example* 10-pole motor [rpm]	Example** 8-pole motor [rpm]	Register settings 9[7:6]MAX_HZ_RCY [1:0]	Releasing Operation of Lead Angle Limiting at High RPM	Releasing Frequency [Hz]	Example* 10-pole motor [rpm]	Example** 8-pole motor [rpm]
00	無効	-	-	-	-	-	-	-
01	250	3000	3750	00	Latch Mode: released by the Speed Command = 0 or Refresh Operation Input			
				01	Released at 25% drop of High Rotation Detection Frequency (Note)	188	2250	2813
				10	Released at 50% drop of High Rotation Detection Frequency (Note)	125	1500	1875
				11	Released at 75% drop of High Rotation Detection Frequency (Note)	63	750	938
10	417	5000	6251	00	Latch Mode: released by Speed Command = 0 or Refresh Operation Input			
				01	Released at 25% drop of High Rotation Detection Frequency (Note)	313	3750	4688
				10	Released at 50% drop of High Rotation Detection Frequency (Note)	208	2500	3125
				11	Released at 75% drop of High Rotation Detection Frequency (Note)	104	1250	1563
11	625	7500	9375	00	Latch Mode: released by Speed Command = 0 or Refresh Operation Input			
				01	Released at 25% drop of High Rotation Detection Frequency (Note)	469	5625	7031
				10	Released at 50% drop of High Rotation Detection Frequency (Note)	313	3750	4688
				11	Released at 75% drop of High Rotation Detection Frequency (Note)	156	1875	2344

Note: Releasing by the Speed Command = 0 or by inputting the Refresh Operation is also available.

Example*: When converted to 10-pole motor rpm
Example**: When converted to 10-pole motor rpm

Table 10.15.6.2 Setting of Limiting Function at High RPM

Register settings 9[2] MAX_HZ_FUNC	Limiting Function at High RPM
0	Lead Angle 0 °
1	Motor Output all OFF (all the Commutation Outputs = Low)

10.15.7. VCC Power Supply Monitoring (UVLO) and VREG Voltage Monitoring

The VCC power supply monitoring and the VREG monitoring functions are built-in, and the Commutation Signal Outputs are set to Low when either one of them falls below the Operating Voltage Range at power ON/OFF and so on.
And when the power is turned on during the Speed Command Input, drive signals are output to restart after 1.5 msec. of the Refresh Operation.
However, the operation of power supply restart is not guaranteed, because the circuit is unstable at power on.

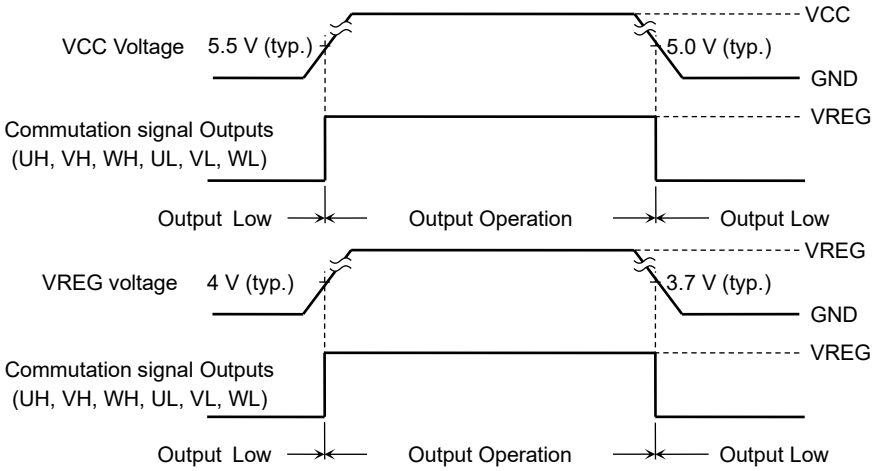


Fig.10.15.7.1 VCC Power Supply Monitoring (UVLO) and VREG Voltage Monitoring

10.15.8. Motor Lock Protection Function

The Motor Lock Protection Function is that a motor lock is detected and the Commutation Signal Outputs are set to Low, when the motor is in Stop State in spite of the Speed Command input and the motor is not rotated even after the driving period of TON (sec.).
During the Lock Detection State, the operation is repeated by maintaining the Stopping Period TOFF (sec.) and then shifting to the Driving Period TON (sec.) again.
The ratio of the Driving Period to the Stopping Period (all the Commutation signal Outputs = Low) is 1:6.
In case of the Sine Wave forced Commutation at Startup, when the rotation exceeds the rotation frequency setting of switching from the Forced Commutation within the Driving Period of TON (sec.), the motor enters rotation state to release the Motor Lock Detection state.
In the Square Wave setting at startup, when the Hall Signal is input for one cycle in sequence from the falling edge of the U-phase Hall Input Signal within the Driving Period TON, the motor enters rotation state to release the Motor Lock Detection State.
And when speed command = 0 or when a Refresh Operation is input, the Lock Detection State is reset and released.
Also, after the Stopping Period TOFF(s), driving signals are output to restart the motor after 1.5 msec. of Refresh Operation.
The Motor Lock Protection Function Valid/Invalid is selectable.

Note: The Motor Lock Protection Function does not operate when the Short Brake Function is turned ON.

Table 10.15.8.1 Settings of Recovery Method from Motor Lock Protection Function

Register settings 11[15] LOCK_LATHC	Recovery method
0	Automatic Recovery Mode TON time : TOFF time = 5 sec. : 30 sec. Released by Speed Command = 0 or by inputting Refresh Operation
1	Latch Mode Released by Speed Command = 0 or by inputting Refresh Operation

Table 10.15.8.2 Motor Lock Protection Function Valid/Invalid

Register settings 11[14] LOCK_MASK	Motor Lock Protection Function
0	Valid
1	Invalid

10.16. Settings of Oscillation Frequency

The Oscillation Frequency can be selected as shown in the table below.
When the Oscillation Frequency is changed, the frequency and the period controlled based on that oscillation frequency are also changed.

Table 10.16.1 Settings of Oscillation Frequency

Register settings:12[15:14] OSC_SEL[1:0]	00	01	10	11	Remarks
Oscillation Frequency fosc [MHz] (typ.)	8.7	10.24	11.26	-	
PWM Frequency [kHz] (typ.)	17	20	22	-	fosc/512
Forced Commutation Frequency [Hz] (typ.)	0.85	1	1.1	-	
Frequency of switching from Square Wave to Sine Wave [Hz] (typ.)	0.85	1	1.1	-	
Frequency of Switchover from Forced Commutation [Hz] (typ.)	1.7	2	2.2	-	00
	3.4	4	4.4	-	01
	4.25	5	5.5	-	10
	6.8	8	8.8	-	11
Reference Frequency of returning from Idle Rotation [Hz] (typ.)	142	166.7	183	-	01
	213	250	275	-	10
	354	416.7	458	-	11
Bootstrap Period [ms] (typ.)	1.8	1.5	1.4	-	
Acceleration/Deceleration/Stop Sequence Deceleration Period [ms] (typ.)	3.8	3.2	2.9	-	
Motor Lock TON Period [s] (typ.)	5.9	5	4.5	-	
Motor Lock TOFF Period [s] (typ.)	35.3	30	27.3	-	
Dead Time 1 hour [µs] (typ.)	1.03	0.88	0.80	-	9/fosc
Dead Time 2 hours [µs] (typ.)	2.07	1.76	1.60	-	18/fosc
Lead Angle Limiting Frequency at High RPM [Hz] (typ.)	213	250	275	-	01
	354	416.7	458	-	10
	531	625	688	-	11
Input Digital Filter period [µs] (typ.)	2.06	1.76	1.6	-	18/fosc

10.16.1. Dead Time Function (Output High-side/Low-side OFF Time)

The Dead Time is generated digitally inside the device to prevent short circuits caused by simultaneous ON of the High-side/Low-side Outputs of External Power Elements in the Sine Wave PWM Drive. (The Dead Time Function also operates during the Full Duty of the Square Wave Drive to prevent short circuits.)

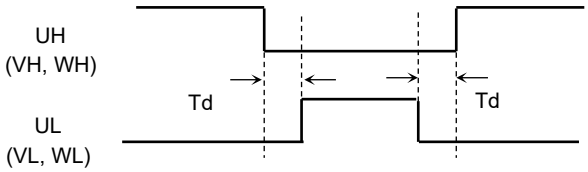


Fig.10.16.1.1 Dead Time Function

Table 10.16.1.1 Settings of Dead Time

Register settings 10[6] DT_SEL	Settings	Dead Time Td	fosc=8.7 MHz (typ.) Td	fosc=10.24 MHz (typ.) Td	fosc=11.26 MHz (typ.) Td
0	Dead Time 1	9/fosc	1.03 µs	0.88 µs	0.80 µs
1	Dead Time 2	18/fosc	2.07 µs	1.76 µs	1.60 µs

fosc : Reference Clock (Oscillation Frequency)

10.17. Settings of Serial Interface

The contents of the internal registers and NVM can be set via the Serial Interface.
The RES pin, the VSP pin and the FG pin are used for SCK, SDI, and SDO respectively.
After accepting Instruction Code of the Serial Communication as shown below, the device enters the Serial (SPI) Mode.

Note: While receiving the Instruction Code of serial communication for starting the serial mode, the device is in control of the Refresh Action or all the motor outputs OFF according to the operation setting of the VSP pin and the RES pin. (In accordance with SCK Low or High at RES pin the Normal Operation and the Failure State are repeated, and in accordance with SDI Low or High at VSP pin the Output all OFF and the Refresh Operation of 1.5 msec. period during the Speed Command ON are repeated.)

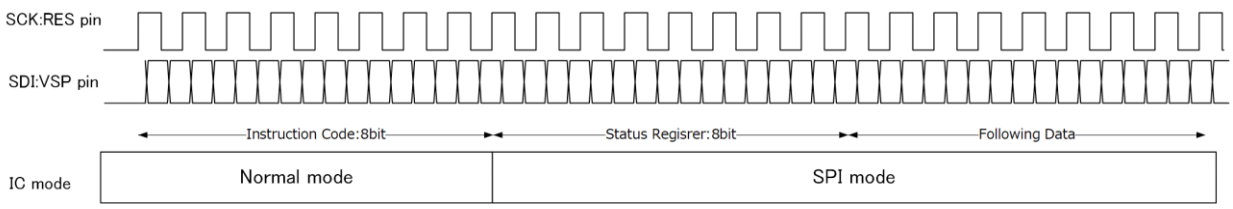


Fig. 10.17.1 Serial Interface Timing Chart

Table 10.17.1 Serial Command (Instruction Code)

Command name	Instruction Code	Description	Following data
SR_READ	010 01 001	Reading out the Status Register	8-bit data out
SR_WRITE	010 01 010	Writing down the Status Register	8-bit data in
REG_READ	010 10 001	Reading from the Normal Register	8-bit addr in + 16-bit data out
REG_WRITE	010 10 010	Writing down to the Normal Register	8-bit addr in + 16-bit data in
NVM_LOAD	010 11 001	Loading the contents of NVM to the Normal Register	none
NVM_SAVE	010 11 010	Saving the contents of the Normal Register to NVM	none
NVM_ABORT	010 11 100	Forcing termination of writing process to NVM	none

Table 10.17.2 Status Register (SR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	NVM_WR	-	ENB	BUSY

Table 10.17.3 Details of Status Register

Name	Description
BUSY	State of register processing BUSY=0：Waiting BUSY=1：Under processing (REG_READ, REG_WRITE, NVM_LOAD, NVM_SAVE,NVM_COPY in execution)
ENB	Serial Mode setting ENB=0: Normal mode, only SR_READ SR_WRITE is accepted ENB=1: Serial mode, all commands accepted
NVM_WR	NVM Mode setting NVM_WR=0: READ Valid, WRITE Invalid NVM_WR=1: READ Invalid, WRITE Valid

Table 10.17.4 Serial Interface

Characteristics		Symbol	Test condition	Min.	Typ.	Max.	Unit
SCK(RES)	Input voltage	VSCK(H)	High voltage	2.0	-	-	V
		VSCK(L)	Low voltage	-	-	0.8	V
		VSCK(hys)	Hysteresis voltage	-	200	-	mV
	Input frequency	fSCK	Note1, Note2	15	-	250	kHz
	High period	tW	Note1	2	-	-	µsec.
	Low period	tWL	Note1	2	-	-	µsec.
SDI (VSP)	Input voltage	VSCK(H)	High voltage	2.0	-	-	V
		VSCK(L)	Low voltage	-	-	0.8	V
		VSCK(hys)	Hysteresis voltage	-	200	-	mV
	Set up time	tSDIS	-	1	-	-	µsec.
	Hold time	tSDIH	-	500	-	-	nsec.
SDO(FG) Set up time		tSDOS	Note1	-	-	1000	nsec.

Note1:The specification value will be for when the FG pin output structure is selected as push-pull output. If you select the FG pin output structure as open-drain output, due to pull-up resistance values and substrate capacitance, etc., a delay may occur in the SDO signal, and there is a possibility that the specification value of the SDO(FG) Set up time may be exceeded. In that case, please consider the delay, take measures such as setting SCK to a lower input frequency, and use serial communication.

Note2: Input frequency of serial signal SCK below 15 kHz is invalid

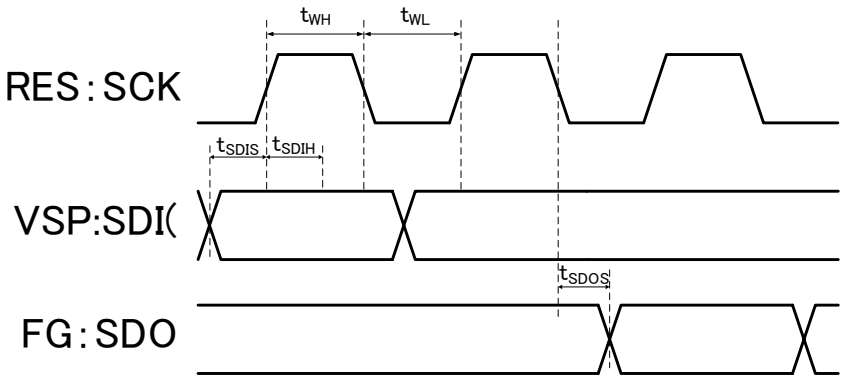


Fig. 10.17.2 Serial Interface Timing Chart

・Procedure for writing to the Normal Registers

1. Instruction Code: SR_WRITE input: 010 01 010
2. Status Register: ENB=1 input: 000 00 010
3. Instruction Code: REG_WRITE input: 010 10 010
4. Following data: 8-bit addr in + 16-bit data in

・To continue writing to the register

5. Instruction Code: REG_WRITE input: 010 10 010
6. Following data: 8-bit addr in + 16-bit data in

・To repeat 5. & 6. to continue writing to the register.

・To exit the serial mode

7. Instruction Code: SR_WRITE input: 010 01 010
8. Status Register: ENB=0 input: 000 00 000

・Procedure for reading the Normal Registers

1. Instruction Code：SR_WRITE input: 010 01 010
2. Status Register：ENB=1 input: 000 00 010
3. Instruction Code：REG_READ input: 010 10 001
4. Following data: 8-bit addr in + 16-bit data out

・To continue reading the registers

5. Instruction Code：REG_READ input: 010 10 001
6. Following data: 8-bit addr in + 16-bit data out

・To repeat 5. & 6. to continue writing to the register.

・To exit the serial mode

7. Instruction Code：SR_WRITE input: 010 01 010
8. Status Register：ENB=0 input: 000 00 000

・Procedure for reading the Status Registers

1. Instruction Code：SR_READ input: 010 01 001
2. Following data：8-bit data out

・To exit the serial mode

3. Instruction Code：SR_WRITE input: 010 01 010
4. Status Register：ENB=0 input: 000 00 000

・Procedure for writing the contents of Normal Registers to Non-volatile Memory (NVM)

1. Instruction Code：SR_WRITE input: 010 01 010
2. Status Register：ENB=1 input: 000 00 010
3. Instruction Code：NVM_SAVE input: 010 11 010
4. Status Register：NVM_WR=1 input: 000 01 000

・To check whether writing to NVM is completed

5. Instruction Code：SR_READ input: 010 01 001
6. Status Register：BUSY=1 output: 000 00 001: Processing
   BUSY=0 Output: 000 00 000: Completed

・To force termination of writing process to NVM

7. Instruction Code：NVM_ABORT input: 010 11 100

・To exit the serial mode

8. Instruction Code：SR_WRITE input: 010 01 010
9. Status Register：ENB=0 input: 000 00 000

・Procedure for loading the contents of Non-volatile Memory (NVM) into Normal Registers

1. Instruction Code：SR_WRITE input: 010 01 010
2. Status Register：ENB=1 input: 000 00 010
3. Instruction Code：NVM_LOAD input: 010 11 001

・To exit the serial mode

5. Instruction Code：SR_WRITE input: 010 01 010
6. Status Register：ENB=0 input: 000 00 000

10.17.1. How to read out the written contents in NVM by using only the VSP pin and the FG pin

When the Power Supply VCC is applied after inputting a voltage of 7.75 V < VSP ≤ 10 V to the VSP pin, the data written to NVM is first output from the FG pin so that the NVM settings can be read.
First, the fixed value: 10101010 01011010 is output from the FG pin, then 16 bits are output in order from address 0 to 15. Then, as in Normal Operation, the motor starts rotating in the Outgoing Test Mode after the Refresh Operation 1.5 msec. (typ.) and the Startup Control.

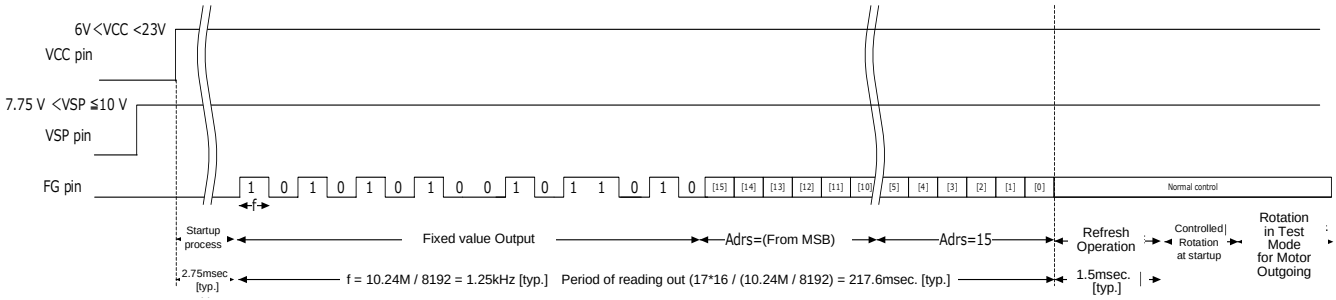


Fig. 10.17.1.1 Timing Chart

10.17.2. Registers

The default figure of NVM at outgoing differs between the TC78B043FTG (WQFN20) and the TC78B043FNG (HTSSOP28).

Table 10.17.2.1 Resister Map

ADDRESS	Bit	Name	Description	Valid NVM Yes: Y No: -	Read: R Write: W	Initial Figure TC78B043FTG: WQFN20	Initial Figure TC78B043FNG: HTSSOP28
0	15:0	USERID	Free	Y	R/W	0	0
1	15	SR_FG	Selection of Output Signal Function Selection during Serial Communication at FG pin	Y	R/W	0	0
1	14:8	STOPDUTY[6:0]	Settings of Stopping Duty	Y	R/W	0	0
1	7:0	STARTDUTY[7:0]	Settings of Duty at Startup	Y	R/W	0	0
2	15:12	PWM_MODE[3:0]	Settings of Driving Waveform	Y	R/W	0	0
2	11:8	-	-	Y	R/W	0	0
2	7:0	MAXDUTY[7:0]	Settings of Maximum Duty	Y	R/W	0	0
3	15:8	-	-	Y	R/W	0	0
3	7:0	STARTOUTDUTY[7:0]	Settings of Minimum Output Duty	Y	R/W	0	0
4	15:14	-	-	Y	R/W	0	0
4	13:0	DUTYSLOPE[13:0]	Settings of Acceleration Slope	Y	R/W	0	0
5	15	STOP_SEQ	Settings of Stop Sequence Valid/Invalid	Y	R/W	0	0
5	14:12	-	-	Y	R/W	0	0
5	11:8	DWN_DUTY_CHANGE_LIMIT[3:0]	Settings of Output Duty for Sequence of Deceleration and Stopping	Y	R/W	0	0
5	7:4	UP_DUTY_CHANGE_LIMIT[3:0]	Settings of Output Duty for Acceleration	Y	R/W	0	0
5	3:0	SS_DUTY_CHANGE_LIMIT[3:0]	Settings of Output Duty for Acceleration at Startup	Y	R/W	0	0
6	15:13	TRQ_SEL[2:0]	Settings of Speed Command	Y	R/W	0	0
6	12:8	-	-	Y	R/W	0	0
6	7:6	HZ_RANGE[1:0]	Settings of Reference Frequency for Initial Output Duty at returning from Idle Rotation	Y	R/W	0	0
6	5:4	AVE_SEL[1:0]	Settings of Averaging Number in Sine Wave Drive	Y	R/W	0	3
6	3:2	SIN_SW_RATIO[1:0]	Settings of Rotation Speed Fluctuation for switching in Sine Wave Reset Method	Y	R/W	0	0
6	1:0	START_FREQ[1:0]	Settings of Rotation Frequency to switch from Forced Commutation	Y	R/W	0	0
7	15:13	LA_TYPE[2:0]	Settings of Lead Angle Function	Y	R/W	0	0
7	12:7	-	-	Y	R/W	0	0
7	6:0	LA[6:0]	Selection of Maximum/Fixed Lead Angle value	Y	R/W	0	0
8	15:8	LA_OFF/SPD_OFF[7:0]	Settings of LA offset and SPD offset	Y	R/W	0	0
8	7:0	MAX_SPD[7:0]	Settings of SPD Figure of Maximum Lead Angle value	Y	R/W	0	255
9	15:8	CHG_SPD[7:0]	Settings of SPD Figure for Quadratic Curve with Inflection Point	Y	R/W	0	0
9	7:6	MAX_HZ_RCY[1:0]	Settings of Releasing Operation from Limiting Function at High RPM	Y	R/W	0	3
9	5:4	MAX_HZ_DECT[1:0]	Settings of High RPM Detection Frequency	Y	R/W	0	2
9	3	-	-	Y	R/W	0	0

ADDRESS	Bit	Name	Description	Valid NVM Yes: Y No: -	Read: R Write: W	Initial Figure TC78B043FTG: WQFN20	Initial Figure TC78B043FNG: HTSSOP28
9	2	MAX_HZ_FUNC	Settings of High RPM Limiting Function	Y	R/W	0	0
9	1:0	-	-	Y	R/W	0	0
10	15:14	-	-	Y	R/W	0	0
10	13	IDC_SEL	Settings of Sine Wave Drive Operation at Current Limiting	Y	R/W	0	0
10	12	DET_INV	Settings of Polarity of Failure Detection Output Signal	Y	R/W	0	0
10	11:8	DET_SEL[3:0]	Setting of Failure Detection Output Signal	Y	R/W	0	0
10	7	BOOT_ON	Settings of Refresh Operation	Y	R/W	0	0
10	6	DT_SEL	Settings of Dead Time	Y	R/W	0	0
10	5	RES_INV	Setting of Input Polarity at RES pin	Y	R/W	0	0
10	4	RES_ON	Settings of Failure Detection Input	Y	R/W	0	0
10	3:0	FG_SEL[3:0]	Settings of Functions at FG pin	Y	R/W	0	0
11	15	LOCK_LATHC	Settings of Recovery Method from Motor Lock Protection	Y	R/W	0	0
11	14	LOCK_MASK	Settings of Motor Lock Protection Valid/Invalid	Y	R/W	0	0
11	13	HA_ERR_MASK	Settings of Position Detection Signal Failure Function Valid/Invalid	Y	R/W	0	0
11	12	TSD_LATCH	Settings of release from Thermal Shut Down Detection	Y	R/W	0	0
11	11	TSD_MASK	Settings of Thermal Shut Down Detection Valid/Invalid	Y	R/W	0	0
11	10	ISD_LATCH	Settings of release from Over-current Detection	Y	R/W	0	0
11	9	ISD_MASK	Settings of Over-current Detection Valid/Invalid	Y	R/W	0	0
11	8	IDC_MASK	Settings of Current Limiting Function Valid/Invalid	Y	R/W	0	0
11	7	C_RST_MASK	Settings of Triangular Wave Reset Function (0: Invalid, 1: Valid)	Y	R/W	0	0
11	6	SHIP_MASK	Settings of High-voltage Input to VSP pin Operation Mode Valid/Invalid	Y	R/W	0	0
11	5	SHIP_CHG	Settings of Operations of High-voltage Input to VSP pin Operation Mode	Y	R/W	0	0
11	4	FG_OD	Selection of Output Structure at FG pin	Y	R/W	0	0
11	3	VIN_MODE3	Settings of LAOFS pin and the Register Valid/Invalid	Y	R/W	0	1
11	2	VIN_MODE2	Settings of LATYPE pin and the Register Valid/Invalid	Y	R/W	0	1
11	1	VIN_MODE1	Settings of LA pin and the Register Valid/Invalid	Y	R/W	0	1
11	0	VIN_MODE0	Settings of FGC pin and the Register Valid/Invalid	Y	R/W	0	1
12	15:14	OSC_SEL[1:0]	Settings of Oscillation Frequency	Y	R/W	0	1
12	13:6	-	-	Y	R/W	0	0
12	5	RES	Settings of Failure Detection Input at DIR pin	Y	R/W	1	0
12	4	DIR	Settings of Rotation Direction Input	Y	R/W	0	0
12	3	BRK_ON	Settings of Short Brake	Y	R/W	0	0
12	2:1	DIR_SEL[1:0]	Setting of Functions at DIR pin	Y	R/W	0	0
12	0	DIR_INV	Settings of Input Polarity at DIR pin	Y	R/W	0	0
13	15:6	TRQ_DUTY[9:0]	Settings of Speed Command value	-	R/W	0	0
13	5:1	-	-	-	R/W	0	0
13	0	SHIP_MODE	Settings of High-voltage Input to VSP pin Operation Mode Valid/Invalid	-	R/W	0	0

11. Absolute Maximum Ratings (Ta = 25 °C)

11.1 Absolute Maximum Ratings (Ta = 25 °C unless otherwise specified)

Characteristics	Symbol	Rating	Unit	Related pin and Remarks
Power suppy voltage	MVCC	25	V	VCC
Input voltage	MVIN1	- 0.3 ~ 25	V	VSP
	MVIN2	- 0.3 ~ VREG+ 0.3	V	HUP, HVP, HWP, HUM, HVM, HWM, FGC, LATYPE, LAOFS, LA
	MVIN3	- 0.3 ~ 6	V	RES, DIR,
	MVIN4	VREG+ 0.3	V	IDC
Output voltage	MVout1	6	V	VREG, FG
	MVout2	- 0.3 ~ VREG+ 0.3	V	UH, VH, WH, UL, VL, WL
Output current	MIOUT	2	mA	UH, VH, WH, UL, VL, WL, FG
VREG output current	MIVREG	35	mA	VREG
Power dissipation	PD1	1.14	W	WQFN20: Note 1
	PD2	1.81	W	HTSSOP28: Note 2
Operating temperature	Topr	- 40 ~ 115	°C	Operating Temperature Range is determined by the PD-Ta characteristic. Please pay attention to design not to exceed the maximum junction temperature (Tj (max) = 150 °C).
Storage temperature	Tstg	- 55 ~ 150	°C	-
Junction temperature	Tjmax	150	°C	-

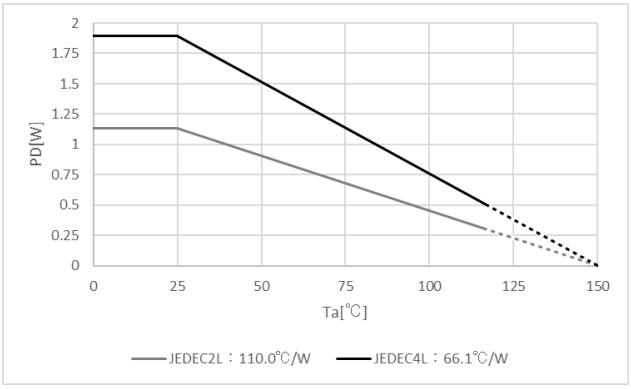
The Absolute maximum ratings are specifications that must not be exceeded even momentarily. Exceeding the absolute maximum ratings may cause destruction, degradation, or damage to the device, and may also cause destruction, damage, or degradation to other than the device. Therefore, in designing the product, please pay attention not exceed the absolute maximum ratings under any operating conditions. In use of this device, please use it within the specified operating range.

Note 1: In case mounted on a JEDEC-compliant 2-layer board (Ta = 25 °C), derating with (by) 9.1mW/°C is required when Ta exceeds 25 °C.

Note 2: In case mounted on a JEDEC-compliant 2-layer board (Ta = 25 °C), derating with (by) 14.5mW/°C is required when Ta exceeds 25 °C.

11.1. Power Dissipation Characteristics (Reference data)

TC78B043FTG(WQFN20)



TC78B043FNG(HTSSOP28)

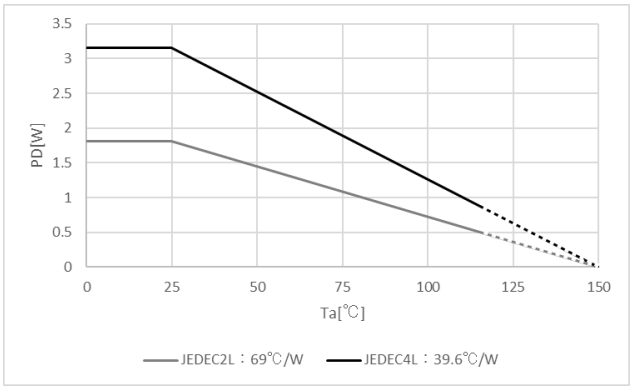


Fig. 11.1.1 Power Dissipation Characteristics

12. Operating Range

Table 12.1 Operating Range (Ta= - 40 to 115 °C unless otherwise specified)

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltaga	VCCopr1	6	15	23	V	VCC
	VCCopr2	10.8	15	23	V	VCC VCC Supply Voltage Range at writing to NVM
Speed command voltage input	VSPopr	0	-	7.3	V	VSP: Normal Control
	VSPoprT	8.2	-	10	V	VSP: Test Mode
Speed command PWM input	fVSPpwm	1	-	100	kHz	VSP: PWM Input
SPI Input CLK Frequency	fspi	15	-	500	kHz	RES

Table 12.2 NVM Characteristics

Characteristics	Condition	Min.	Max.	Unit
Number of Rewrite Cycles	Tj = 0 to 90 °C	10	-	Cycle

13. Electrical Characteristics (VCC=15V,Ta=25°C unless otherwise specified)

Table 13.1 Electrical Characteristics

Characteristics		Symbol		Test conditions	Min.	Typ.	Max.	Unit
Power supply current		ICC		VREG = OPEN	1	2.5	4	mA
Input current		IIN1		VIN = 5 V : VSP	17	33	70	µA
		IIN2		VIN = 5 V : HUP, HVP, HWP, HUM, HVM, HWM,FGC,LATYPE,LAOFS,LA (Note1)	-1	0	1	
		IIN3		VIN=5 V : RES,DIR,FGC,LATYPE,LAOFS,LA (Note1)	35	50	75	
		IIN4		VIN = 1 V :IDC	-1	0	1	
Input voltage		VIN1	H	DIR	2	-	-	V
			L	DIR	0	-	0.8	
			Hys	DIR (Reference value)	-	0.2	-	
		VIN2	HVTH	RES	1.8	1.9.	2	V
			LVTH	RES	1.7	1.8	1.9	
			Hys	RES (Reference value)	-	0.1	-	
		TSP	H	VSP:PWM Duty Input	2	-	-	V
			L	VSP:PWM Duty Input	0	-	0.8	
			Hys	VSP:PWM Duty Input	-	0.2	-	
		VSPA	T	PWM Max, ON Duty → High Voltage Input to VSP pin Operation Mode	7.3	7.75	8.2	V
			H	Motor in operation → PWM Max, ON Duty	5.1	5.4	5.7	
			M	Refresh Operation → Output Duty Operation started	1.8	2.1	2.4	
			L	Commutation OFF → Refresh Operation	0.7	1.0	1.3	
		VSPB	T	PWM Max, ON Duty → High Voltage Input to VSP pin Operation Mode	7.3	7.75	8.2	V
			H	Motor in operation → PWM Max, ON Duty	4.7	5	5.3	
			M	Refresh Operation → Output Duty Operation started	0.1	0.2	0.3	
AD input voltage STEP width		VAD64		LATYPE (Reference value)	-	0.078	-	V
		VAD8		FGC (Reference value)	-	0.625	-	V
		VAD128		LA (Reference value)	-	0.039	-	V
		VAD64		LAOFS (Reference value)	-	0.078	-	V
		VAD256		LAOFS (Reference value)	-	0.019	-	V
Hall element	Input sensitivity	VS		Differential Input	40	-	-	mVpp
	Common mode range	VW		-	0.2	-	3.5	V
	Input hysteresis	VHhys		(Reference value)	±1.5	±8.5	±15	mV
Hall IC input		VHIN	H	HUP, HVP, HWP: HUM, HVM, HWM = VREG/2	VREG - 1	-	VREG	V
			L		0	-	0.8	
Output voltage		VOUTH		IOUT = -2 mA: UH, VH, WH, UL, VL, WL, FG	VREG - 0.78	VREG - 0.3	-	V
		VOUTL		IOUT = 2 mA: UH, VH, WH, UL, VL, WL, FG	-	0.3	0.78	
		VREGA		VREG = 0 mA	4.7	5.0	5.3	
		VREGB		VREG = -35 mA	4.7	5.0	5.3	
Output leakage current		ILH		VOUT = 0 V: UH, VH, WH, UL, VL, WL, FG	-	0	1	µA
		ILL		VOUT = VREG: UH, VH, WH, UL, VL, WL, FG	-	0	1	
Output off time1 (Dead		TOFF1(17)		-	0.98	1.03	1.10	µs

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
time)	TOFF1(20)	-	0.83	0.88	0.93	
	TOFF1(22)	-	0.75	0.80	0.85	
Output off time2 (Dead time)	TOFF2(17)	-	1.95	2.07	2.20	µs
	TOFF2(20)	-	1.66	1.76	1.87	
	TOFF2(22)	-	1.51	1.60	1.70	
Oscillation frequency	fosc(17)	-	8.19	8.70	9.22	MHz
	fosc(20)	-	9.63	10.24	10.84	
	fosc(22)	-	10.60	11.26	11.93	
PWM frequency (Carrier frequency)	FC(17)	-	16	17	18	kHz
	FC(20)	-	18.8	20	21.2	
	FC(22)	-	20.7	22	23.3	
Forced commutation frequency	Fst(17)	(Reference value)	0.8	0.85	0.9	Hz
	Fst(20)	(Reference value)	0.9	1	1.1	
	Fst(22)	(Reference value)	1.04	1.1	1.16	
Motor lock detection ON time	TON (17)	(Reference value)	5.5	5.9	6.2	s
	TON(20)	(Reference value)	4.7	5	5.3	
	TON(22)	(Reference value)	4.3	4.5	4.8	
Motor lock detection OFF time	TOFF (17)	(Reference value)	33.2	35.3	37.4	s
	TOFF(20)	(Reference value)	28.2	30	31.8	
	TOFF(22)	(Reference value)	25.7	27.3	28.9	
Output maximum ON width (Sine Wave/150 ° Commutation/120 ° Commutation without Refresh Operation)	TON180MAX	fosc=10.24 MHz (Reference value)	-	98 (Note2)	-	%
Output maximum ON width (120 ° commutation with Refresh Operation)	TON120MAX	fosc=10.24dMHz (Reference value)	-	88.5 (Note2)	-	%
Current limiting voltage	VIDC	IDC	0.475	0.5	0.525	V
Over-current detection voltage	VIDCO	IDC	0.76	0.8	0.84	V
Current detection input delay	TIDC	IDC (Reference value)	-	3.2	-	µs.
VCC power supply monitoring	VCC(H)	Output Operation Starting Point	5.0	5.5	5.9	V
	VCC(L)	Output Operation Stopping Point	4.5	5	5.5	
	VCC(Hys)	Input Hysteresis Width (Reference value)	-	0.5	-	
VREG voltage monitoring	VREG(H)	Output Operation Starting Point	3.7	4	4.3	V
	VREG(L)	Output Operation Stopping Point	3.4	3.7	4	
	VREG(Hys)	Input Hysteresis Width (Reference value)	-	0.3	-	
Thermal shut down	Ttsdd	Thermal Shut Down Detection Temperature (Reference value)	150	165	180	°C
	Ttsdhys	Thermal Shut Down Detection Hysteresis Temperature (Reference value)	20	30	40	
	Ttsdr	Thermal Shut Down Release Temperature (Reference value)	120	135	150	

Reference values: It is the designed value and no outgoing test is performed.

Note1: LAOFS, LATYPE, LA, FG pins correspond to the input current IIN2 item when the setting of register setting 11[3:0] VIN_MODE3,2,1,0 is 1, and correspond to the input current IIN3 item when the setting is 0.

Note2: The value of the Maximum Output ON width is the designed values, because the output duty cycle is controlled by the logic circuit. But this value may differ slightly due to delays caused by load capacitance and other factors.

14. TC78B043FTG (WQFN20) Application Circuit Example

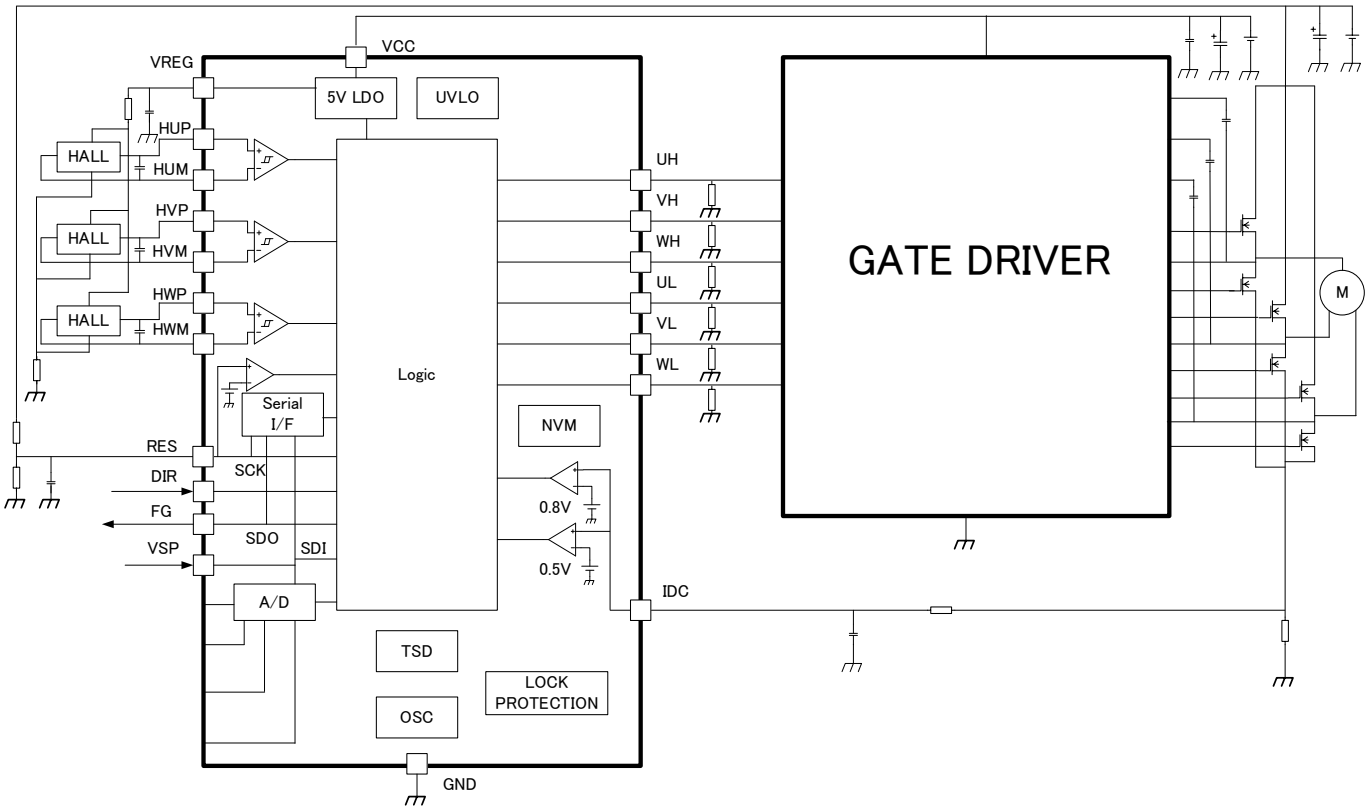


Fig. 14.1 Application Circuit Example

Note: The application circuit example has been partially omitted or simplified to explain the circuit.

15. 1TC78B043FNG (HTSSOP28) Application Circuit Example

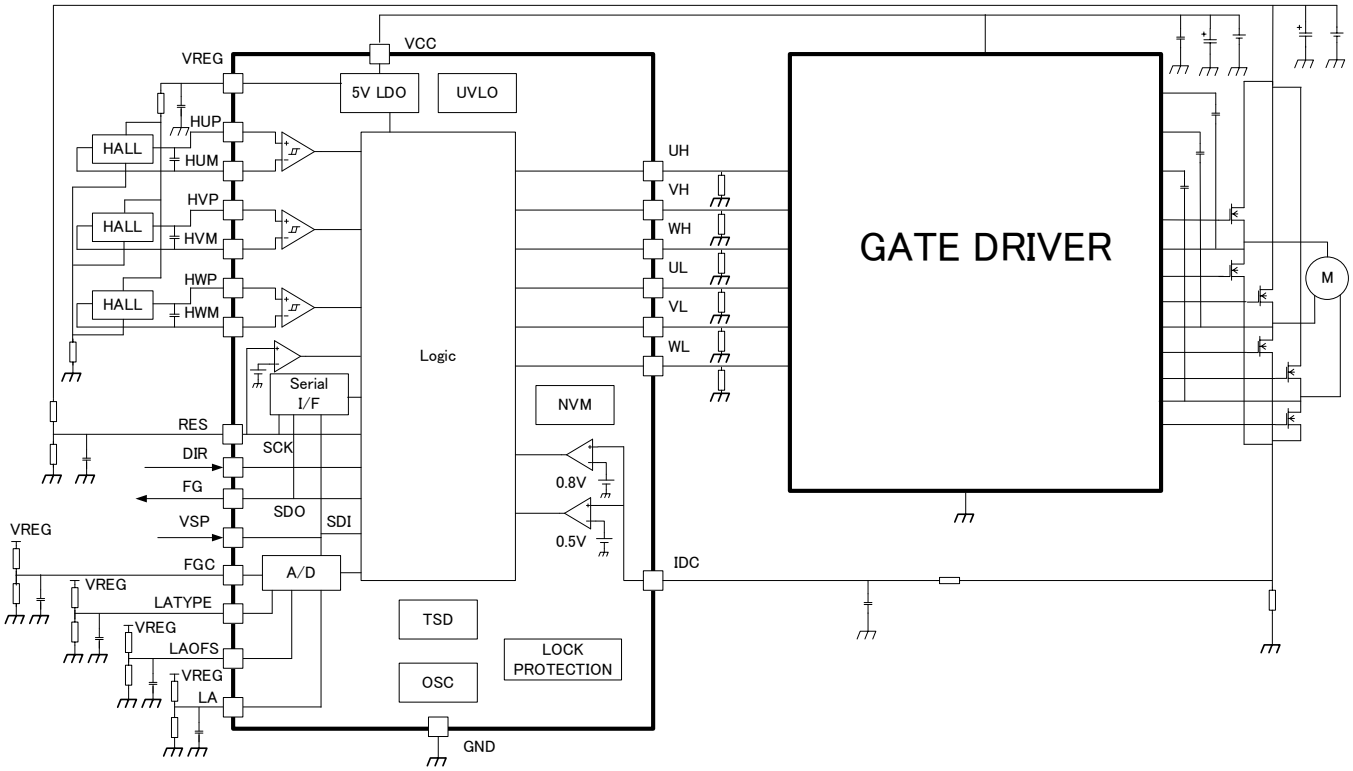
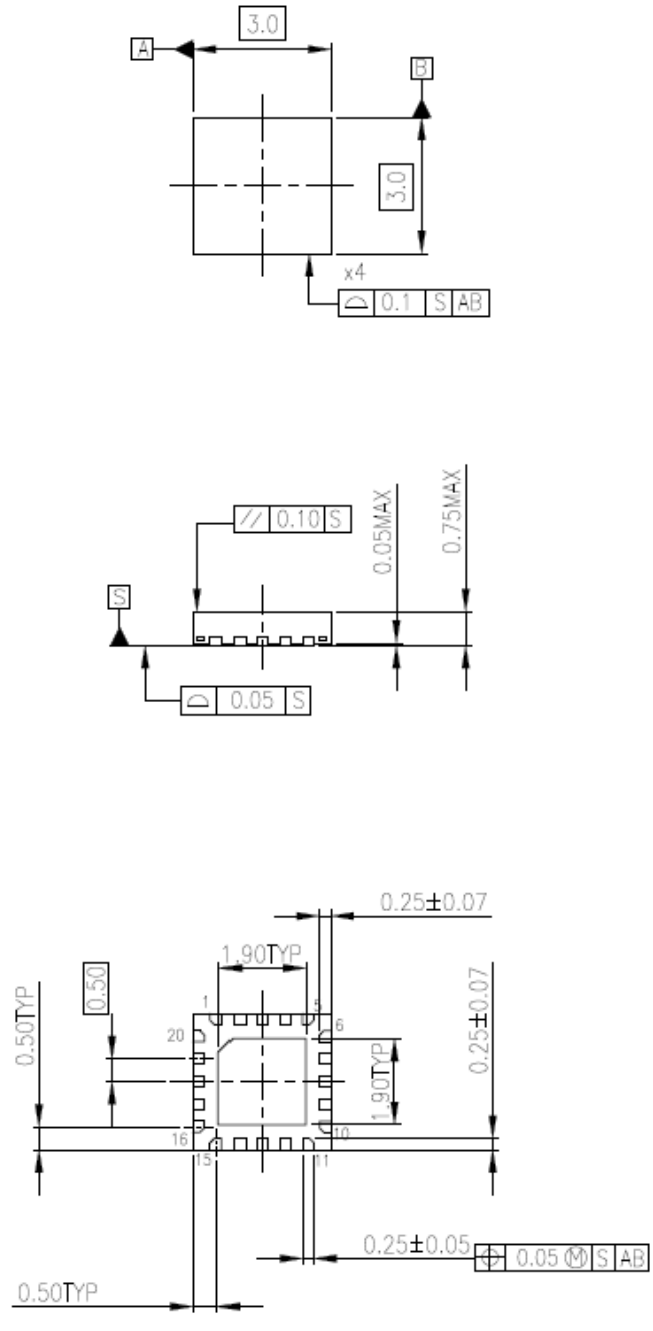


Fig. 15.1 Application Circuit Example

Note: The application circuit example has been partially omitted or simplified to explain the circuit.

16. TC78B043FTG Package Dimensions

Package dimensions
P-WQFN20-0303-0.50-002 "Unit:mm"



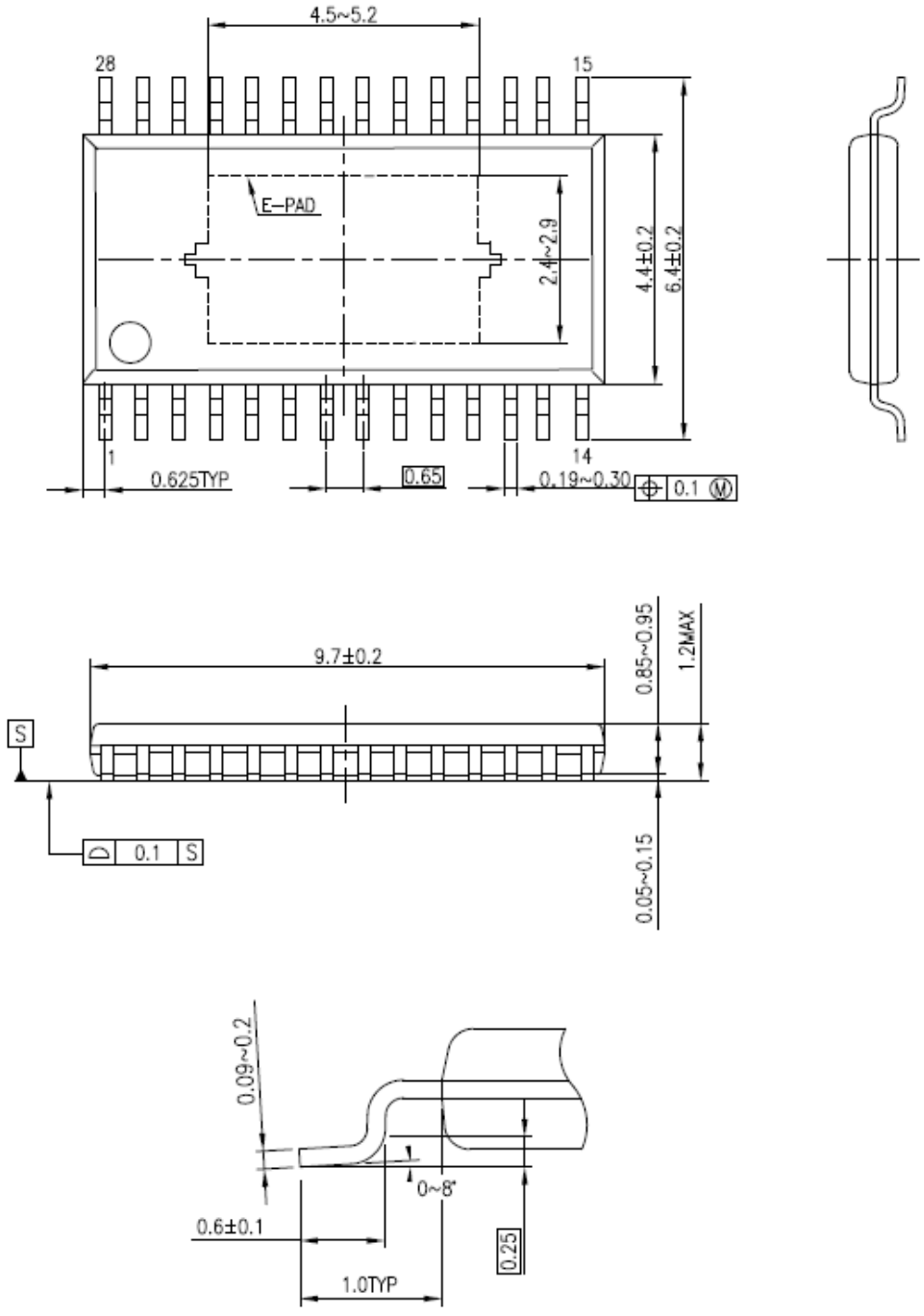
Weight: 0.02 g (typ.)

Table 16.1. Package Dimensions

17. TC78B043FNG Package Dimensions

Package dimensions
P–HTSSOP28–0510–0.65–001

"Unit:mm"



Weight: 0.10 g (typ.)

Fig. 17.1. Package Dimensions

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified or explanatory purposes.

2. Input / Output Equivalent Circuit

The equivalent circuit diagrams may be simplified for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage. Providing these application circuit examples does not grant a license for industrial property rights.

IC Usage Considerations

Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(3) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(4) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

Points to Remember on Handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor reverses the rotation direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, Class 3 medical devices, equipment used for automobiles, and military vehicles and munitions. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**