10kW 3-Phase AC 400V Input PFC Converter

Design Guide

RD263-DGUIDE-01

Toshiba Electronic Devices & Storage Corporation

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1. Introduction

This design guide describes the design overview of each circuit block of the 10kW 3-Phase AC 400V Input PFC Power Supply (hereafter referred to as "this design").

This design can provide 10kW at the output DC 750V. 3-phase AC power supply (312V to 528V) is input, and DC 750V is output in a 3-phase totem pole configuration employing a 1200V SiC MOSFET. It can be applied to various industrial equipment with 3-phase AC power input, such as charging stations for electric vehicles.

The PFC stage uses our latest 1200V SiC MOSFET TW060N120C, which contributes to low power loss. The TLP5214A gate driver photocoupler is used for isolated gate driving of the MOSFETs, and the TLP7920 optically isolation amplifier is used for isolated sensing of the input and output voltages.

2. Main Components

This chapter describes the main components used in this design.

2.1. SiC MOSFET TW060N120C

This design uses the 1200V SiC MOSFET (TW060N120C) as the switching device, with a configuration that directly switches each phase. The main features of the TW060N120C are as follows:

- Chip design of 3rd generation (Built-in SiC schottky barrier diode)
- Low diode forward voltage: V_{DSF} = -1.35V (Typ.)
- High voltage: V_{DSS} = 1200V
- Low drain-source on-resistance: $R_{DS(ON)}$ = 60mΩ (Typ.)
- Less susceptible to malfunction due to high threshold voltage: V_{th} = 3.0 to 5.0V
  (V_{DS} = 10V, I_D = 4.2mA)
- Enhancement mode

Appearance and Terminal Layout

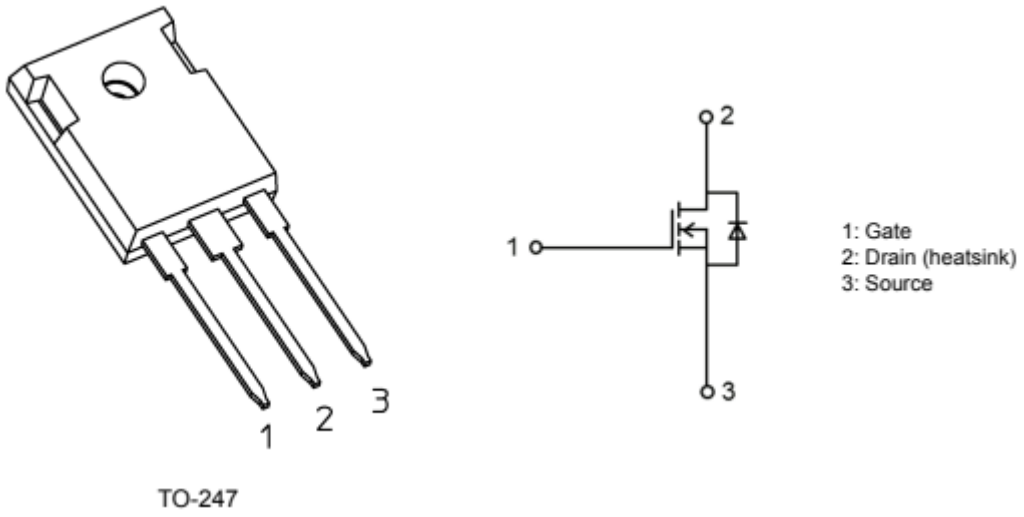


Fig. 2.1 Appearance and Terminal Layout of TW060N120C

2.2. Gate Driver Photocoupler TLP5214A

This design uses the TLP5214A for isolated driving of the MOSFET.
The main features of the TLP5214A are as follows:

- Peak output current: ±4.0A (Max.)
- Guaranteed performance over temperature: -40 to 110°C
- Supply current: 3.8mA (Max.)
- Power supply voltage: 15V to 30V
- Threshold input current: 6mA (Max.)
- Propagation delay time: 150ns (Max.)
- DESAT leading edge blanking time: 1.1μs (Typ.)
- Common-mode transient immunity: ±35kV/μs (Min.)
- Isolation voltage: 5000Vrms (Min.)
- Safety standards
  UL-recognized: UL 1577, File No.E67349
  cUL-recognized: CSA Component Acceptance Service
  No. 5A, File No.E67349
  VDE approved: EN 60747-5-5, EN 62368-1
- Creepage Distance: 8.0mm (Min.)

Appearance and Block Diagram

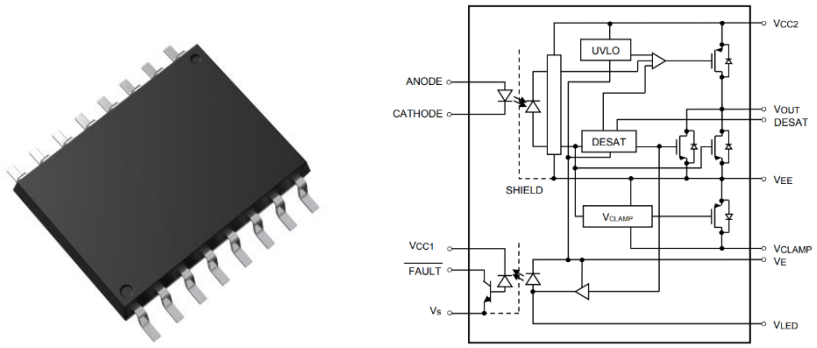


Fig. 2.2 Appearance and Block Diagram of TLP5214A

2.3. Optically Isolation Amplifier TLP7920

This design uses the optically isolation amplifier TLP7920 for isolated sensing of input and output voltages.

The main features of the TLP7920 are as follows:

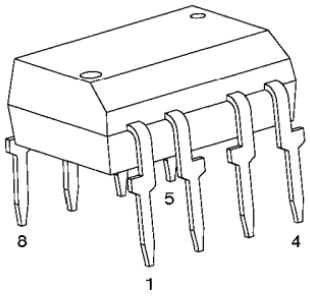
- Output side supply voltage: 3.0 to 5.5V
- Output side supply current: 6.2mA (Typ.)
- Operating temperature range: -40 to 105℃
- Common-mode transient immunity: 15kV/μs (Min.)
- Safety standards

  UL-recognized: UL 1577, File No.E67349

  cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349

  VDE-approved: EN IEC 60747-5-5

Appearance and Pin Configuration Diagram



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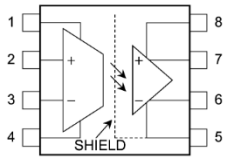

Pin No.	Symbol	Description
1	V_{DD1}	Input side supply voltage
2	V_{IN+}	Positive input
3	V_{IN-}	Negative input
4	GND1	Input side ground
5	GND2	Output side ground
6	V_{OUT-}	Negative output
7	V_{OUT+}	Positive output
8	V_{DD2}	Output side supply voltage

Fig. 2.3 Appearance and Pin Configuration Diagram of TLP7920

3. Circuit design

This section describes the points of circuit design of this design.

3.1. AC line circuit design

This section describes the AC line design of this design. The AC line circuit of this design is shown in Fig. 3.1.

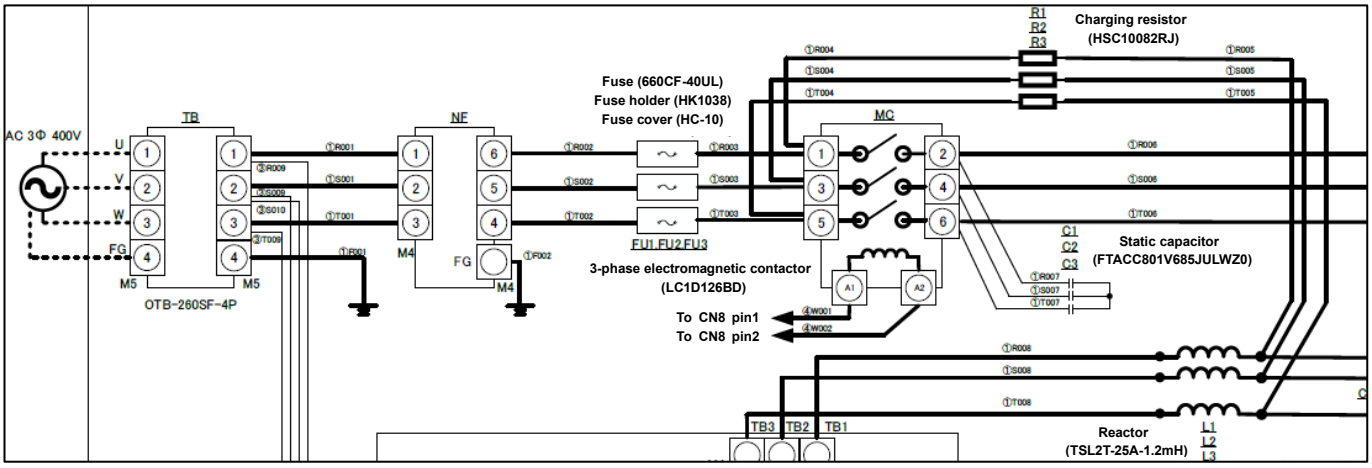

Fig. 3.1 AC Line Circuit

Fuse

Fuses (FU1, FU2, FU3) are installed to shut off the AC line when abnormal current flows through the AC line. Select a fuse from the maximum current value of the AC line. The effective value of the maximum AC line input current is calculated by the following formula.

Maximum

AC line input current = maximum power/power supply efficiency/power factor/input phase voltage effective value (min)/3

This design has a 3-phase AC 400V system for input and 10kW for output. Generally, the power supply efficiency of the PFC is lower when the input voltage is low. Therefore, when calculating the AC line maximum current value, consider that the input voltage is 312V, the lowest value in the input range of this design. When the line voltage is 312V, the phase-to-phase voltage is 180 V. Therefore, assuming that the input phase voltage rms value = 180 , the maximum power = 10kW, the power supply efficiency = 97%, and the power factor = 0.99, the maximum AC-line current value of this design is approximately 19.3A. 40A fuses are used in this design, taking into account the margins of fusing times. When selecting a fuse, it is necessary to consider the inrush current when the AC power is turned on, whether the product has obtained the safety standards to be complied with, etc., in addition to the above maximum current.

Inrush current countermeasures

Resistors (R1, R2, R3) are installed to suppress inrush current when the AC power is turned on. The resistance value must be set according to the maximum input current flowing through the AC line. Since the maximum input current is 20A in this design, the resistance value is calculated from the following equation.

Resistance > Maximum Input Phase Voltage/Maximum Input Current

When the maximum input line voltage of this design is 528V, the phase-to-phase voltage is 305 V as an effective value, and the peak voltage at that time is 431V. Therefore, assuming that the maximum input current is 20A, the resistance value is approximately 22Ω from the above equation.

This design uses an 82Ω resistor for margin considerations. The current value is 5.25A when an 82Ω resistor is used.

3.2. PFC circuit design

Inductor selection

This section explains how to select inductors (L1, L2, L3). The inductance value in this circuit can be calculated using the following items, which are power supply specifications.

- Max. output power: P_{out} (W)
- Ac-line minimum-phase effective voltage: V_{in_min} (V)
- PFC power conversion efficiency: η (%)
- PFC-output voltage: V_{out} (V)
- Switching frequency: F_c (Hz)
- Allowable ripple current width: ΔI_{ripple} (%)

Calculate the inductance value using the following formula.

$$L = \frac{\left(V_{out} - \sqrt{2} \times V_{in\_min}\right) \times \eta \times 0.01 \times {V_{in\_min}}^2}{F_c \times 0.01 \times \Delta I_{ripple} \times P_{out} \times V_{out}}$$

Here, assuming that the maximum output power (P_{out}) is 10kW, the minimum phase-to-phase voltage (V_{in_min}) of the AC line is 180V, the PFC output voltage (V_{out}) is 750V, the switching frequency (F_c) is 50kHz, the PFC power conversion efficiency (η) is 97%, and the allowable ripple current width is 30%, the above equation shows that the calculated inductance value (L) is 138μH. Therefore, the setting value of this design is 1.2mH considering the margin.

In the actual design, the inductance value of the inductor varies depending on the DC bias characteristics. Select a component that can secure the above calculated value with the inductance value decreased due to DC bias characteristics.

Gate drive circuit

Fig. 3.2 shows the gate drive circuit of the lower arm of the U-phase as a typical gate drive circuit. The design of the gate drive circuit affects power supply efficiency and EMI noise. Generally, power supply efficiency and EMI noise have a trade-off relationship, so it is necessary to design both in a balanced manner. The gate drive circuit of this design can adjust the switching speed of MOSFET. If you need to reduce the noise at turn-on of MOSFET, changing the gate series resistor (R48) to a large value may reduce EMI noise. Note that if the gate series resistor is changed to a large value, not only the turn-on speed of MOSFET but also the turn-off speed will be reduced, which may result in a worsening of the power supply efficiency. Only MOSFET turn-off speed should be increased in order to reduce power-efficiency degradation in this situation. Changing the gate-series resistor (R46) to a small value may only increase the turn-off speed of MOSFET and reduce the power-efficiency degradation of the system. When changing the gate series resistor, it is necessary to confirm that the EMI noise, power efficiency performance, and heat dissipation performance required for the system are satisfied.

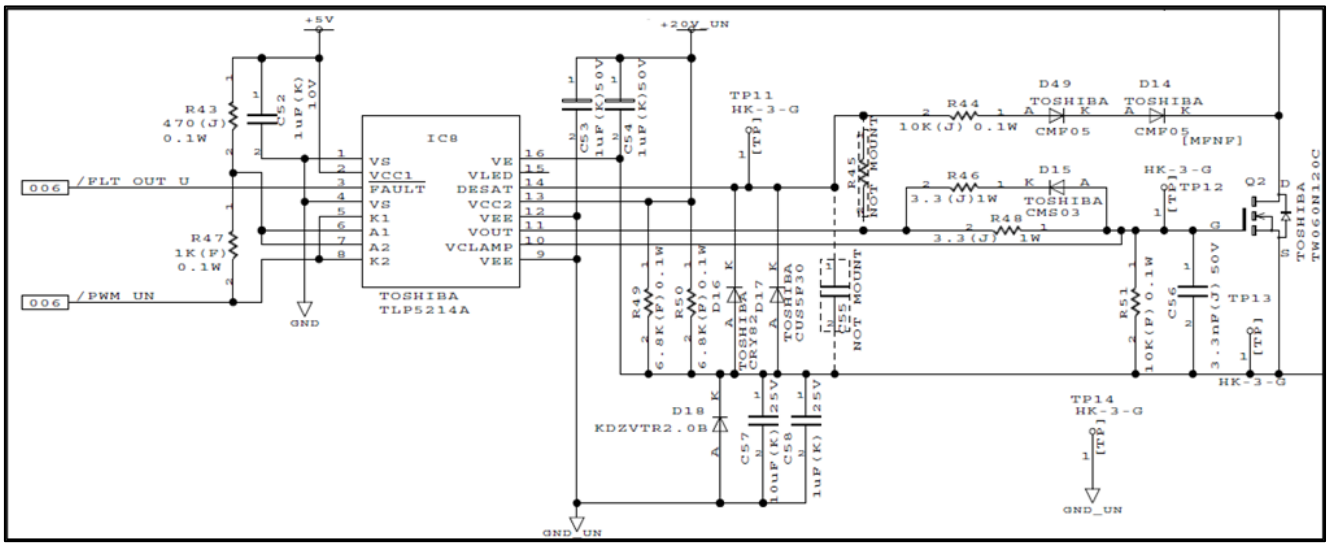

Fig. 3.2 Gate Drive Circuit (U-Phase Lower Arm)

Negative bias circuit

Use a negative-bias circuit if there is a risk of malfunction due to the parasitic mirror capacitance between the drain-gate of MOSFET. Fig. 3.2 shows the gate drive circuit that is used for the lower arm. When the lower arm is turned off and the upper arm is turned on, the intermediate potential rises steeply and displacement current is generated through the mirror capacitance between the drain-gate of the lower arm MOSSET, and flows toward VOUT terminal of the gate driver photocoupler (IC8). When this displacement current passes through the gate resistor of the circuit, a voltage drop occurs, and when the gate voltage rises, the lower arm may be faultily turned on, resulting in a short circuit of the upper and lower arms. By using a negative bias circuit using a Zener diode (D18), the gate voltage becomes negative when the lower arm is turned off, thereby preventing fault turning-on. This design uses a 2V zener diode to make a -2V negative bias circuit.

Output Capacitor

The capacitance of the output capacitor (C147 to C152) is calculated based on the hold-up time requirement. The hold-up time Thold is calculated by the following equation, assuming that the capacitance of the output capacitor is Cout, the output voltage is V_{out_PFC}, the lower limit voltage of the output voltage is V_{min}, and the maximum output power is P_{out}.

$$T_{hold} = C_{out} \times \frac{({V_{out\_PFC}}^2 - {V_{min}}^2)}{2 \times P_{out}}$$

The default setting is C_{out} = 705μF, V_{out_PFC} = 750V, V_{min} = 700V, and Pout = 10kW. The hold-up time is 2.56ms. Adjust the capacitance of the output capacitor to satisfy the hold-up time required for the system. In addition, when the output ripple specification is defined, the capacity required to satisfy the output ripple specification must be calculated and compared with the capacity that satisfies the hold-up time, and a large capacity value must be used. In addition, tolerances and aging degradation must be considered when selecting a capacitor.

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