32-bit RISC Microcontroller
Reference Manual

Non Break Debug Interface (NBDIF-A)

Revision 1.1

2025-08

Toshiba Electronic Devices & Storage Corporation

Contents

List of Figures

List of Tables

Preface

Related Document

Document name
Clock Control and Operation Mode
Memory Map
Input/ Output Ports
Product Information

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: [ABCD]<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

Terms and Abbreviations

The following words are terms or abbreviations mainly used in this datasheet.

AHB	Advanced High performance Bus
DMA	Direct Memory Access
NBD	Non Break Debug

1. Outline

The Non Break Debugging Interface (NBDIF) is an interface of the 4 bits width which supports the debug function using the conformity tool of the NBD protocol.

Note: DTS INSIGHT Corporation gives a definition and exhibited. For detail of NBD, please refer to disclosed documents by DTS INSIGHT Corporation.

Function classification	Function	Functional description
Data read-out	RAM monitor	Data is read from RAM and the register inside a chip during CPU operation.
Data writing	Dynamic tuning	Data is written in RAM and the register inside a chip during CPU operation.

2. Configuration

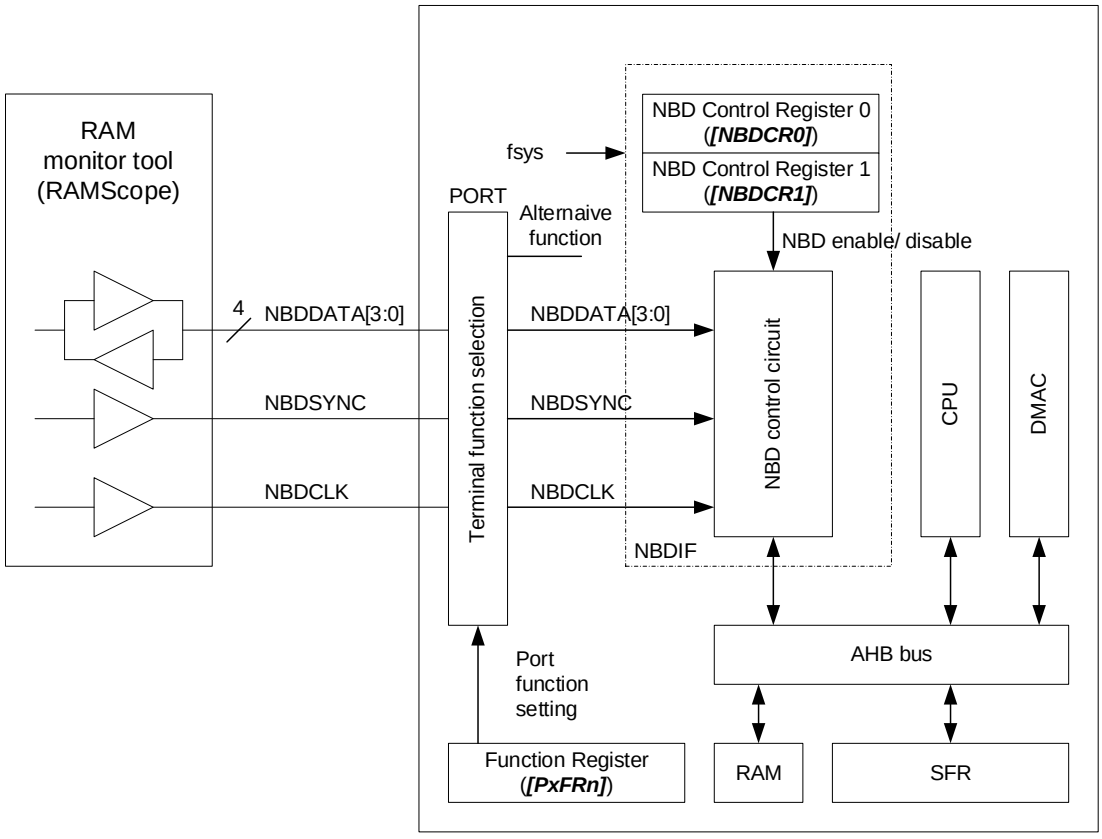


Figure 2.1 Configuration of NBDIF

Table2.1 Signal Table

No.	Signal name	Signal name	I/O	Related reference manual
1	fsys	System clock	Input	Clock Control and Operation Mode
2	NBDCLK	NBD clock	Input	Input/Output ports
3	NBDSYNC	NBDSYNC input	Input	Input/Output ports
4	NBDDATA0	NBD data bus input/output 0	Input/output	Input/Output ports
5	NBDDATA1	NBD data bus input/output 1	Input/output	Input/Output ports
6	NBDDATA2	NBD data bus input/output 2	Input/output	Input/Output ports
7	NBDDATA3	NBD data bus input/output 3	Input/output	Input/Output ports

3. Description of Operation

In the single chip mode, NBD control register (***[NBDCR0]***<NBDEN>) is set to "1", NBDIF circuit is enabled. In addition, need to select NBDIF pin by function register in PORT. For detail please refer to “3.2.2. Connecting Terminals of NBDIF”.

3.1. Clock Supply

When you use NBDIF, please set an applicable clock enable bit to "1" (clock supply) in fsys supply stop register A (***[CGFSYSENA]***, ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]***, ***[CGFSYSMENB]***), and fc supply stop registers (***[CGFCEN]***).

An applicable register and the bit position vary according to a product. Therefore, the register may not exist with the product. Please refer to "Clock Control and Operation Mode" of the reference manual for the details.

3.2. NBD Control Circuit

3.2.1. Function of NBDIF

When NBDSYNC is asserted, data is input/ output via 4 bits width NBDDATA[3:0] (data/ address/ command bus) at the clock timing of NBDCLK.

Access to RAM and registers can be read/ written by setting the mode setting bit <I/T> to "1" and setting the 32-bit address to the command packet.

3.2.2. Connecting Terminals of NBDIF

NBDIF communicates with a NBD tool by six wires.

When using NBDIF, set NBDCLK, NBDSYNC and NBDDATA[3:0] for input/ output for port alternate function before switching to NBD mode. For switching to alternate function terminals, refer to reference manual "Input/ Output Ports".

NBDDATA[3:0] should be built-in pull-up enable, or pull-up externally. This is to prevent malfunction when NBDDATA[3:0] becomes Hi-z and countermeasures against through current.

Table 3.1 Terminals (Signals) of NBDIF

Signal name	Input/output	Functional outline
NBDCLK	Input	Serial clock for NBD (1MHz(min) to 12.5MHz(max) (Note) (Input from NBD tool to MCU)
NBDSYNC	Input	It asserts at the time of command packet transmission. (Input from NBD tool to MCU)
NBDDATA[3:0]	Input/Output	The input/output(4bits) of command data and RAM data (Bidirectional signal between NBD tool and MCU)

Note: It is necessary to be fsys > (NBDCLK × 1.6).

3.2.3. About Bus Connection of NBDIF

NBDIF serves as a bus manager of AHB and performs read and write to each resource inside MCU.

The bus manager includes CPU, DMAC, NBDIF, etc. The priority order when the same subordinate accesses at the same time differ depending on the product. For details, refer to reference manual "Clock Control and Operation Mode" or "Memory Map".

3.2.4. Command Packet of NBDIF

NBDIF performs read and write to each resource inside MCU according to the command demand from a NBD tool. The NBD command is shown below.

(1) Command Packet

For read/write to RAM/SFR from outside of MCU, it is to input command packet via NBDDATA[3:0] pins. The command packet format is as follows. It is transmitted one by one from AUX3:AUX0.

Table 3.2 Command Packet

NBDDATA3	NBDDATA2	NBDDATA1	NBDDATA0	Explanation
AUX3	AUX2	AUX1	AUX0	For extension: 000 fixed
SIZ1	SIZ0	R/W	I/T	I/T: Address space mode (mode setting bit) 0: Reserved 1: MCU address space R/W: Access mode (access seen from the external root) 0: Read 1: Write SIZ[0:1]: Data length 00: 8bits 01: 16bits 10: 32bits 11: Reserved
A3	A2	A1	A0	Address information: Specified address
A7	A6	A5	A4	
A11	A10	A9	A8	
A15	A14	A13	A12	
A19	A18	A17	A16	
A23	A22	A21	A20	
A27	A26	A25	A24	
A31	A30	A29	A28	
D3	D2	D1	D0	Data: The data which are re-write data for Data tuning function, etc.
D7	D6	D5	D4	
D11	D10	D9	D8	
D15	D14	D13	D12	
D19	D18	D17	D16	
D23	D22	D21	D20	
D27	D26	D25	D24	
D31	D30	D29	D28	

(2) Data Packet

When monitored a RAM domain, the data packet format of the RAM data read via NBDDATA[3:0] pins are as follows. It is transmitted one by one from D3:D0.

Table 3.3 Data Packet

NBDDATA3	NBDDATA2	NBDDATA1	NBDDATA0	Explanation
D3	D2	D1	D0	Data: Data for RAM monitor
D7	D6	D5	D4	
D11	D10	D9	D8	
D15	D14	D13	D12	
D19	D18	D17	D16	
D23	D22	D21	D20	
D27	D26	D25	D24	
D31	D30	D29	D28	

(3) Flag Sense Packet

The flag sense is prepared in order to judge the termination of transmission of a command packet, and the read timing of data. The flag sense packet format is as follows.

Table 3.4 Flag Sense Packet

NBDDATA3	NBDDATA2	NBDDATA1	NBDDATA0	Explanation
N/A	N/A	N/A	Ready	Ready: Ready judging flag 0: Not Ready 1: Ready

3.3. Memory Map

Figure 3.1 shows the monitor target area which can access by a NBD tool.

SFR and RAM can be monitored by NBDIF and accessed from the NBD tool, but whether monitor (read) only or tuning (write) is also possible is set with ***[NBDCR1]***<NBDCREN>.

Flash, Boot ROM, and Bit Band area are not a monitor target. Please do not access with NBDIF when not monitor target. When accessing, undefined value is read.

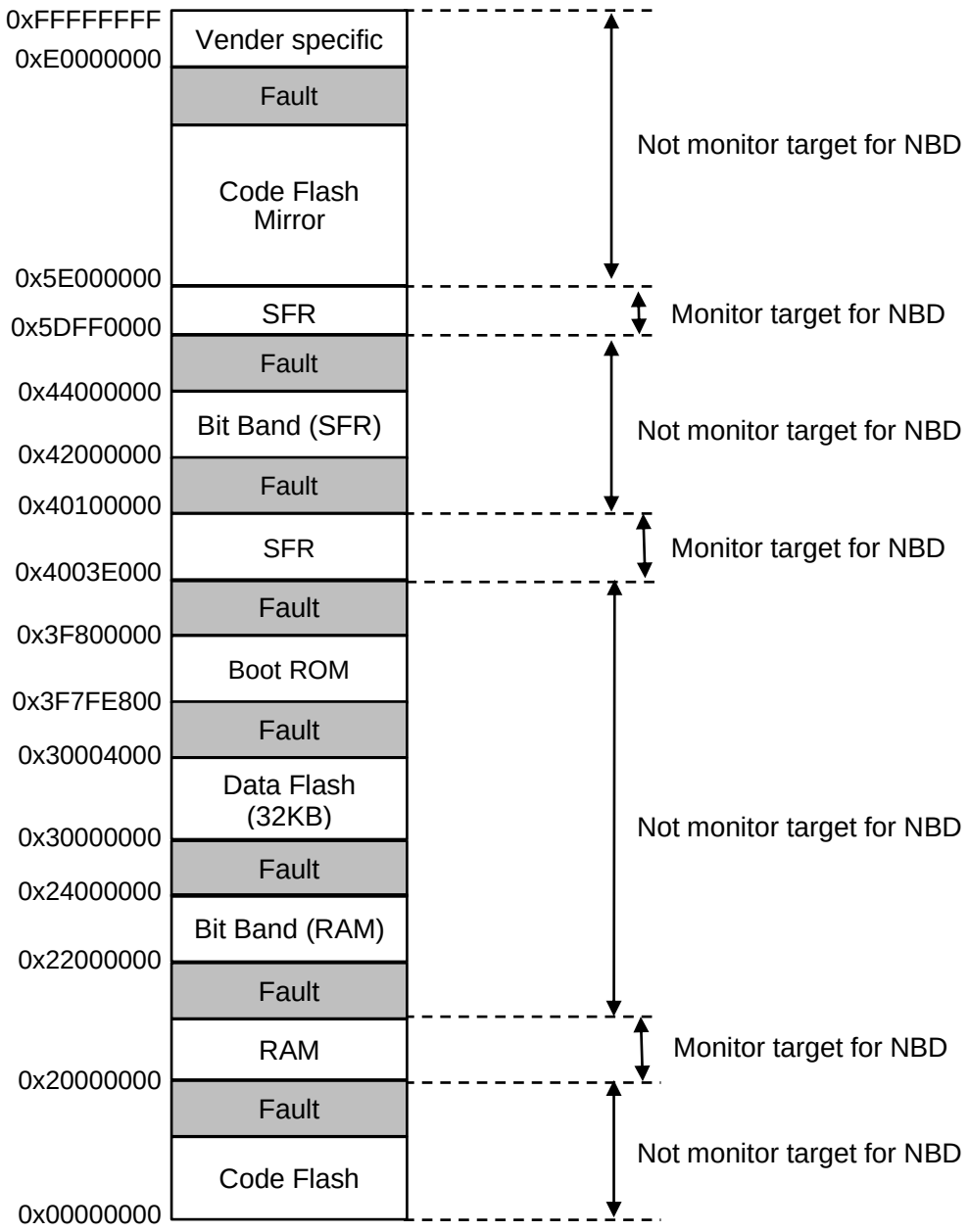


Figure 3.1 Example of Memory Map (Target for NBDIF Access)

Note: The address of each area differs depending on the product. For details, refer to reference manual "Clock Control and Operation Mode" or "Memory Map".

3.4. RAM Monitor Function

This function reads RAM/ SFR data via NBD tool during CPU is operating. The communication protocol between the RAM monitor tool and the MCU is shown below.

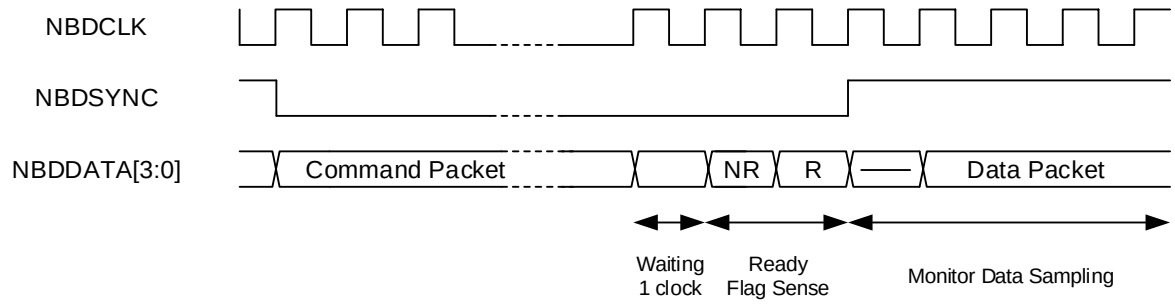


Figure 3.2 Timing Chart for RAM Monitor

Table 3.5 RAM Monitor Command

	Tool of RAM monitor	Debug function in TXZ MCU
(1) Transmit command	1. Assert NBDSYNC 2.Transmit command packet (Address of monitor RAM)	-
(2) Interpret command	One clock wait for Ready flag sense	1. Interpret command 2. Set "Not Ready (NR)" to flag sense 3. DMA setting for RAM monitor
(3) Waiting for data setup	Ready flag sense	1. Waiting DMA will be finish 2. After DMA finished set "Ready" to flag sense (Output “Ready(R)” until deassert NBDSYNC)
(4) Assert data	1. Ready detection 2. deassert NBDSYNC 3. sampling RAM data	Data output from the timing of deassert NBDSYNC

3.5. Dynamic Tuning Function

This function rewrites RAM/ SFR data from the outside of the MCU via the NBD tool during CPU is operating. The communication protocol between the RAM monitor tool and this product is shown below.

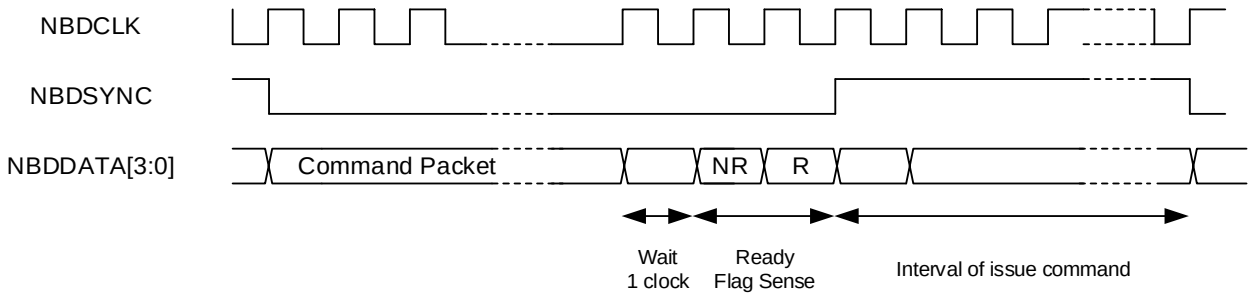


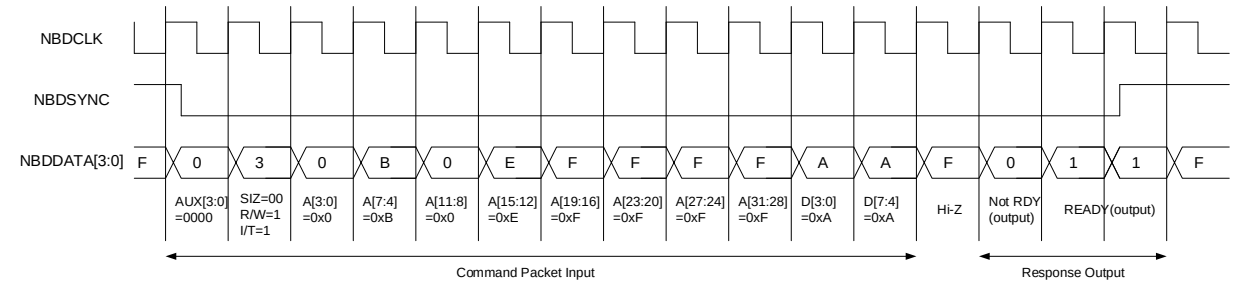
Figure 3.3 Timing Chart for Rewritten Data Transfer

Table 3.6 Command of Data Tuning

	RAM monitor tool	Debug function in MCU
(1) Transmit command	1. Assert NBDSYNC 2. Transmit command packet (Changing address, Transmit data)	-
(2) Interpret command	1 clock wait for Ready flag sense	1. Interpret command 2. Set "Not Ready (NR)" to flag sense
(3) Waiting for complete data rewriting	Ready flag sense	1. Data rewriting of the appointed address 2. After completed rewrite data, set "Ready(R)" to flag sense (Output “Ready(R)” until deassert NBDSYNC)
(4) The completion of command transmission	Deassert NBDSYNC	-

3.6. Operation of NBDIF

(a) Writing byte data (0xAA) to address "0xFFFFE0B0"



(b) Reading word data (0x8765432C) from address "0xFFFFE0B0"

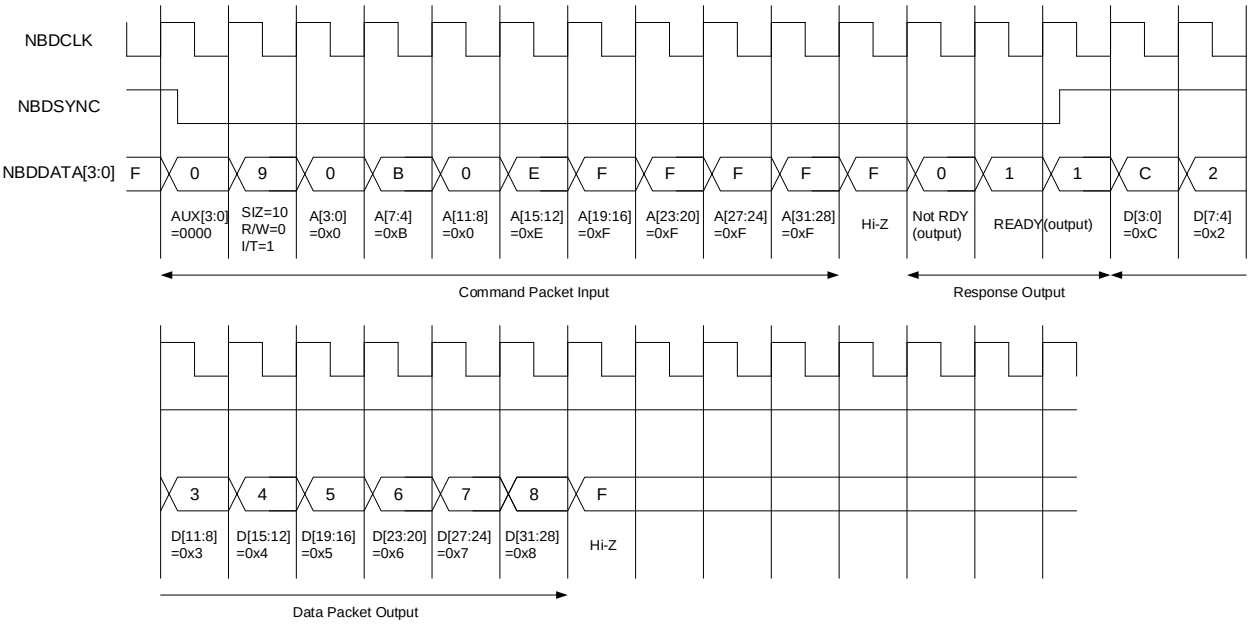


Figure 3.4 Example of Operation of NBDIF

4. Registers

Describes the NBDIF control registers.

4.1. Register List

The NBDIF control registers and the address are as follows.

Peripheral function	Function name	Channel/unit	Base address	
			TYPE1	TYPE2
Non Break Debug Interface	NBDIF	-	0x400BBA00	0x400A2000

Note: The channel/unit and base address type are different by products. Please refer to "Product Information" of the reference manual for the details.

Register name		Base address(Base+)
NBDIF Control Register 0	***[NBDCR0]***	0x0000
NBDIF Control Register 1	***[NBDCR1]***	0x0004

4.2. Details of Register

4.2.1. *[NBDCR0]* (NBDIF Control Register 0)

Bit	Bit symbol	After reset	Type	Function
31:1	-	0	R	Read as “0”.
0	NBDEN	0	R/W	NBD functional control 1: NBDIF enable 0: NBDIF disable

Note: In order to prevent erroneous writing due to software runaway, writing "0xF9" to ***[NBDCR1]***<NBDCREN>, enable to writing to <NBDEN>. After writing "1", wait for 3 clocks or more after input NBDCLK and issue the command.

4.2.2. *[NBDCR1]* (NBDIF Control Register 1)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as “0”.
7:0	NBDCREN[7:0]	0x06	W	***[NBDCR0]*** write control 0xF9: enable for writing to ***[NBDCR0]*** register Except 0xF9: disable for writing to ***[NBDCR0]*** register
			R	0x06: ***[NBDCR0]*** write disable state 0xF9: ***[NBDCR0]*** write enable state

5. Revision History

Table 5.1 Revision History

Revision	Date	Description
1.0	2017-11-09	- First release
1.1	2025-08-08	- Appearance update

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as "TOSHIBA".
Hardware, software and systems described in this document are collectively referred to as "Product".

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**