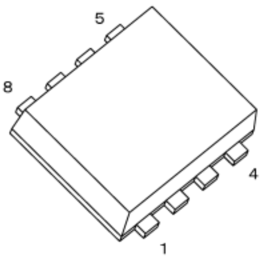
Toshiba Bi-CMOS Linear Integrated Circuits Silicon Monolithic

TPD7110F

High-Side N channel MOSFET Gate Driver

1. Description

TPD7110F is a single-output N-channel MOSFET gate driver. It incorporates a charge pump circuit, a reverse current blocking circuit from the load side, protection circuits against undervoltage and overvoltage of the power supply, and a reverse connection protection circuit. When combined with an external N-channel MOSFET, it can be used to configure an ideal diode or a back-to-back relay switch.



SON8-P-0303-0.65

Weight : 0.017g (typ.)

2. Applications

Power lines for automotive body control modules, BMS (Battery Management System), HUD (Head-Up Display), etc.

3. Features

- Operating voltage range : 3 to 32 V
- Reverse current blocking from the load side
- Undervoltage/Overvoltage Protection for Power Supply
- Reverse connection protection of the power supply up to -32V
- Current consumption during output ON : 100 μA (typ.)
- Current consumption during output OFF : 2 μA (typ.)
- Meets AEC-Q100 standards
- Small package : PS-8
- Operating temperature range : T_j = -40 to 125 °C

Start of commercial production
2025-10

4. Block Diagram

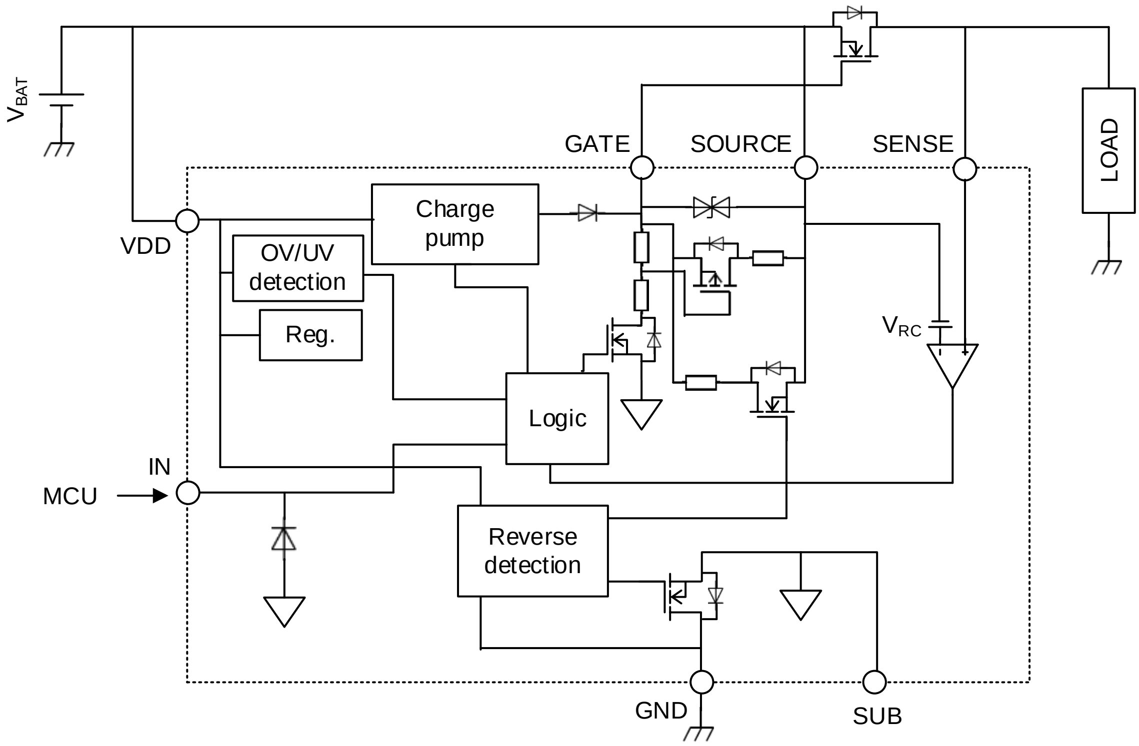


Fig. 4.1 Block Diagram

Note : The block diagram is simplified and intended for illustration only.
The surrounding connections are for reference only.

5. Pin Assignments Top view

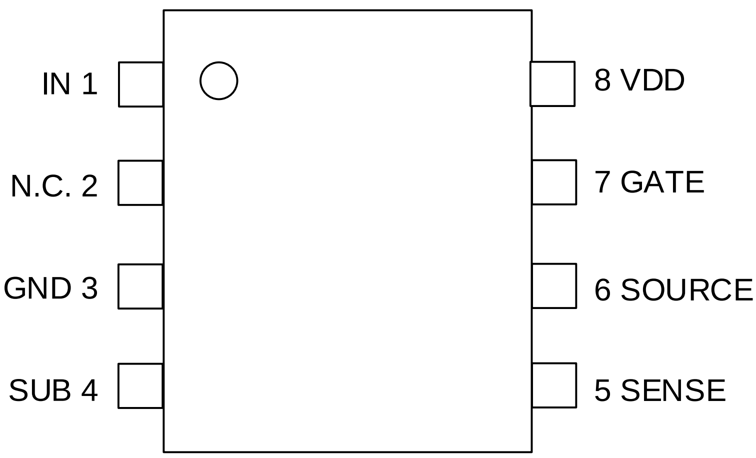


Fig. 5.1 Pin Assignments (top view)

6. Pin Description

Table 6.1 Pin Description

No.	Name	I/O	Pin Description
1	IN	INPUT	Gate driver input pin
2	N.C.	-	No-connect pin
3	GND	-	GND pin
4	SUB	-	Keep this pin open to activate reverse connection protection of the power supply
5	SENSE	INPUT	Reverse current sense pin
6	SOURCE	INPUT	Source connection pin for external N-channel MOSFET
7	GATE	OUTPUT	Gate drive pin for external N-channel MOSFET
8	VDD	-	Power supply pin

7. Operation Description

This product controls the on/off state of an N-channel MOSFET (hereafter referred to as "MOSFET") used in circuits such as ideal diodes or back-to-back relay switch configurations. When the MOSFET is on, if reverse current is detected from the load side, the MOSFET is turned off to block the reverse current.
Additionally, the MOSFET is turned off when the power supply voltage drops, becomes excessively high, or is connected in reverse.

7.1. Normal On/Off Operation

When the IN pin is in a high state (i.e., at or above the high-level input voltage, V_{IH}), the charge pump operates and generates a high-level output voltage between the GATE and SOURCE pins to turn on the MOSFET. Depending on the power supply voltage (V_{DD}), either $V_{GS(1)}$ or $V_{GS(3)}$ is output as the high-level gate-source voltage.
When the IN pin is in a low state (i.e., at or below the low-level input voltage, V_{IL}), the charge pump stops, the off-driver turns on, and the voltage between the GATE and SOURCE pins becomes a low level (V_{GSL}), turning off the MOSFET.Stopping the charge pump during the MOSFET off state helps reduce current consumption.
The rise time of the output voltage when the power supply voltage is 12 V is defined by t_{ON1} and t_{ON2}, and the fall time is defined by t_{OFF1}.

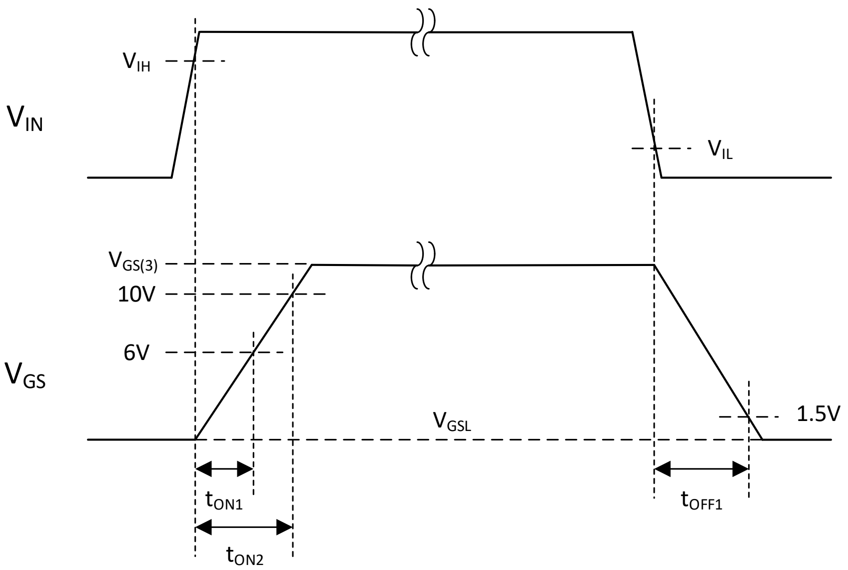


Fig. 7.1 Normal On/Off Waveform (V_{DD} = 12 V)

7.2. Reverse current blocking

This product blocks reverse current flowing from the load side back to the power supply, which can occur in redundant power systems.
The MOSFET's drain voltage is input to the SENSE pin, and the source voltage is input to the SOURCE pin. These voltages are compared by a comparator circuit, and when the SENSE pin voltage exceeds the SOURCE pin voltage by V_{RC} or more, the MOSFET is turned off.
Afterward, when the voltage difference between the SENSE and SOURCE pins falls below V_{RCr}, the MOSFET can be turned on or off again under the control of the IN pin.

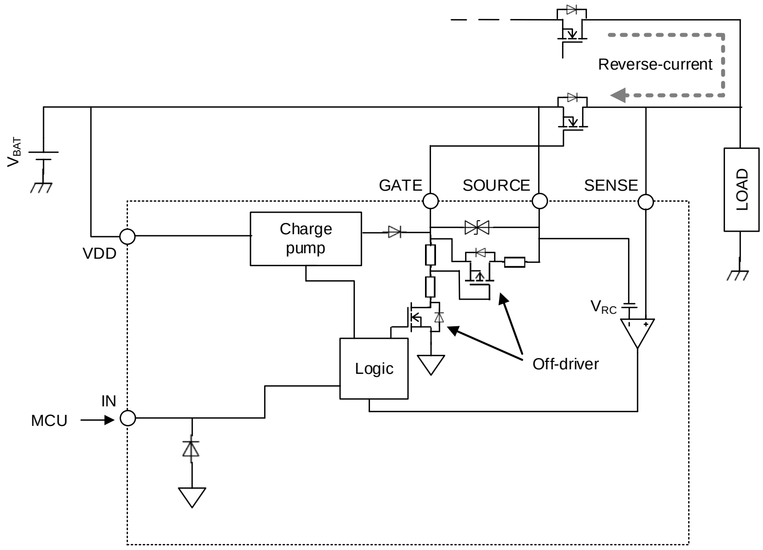


Fig. 7.2 Operation Block (Normal On/Off, Reverse Current Blocking)

7.3. Undervoltage Protection

This product stops operating when the power supply is in a low-voltage condition.
When the IN pin is in a high state and the voltage between the GATE and SOURCE pins is at a high level, turning on the MOSFET, the voltage between the GATE and SOURCE pins transitions to a low level (V_{GSL}) if the power supply voltage drops below V_{UVL}, thereby turning off the MOSFET.
Once the power supply voltage rises above V_{UVH}, the device resumes normal on operation.
Note that if the IN pin is in a low state and the MOSFET is off, it remains off regardless of the power supply voltage.

7.4. Overvoltage Protection

This product stops operating when the power supply is in an overvoltage condition.
When the IN pin is in a high state and the voltage between the GATE and SOURCE pins is at a high level, turning on the MOSFET, the voltage between the GATE and SOURCE pins transitions to a low level (V_{GSL}) if the power supply voltage exceeds V_{OVH}, thereby turning off the MOSFET.
Once the power supply voltage drops below V_{OVL}, the device resumes normal on operation.
Note that if the IN pin is in a low state and the MOSFET is off, it remains off regardless of the power supply voltage.

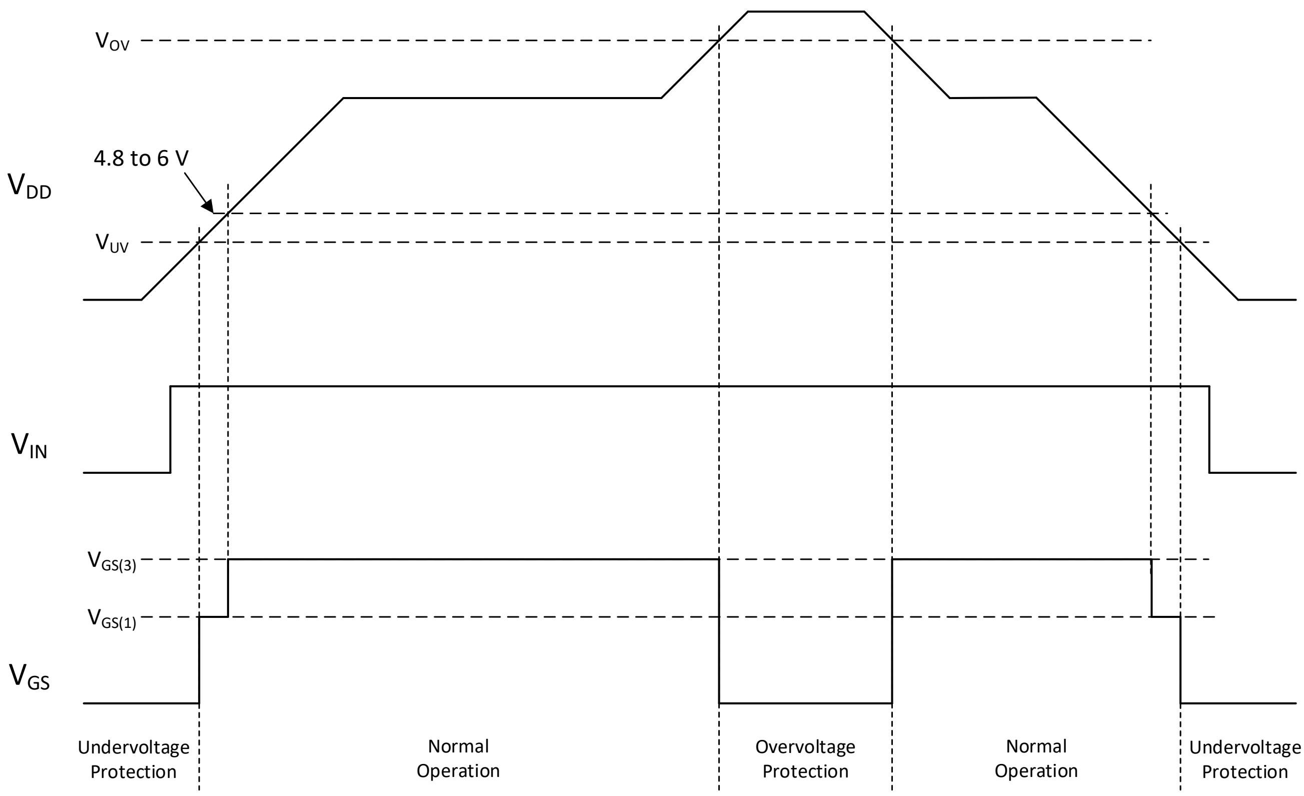


Fig. 7.3 Undervoltage and Overvoltage Protection – Operation Image

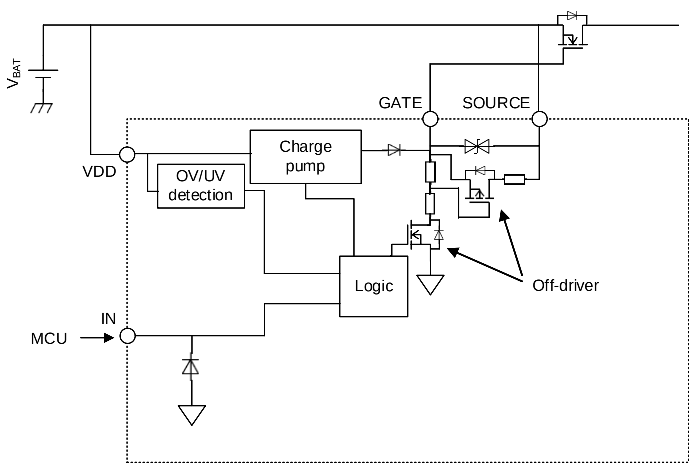


Fig. 7.4 Operation Block (Undervoltage / Overvoltage Protection)

7.5. Reverse Connection Protection

This product protects the system by turning off the MOSFET when the power supply is reverse connected. The reverse connection detection circuit monitors the voltages at the VDD and GND terminals. When a reverse connection is detected, the reverse connection protection off-driver is activated, setting the voltage between the GATE and SOURCE terminals to a low level (V_{GSL}), thereby turning off the MOSFET. Additionally, the GND switch is turned off to disconnect the internal GND wiring of the IC from the external GND, preventing reverse current from flowing into the IC through the GND terminal.

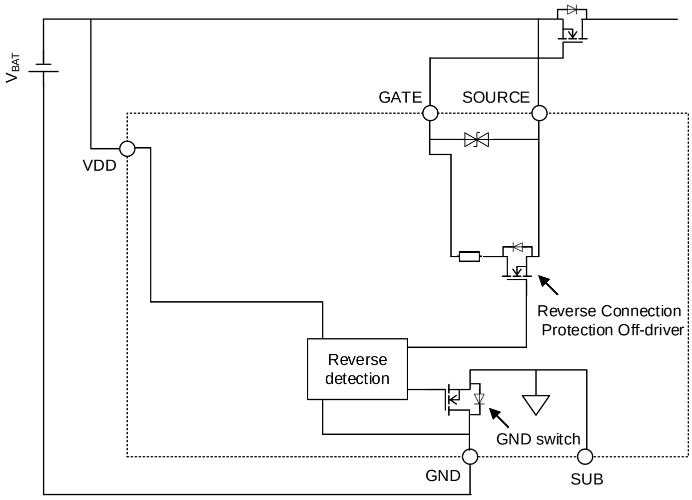


Fig.7.5 Operation Block (Reverse Connection Protection)

7.6. Truth Table

Table 7.1 Truth Table

Operating Mode		V_{DD}	IN	V_{GS} (Note 1)	MOSFET
Normal Operation	Normal On/Off Operation	$V_{UVL} < V_{DD} < V_{OVH}$	H	H	ON
			L	L	OFF
	Reverse current blocking ($V_{SENSE} - V_{SOURCE} \geq V_{RC}$)		H	L	OFF
Protect Operation	Undervoltage Protection	$V_{GND} \leq V_{DD} \leq V_{UVL}$	-	L	OFF
	Overvoltage Protection	$V_{DD} \geq V_{OVH}$	-	L	OFF
	Reverse Connection Protection	$V_{GND} > V_{DD}$	-	L	OFF

Note 1 : Voltage between the GATE and SOURCE terminals

7.7. State Transition Diagram

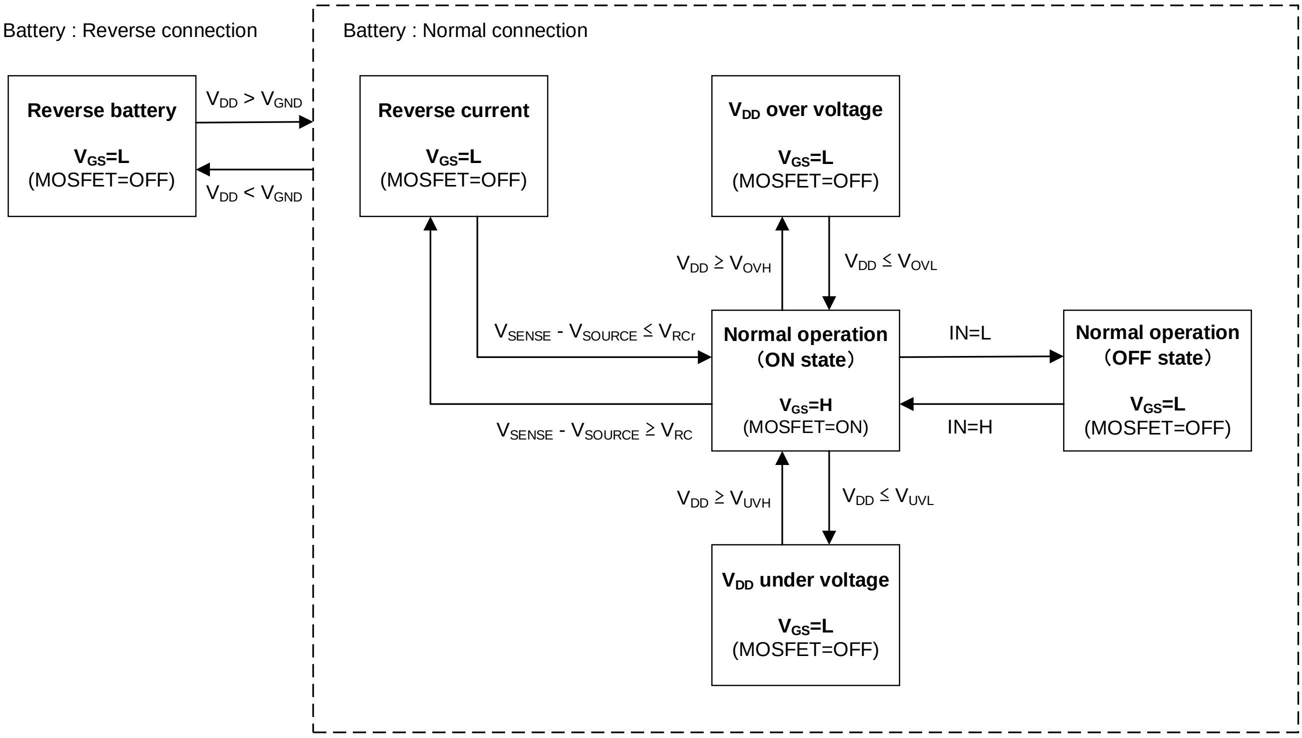


Fig. 7.6 State Transition Diagram

8. Absolute Maximum Ratings

Table 8.1 Absolute Maximum Ratings (Note)

(Unless otherwise specified, Ta = 25 °C)

Item	Symbol	Rating	Unit	Conditions
Power supply voltage	$V_{DD(1)}$	-0.3 to 60	V	DC
Power supply voltage under reverse connection	$V_{DD(2)}$	-32	V	SUB pin : Open
Input voltage (1)	V_{IN}	-0.3 to 6	V	IN pin
Input voltage (2)	V_{SENSE}	-0.3 to 60	V	SENSE pin
Input voltage (3)	V_{SOURCE}	-0.3 to 60	V	SOURCE pin
Output voltage	V_{GATE}	-0.3 to 60	V	GATE pin
Output source current	$I_{GS(-)}$	Internal capacity	µA	-
Output sink current	$I_{GS(+)}$	200	mA	-
Allowable power dissipation	P_D	0.99	W	JEDEC 4-layer board
Operating temperature	T_{opr}	-40 to 125	°C	-
Junction temperature	T_j	150	°C	-
Storage temperature	T_{stg}	-55 to 150	°C	-

Note : Absolute maximum ratings are specifications that must never be exceeded, even momentarily. Exceeding these ratings may result in destruction, degradation, or damage to the IC, and may also cause harm to other components.
Ensure that your design does not exceed the absolute maximum ratings under any operating conditions.
Please use the product within the operating ranges specified in the documentation.

8.1. Thermal Resistance

Table 8.2 Thermal Resistance

Item	Symbol	Rating	Unit
Thermal resistance (junction-to-ambient)	$R_{th\ (j\text{–}a)}$	126	°C / W

Board Conditions : JEDEC 4-layer board

9. Operating Range

Table 9.1 Operating supply voltage

Item	Symbol	Condition	Min	Typ.	Max	Unit
Operating supply voltage	$V_{DD(opr)}$	T_j = -40 to 125 °C	3	-	32	V

10. Electrical Characteristics

Table 10.1 Electrical Characteristics

(Unless otherwise specified, T_j = -40 to 125 °C, V_{DD} = 3 to 32 V)

Item	Symbol	Test Conditions	Min	Typ.	Max	Unit
Supply current	$I_{DD(ON1)}$	Refer to test circuit 1 V_{DD} = 12 V, V_{IN} = 5 V T_j = 25 °C	-	100	150	μA
	$I_{DD(ON2)}$	Refer to test circuit 1 V_{DD} = 32 V, V_{IN} = 5 V T_j = -40 °C to 125 °C	-	-	280	μA
	$I_{DD(OFF1)}$	Refer to test circuit 1 V_{DD} = 12 V, V_{IN} = 0 V T_j = 25 °C		2	3	μA
	$I_{DD(OFF2)}$	Refer to test circuit 1 V_{DD} = 32 V, V_{IN} = 0 V T_j = -40 °C to 125 °C		-	10	μA
High level input voltage	V_{IH}	-	2.4	-	-	V
Low level input voltage	V_{IL}	-	-	-	0.6	V
Input voltage hysteresis	V_{IHYS}	-	-	0.5	-	V
High level input current	I_{IH}	V_{IN} = 5 V	-	0.3	1.0	μA
Low level input current	I_{IL}	V_{IN} = 0 V	-2.0	-0.3	-	μA
High level output voltage(1)	$V_{GS(1)}$	Refer to test circuit 2 V_{DD} = 3 V to 4.8 V, V_{IN} = 5 V	6.0	7.0	8.0	V
High level output voltage(2)	$V_{GS(2)}$	Refer to test circuit 2 V_{DD} = 4.8 V to 6 V, V_{IN} = 5 V	6.0	-	13.5	V
High level output voltage(3)	$V_{GS(3)}$	Refer to test circuit 2 V_{DD} = 6 V to 32 V, V_{IN} = 5 V	10.0	12.0	13.5	V
Low level output voltage	V_{GSL}	Refer to test circuit 2 V_{IN} = 0 V	-	-	0.5	V
Output clamp voltage	V_{CL}	-	15.5	18.0	19.5	V
Overvoltage detection voltage	V_{OVH}	-	33	36	39	V
Overvoltage release voltage	V_{OVL}	-	32	-	-	V
Overvoltage detection hysteresis	V_{OVHYS}	-	-	1	-	V
Undervoltage detection voltage	V_{UVL}	-	2.4	-	2.9	V
Undervoltage release voltage	V_{UVH}	-	-	-	3.0	V
Undervoltage detection hysteresis	V_{UVHYS}	-	-	0.1	-	V
Output resistance	R_{SINK}	Refer to test circuit 3	-	30	40	Ω
Reverse current blocking threshold voltage	V_{RC}	Refer to test circuit 4 T_j = 25 °C	20	30	40	mV
Reverse current blocking release voltage	V_{RCr}	Refer to test circuit 4 T_j = 25 °C	-	-	23	mV
Reverse current blocking voltage hysteresis	V_{RCHYS}	Refer to test circuit 4 T_j = 25 °C	-	22	-	mV

Output voltage under reverse connection	V_{GSREV}	Refer to test circuit 5 V_{DD} = -3 V to -32 V, T_j = 25 °C	-	-	0.5	V
Supply current under reverse connection	I_{REV}	Refer to test circuit 5 V_{DD} = -3 V to -32 V, T_j = 25 °C	-	-	100	μA
Switching time	t_{ON1}	Refer to test circuit 6 T_j = 25 °C	-	1.6	2.8	ms
	t_{ON2}		-	3.2	5.8	ms
	t_{OFF1}		-	3.9	5.0	μs

11. Test circuits

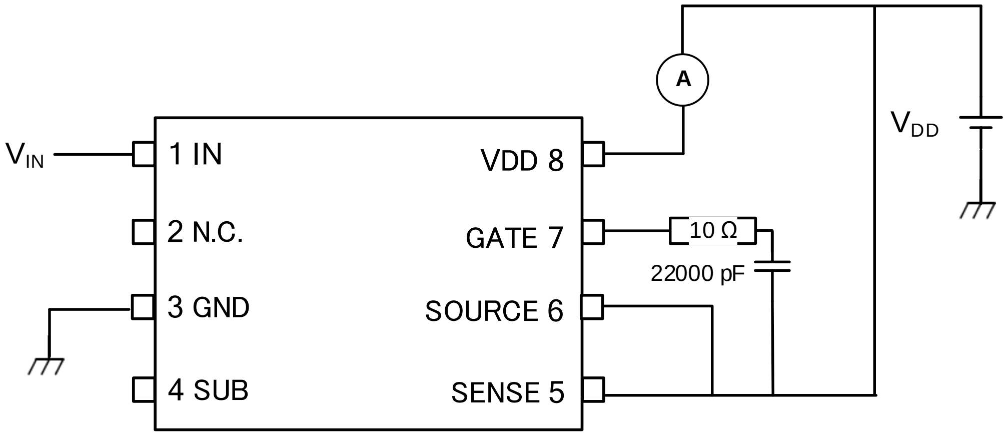


Fig. 11.1 Test circuit 1

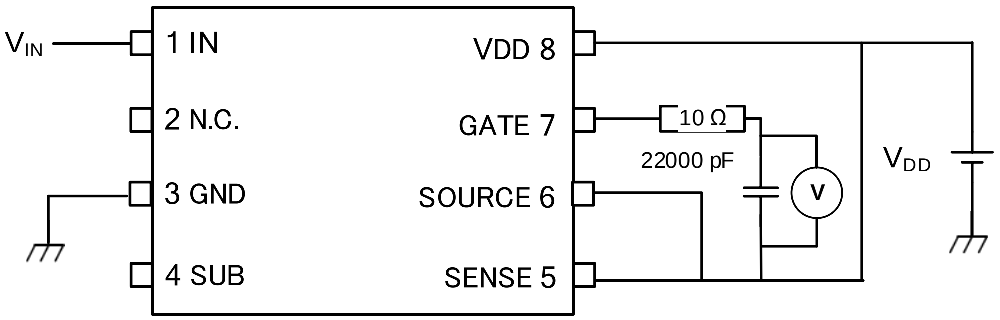


Fig. 11.2 Test circuit 2

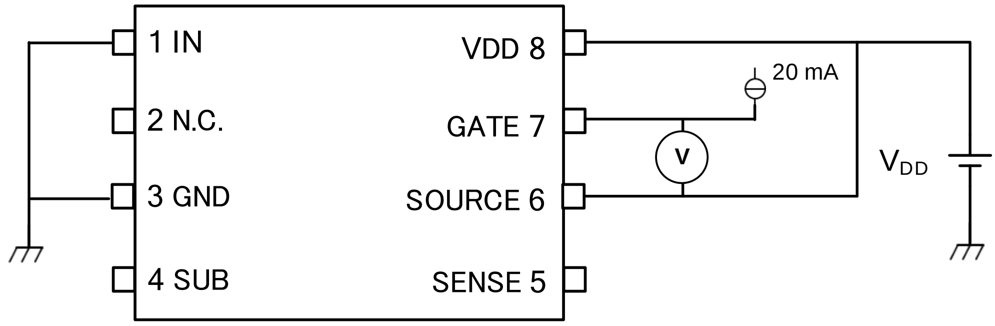


Fig. 11.3 Test circuit 3

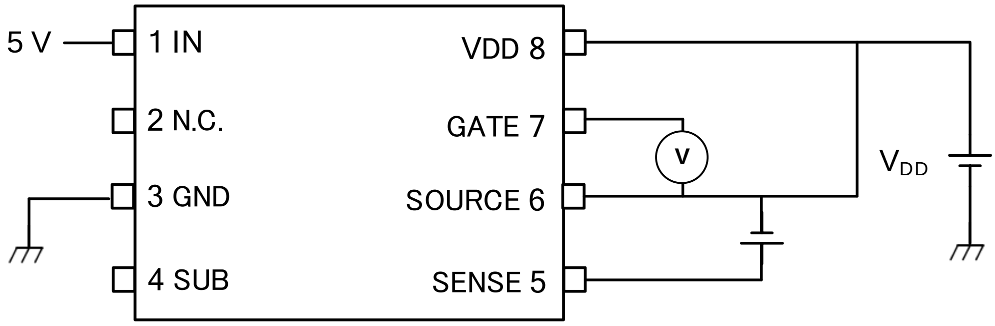


Fig. 11.4 Test circuit 4

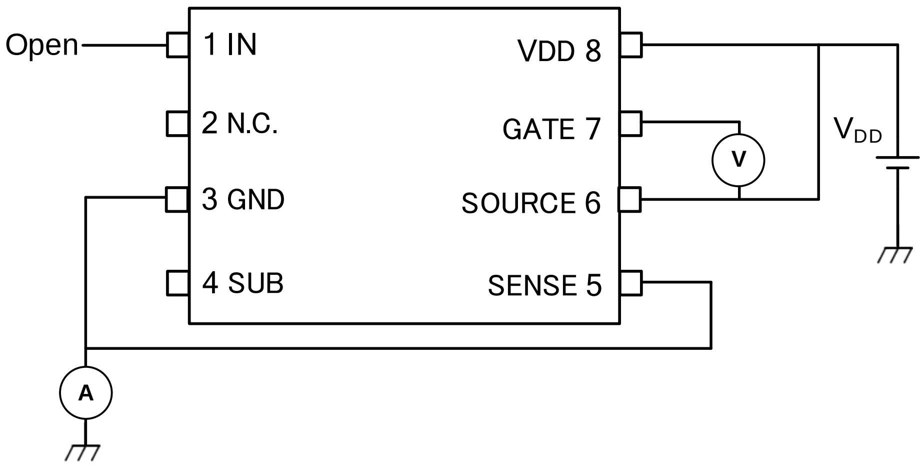


Fig. 11.5 Test circuit 5

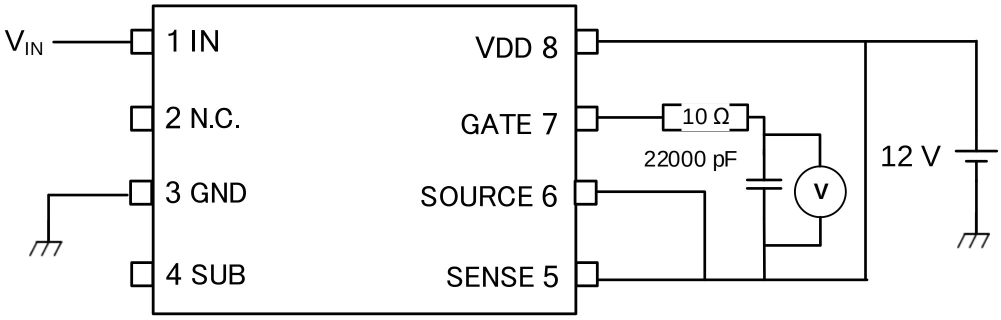


Fig. 11.6 Test circuit 6

12. Characteristic curves

The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

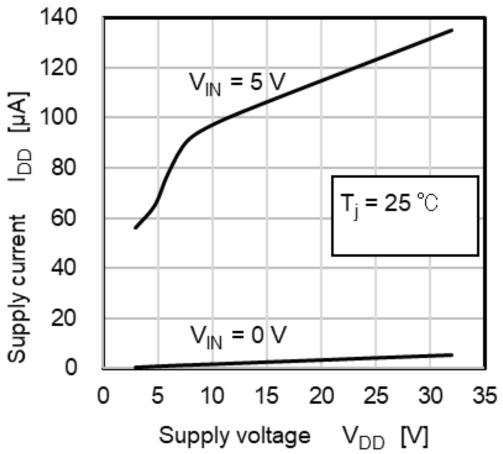


Fig. 12.1 I_{DD} - V_{DD}

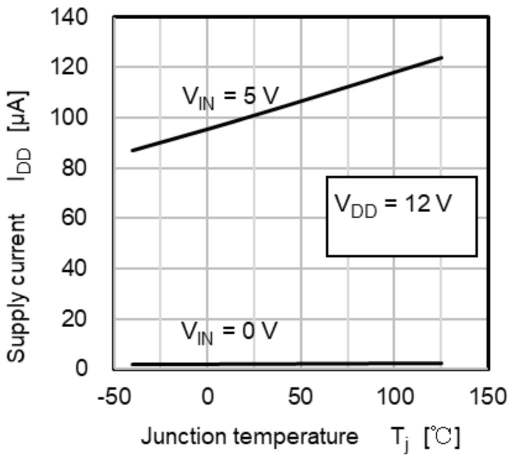


Fig. 12.2 I_{DD} - T_j

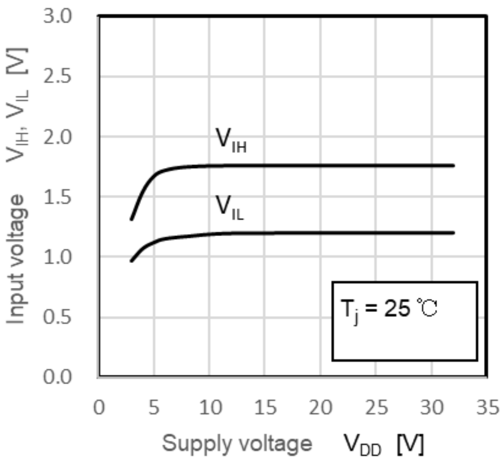


Fig. 12.3 V_{IH},V_{IL} - V_{DD}

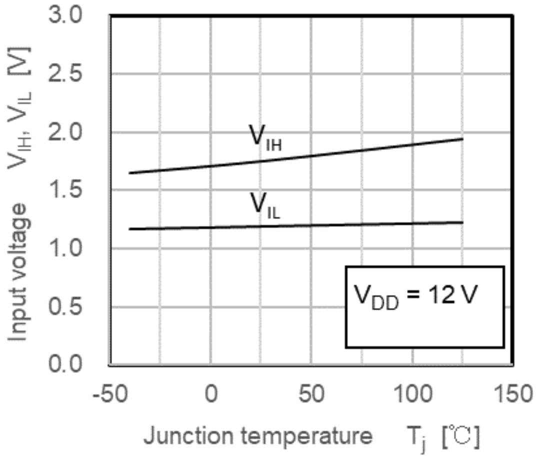


Fig. 12.4 V_{IH},V_{IL} - T_j

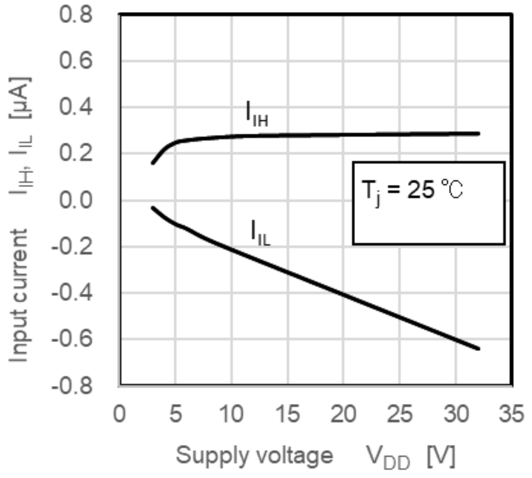


Fig. 12.5 I_{IH},I_{IL} - V_{DD}

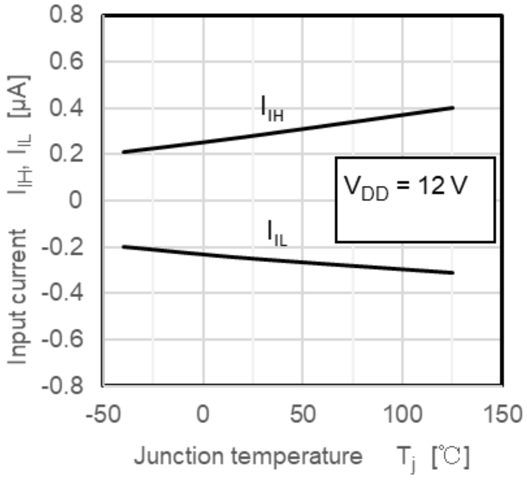


Fig. 12.6 I_{IH},I_{IL} - T_j

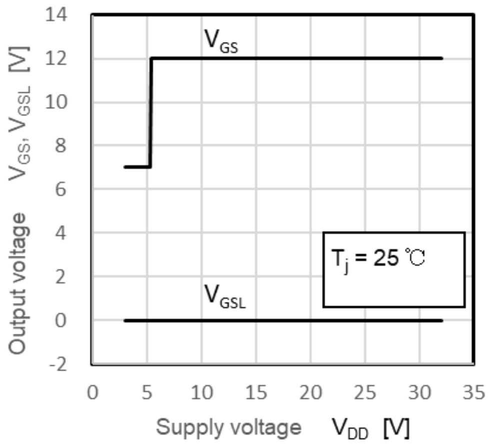


Fig. 12.7 V_{GS},V_{GSL} - V_{DD}

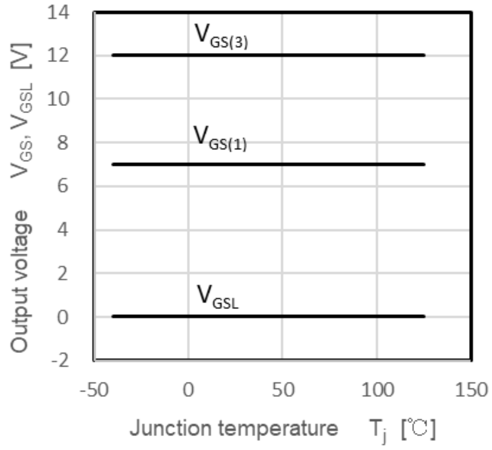


Fig. 12.8 V_{GS},V_{GSL} - T_j

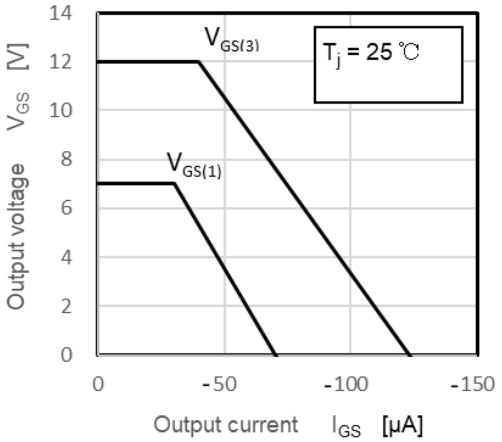


Fig. 12.9 V_{GS} - I_{GS}

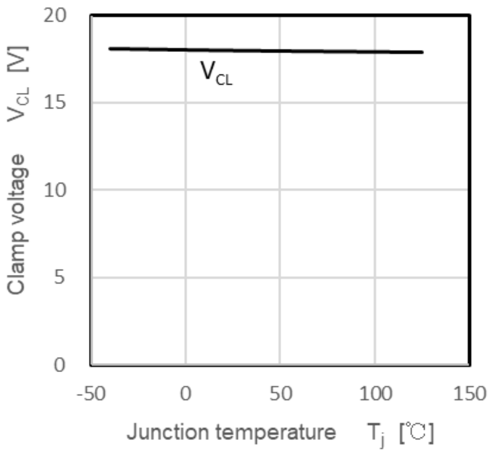


Fig. 12.10 V_{CL} - T_j

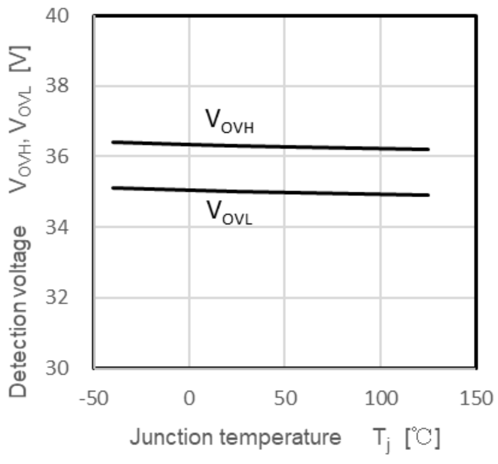


Fig. 12.11 V_{OVH}, V_{OVL} - T_j

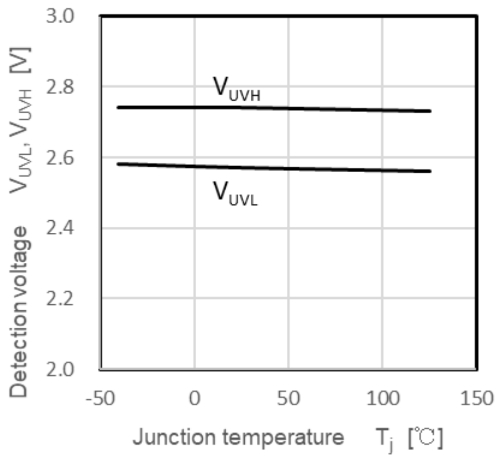


Fig. 12.12 V_{UVL}, V_{UVH} - T_j

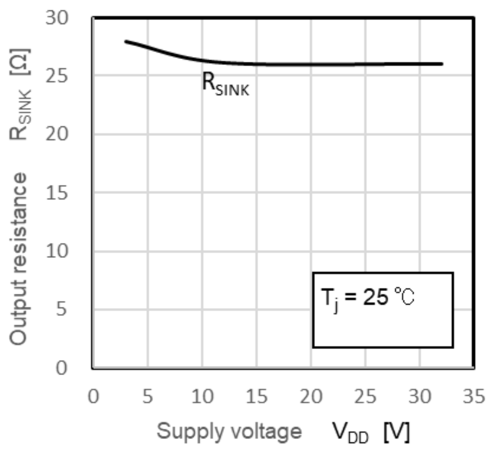


Fig. 12.13 R_{SINK} - V_{DD}

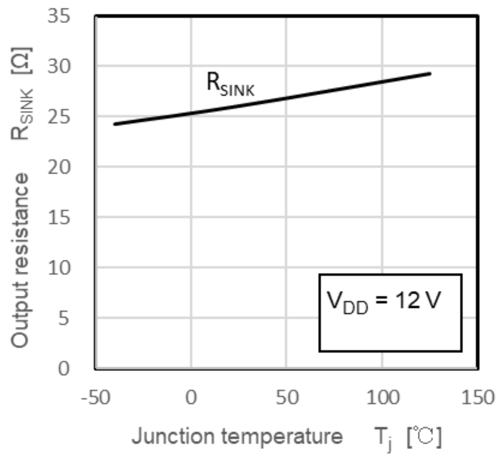


Fig. 12.14 R_{SINK} - T_j

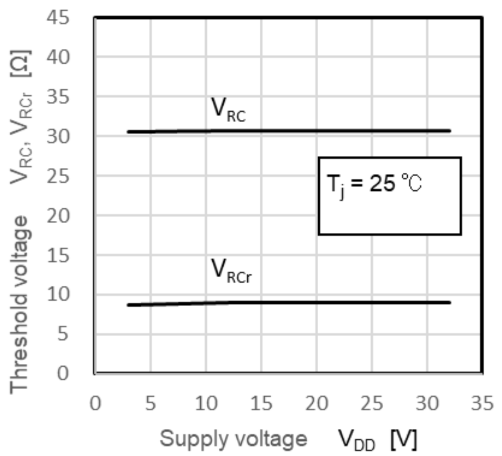


Fig. 12.15 V_{RC}, V_{RCr} - V_{DD}

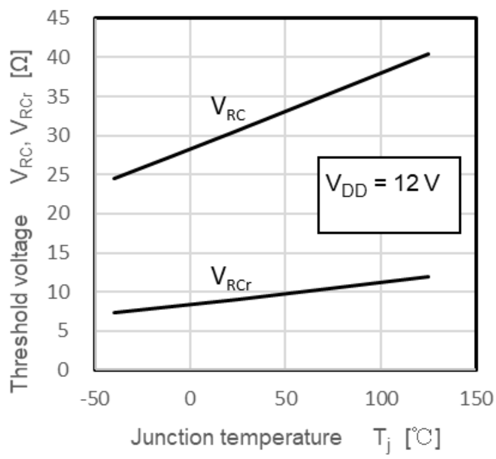


Fig. 12.16 V_{RC}, V_{RCr} - T_j

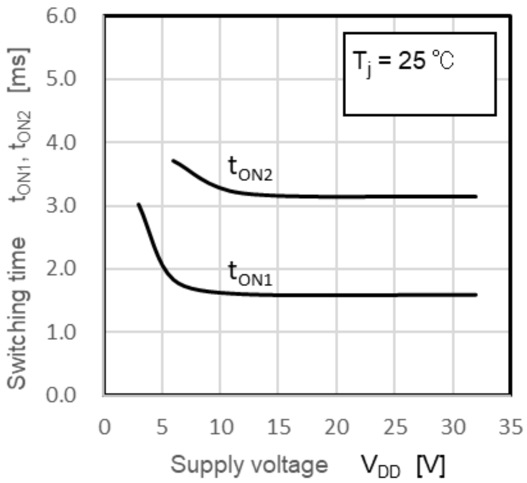


Fig. 12.17 t_{ON1},t_{ON2} - V_{DD}

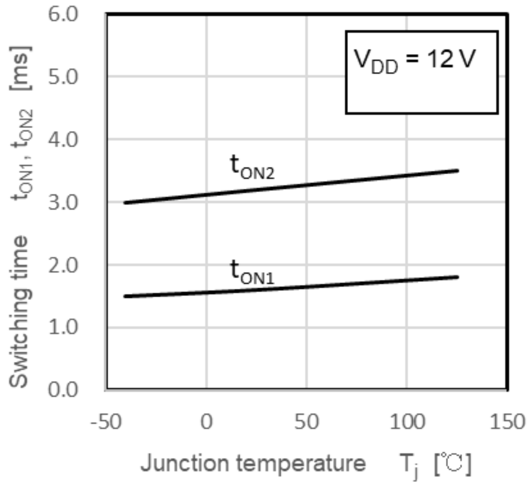


Fig. 12.18 t_{ON1},t_{ON2} - T_j

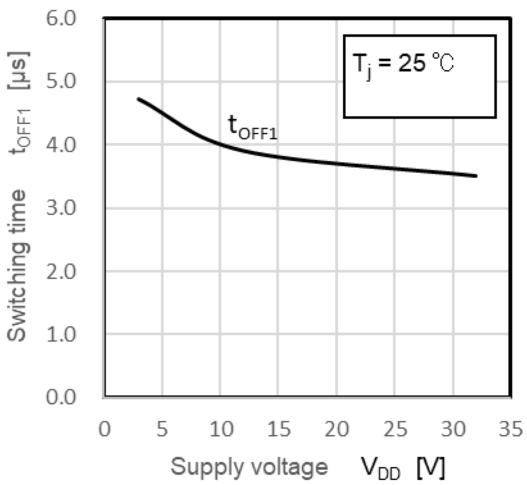


Fig. 12.19 t_{OFF1} - V_{DD}

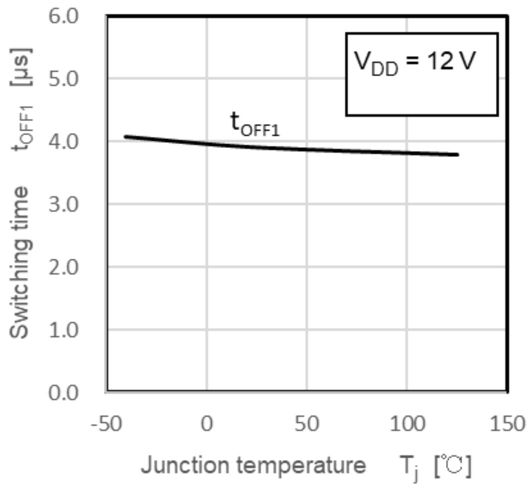


Fig. 12.20 t_{OFF1} - T_j

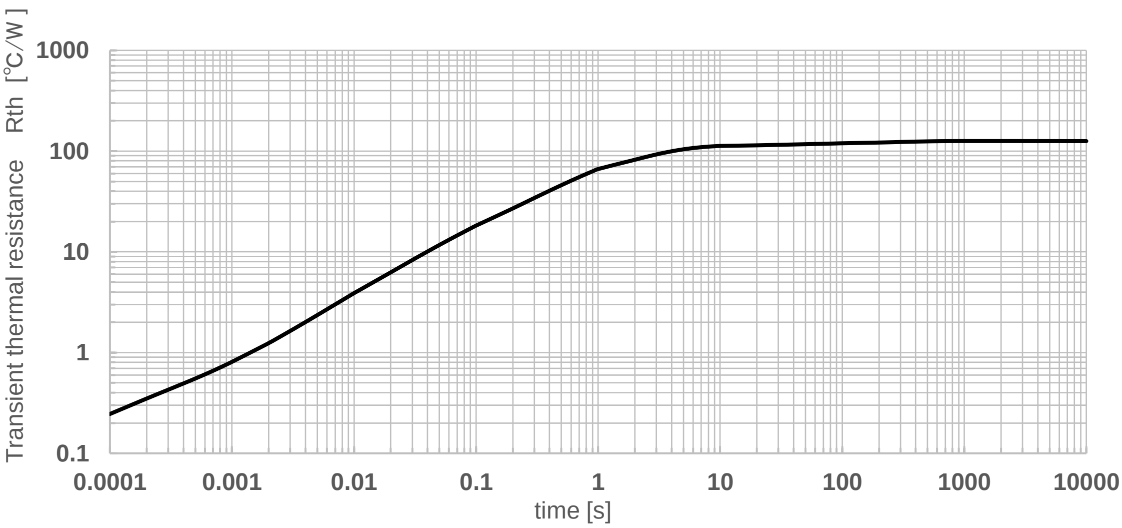


Fig. 12.21 Rth - t

13. Application circuit examples

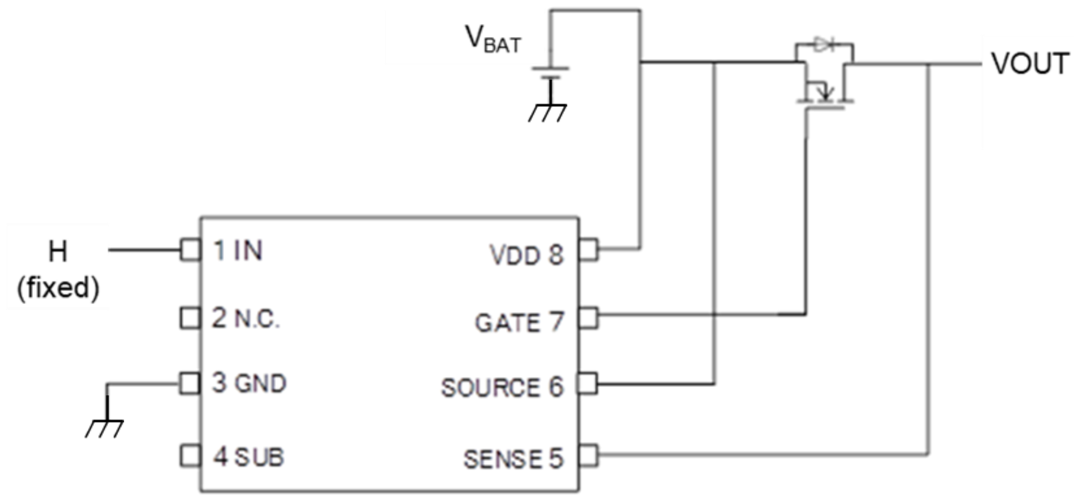


Fig. 13.1 Ideal diode connection example

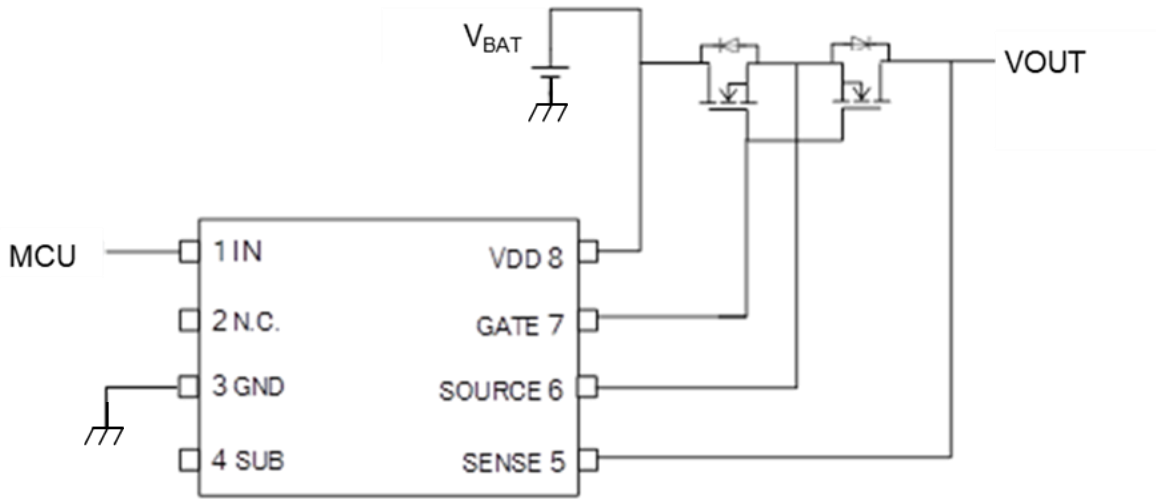
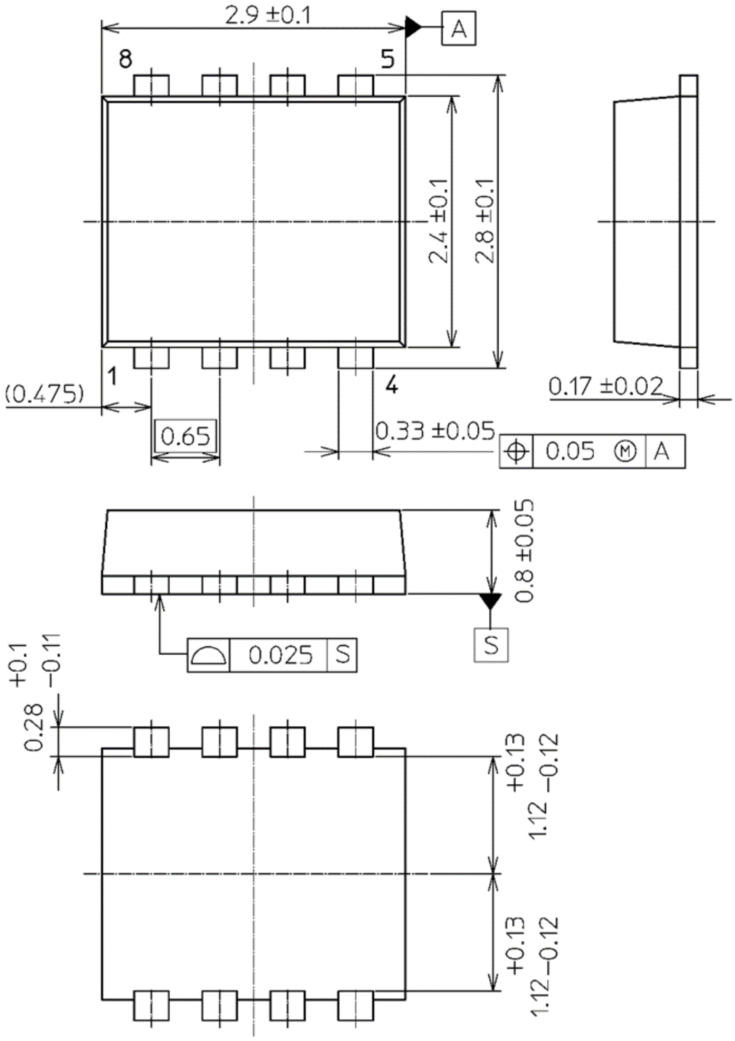


Fig. 13.2 Back-to-back MOSFET connection example

14. Package Information

14.1. Dimensions

SON8-P-0303-0.65 Unit : mm



Weight : 0.017 g(typ.)

Fig. 14.1 Dimensions

14.2. Marking

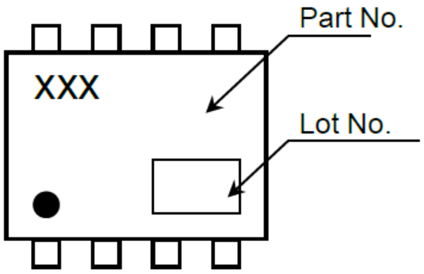
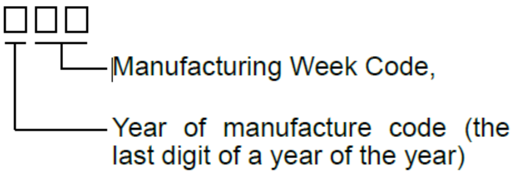


Fig. 14.2 Marking

- The mark bottom dot (●) indicates terminal 1 when viewed from the front.
- Weekly lot display
- Consists of three-digit mathematical figures, with the last one digit of the calendar year and the remaining two digits being the manufacturing week.



14.3. Land Pattern Dimensions (for reference only)

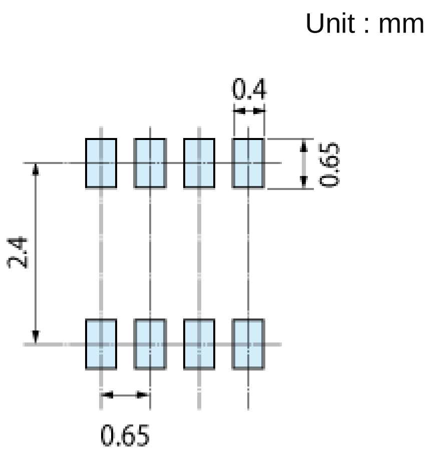


Fig. 14.3 Land Pattern Dimensions (for reference only)

15. IC Usage Considerations

15.1. Notes on handing of ICs

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. It cannot be exceeded for any of multiple ratings. Exceeding the absolute maximum ratings may cause breakage, damage or deterioration, resulting in injury due to explosion or combustion.

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**

Toshiba Electronic Devices & Storage Corporation

https://toshiba.semicon-storage.com/