TB9103FTG Application Note

Introduction

This document serves as a reference material to provide technical information to those using the TB9103FTG. Please ensure to refer to the latest datasheet and use this document as a supplement. Especially for numerical values, please refer to the datasheet.

Overview

The TB9103FTG is an automotive brushed motor driver. It incorporates two channels of half-bridge gate drivers, which can operate as half-bridge gate drivers or as a single channel H-bridge gate driver. The TB9103FTG is compact, focusing its functions and performance on motor on-off operations. It includes a 2x boost charge pump circuit, allowing the external power MOSFETs to be composed solely of n-type MOSFETs. When using the power supply voltage near the lower limit, it is recommended to use external n-type MOSFETs ("nMOSFETs") with a gate-source drive voltage type of "logic level gate drive." The TB9103FTG monitors the gate-source voltage of the nMOSFETs and performs dead-time control to prevent shoot-through current. The TB9103FTG can reduce power consumption by entering a sleep state during standby. It is equipped with various abnormality detection functions, and in the event of an abnormality, it stops the gate drive and notifies the abnormality via the DIAG terminal.

Toshiba Electronic Devices & Storage Corporation

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1. Power Supply Voltage

1.1. Operating Range of Power Supply Voltage

The TB9103FTG has two power supply systems: VB, which connects to the battery, and VCC, which is used for interfacing with the MCU and other components.
The operating voltage range for the VB terminal is 7 to 18V.
The operating voltage range for the VCC terminal is 4.5 to 5.5V.
In this document, the voltages of each terminal may be referred to by their terminal names.

1.2. Power-on/off Sequence

The TB9103FTG has two power supply systems: VB and VCC. The control circuit operates on VCC, and if the voltage at the VCC terminal is low, the control circuit is initialized, and gate drive is not performed. Additionally, in the sleep state controlled by the nSLEEP terminal, the internal status is maintained, but gate drive is not performed. For explanation purposes, the terminal voltages related to power supply and operation are shown in Fig. 1.2.1-1.

1.2.1. Power-on Sequence

The power-on sequence for VB and VCC should be either simultaneous or with VB first. It is recommended to keep the nSLEEP terminal Low until each power supply reaches its operating voltage range. When the voltage at the VCC terminal is lower than VCCLOd, the system is in a reset state. When the voltage at the VCC terminal exceeds VCCLOr, the system transitions from the reset state to either the sleep state or the normal state, depending on the state of the nSLEEP terminal. If the system transitions to the normal state after the reset is released, abnormality detection operation starts immediately. If the voltage at the VB terminal is lower than VBLOd at this time, a VB low voltage abnormality occurs, requiring error handling. To avoid this, it is recommended to keep the nSLEEP terminal Low during power-on and set it to High after each power supply reaches its operating voltage range. Even after transitioning to the normal operating state, the voltage at the VCP terminal will not become sufficiently high until tWAKE (Max 0.5ms) has elapsed. After transitioning from the sleep state to the normal state, wait for the tWAKE time before issuing instructions to the gate drive.

Recommended state transitions: Reset state → Sleep state → Normal state (waiting for VCP boost) → Normal state (gate drive enabled)

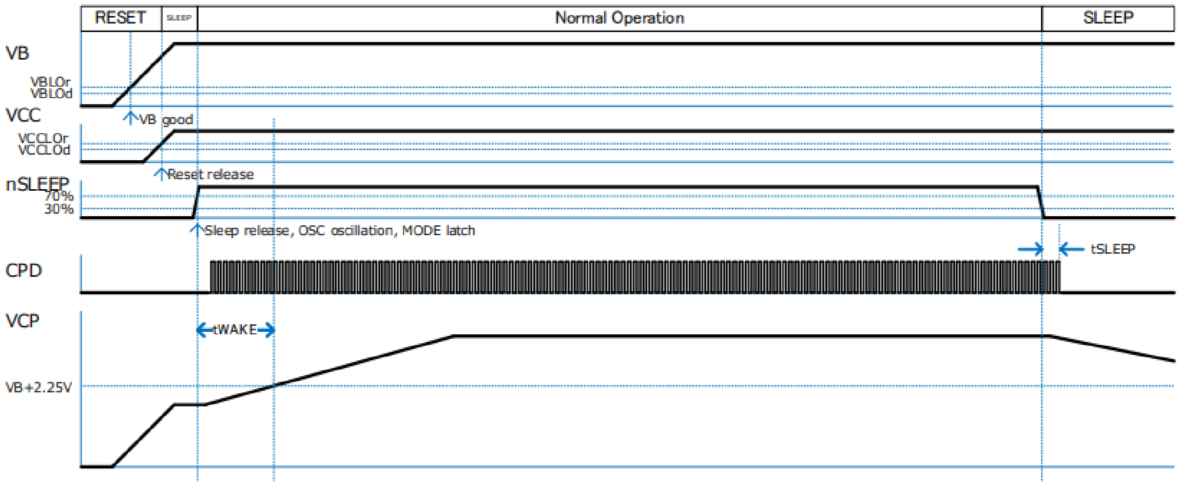

Fig. 1.2.1-1 Power-on/off Sequence

Note: The above diagram is simplified and partially omitted to explain the functions and operations of the IC.

1.2.2. Power-off Sequence

When turning off the power, ensure that the IN1, IN2, IN3, and IN4 terminals are all set to Low for safety, and that the motor and other components are in a stopped state. The power-off sequence for VB and VCC should be either simultaneous or with VCC first. It is recommended to set the nSLEEP terminal to Low in advance to put the system in sleep mode, in order to avoid unnecessary operations before and after power loss.

Recommended state transitions: Normal state (gate drive enabled) → All gate drives off → Sleep state → Reset state

2. High Voltage and Negative Voltage Application Due to Motor Back Electromotive Force

Immediately after stopping the motor drive or when the motor rotates due to external force, the motor generates electricity, causing a voltage to be applied from the motor to the drive circuit. In some cases, this voltage may exceed the rated voltage of each terminal of the TB9103FTG.

Particular attention should be paid to the circuit design to ensure that the SH1 and SH2 terminals, which are directly connected to the motor, do not exceed their rated values.

Additionally, when all external MOSFETs are off (high impedance), the back electromotive force will increase the voltage at the DH terminal through the body diodes of the external MOSFETs. If the power supply's sink capability is insufficient, the voltage at the DH and VB terminals may rise to unexpected levels.

Figure 2-1 shows the current path of the motor's back electromotive force at this time. The path changes depending on the polarity of the electromotive force.

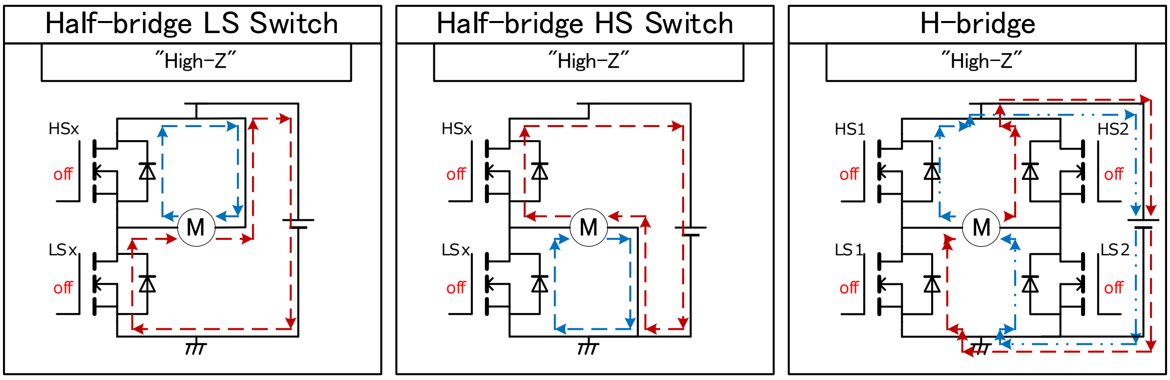

Fig. 2-1　Moter Back Electromotive Force Path

Note: The above diagram is simplified and partially omitted to explain the functions and operations of the IC.

The back electromotive force of the motor varies depending on the usage conditions and the characteristics of the motor. Please ensure that under your usage conditions, there is no risk of IC destruction or malfunction, and no risk of destruction or malfunction of the surrounding circuits.

2.1. Impact of ESD Protection Devices

For terminals that may be affected by the back electromotive force of the motor, the ESD network diagram is shown in Fig. 2.1-1.

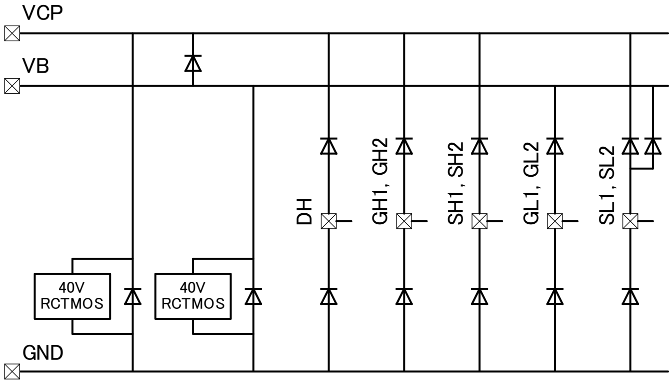

Fig. 2.1-1 ESD Network for External MOSFET Connection Terminals

Note: The above diagram is simplified and partially omitted to explain the functions and operations of the IC.

The SH1, SL1, SH2, and SL2 terminals have ESD protection diodes connected to GND. If a negative voltage is applied to these four terminals, current will flow through the diodes in the forward direction. Additionally, there is a constraint that the positive voltage must not exceed the absolute maximum rating of +40V. Therefore, please thoroughly consider the voltage generated by the motor and, if necessary, provide appropriate protection circuits.

2.2. Terminal Constraints

For terminals affected by the motor, the constraints listed in the datasheet are summarized in Table 2.2-1.

Table 2.2-1 Terminal Constraints Affected by Back Electromotive Force

Target Terminal Voltage	Constraint 1	Constraint 2	Unit
VB Terminal Voltage	Absolute Maximum Rating Vb	(-0.3 to 0) or (0 to VCP Terminal Voltage + 0.3) and (0 to 18) or [(0 to VCP Terminal Voltage + 0.3) and (0 to 40)] at ≦1s	V
DH Terminal Voltage	Absolute Maximum Rating Vdh	(-0.3 to 0) or (0 to VCP Terminal Voltage + 0.3) and (0 to 40)	V
SH1 Terminal Voltage, SH2 Terminal Voltage	Absolute Maximum Rating Vsh	(-1.2 to -0.3) at ≦0.1ms or (-0.3 to 0) or (0 to VCP Terminal Voltage + 0.3) and (0 to 40)	V
SL1 Terminal Voltage, SL2 Terminal Voltage	Absolute Maximum Rating Vsl	(-1.2 to -0.3) at ≦0.1ms or (-0.3 to 0) or (0 to VB Terminal Voltage + 0.3) and (0 to 40)	V
VB, DH Terminal Voltage (VB-DH)	Absolute Maximum Rating Vdif1	(-2 to 0) or (0 to 2)	V
SH1, DH Terminal Voltage (SH1-DH), SH2, DH Terminal Voltage (SH2-DH)	Absolute Maximum Rating Vdif2	To 2	V
SL1, SH1 Terminal Voltage (SL1-SH1), SL2, SH2 Terminal Voltage (SL2-SH2)	Absolute Maximum Rating Vdif3	To 2	V

2.3. Negative Voltage Characteristics of SH1, SH2Terminals

The SH1 and SH2 terminals are directly connected to the motor and are exposed to both high positive and high negative voltages generated by the motor. As stated in §2.1, these terminals are connected to the GND terminal via ESD protection devices, allowing current to flow easily when a negative voltage is applied. The characteristics of the SH1, SH2, SL1, and SL2 terminals when a negative voltage is applied are shown in Fig. 2.3-1. When calculating the resistance values for protection resistors, please ensure to provide sufficient margin.

If the current is large, the TB9103FTG will generate heat. Please thoroughly verify under your usage conditions to ensure that the absolute maximum ratings are not exceeded.

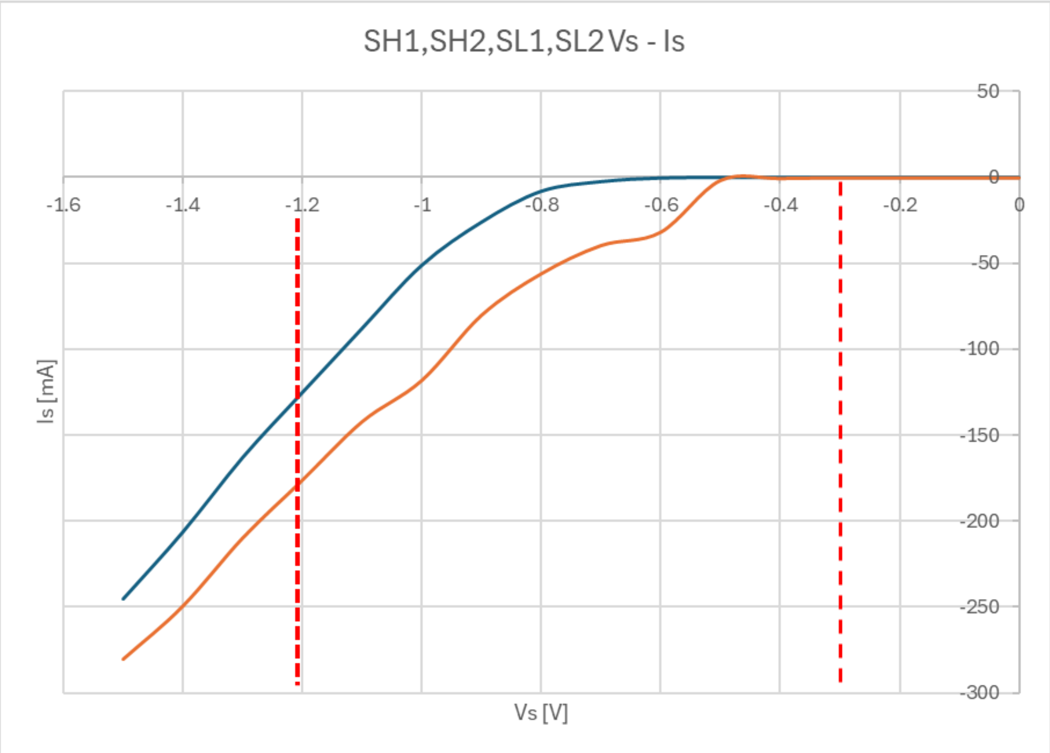

Fig. 2.3-1 Negative Voltage Characteristics of SH1, SH2, SL1, SL2 Terminals (Max, Min)

2.4. Example of Countermeasure Circuit

An example of a countermeasure circuit is shown in Fig. 2.4-1.

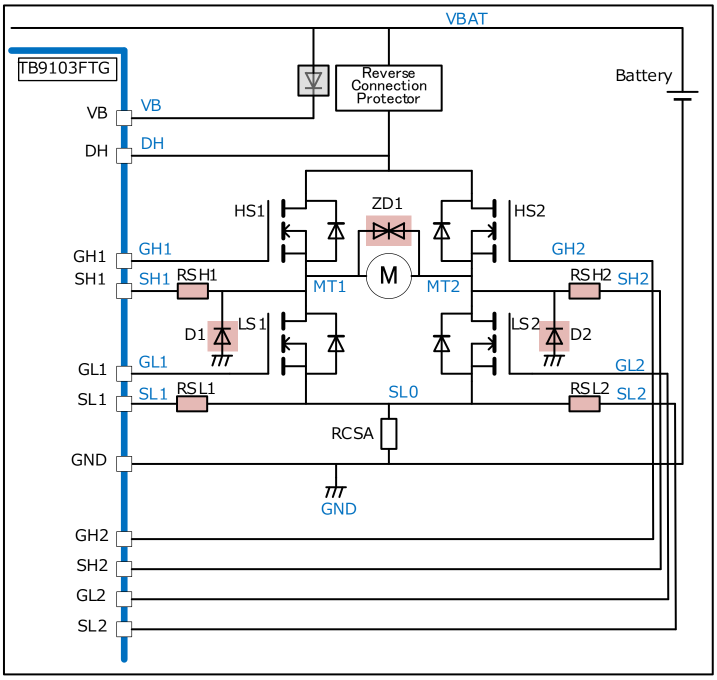

Fig. 2.4-1 Countermeasures for Excessive High Voltage and Excessive Negative Voltage in H-Bridge Circuit

Note: The above diagram is simplified and partially omitted to explain the functions and operations of the IC.

The bidirectional Zener diode ZD1 is connected close to the motor to limit the maximum value of the electromotive force generated by the motor. Diodes D1 and D2 share and bear the current flowing through the SH1 and SH2 terminals during negative voltage. Resistors RSH1 and RSH2 limit the current flowing through the SH1 and SH2 terminals. Additionally, they also serve as slew rate control by limiting the gate drive current. Resistors RSL1 and RSL2 are made equal to RSH1 and RSH2 to match the slew rates of HS1 and LS1, and HS2 and LS2. Diodes are not connected to the SL1 and SL2 terminals for current sharing because they are connected to GND through the low-resistance current detection resistor RCSA. In some cases, diodes similar to D1 and D2 may need to be provided.

This diagram is an example. Please take necessary measures according to your usage environment.

3. Maximum Voltage of GH1, GH2 Terminals is VCP

Do not fix the source terminals of the nMOSFETs connected to the GH1 and GH2 terminals for the high side to GND. The TB9103FTG is designed for a half-bridge configuration with nMOSFETs placed on both the high side and the low side. There are no voltage limiting circuits between the GH1 and SH1 terminals, or between the GH2 and SH2 terminals. When the gate drive is turned on, the voltage of the charge pump output, VCP, is output through an internal resistance equivalent to 500Ω at the GH1 and GH2 terminals. As the charge progresses in the gate-source capacitance of the nMOSFET, a voltage equivalent to the VCP terminal voltage eventually appears. It is assumed that the voltage between the drain and source will be almost 0V when the nMOSFET is turned on. If the source terminal of the nMOSFET is fixed to GND, the maximum rating of the gate-source voltage of the nMOSFET may be exceeded, leading to destruction.

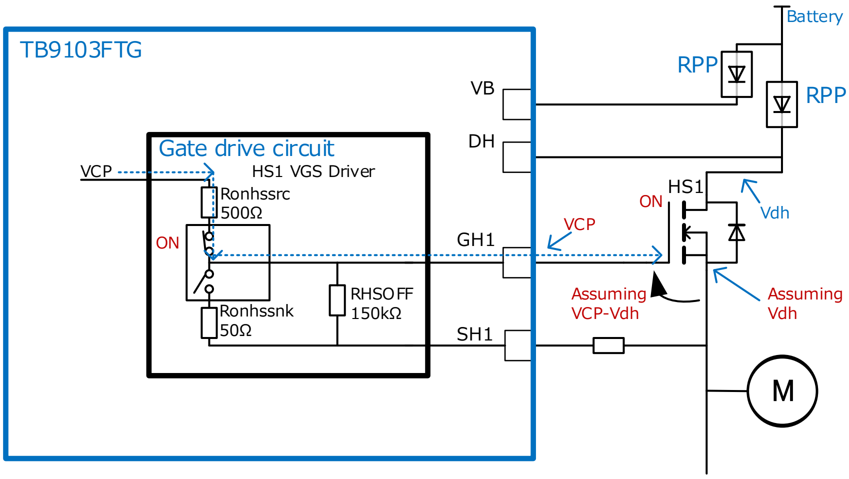

Fig. 3-1 Voltage of GH1, GH2 Terminals

Note: The above diagram is simplified and partially omitted to explain the functions and operations of the IC.

4. PWM Drive frequency

When driving the TB9103FTG with PWM, there are limitations on the driving frequency. After changing the drive instructions to the IN11, IN12, IN21, and IN22 terminals, the TB9103FTG does not detect high VDS voltage during the fault detection mask time tVDSF (Min 134μs, Max 536μs). If the drive instructions are changed faster than this period, the stop due to overcurrent detection will not be performed. If the overcurrent detection stop function is required, please provide another means externally.

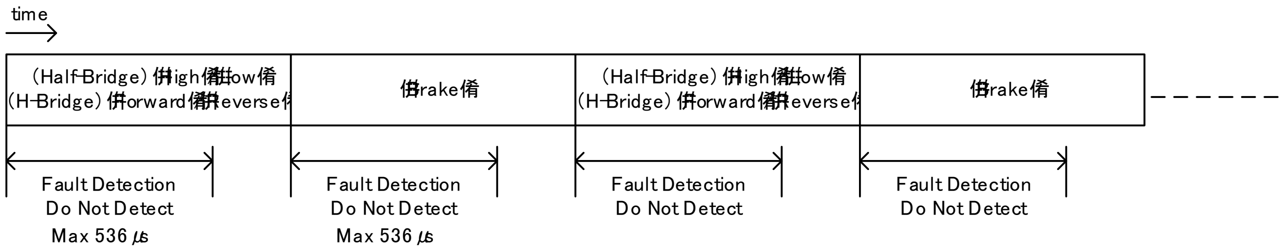

Fig. 4-1 Fault Detection at PWM

Due to the high drive output resistance and low slew rate, it may take time for the external nMOSFET to turn on/off as instructed by the MCU. If the instruction is changed before the instructed on/off operation is performed, there is a risk of shoot-through current. Please thoroughly verify this when using the device. Additionally, there is a risk that the drive frequency may fall within the audible range. Please verify this thoroughly before use. As an example, Fig. 4-2 shows the timing related to alternating instructions for Forward and Brake in H-bridge mode. The same applies to PWM operation in Reverse.

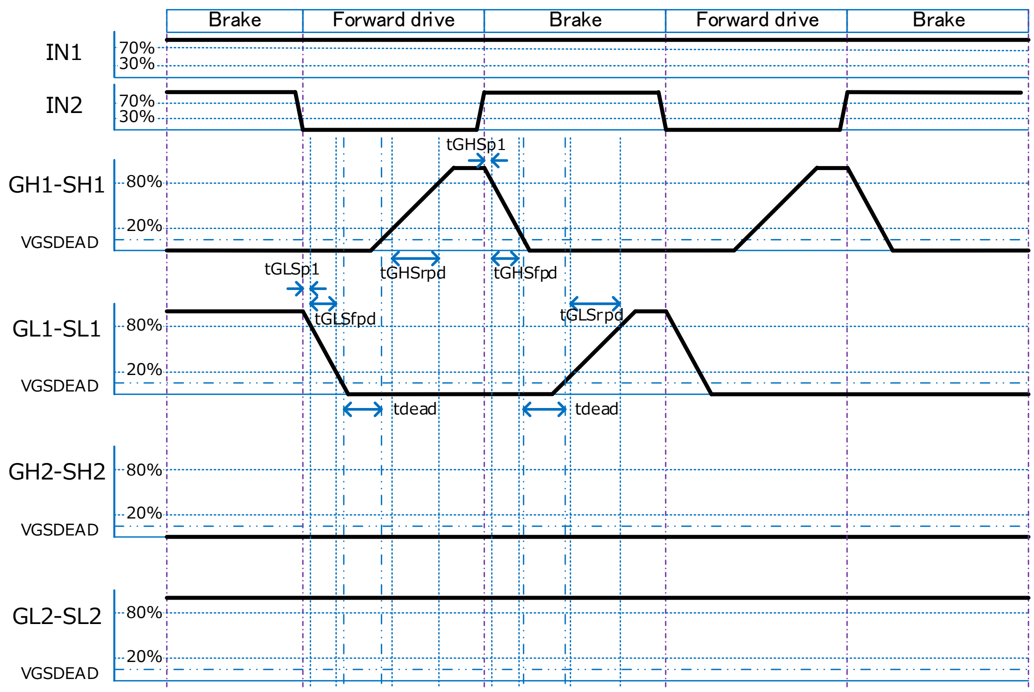

Fig. 4-2 PWM waveform (H-bridge, Forward to Brake)

5. Application Circuit Examples

5.1. Application Circuit Example in Half-Bridge Mode

An example of an application circuit in half-bridge mode is shown in Fig. 5.1-1.

The capacitors connected to the VB and VCC terminals are for smoothing and noise suppression. Please adjust them as needed for your environment. The resistor (≤10Ω) connected to the CPD terminal is for current limiting to reduce noise. Please measure the noise level in your environment and adjust accordingly. The resistors connected to the SH1, SL1, SH2, and SL2 terminals are for current limiting when turning the external nMOSFETs on and off. Please adjust them according to your environment.

The half-bridge can operate independently on two channels. However, the VDS on high voltage detection threshold voltage is common for both channels. When utilizing external nMOSFETs with varying performance across channels, it is important to assess whether the threshold voltages are consistent.

The motor connected in parallel with the external nMOSFET HS1 starts rotating when LS1 is turned on. The motor connected in parallel with LS2 starts rotating when HS2 is turned on.

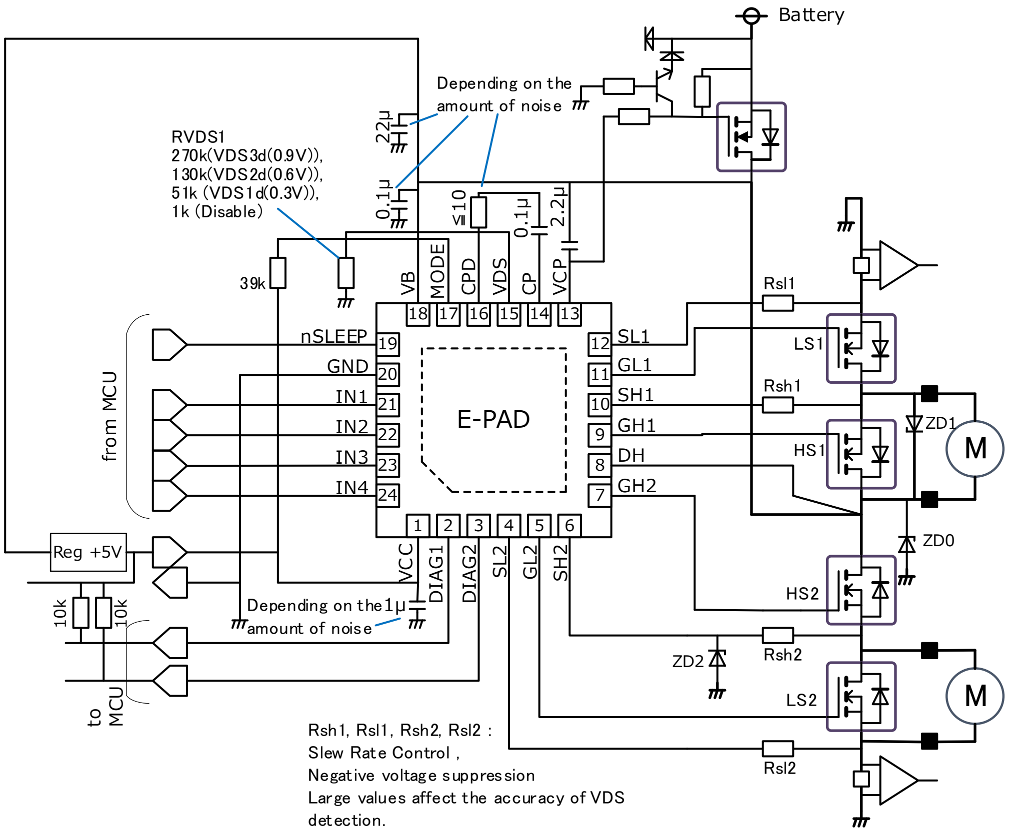

Fig. 5.1-1 Application Circuit Example in Half- Bridge Mode

Note: The above diagram is simplified and partially omitted to explain the functions and operations of the IC.

5.2. Application Circuit Example in H-Bridge Mode

An example of an application circuit in H-bridge mode is shown in Fig. 5.2-1.

The capacitors connected to the VB and VCC terminals are for smoothing and noise suppression. Please adjust them as needed for your environment. The resistor (≤10Ω) connected to the CPD terminal is for current limiting to reduce noise. Please measure the noise level in your environment and adjust accordingly. The resistors connected to the SH1, SL1, SH2, and SL2 terminals are for current limiting when turning the external nMOSFETs on and off. Please adjust them according to your environment. Additionally, as mentioned in §2, these resistors also have the effect of suppressing negative voltage applied to the SH1, SL1, SH2, and SL2 terminals.

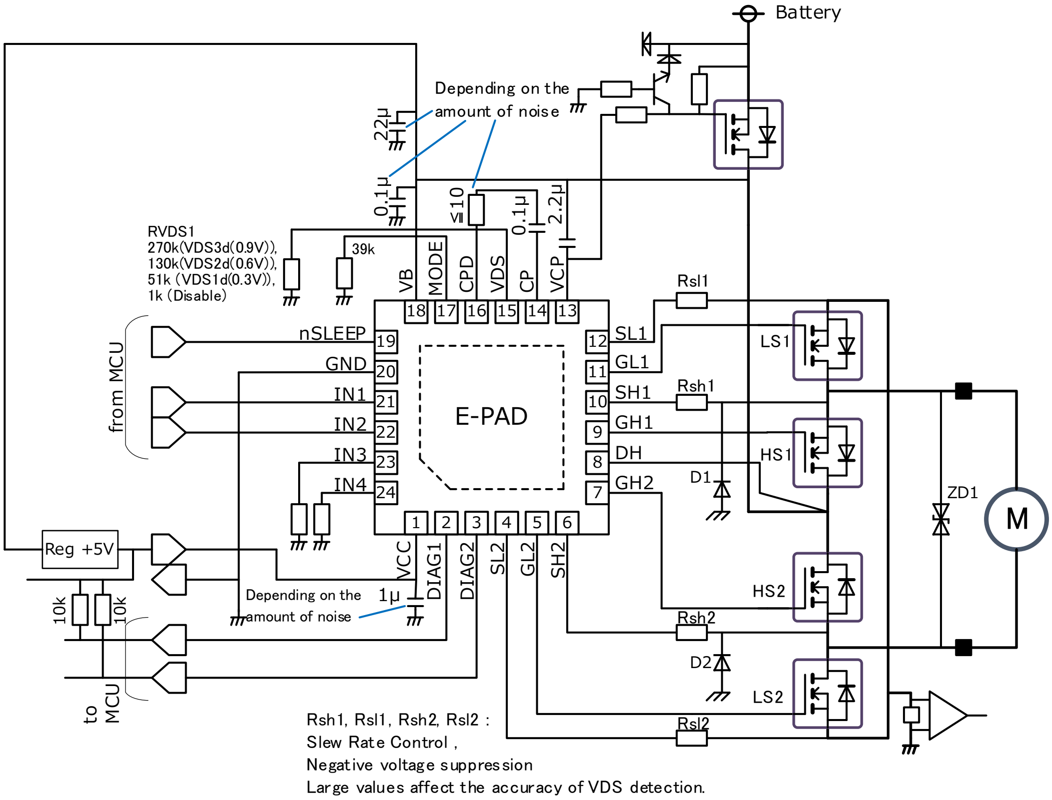

Fig. 5.2-1 Application Circuit Example in H-Bridge Mode

Note: The above diagram is simplified and partially omitted to explain the functions and operations of the IC.

6. Power Dissipation

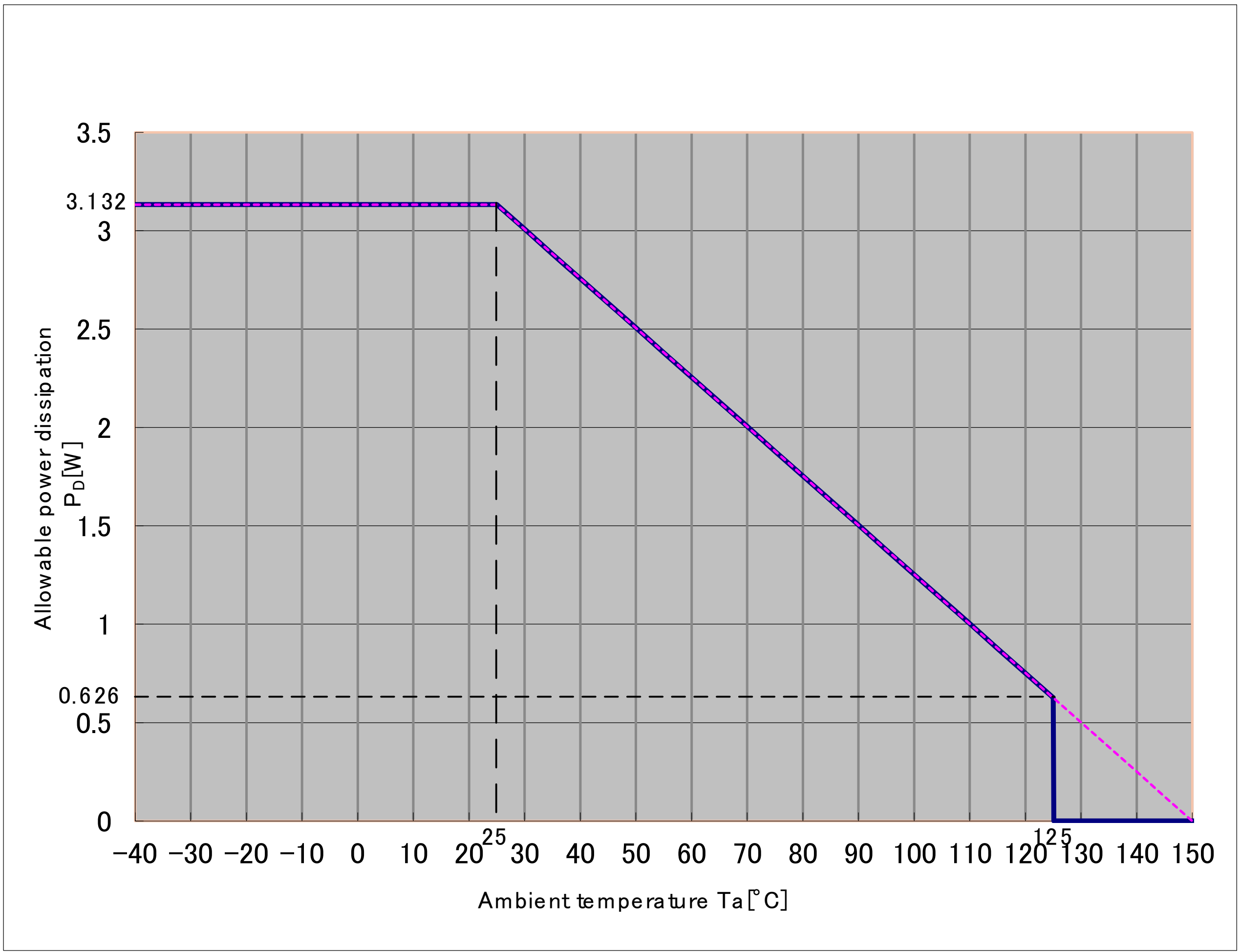

Fig. 6-1 Power Dissipation

Conditions: JEDEC Four-Layer Board

The allowable loss varies depending on the ambient temperature and heat dissipation conditions. Please design with sufficient margin after thorough consideration.

Notes on Contents

1. **Block Diagrams**
   Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. **Equivalent Circuits**
   The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

IC Usage Considerations

Notes on Handling of Ics

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure.

Points to Remember on Handling of ICs

(1) Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature clears the heat generation status immediately.

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