TB9084FTG
Application Note

1. INTRODUCTION

TB9084FTG is a gate-driver IC for brushless motors in vehicle application.
It features the three-phase gate-driver. It also has a charge pump, a motor current detector circuit, an oscillator circuits and an SPI communication circuit. It has multiple error detection features. Trigger threshold, response action and other settings are modified via the SPI communication.

Contents

2. Power Voltage

2.1. Operating voltage ranges

Table 2.1 Operating voltage ranges

Parameter	Applied pin	Symbol	Operating voltage range	Unit	Condition
Input voltage	VB	Vb	5.7 to 28	V	DC
	VCC	Vcc	3.0 to 5.5	V	DC

Note: This product assumes to be used with a 12 V battery.
Note: It is not recommended to use this product at Vb<4.8 V all the time.

2.2. Startup sequence

Apply voltage to VB and VCC. (Apply voltage to VCC after applying voltage to VB.)
Slew rates of Vb and Vcc should be within the ranges below.
(Vb= less than 8V/μs, Vcc= less than 0.3V/μs)
After the low-voltage condition on VCC is undetected, the charge pump starts operation.
Once the charge pump completes its startup, NDIAG signal transitions to high,
enabling control of the gate driver for motor operation.

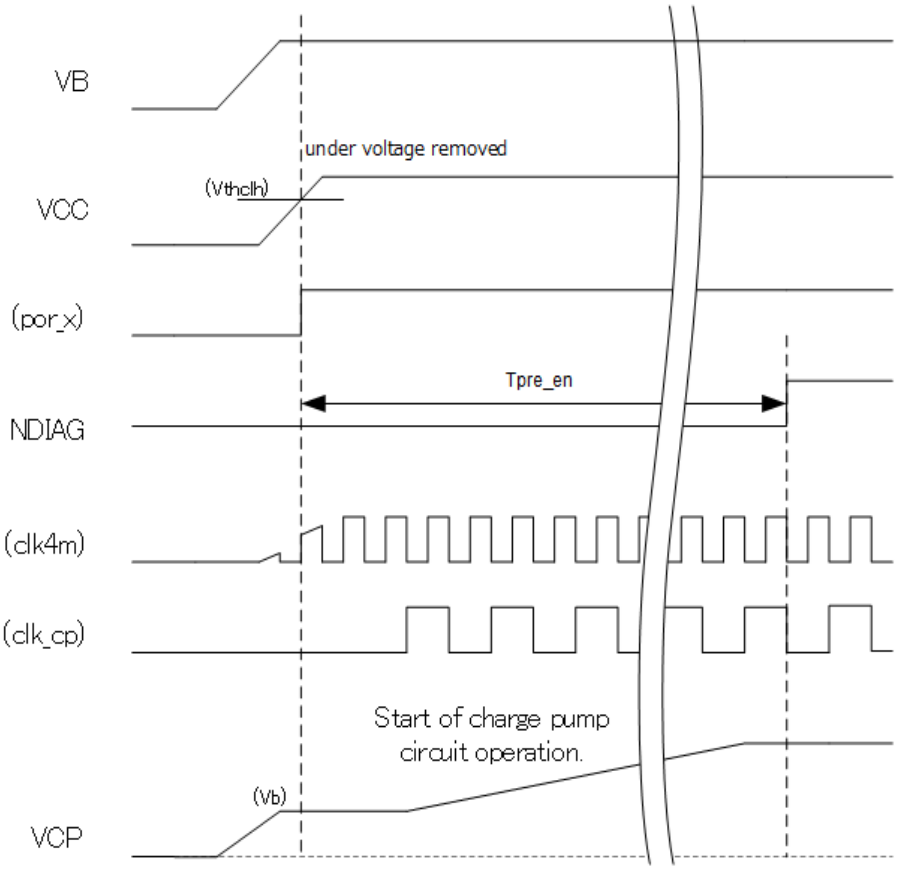

Fig. 2.1 Startup sequence

3. Application circuit example

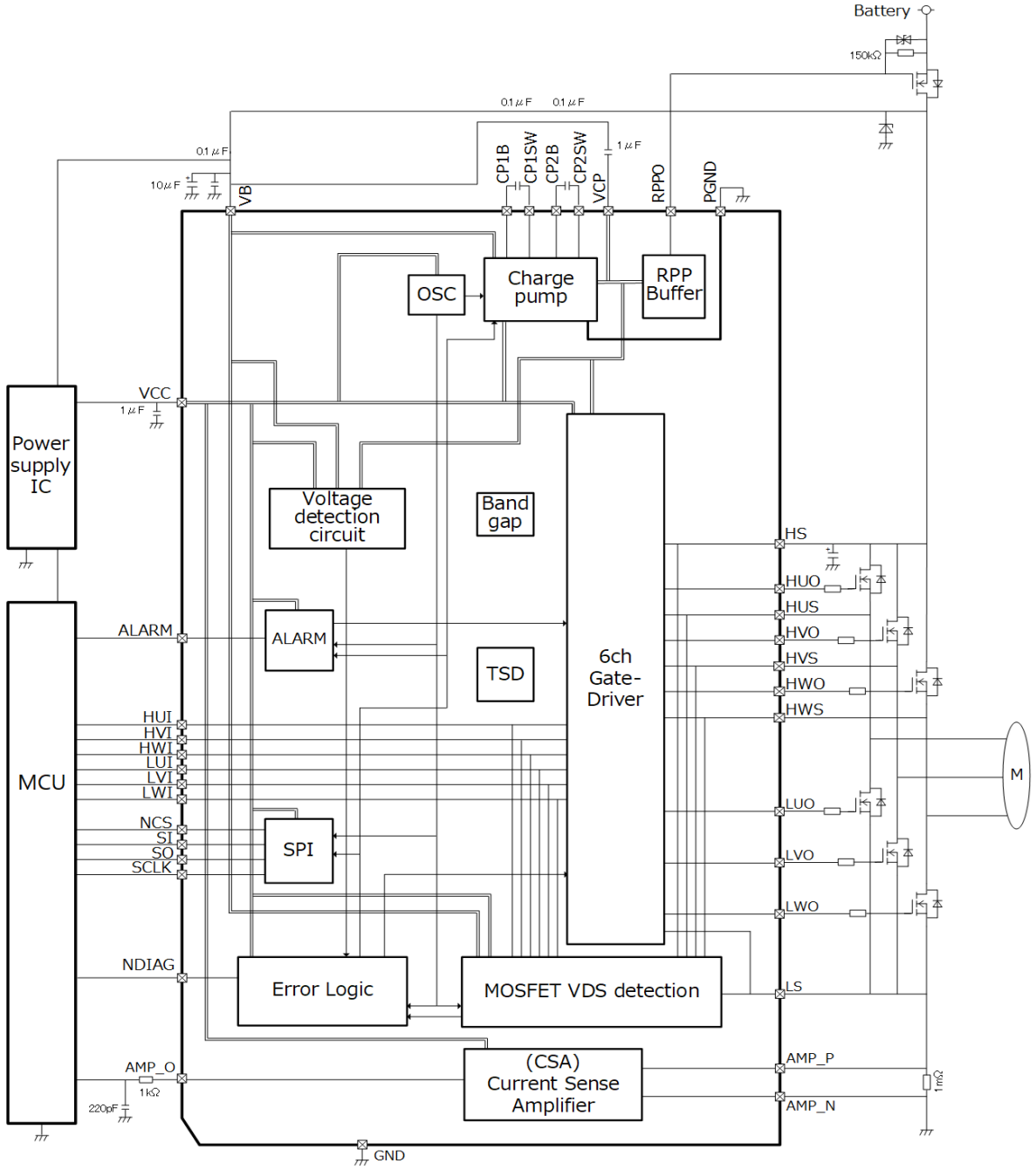

Fig. 3.1 Application circuit example

≪Notes for users≫

- Circuit constants shown here are for this application circuit example and not guaranteed. Determine peripheral circuits based on thorough evaluation and check under conditions assuming an operating environment on a board. Providing these application circuit examples does not grant a license for industrial property rights.
- Place smoothing capacitors externally connected to the power source terminals (VB, VCC, VCP) as close to the base of the IC as possible.
- Use solid GND (the same potential ±0.3V) on the board for GND terminal.
- In designing a unit, take into notes for each block into consideration as well.
- Do not connect this product incorrectly. It may break this IC and/or damage the equipment.

4. Power consumption

Fig 4.1 shows the graph of thermal resistance and allowable power dissipation (excerpted from the TB9084FTG datasheet).

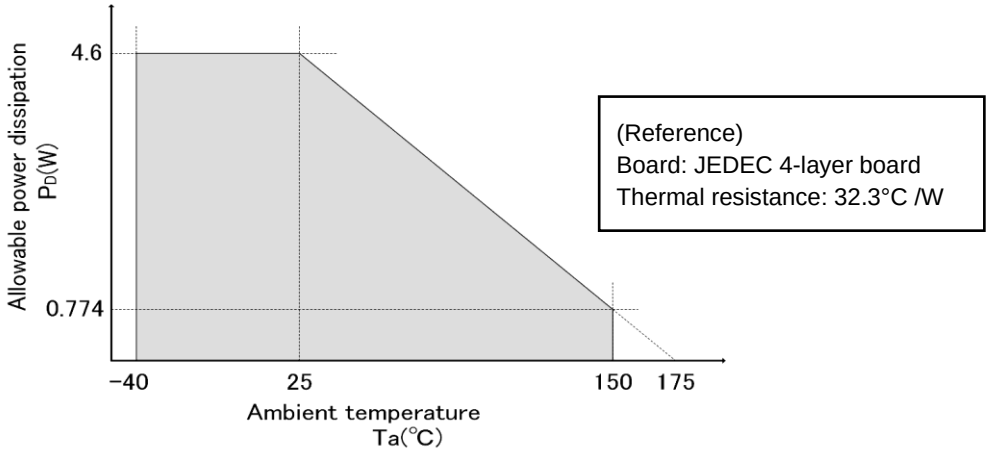

Fig. 4.1 Allowable dissipation curve

Fig 4.2 shows a graph of thermal resistance and allowable power dissipation, comparing different numbers of thermal vias (4 and 8) on the PCB for this IC package.
Differences in the number of thermal vias result in variations in thermal resistance.
Therefore, it is important to optimize the PCB design to ensure sufficient allowable power dissipation.
For layout design of QFN packages, refer to our website's "Package Mounting Guide QFN".
https://toshiba.semicon-storage.com/info/MountManual_en_20160317.pdf?did=36457

In PCB layout design, factors such as the heat dissipation area, number of board layers, copper thickness, and the presence of heat-generating components on the same board can affect the allowable power dissipation.
Therefore, it is essential to validate the design under the intended operating conditions.

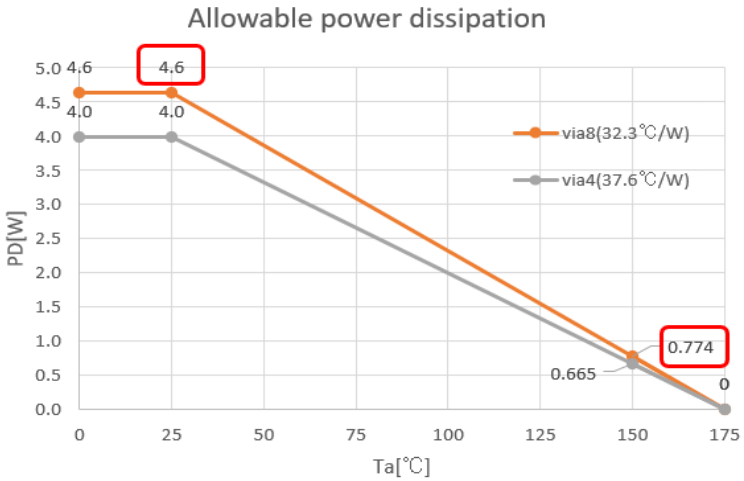

Fig. 4.2 Allowable power dissipation (Example Comparison by Number of Vias)

4.1. Calculation of power consumption

4.1.1. Power consumption of gate driver section

As a user-configurable factor that affects power consumption, this section explains the power consumption involved in charging and discharging the gate capacitance (Cg) of an external NMOS transistor during PWM operation.

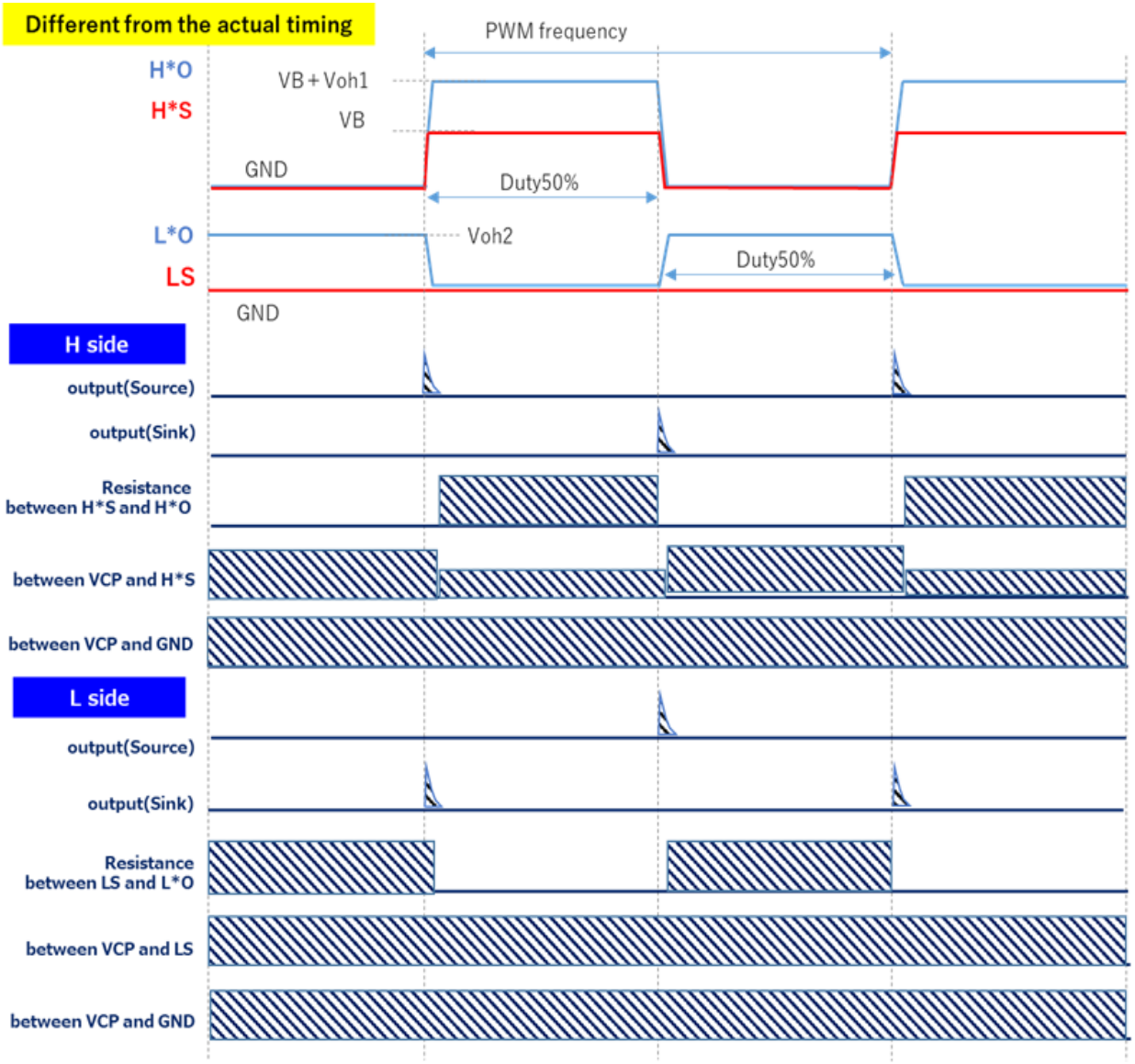

Fig. 4.3 Power consumption chart of gate driver section

■General Formula for Power Consumption (Charging/Discharging) in Gate Driver Section

In the case of a 3-phase brushless motor (6 channels) operating at a PWM frequency of 20 kHz, the power consumption of one H*O channel is calculated based on one charge and one discharge cycle within each 50µs PWM period.
When using methods such as applying the differential equation of the RC circuit shown in Equation (1) to the circuit configuration, or integrating and time-averaging the sampled values of v(t) * i(t) as shown in Equation (2) to calculate average power, or using simulation tools, the verification process becomes more constrained.

Differential Equation of an RC Circuit：$q(t)=CE(1-e^{-t/RC})$ ・・・・・・・・・・・・（1）

Average Power Calculation Formula： $P=\frac{1}{T}*\int_0^t v(t)*i(t)dt$ ・・・・・・・・・・・・（2）

High-side gate driver (1 channel) ：$P(H*O)=\frac{1}{50\mu s}*\int_0^{50\mu s} v(t)*i(t)dt$

Low-side gate driver (1 channel) ：$P(L*O)=\frac{1}{50\mu s}*\int_0^{50\mu s} v(t)*i(t)dt$

P (Charging and Discharging for 6 Channels) = P(H*O) *3 + P(L*O) *3

■Calculation conditions for gate driver power dissipation

The table below summarizes the conditions used to calculate power consumption.
The yellow-highlighted cells indicate parameters that can be freely modified by the user and have a direct impact on power consumption.
Other parameters are less sensitive and can be treated as provisional fixed values.
Assuming an external resistor Rs of 10 Ω or higher, the total power consumption of the IC can be reasonably estimated.

Power Consumption Calculation

input

<Calculation Conditions>

VB (V)	VCP (V)	VCC (V)	Ta (℃)	HS (V)
12	24.0	5	25	12

●Calculation of Average Output Current of Gate Driver

GateDriver PWM frequency (kHz)	PWM Duty (%)	Hi-sideGate RDS(on) (Ω)	L-sideGate RDS(on) (Ω)	Hi-sideGate resistance Rs= (Ω)	L-sideGate resistance Rs= (Ω)	C-gate (nF)	Hi-sideGate saturation voltage Voh1(V)	L-sideGate saturation voltage Voh2(V)	Resistance between H*O and H*S (kΩ)	Resistance between L*O and LS (kΩ)
20.0	20.0	8.8	3.0	22.0	22.0	6.1	9.46	9.91	50.0	50.0
				10Ω<Rs	10Ω<Rs					

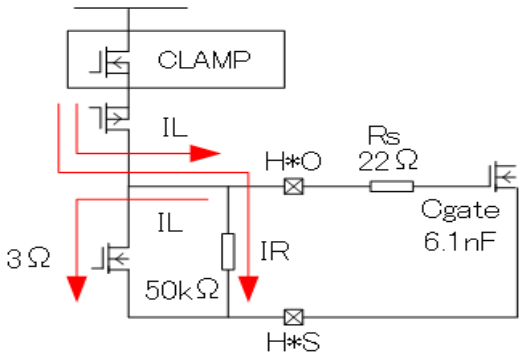

Fig. 4.4 Power consumption diagram of gate driver section

■Gate Capacitance Charge and Discharge Component

When the external resistor Rs inserted between H*O and Cgate is 10Ω or more, the following approximation generally holds.

With VB fixed at 12V and VCC at 5V, the following calculation can be performed.
IL(H)=Voh1*Cgate*PWM=9.46V*6.1nF*20kHz=1.15mA
P(H)=24*1.15m*(8.8+3)/ (8.8+22+22+3) =5.83[mW]

Similarly, for L*O, the value can be derived in the same manner.
IL(L)=Voh2*Cgate*PWM=9.91V*6.1nF*20kHz=1.21mA
P(L)=24*1.21m*(8.8+3)/ (8.8+22+22+3) =6.12[mW]

The total for the 6-channel gate driver
P=P(H)*3+P(L)*3 = 36[mW] is calculated to be approximately.

Fig 4.5 illustrates the relationship between the value of the external resistor Rs and the power consumption of the IC gate driver section. It can be observed that when the value of Rs is small, the power consumption of the IC gate driver increases proportionally with the increase in the external NMOS gate capacitance (Cg).

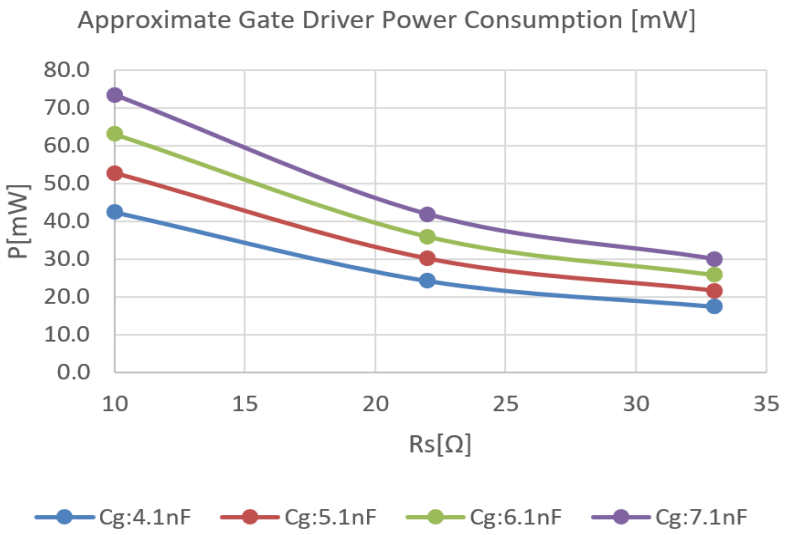

Fig. 4.5 Power Consumption Image of Gate Driver Section

■Power Consumption of External Resistor Rs

When the external resistor Rs inserted between H*O and Cgate is 10Ω or more, the following approximation generally holds.

IL=Voh1*Cgate*PWM=9.91V*6.1nF*20kHz=1.21mA

The external resistor Rs conducts current twice during one PWM cycle—once during charging and once during discharging.
P(Rs) =24*1.22m*(22+22)/ (8.8+22+22+3) =23[mW]→The power loss for Rs is estimated to be approximately 23mW per chip.

Figure 4.6 shows the relationship between the value of the external resistor Rs and power consumption. It can be seen that as the value of Rs increases—proportional to the increase in the external NMOS gate capacitance (Cg)—the power consumption of Rs also tends to increase.

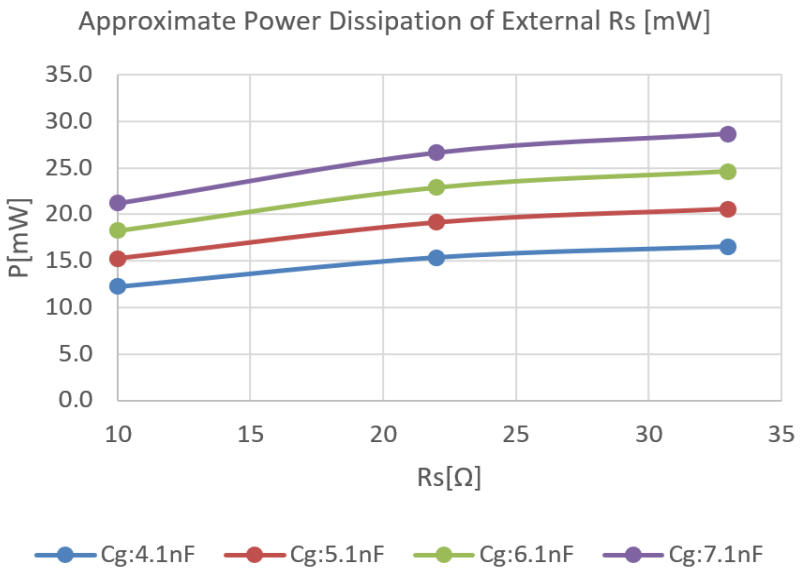

Fig. 4.6 Power Consumption Image of External Resistor Rs

There is a trade-off relationship between IC power consumption and Rs power consumption depending on the value of the external resistor Rs.
In addition, component selection must take into account factors such as temperature derating and EMI.

4.1.2. Total IC Power Consumption

Fig 4.7 shows a reference for IC power consumption under the conditions of VB = 12 V, VCC = 5 V, and PWM = 20 kHz.
The power consumption of the charge pump (CP) circuit varies depending on the gate capacitance (Cg) of the external NMOS transistor in the subsequent stage.
The power consumption of the gate driver section depends on both the external resistor Rs and the gate capacitance Cg of the external NMOS.

For the CP circuit section, component selection should be based on a thorough evaluation of the DC bias and temperature characteristics of the flying capacitors (e.g., 0.1 µF × 2) and the smoothing capacitor connected to VB (e.g., 1 µF). Even if the constants are not changed, we kindly ask that you conduct a thorough evaluation in your environment.

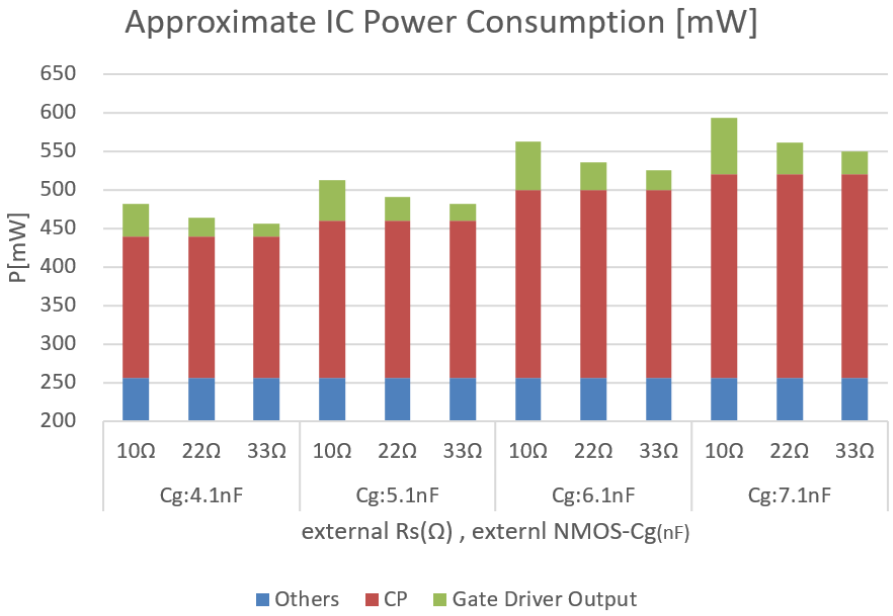

Fig. 4.7 Approximate IC Power Consumption Value

In the graph of allowable loss shown in Figure 4.1, it can be confirmed through calculation that if the value remains within 774 mW, then even after adding the ΔTj margin to Ta = 150 °C, the operating junction temperature Tj will not exceed 175 °C.

Notes on the contents of the description

1. **Block diagram**
   Functional blocks/circuits/constants in the block diagram may be partially omitted or simplified to explain their functions.

2. **Equivalent circuit**
   Equivalent circuits may be partially omitted or simplified to explain the circuit.

Rev.	Editing content	Date
1.0	New	2025-09-01

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