# Notes in use of TB67Z83xxFTG/Z85xxFTG

## Description

TB67Z83xxFTG/TB67Z85xxFTG series have a built-in circuit that can drive three phases of high-side and low-side MOSFETs. Gate drive current of external MOSFETs can be set from 10 mA to 1 A(peak) for source current and from 20 mA to 2 A (peak) for sink current. VM supply voltage can be used in a wide operating range from 8 to 75V and VDRAIN voltage can be used in a wide operating range from 6 to 75V. TB67Z833xFTG/TB67Z853xFTG devices incorporate three gain-adjustable amplifiers, which can be used for shunt current sensing.

Toshiba Electronic Devices & Storage Corporation

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# 1. Main differences between TB67Z83xxFTG, TB67Z85XXFTG

Main differences are shown in table below.

**Table 1.1 Product comparison**

| Product Name | Built-in regulator voltage | Number of current sense amplifiers | Interface | Package |
|---|---|---|---|---|
| TB67Z830HFTG | 3.3 V | 0 ch | Hardware | P-VQFN32-0505-0.50-007 |
| TB67Z830SFTG | | | SPI | |
| TB67Z833HFTG | | 3 ch | Hardware | P-WQFN40-0606-0.50-003 |
| TB67Z833SFTG | | | SPI | |
| TB67Z850HFTG | 5 V | 0 ch | Hardware | P-VQFN32-0505-0.50-007 |
| TB67Z850SFTG | | | SPI | |
| TB67Z853HFTG | | 3 ch | Hardware | P-WQFN40-0606-0.50-003 |
| TB67Z853SFTG | | | SPI | |

# 2. Power Supply Voltage

## 2.1. Operating Range of Power Supply Voltage

**Table 2.1 Operating range of power supply voltage**

| Characteristic | Symbol | Operating Voltage Range | Absolute Maximum Ratings | Unit |
|---|---|---|---|---|
| VM supply voltage | $V_{VM}$ | 8 ~ 75 | 80 | V |
| VDRAIN voltage | $V_{VDR}$ | 6 ~ 75 | 80 | V |

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.

## 2.2. Power-on Sequence with Control Input Signals

The IC supports single power supply operation. To prevent malfunction when the supply voltage is low, it incorporates an undervoltage lockout (UVLO) circuit.
During unstable power supply conditions, such as power-up or power-down (transient regions), it is recommended to keep the motor in the OFF state. Operate the motor only after the supply voltage has stabilized and then switch the input signals. Similarly, it is recommended to turn off the power only after the motor has completely stopped.
Example of power-on sequence is shown below.

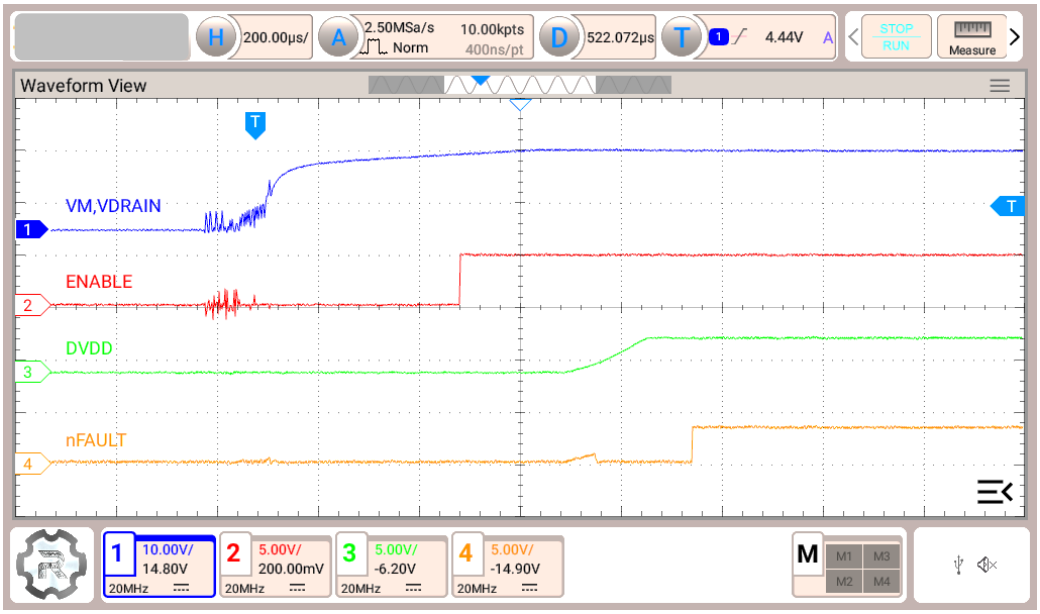
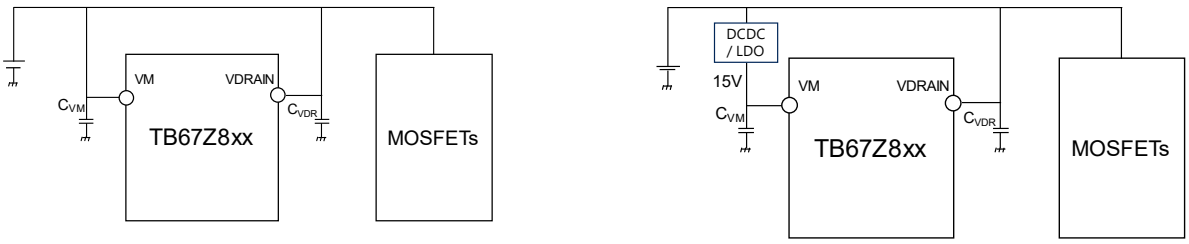



**Figure 2.1 Power-on sequence (nFAULT is pull-up to DVDD)**

Please input the motor control signal only after nFAULT goes High.

It is also possible to apply separate power supplies to VM and VDRAIN. In this case, the IC is powered from VM, while the reference voltage for the charge pump is VDRAIN. When the system supply voltage is high, using a dual-supply configuration can reduce the IC's power consumption and heat generation.




Single power supply configuration

Dual power supply configuration

**Figure 2.2 Power Supply Configuration Examples**

For a dual-supply configuration, to ensure sufficient gate drive voltage for the external MOSFETs, a VM voltage of approximately 15 V is recommended. The VM voltage can be generated using a DC-DC converter or a linear regulator, or it can be supplied simply through a resistor from the power source.

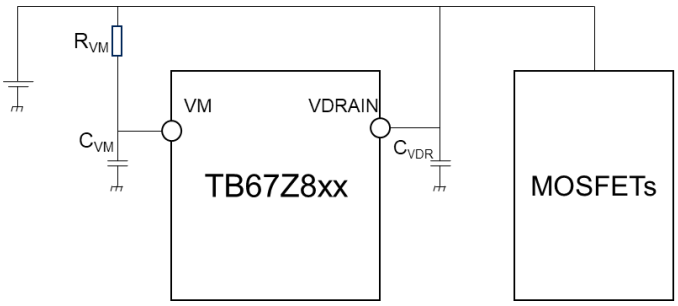



**Figure 2.3 Example of supplying VM through a resistor**

Select the resistor so that the VM pin voltage is approximately 15 V, taking into account the IC's VM current consumption and voltage fluctuations on the power line.
For example, if the power line voltage is 48 V and the VM current consumption is 15 to 20 mA, inserting a 1.5 kΩ resistor will result in a VM voltage of 18 to 22.5 V (excluding power line voltage variations).
In this case, the resistor's power dissipation is $(20\,\text{mA})^2 \times 1.5\,\text{k}\Omega = 0.6\,\text{W}$, therefore, a resistor with a power rating of at least 1 W is recommended.

## 3. Output Current

To control the ON, OFF speed of external MOSFETs, the IC incorporates a function to adjust the gate drive current (source and sink current) capability. The source current capability can be set from 10 mA to 1 A, and the sink current capability can be set from 20 mA to 2 A.
In the SPI interface version, the gate drive current capability can be configured via registers. In the hardware interface version, it can be configured through the IDRIVE pin.

**Table 3.1 SPI I/F Gate drive current setting register**

| Register | Setting contents |
|---|---|
| IDRIVEP_HS | High-side gate drive source current capability |
| IDRIVEN_HS | High-side gate drive sink current capability |
| IDRIVEP_LS | Low-side gate drive source current capability |
| IDRIVEN_LS | Low-side gate drive sink current capability |

**Table 3.2 Gate drive current capability setting**

| Source current capability (mA) | Sink current capability (mA) | SPI I/F Register value | Hardware I/F IDRIVE |
|---|---|---|---|
| 10 | 20 | 0000b | Mode 1 |
| 30 | 60 | 0001b | Mode 2 |
| 60 | 120 | 0010b | Mode 3 |
| 80 | 160 | 0011b | — |
| 120 | 240 | 0100b | Mode 4 |
| 140 | 280 | 0101b | — |
| 170 | 340 | 0110b | — |
| 190 | 380 | 0111b | — |
| 260 | 520 | 1000b | Mode 5 |
| 330 | 660 | 1001b | — |
| 370 | 740 | 1010b | — |
| 440 | 880 | 1011b | — |
| 570 | 1140 | 1100b | Mode 6 |
| 680 | 1360 | 1101b | — |
| 820 | 1640 | 1110b | — |
| 1000 | 2000 | 1111b | Mode 7 |

Set the gate drive current according to the characteristics of the external MOSFET.
First, to ensure that the external MOSFET can be reliably turned ON and OFF within the drive time, the required source and sink current capability can be estimated using the following formula:

$$I_{Dirve}(min) = Qg / (t_{DRIVE} - t_{PD}) \quad \text{(Eq.3.1)}$$

Qg: Gate charge of the external MOSFET
$t_{DRIVE}$: Drive time
$t_{PD}$: Input propagation delay

Example: Driving TPH1R204PB, since the MOSFET's Qg is 44 nC (typ.),
When the drive time is set to the maximum of 4000 ns, $I_{Drive}(min)$ = 11.5 mA
When the drive time is set to the minimum of 600 ns, $I_{Drive}(min)$ = 103.5 mA

When turning the MOSFET ON, the source current capability decreases as the gate voltage rises; when turning it OFF, the sink current capability decreases as the gate voltage falls. In addition, drive current should be set with sufficient margin, taking into account variations in drive time, input propagation delay,

and MOSFET gate charge.
If the drive current is too small, the MOSFET may not turn ON/OFF reliably within the drive time, and a gate drive voltage fault may be detected. Conversely, if the drive current is too large, there is a risk of ringing, oscillation, and degraded EMI noise performance. Always evaluate thoroughly on actual hardware and set an appropriate drive current capability.


Figure 3.1 Isource = 1 A, H-side, Positive current


Figure 3.2 Isource = 1 A, H-side, Negative current

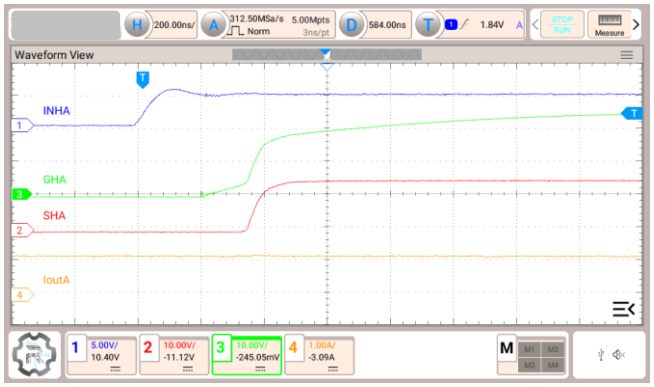



Figure 3.3 Isource = 120 mA, H-side, Positive current


Figure 3.4 Isource = 120 mA, H-side, Negative current

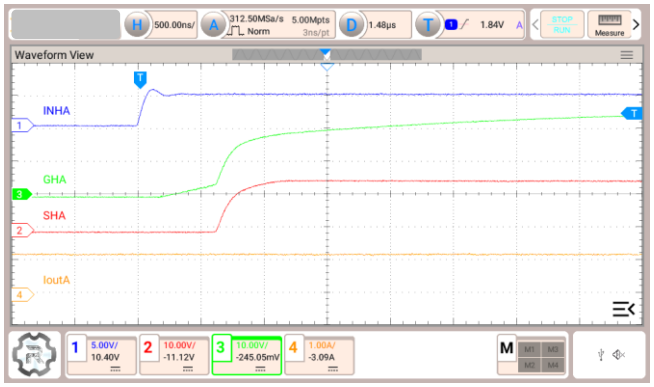



Figure 3.5 Isource = 30 mA, H-side, Positive current


Figure 3.6 Isource = 30 mA, H-side, Negative current


Figure 3.7 Isource = 1 A, L-side, Positive current


Figure 3.8 Isource = 1 A, L-side, Negative current


Figure 3.9 Isource = 120 mA, L-side, Positive current


Figure 3.10 Isource = 120 mA, L-side, Negative current


Figure 3.11 Isource = 30 mA, L-side, Positive current

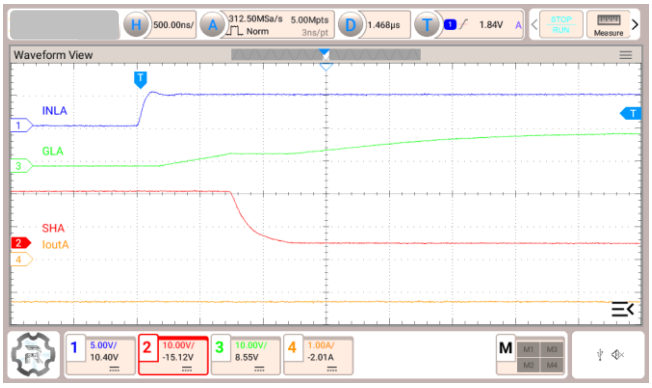



Figure 3.12 Isource = 30 mA, L-side, Negative current


Figure 3.13 Isink = 2 A, H-side, Positive current


Figure 3.14 Isink = 2 A, H-side Negative current


Figure 3.15 Isink = 240 mA, H-side, Positive current


Figure 3.16 Isink = 240 mA, H-side, Negative current


Figure 3.17 Isink = 60 mA, H-side, Positive current


Figure 3.18 Isink = 60 mA H-side Negative current

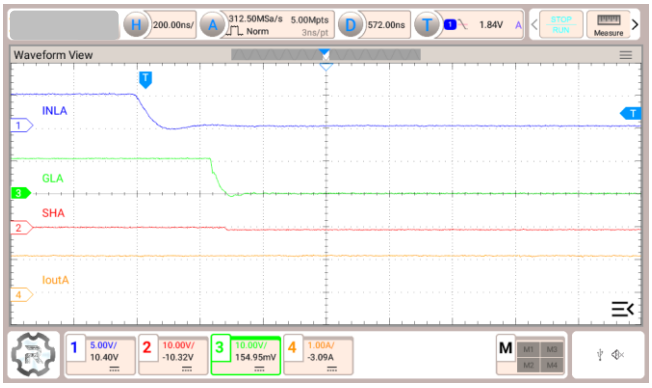



Figure 3.19 Isink = 2 A, L-side, Positive current


Figure 3.20 Isink = 2 A, L-side, Negative current

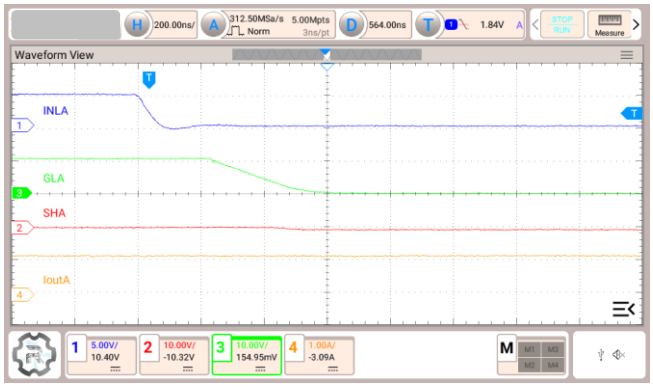



Figure 3.21 Isink = 240 mA, L-side, Positive current


Figure 3.22 Isink = 240 mA, L-side, Negative current


Figure 3.23 Isink = 60 mA, L-side, Positive current


Figure 3.24 Isink = 60 mA, L-side, Negative current

# 4. Control inputs

## 4.1. ENABLE signal input

The IC enters standby mode If the ENABLE pin remains Low for 40 µs or longer. If the Low period of the ENABLE pin is between 5 and 40 µs, it is recognized as an error reset pulse, which clears the fault flag without transitioning to standby mode.
Note that the above timing depends on the internal oscillator frequency ($f_{OSC}$). When $f_{OSC}$ is 20 MHz, the time recognized as an error reset pulse is 5 to 40 µs. If $f_{OSC}$ is higher, this time becomes shorter. Control the ENABLE signal while considering the variation range of $f_{OSC}$.

## 4.2. INHx/INLx input

The states of each gate drive output terminal (GHx / GLx) can be controlled via the INHx and INLx pins. This IC supports four types of control modes.

### 4.2.1. 6-PWM input mode

6-PWM input mode is a commonly used mode, in this mode, each of the three half-bridges can be controlled independently. The state of each half-bridge can be controlled to Low, High, and High impedance (Hi-Z) through the inputs of the INHx and INLx pins.

**Table 4.1 6-PWM input mode**

| INLx | INHx | GLx | GHX | SHx |
|---|---|---|---|---|
| L | L | L | L | Hi-Z |
| L | H | L | H | H |
| H | L | H | L | L |
| H | H | L | L | Hi-Z |

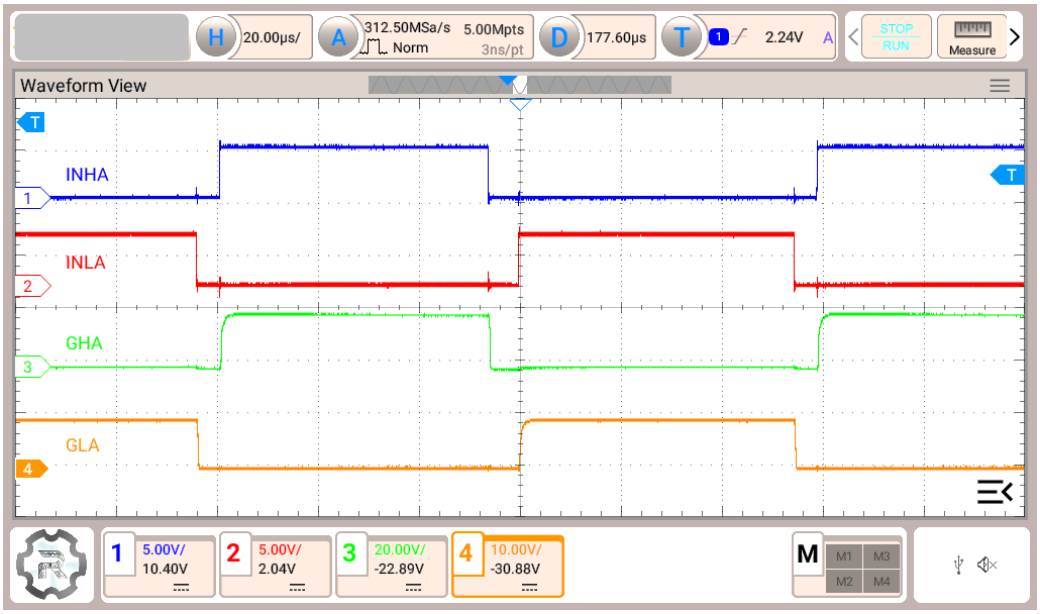



**Figure 4.1 6-PWM input mode waveform example**

As a noise countermeasure for the INHx/INLx pins, consider adding a capacitor (approximately 1000 pF) between the pins and GND.

### 4.2.2. 3-PWM input mode

In 3-PWM input mode, each half-bridge can be controlled to either Low or High state via the INHx pin. The INLx pin can be used to set the half-bridge to a high-impedance (Hi-Z) state.

**Table 4.2 3-PWM input mode**

| INLx (ENABLE) | INHx (PWM) | GLx | GHX | SHx |
|---|---|---|---|---|
| L | X | L | L | Hi-Z |
| H | L | H | L | L |
| H | H | L | H | H |

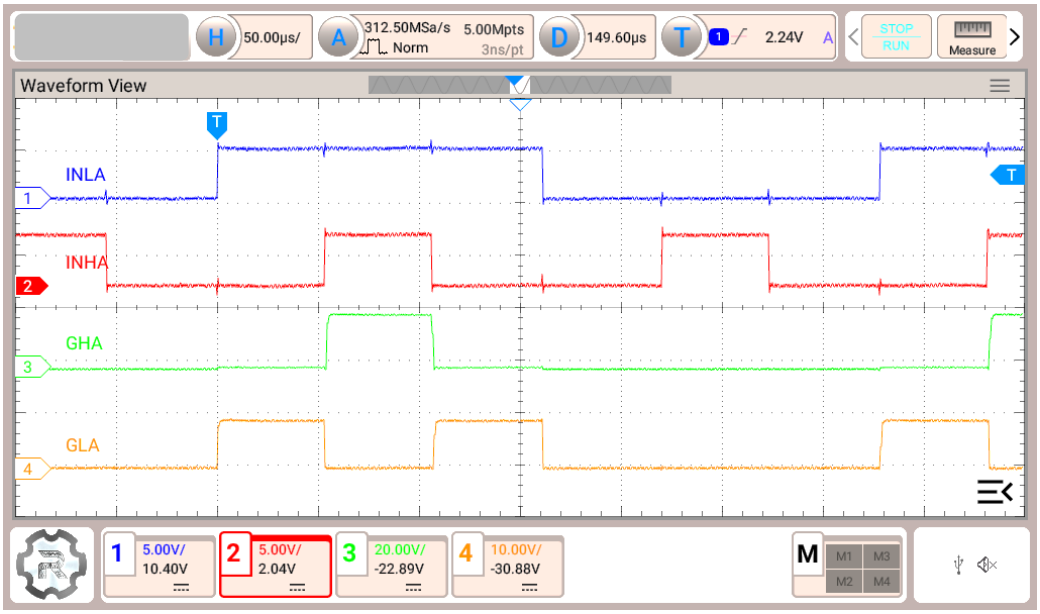



**Figure 4.2 3-PWM input mode waveform example**

As a noise countermeasure for the INHx/INLx pins, consider adding a capacitor (approximately 1000 pF) between the pins and GND.

### 4.2.3. Hall input mode

In Hall input mode, by inputting the three-phase Hall signals to the INLA, INHB, and INLB pins, and providing the PWM frequency and PWM duty to the INHA pin and the rotation direction signal to the INHC pin, rectangular wave drive (120° conduction) can be easily achieved. Additionally, the INLC pin can be used to control the BRAKE function. For details, refer to the datasheet section “11.1.1.3. Hall Input Mode.”

When using Hall signals from an open collector output Hall IC, a pull-up circuit is required. Also, as a noise countermeasure, consider adding a capacitor (100–1000 pF) to GND.

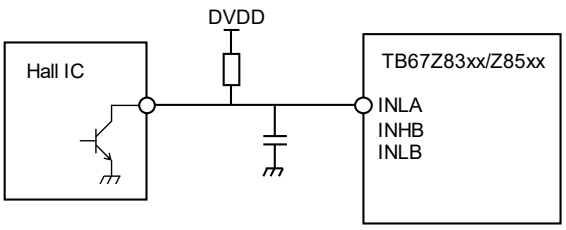



**Figure 4.3 Hall signal pull-up example**

### 4.2.4. Independent PWM mode

In independent PWM mode, high-side and low-side gate drive is controlled separately.

**Table 4.3 Independent PMW mode**

| INLx | INHx | GLx | GHX |
|---|---|---|---|
| L | L | L | L |
| L | H | L | H |
| H | L | H | L |
| H | H | H | H |

When using both the high-side and low-side of the same half-bridge simultaneously in Independent PWM mode, please disable the VDS over current detection function to avoid false detection.

As a noise countermeasure for the INHx/INLx pins, consider adding a capacitor (approximately 1000 pF) between the pins and GND.

## 4.3. Hardware Control interface

In the Hardware I/F version, the functions of the IC are controlled using four pins: GAIN, IDRIVE, MODE, and VDS. Additionally, functions can be configured by shorting to IC's DVDD and AGND or connect through a resistor, eliminating the need to directly apply external voltage.
As a noise countermeasure for the pins, consider adding a capacitor (approximately 1000 pF) between the pins and GND.

## 4.4. SPI Control interface

In the SPI I/F version, communication with the IC and control of its functions are performed using four pins: nCS, SCLK, SDI, and SDO.
nCS is the chip select pin, and communication is enabled when it is Low. SCLK is the clock signal input pin, SDI is the data input pin. and SDO is the data output pin.
While nCS is High, inputs to SCLK and SDI are ignored, and the SDO pin is Hi-Z state. During transitions of nCS from High to Low or Low to High, SCLK must be held Low. Additionally, nCS should remain High for at least 400 ns between two communications.

The input data from SDI consists of 1-bit command, 4-bit address, and 11-bit data. The first 1-bit (RW) indicates the read/write command, RW = 0b for write, RW = 1b for read. The next 4 bits specify the target register address, and the final 11 bits represent the data content.
The output data from SDO consists of the first 5 bits as “Don’t care” bits, and the remaining 11 bits as the register content.

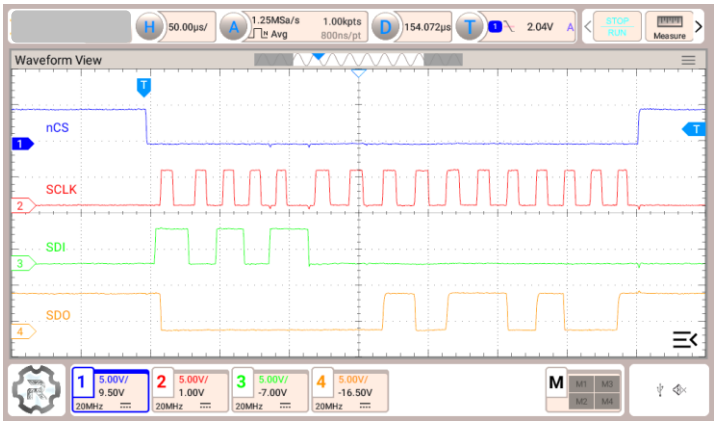



**Figure 4.4 SPI read waveform example**

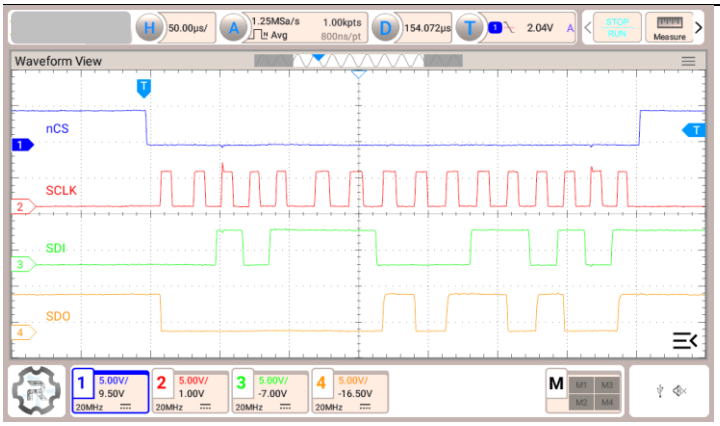



**Figure 4.5 SPI write waveform example**

## 5. DVDD output

The DVDD pin is the output of the internal regulator. For the TB67Z83xxFTG, the output voltage is 3.3 V (typ.), and for the TB67Z85xxFTG, it is 5 V (typ.).

To stabilize the internal regulator, add a ceramic capacitor with a capacitance of 1 µF, a withstand voltage of 6.3 V or more, and a temperature characteristic of X5R or X7R, between the DVDD and AGND pins, and place it as close to the device as possible.

If the regulator is used as a power source for external circuits, the output current must be limited to 30 mA. Also, note that the IC may generate heat depending on the regulator's power consumption, so please pay attention to the absolute maximum temperature rating.

## 6. Charge pump

To generate the power supply for driving the high-side external MOSFET, a charge pump circuit is built into the IC. The operation of the charge pump is as follows:
First, as indicated by the blue arrows in the diagram, electric charge supplied from VDRAIN is charged into C1 (flying capacitor). Next, as indicated by the red arrows, the lower terminal of C1 (CPL) is boosted up to the VM voltage level. Since the potential difference across C1 is already charged and maintained, the upper terminal (CPH) is also boosted by the same amount as CPL, and this voltage is then charged into C2. When the voltage at the VCP pin exceeds VDRAIN + 11 V, the charge pump operation stops.

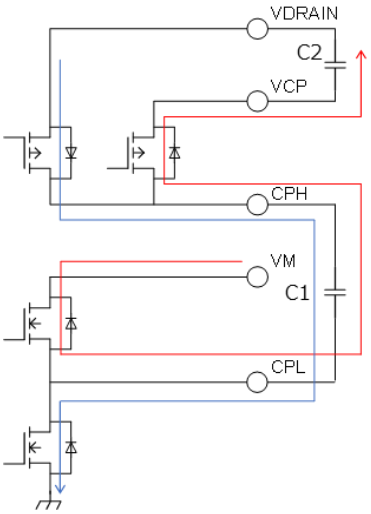



**Figure 6.1 Charge pump circuit**

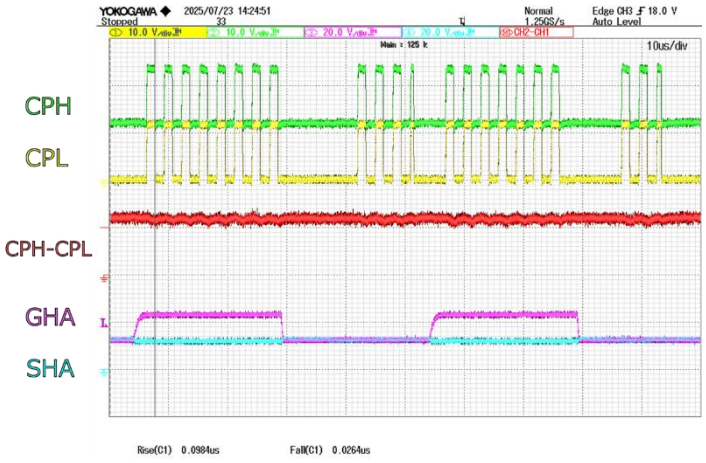



**Figure 6.2 Charge pump waveform example**

The charge pump voltage depends on the VM voltage. If the VM voltage is below 12 V, the charge pump voltage decreases accordingly.

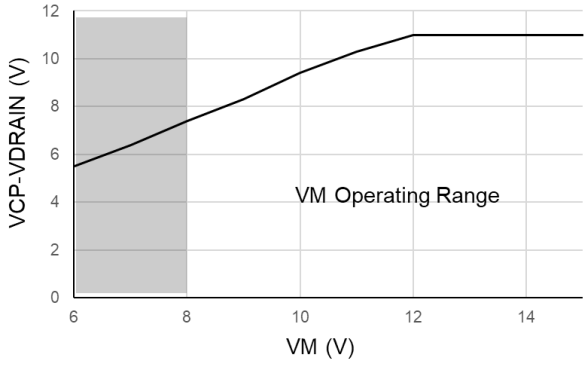
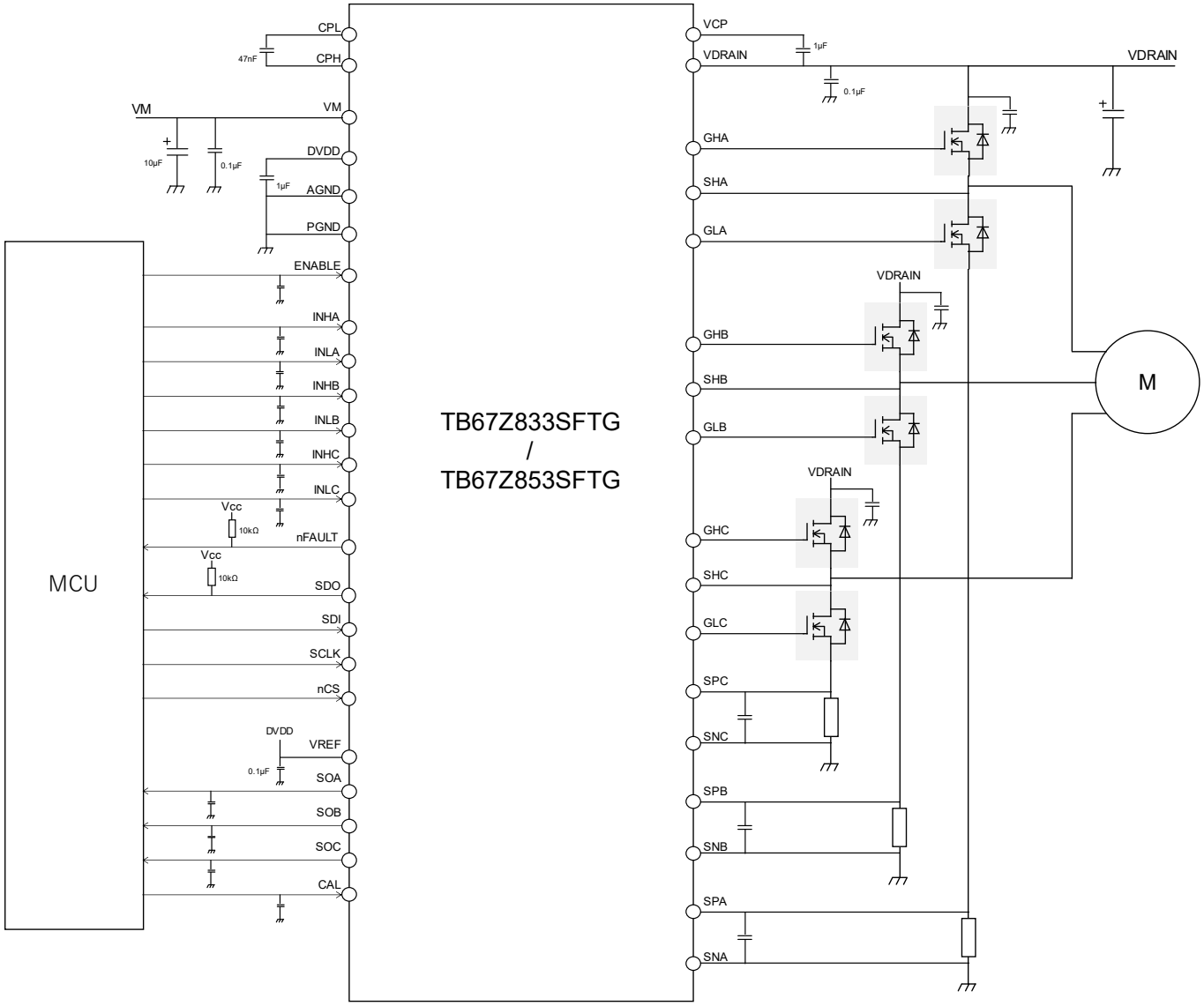



**Figure 6.3 Relationship between VCP and VM (reference date)**

## 7. Application Circuit Example




Note: Add capacitors for noise rejection to the input pins as required.

Note: In the event of a short circuit between pins, or a ground/supply fault in output, there is a possibility that device is destroyed or ignited, or over-voltage or over-current may be applied to peripheral components. Therefore, be especially careful when designing the output lines, VM lines, VDRAIN lines and ground lines. In addition, rotary insertion (reverse insertion) of the device may also cause breakdown or ignition.

Note: The application circuit examples are not guaranteed for mass production design. Thorough evaluation is required, especially at the mass production design stage. Providing these application circuit examples does not grant a license for industrial property rights.

**Figure 7.1 Application circuit example**

## 8. Power Dissipation

Regarding the power consumption of the IC, it can be broadly divided into three components:

1. Power consumed by internal logic and analog circuits
2. Power consumed by the gate driver
3. Power consumed by the regulator

This can be expressed as:

$P_{(Total)} = P_{(Inter)} + P_{(Gate)} + P_{(DVDD)}$

Power consumed by internal logic and analog circuits can be estimated using the following formula:

$P_{(Inter)} = P_{(VM)} + P_{(VDRAIN)}$
$= V_{VM} \times I_{VM} + V_{VDRAIN} \times I_{VDRAIN}$ (Eq.8.1)

Power consumed by the gate driver can be estimated using the following formula:

$P_{(Gate)} = P_{(HS)} + P_{(LS)}$
$= V_{VCP} \times I_{GATE\_HS} + V_{VM} \times I_{GATE\_LS}$ (Eq.8.2)

The average gate drive current, $I_{GATE\_xx}$, depends on the MOSFET's gate charge (Qg), the PWM frequency ($f_{PWM}$), and the drive method.

For rectangular wave drive with synchronous rectification (120° commutation): $I_{GATE\_xx} = Qg \times f_{PWM}$
For two-phase modulated sine wave drive (180° commutation): $I_{GATE\_xx} = 2 \times Qg \times f_{PWM}$

Please ensure that $I_{GATE\_xx}$ remains within the operating range of 25 mA.
For a PWM frequency of 20 kHz, in the case of rectangular wave drive (120° commutation), use MOSFETs with Qg < 1250 nC, in the case of two-phase modulated sine wave drive (180° commutation), use MOSFETs with Qg < 625 nC.

Power consumed by the regulator can be estimated using the following formula:

$P_{(DVDD)} = (V_{VM} - V_{DVDD}) \times I_{DVDD}$ (Eq.8.3)

Example:
under the conditions where TB67Z83xxFTG is used with VM = VDRAIN = 24 V, an external MOSFET TPH1R204PB (Qg = 44 nC), 20 kHz two-phase modulated sine wave drive, and 5 mA current supplied externally from DVDD, the IC's power consumption can be estimated as follows:

$P_{(Inter)} = 24\ V \times 15\ mA + 24\ V \times 4\ mA = 0.45\ W$
$P_{(Gate)} = (24\ V + 11\ V) \times (2 \times 44\ nC \times 20\ kHz) + 24\ V \times (2 \times 44\ nC \times 20\ kHz) = 0.10\ W$
$P_{(DVDD)} = (24\ V - 3.3\ V) \times 5\ mA = 0.10\ W$
$P_{(Total)} = P_{(Inter)} + P_{(Gate)} + P_{(DVDD)} = 0.66W$

## 8.1. Heat dissipation design

When using ICs, ensure that proper heat dissipation design is implemented so that the specified junction temperature ($T_j$) is never exceeded under any circumstances.

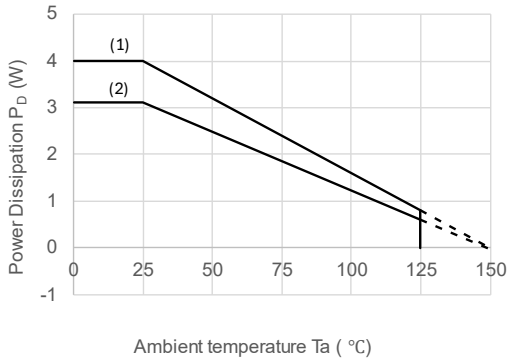
$T_j = P_{(Total)} \times R_{th\ (j\text{-}a)} + T_a$

$R_{th\ (j\text{-}a)}$: Thermal resistance between junction and ambient.

$T_a$: Ambient temperature.

Please note that the $R_{th\ (j\text{-}a)}$ will be affected due to the circumstances around the device.

Based on the above calculation values, please ensure thorough implementation evaluation for thermal design on the PCB and other components, and design with sufficient margin.



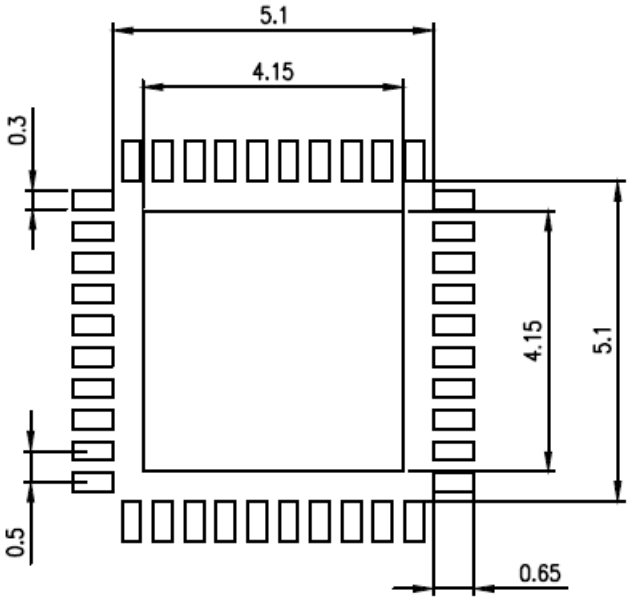

(1) WQFN40. On PCB (JEDEC 4 layers) and Ta=25 °C, $R_{th\ (j\text{-}a)}$ = 31°C/W
(2) VQFN32, On PCB (JEDEC 4 layers) and Ta=25 °C. $R_{th\ (j\text{-}a)}$ = 40°C/W

**Figure 8.1 Power dissipation**

## 9. Reference land pattern

P-WQFN40-0606-0.50-003

unit: mm




P-VQFN32-0505-0.50-007

unit: mm

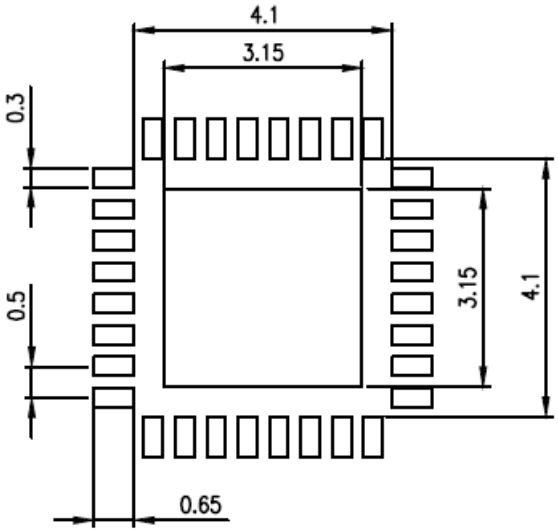



**Figure 9.1 Reference land pattern**

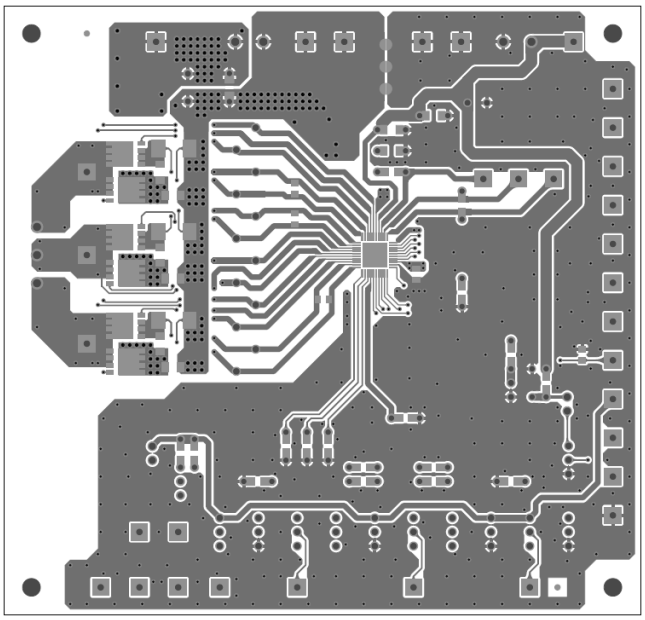
Notes

- All linear dimensions are given in millimeters unless otherwise specified.
- This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only TOSHIBA is not responsible for any incorrect or incomplete drawing and information.
- You are solely responsible for all aspects of your own land pattern, including but not limited to soldering processes.
- The drawing shown may not accurately represent the actual shape or dimensions
- Before creating and producing design and using, customers must also refer to and comply with the latest versions of all relevant TOSHIBA information and the instructions for the application that Product will be used with or for.

# 10. Layout Example

## 10.1. B67Z833xFTG / Z853xFTG

表



裏

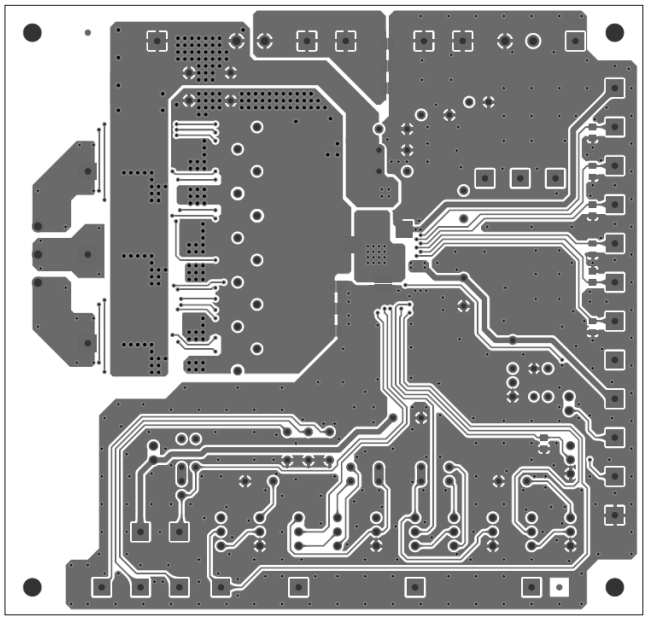
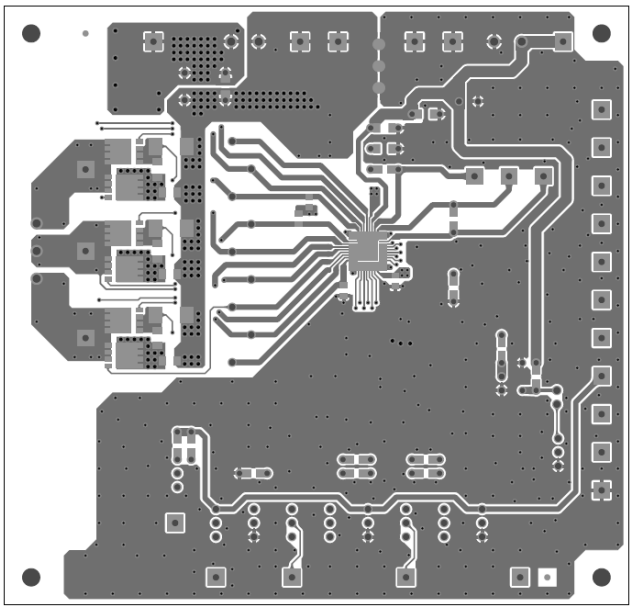


**Figure 10.1　Layout example (WQFN40)**

## 10.2. TB67Z830xFTG / Z850xFTG

表



裏

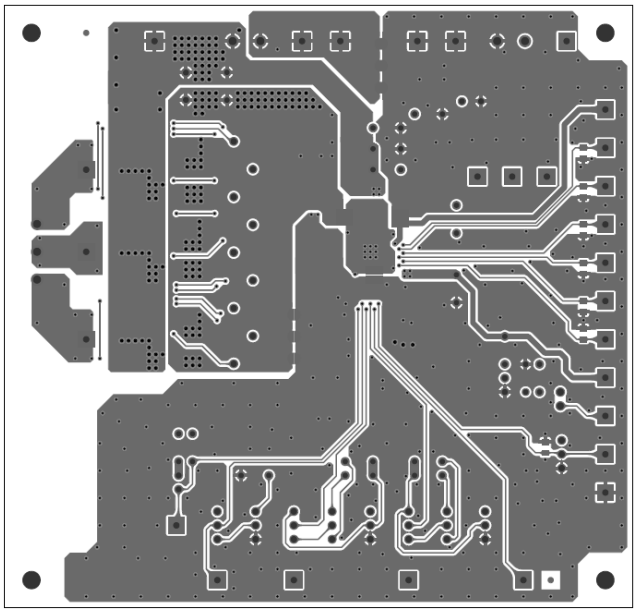


**Figure 10.2　Layout example (VQFN32)**

### Notes on Contents

1. **Block Diagrams**
   Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. **Equivalent Circuits**
   The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. **Timing Charts**
   Timing charts may be simplified for explanatory purposes.

4. **Application Circuits**
   The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage. Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

## IC Usage Considerations

### Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause the device breakdown, damage, or deterioration, and may result in injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke, or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. In addition, do not use any device that has been powered on while inserted in the wrong orientation or incorrectly even just one time.

## Points to Remember on Handling of ICs

(1) Over current Protection Circuit
Over current protection circuits do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if overcurrent continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.

(4) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor’s power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device’s motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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