1.1kW ITTF
(Interleaved Two Transistor Forward)
AC-DC Converter for Servers
Design Guide

RD226-DGUIDE-01

Toshiba Electronic Devices & Storage Corporation

Table of Contents

1. Introduction

This design guide explains the design overview of each circuit block of the 1.1kW server-use AC-DC converter employing the ITTF (Interleaved Two Transistor Forward) topology (hereinafter referred to as "this design").

This design is an AC-DC converter for servers that generates DC 12V from an input of AC 90V to 264V and outputs up to 1.1kW. It is equipped with an output ORing circuit, enabling redundant operation. Components are selected with consideration for height during board mounting, making it applicable to 1U-size power supplies. To improve power efficiency, it adopts a totem-pole PFC circuit that does not use a diode bridge and an ITTF topology DC-DC converter, achieving efficiency exceeding the 80 PLUS Platinum standard under 230V input conditions.

In this design, the high-frequency switching element of the totem-pole PFC circuit uses the SiC MOSFET TW107Z65C, and the low-frequency switching element uses the power MOSFET TK024N60Z1. In the ITTF topology DC-DC converter circuit, the primary-side uses the power MOSFET TK165V60Z1, and the secondary-side uses the power MOSFET TPH1R204PL and TPH1R306PL. For isolated gate signal transmission from the primary-side controller, the digital isolator DCL541A01 is used. Additionally, the output ORing circuit uses the power MOSFET TPHR6503PL. These latest Toshiba devices contribute to reduced losses and high-efficiency operation.

※80 PLUS: An efficiency standard for power supply units used in computers such as servers.

2. Main Components

This chapter describes the main components used in this design.

2.1. SiC MOSFET TW107Z65C

The 650V-rated SiC MOSFET TW107Z65C is used as the high-frequency switching element in the totem-pole PFC circuit. The main features of TW107Z65C are as follows:

- Chip design of 3rd generation (Built-in SiC schottky barrier diode)
- Low diode forward voltage: V_{DSF} = -1.35V (Typ.)
- High voltage: V_{DSS} = 650V
- Low drain-source on-resistance: $R_{DS(ON)}$ = 107mΩ (Typ.)
- Less susceptible to malfunction due to high threshold voltage: V_{th} = 3.0 to 5.0V (V_{DS} = 10V, I_D = 1.2mA)
- Recommended gate - source drive voltage: V_{GS_on} =18V, V_{GS_off} = 0V
- Enhancement mode.

Packaging and Internal Circuit

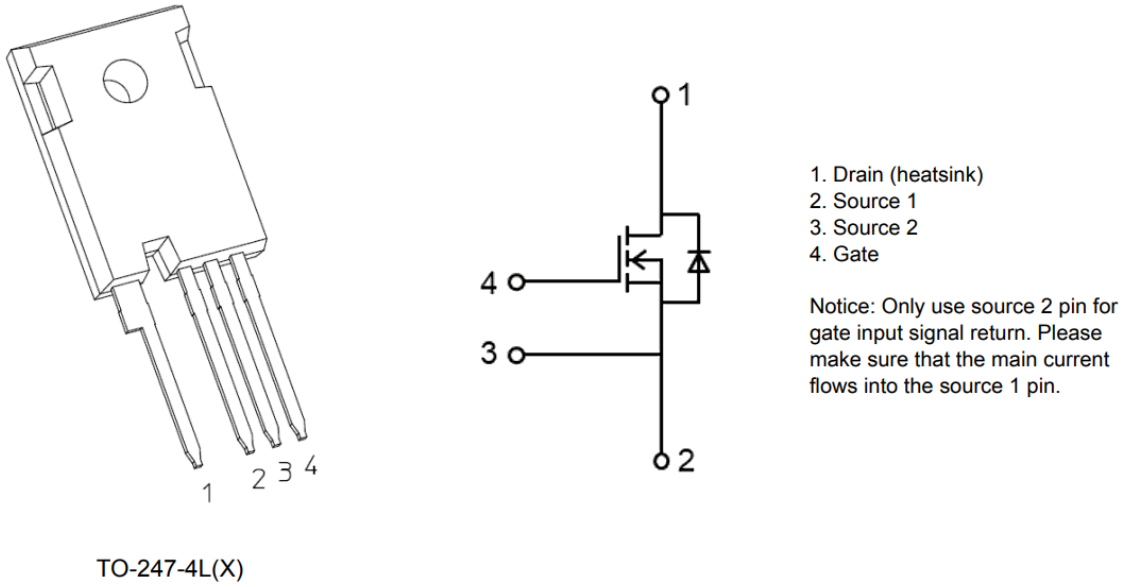

Fig. 2.1 Packaging and Internal Circuit of TW107Z65C

2.2. Power MOSFET TK024N60Z1

The 600V-rated N-channel MOSFET TK024N60Z1 is used as the low-frequency switching element in the totem-pole PFC circuit. The main features of TK024N60Z1 are as follows:

- Low drain-source on-resistance: $R_{DS(ON)}$ = 0.02Ω (Typ.)
- High-speed switching properties with lower capacitance.
- Enhancement mode: V_{th} = 3 to 4V (V_{DS} = 10V, I_D = 3.84mA)

Packaging and Internal Circuit

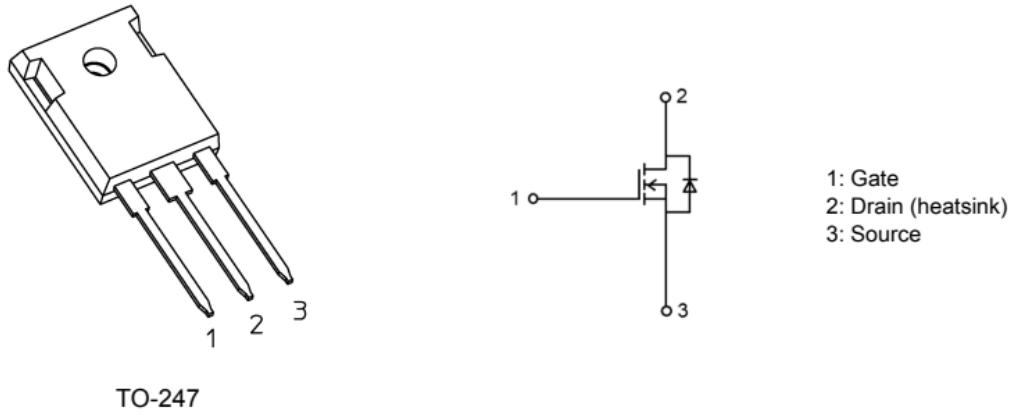

Fig. 2.2 Packaging and Internal Circuit of TK024N60Z1

2.3. Power MOSFET TK165V60Z1

The 600V-rated N-channel MOSFET TK165V60Z1 is used as the primary-side switching element in the ITTF topology DC-DC converter circuit. The main features of TK165V60Z1 are as follows:

- Low drain-source on-resistance: $R_{DS(ON)}$ = 0.138Ω (Typ.)
- High-speed switching properties with the lower capacitance.
- Enhancement mode: V_{th} = 3 to 4V (V_{DS} = 10V, I_D = 0.61mA)

Packaging and Internal Circuit

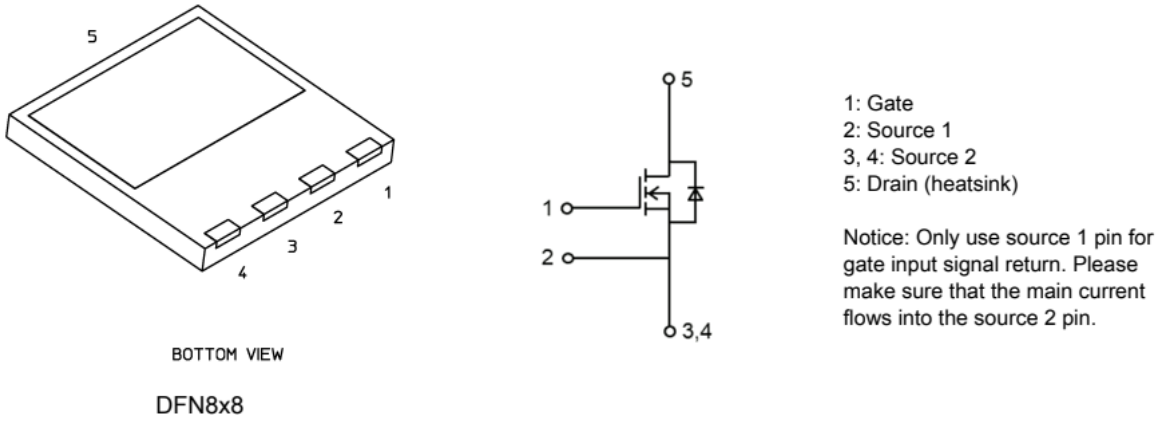

Fig. 2.3 Packaging and Internal Circuit of TK165V60Z1

2.4. Power MOSFET TPH1R204PL

The 40V-rated N-channel MOSFET TPH1R204PL is used as the secondary-side switching element (catch side) in the ITTF topology DC-DC converter circuit. The main features of TPH1R204PL are as follows:

- High-speed switching
- Small gate charge: Q_{SW} = 17nC (Typ.)
- Small output charge: Q_{oss} = 56nC (Typ.)
- Low drain-source on-resistance: $R_{DS(ON)}$ = 1.0mΩ (Typ.) (V_{GS} = 10V)
- Low leakage current: I_{DSS} = 10μA (Max.) (V_{DS} = 40V)
- Enhancement mode: V_{th} = 1.4 to 2.4V (V_{DS} = 10V, I_D = 0.5mA)

Packaging and Internal Circuit

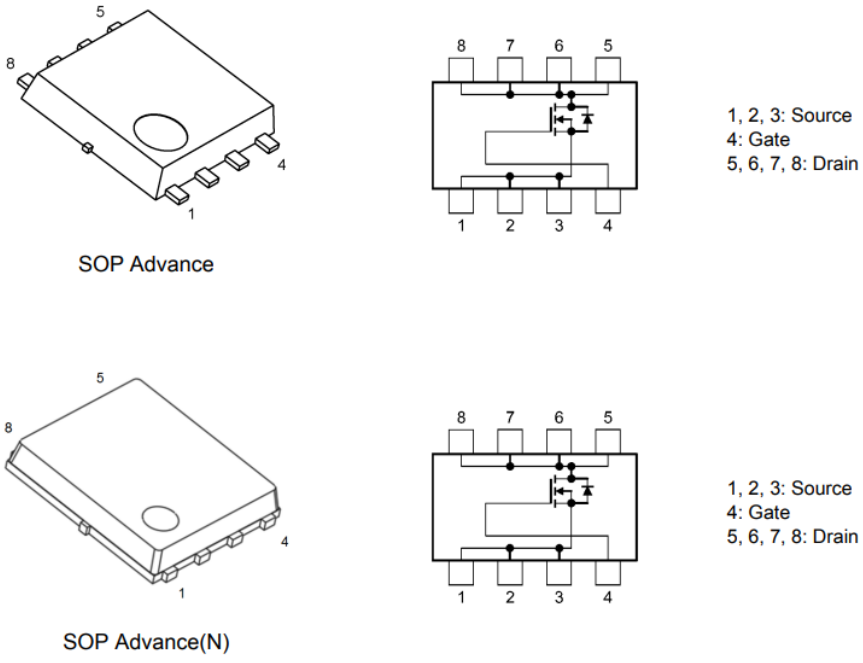

Fig. 2.4 Packaging and Internal Circuit of TPH1R204PL

2.5. Power MOSFET TPH1R306PL

The 60V-rated N-channel MOSFET TPH1R306PL is used as the secondary-side switching element (forward side) in the ITTF topology DC-DC converter circuit. The main features of TPH1R306PL are as follows:

- High-speed switching
- Small gate charge: Q_{SW} = 22nC (Typ.)
- Small output charge: Q_{oss} = 77.5nC (Typ.)
- Low drain-source on-resistance: $R_{DS(ON)}$ = 1.0mΩ (Typ.) (V_{GS} = 10V)
- Low leakage current: I_{DSS} = 10μA (Max.) (V_{DS} = 60V)
- Enhancement mode: V_{th} = 1.5 to 2.5V (V_{DS} = 10V, I_D = 1.0mA)

Packaging and Internal Circuit

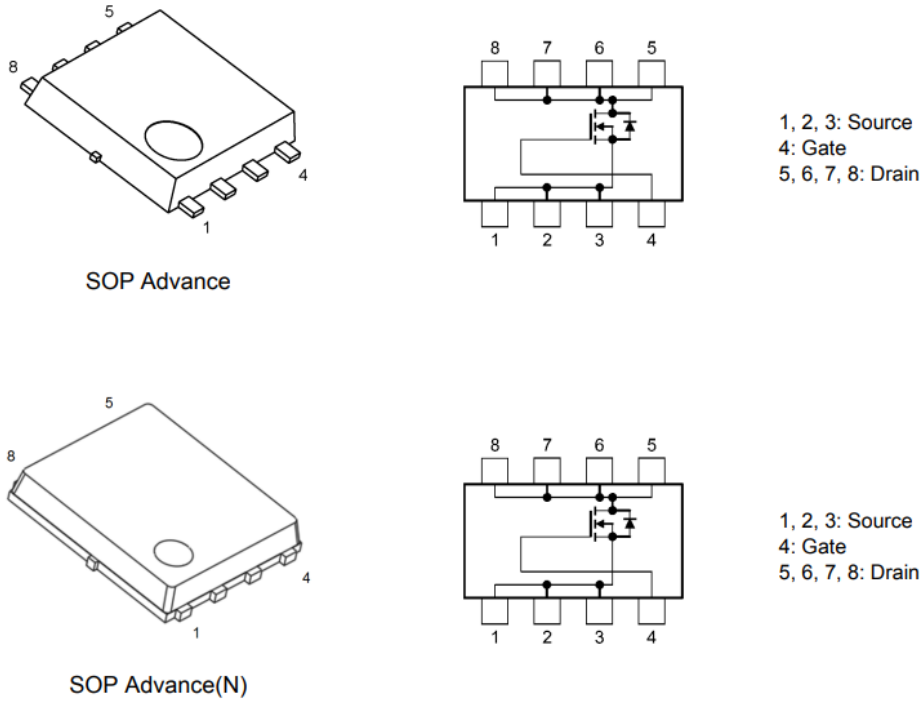

Fig. 2.5 Packaging and Internal Circuit of TPH1R306PL

2.6. Power MOSFET TPHR6503PL

The 30V-rated N-channel MOSFET TPHR6503PL is used as the switching element in the output ORing circuit of the ITTF topology DC-DC converter. The main features of TPHR6503PL are as follows:

- High-speed switching
- Small gate charge: Q_{SW} = 30nC (Typ.)
- Small output charge: Q_{oss} = 81.3nC (Typ.)
- Low drain-source on-resistance: $R_{DS(ON)}$ = 0.41mΩ (Typ.) (V_{GS} = 10V)
- Low leakage current: I_{DSS} = 10μA (Max.) (V_{DS} = 30V)
- Enhancement mode: V_{th} = 1.1 to 2.1V (V_{DS} = 10V, I_D = 1.0mA)

Packaging and Internal Circuit

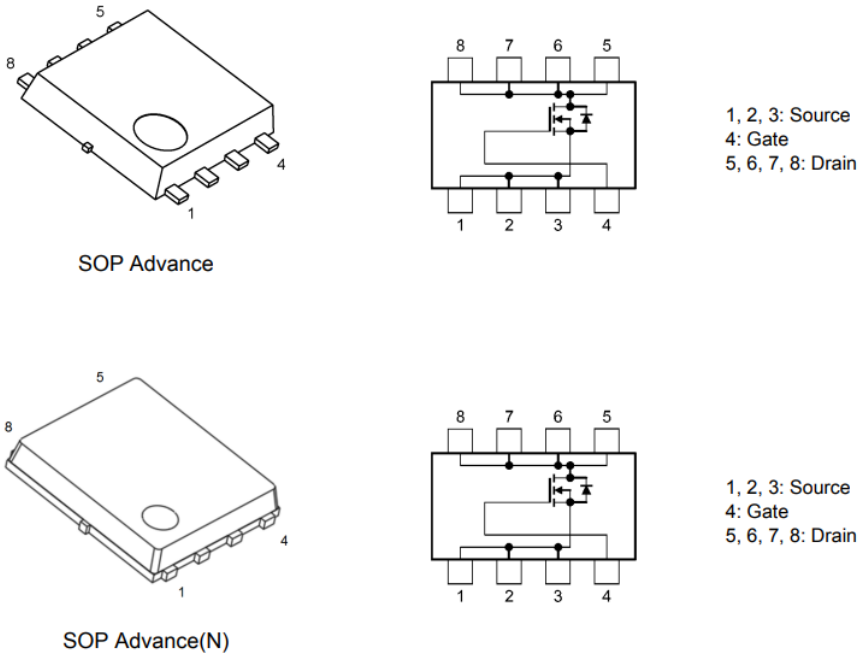

Fig. 2.6 Packaging and Internal Circuit of TPHR6503PL

2.7. Digital Isolator DCL541A01

The digital isolator DCL541A01 is used for gate drive signal transmission from the primary-side controller to the secondary-side. The main features of DCL541A01 are as follows:

- High-speed data transmission: up to 150Mbps
- CMTI(Min): ±100kV/μs
- Isolation voltage: 5kVrms
- Safety standards:
  - UL: UL1577, File No. E519997
  - cUL: CSA Component Acceptance Service Notice No. 5A, File No. E519997
  - VDE: DIN VDE V 0884-11 (VDE V 0884-11) Certificate No. 40055132
  - CQC: GB 4943.1-2022 Certificate No. CQC22001345018

Terminal Layout

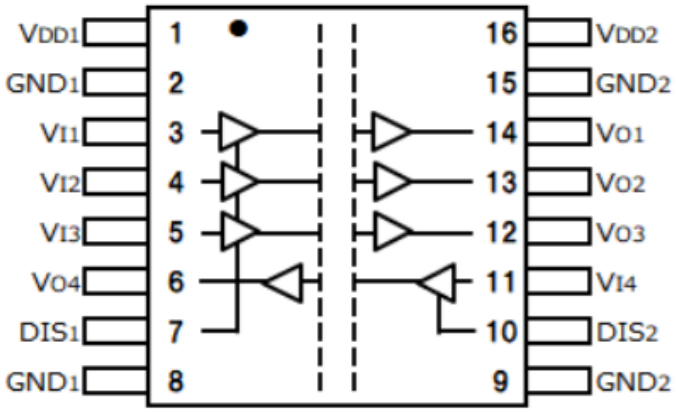

Fig. 2.7 Terminal Layout of DCL541A01

3. Totem-Pole PFC Circuit and ITTF DC-DC Converter

This chapter explains the basic concepts of the Totem-Pole PFC circuit and the ITTF DC-DC converter adopted in this design.

3.1. Totem-Pole PFC Circuit

Figure 3.1 shows the basic configuration of the PFC circuit. Q_c and Q_d alternately turn on and off according to the half-wave of the AC input voltage, while Q_a and Q_b perform PWM control through high-speed switching to generate an input current synchronized with the phase of the AC input voltage.

The PFC circuit rectifies and boosts the AC input to obtain a DC output voltage. Conceptually, it performs boost chopper operation for both the upper and lower half-waves of the AC input. The following sections describe each operation mode in detail.

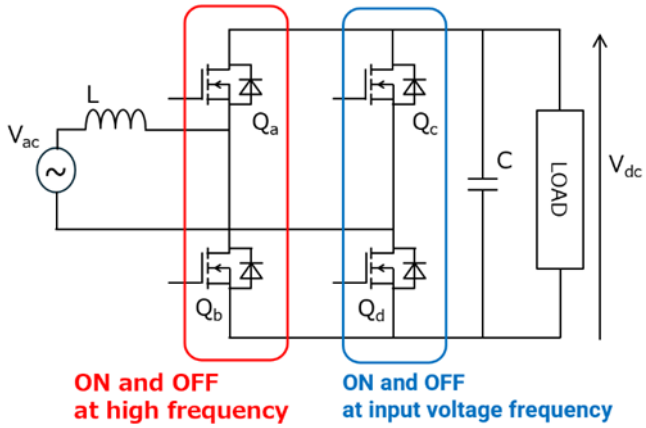

Fig. 3.1 Totem-pole PFC Circuit

As shown in Figure 3.2, the operation of the Totem-Pole PFC is classified into four modes (Modes 1 to 4):

During the upper half-wave of the AC input, Q_c is always off and Q_d is always on, while Q_a and Q_b alternately switch on and off (Mode 1 and 2). During the lower half-wave, Q_c is always on and Q_d is always off, and similarly, Q_a and Q_b alternate switching (Mode 3 and 4).

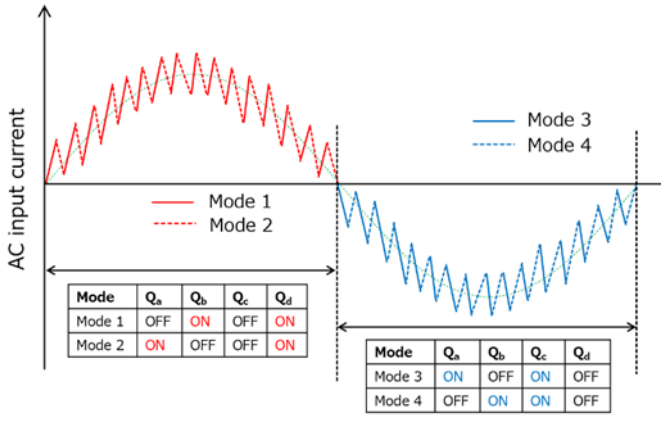

Fig. 3.2 Totem-pole PFC Current Waveforms

【Mode 1】

This mode operates when the positive half-wave of the power supply voltage is applied.Q_b and Q_d are on, while Q_a and Q_c are off. The current path is shown in Figure 3.3.The inductor is charged with the supply voltage V_{ac}, and the inductor current I_L increases with a slope of V_{ac}/L_{as} shown in the equation below. Refer to the current waveform in Figure 3.2.

$$I_L = \frac{V_{ac}}{L} \times t$$

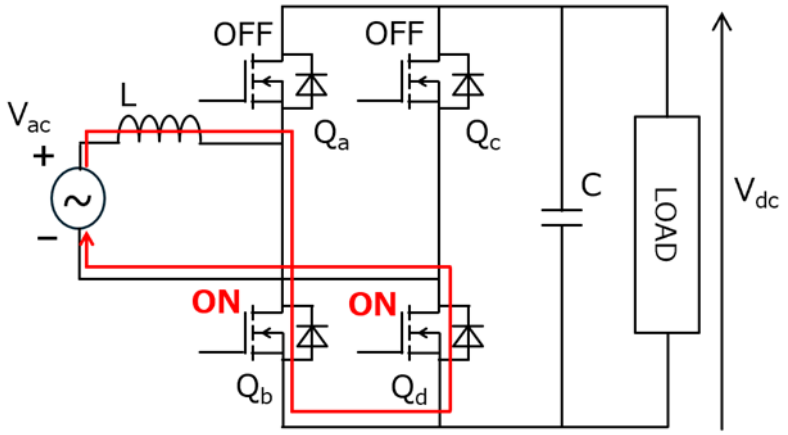

Fig. 3.3 Mode1 Circuit Operation

【Mode 2】

This mode continues during the positive half-wave of the AC input voltage.

Q_a and Q_d are on, while Q_b and Q_c are off. The current path is shown in Figure 3.4.The inductor is applied with a voltage of ($V_{ac} - V_{dc}$). If $V_{dc} > V_{ac}$, the applied voltage becomes negative, but the inductor cannot change the current direction abruptly, so the current decreases with a slope of ($V_{ac} - V_{dc}$)/L and flows to the output side.

$$I_L = \frac{(V_{ac} - V_{dc})}{L} \times t$$

During the positive half-wave of the power supply voltage, Modes 1 and 2 are repeated rapidly. Refer to the current waveform in Figure 3.2.

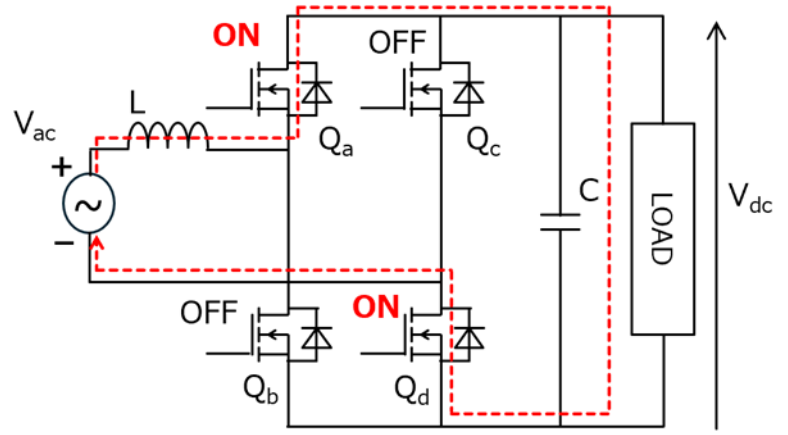

Fig. 3.4 Mode2 Circuit Operation

【Mode 3】

This is the Mode1 operation during the negative half-wave of the AC input voltage. Q_a and Q_c are on, while Q_b and Q_d are off. The current path is shown in Figure 3.5.

The supply voltage V_{ac} is applied to the inductor in the reverse direction, and energy is stored in the reverse direction. Refer to the current waveform in Figure 3.2.

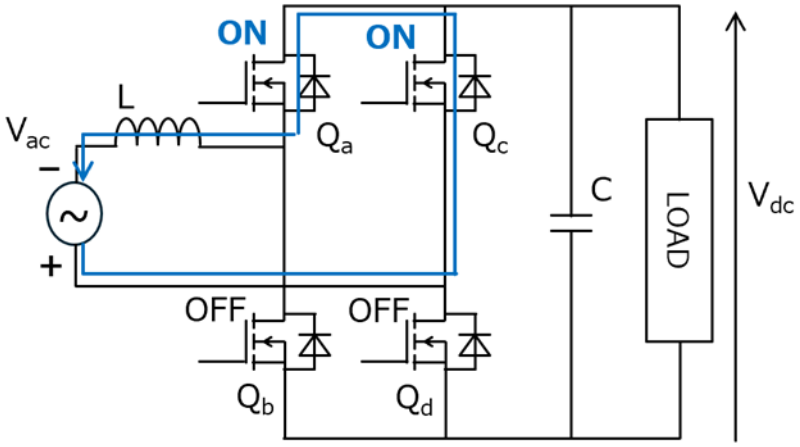

Fig. 3.5 Mode3 Circuit Operation

【Mode 4】

Mode 2 operates during the negative half-cycle of the AC input voltage. In this mode, transistors Q_b and Q_c are turned on, while Q_a and Q_d are turned off. The current path follows the configuration shown in Figure 3.6.

An effective voltage of (V_{ac} − V_{dc}) is applied across the inductor through a conduction path that starts from transistor Q_c, passes through the DC link (V_{dc}), and continues to transistor Q_b. Due to the inductor's inherent tendency to maintain current flow, it continues to deliver power to the output side. For details on the current waveform, refer to Figure 3.2.

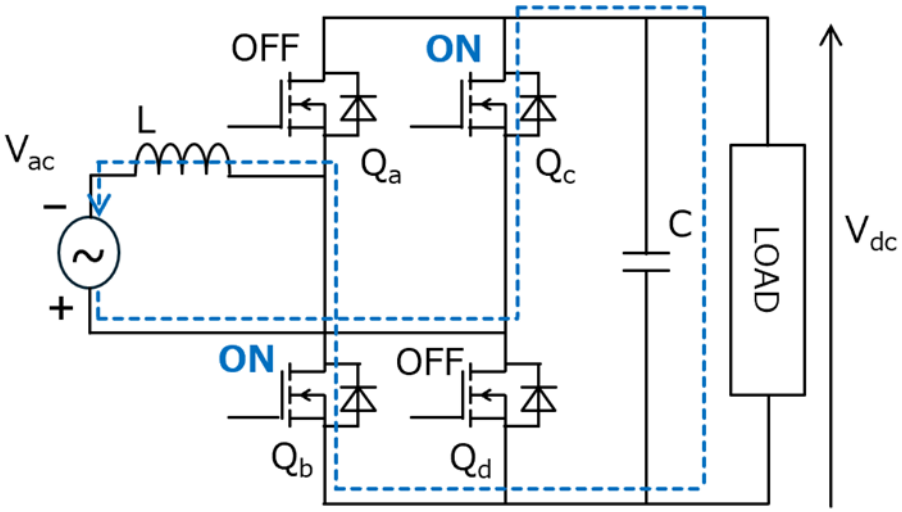

Fig. 3.6 Mode4 Circuit Operation

3.2. ITTF DC-DC Converter

3.2.1. TTF (Two Transistor Forward) DC-DC Converter

Figure 3.7 shows the circuit configuration of the TTF converter.

This circuit adopts synchronous rectification on the secondary side. The two transistors (MOSFETs) on the primary-side turn on and off simultaneously, and power is supplied to the output capacitor and load via the transformer.

In a single-transistor forward converter, a large surge voltage tends to occur due to the leakage inductance of the transformer. In contrast, the TTF topology clamps the surge voltage caused by leakage inductance to the supply voltage via diodes, allowing the stored energy to be efficiently recovered to the power source.

Thanks to this characteristic, the TTF topology is suitable for constructing high-capacity DC-DC converters in the several-kilowatt class, compared to single-transistor configurations.

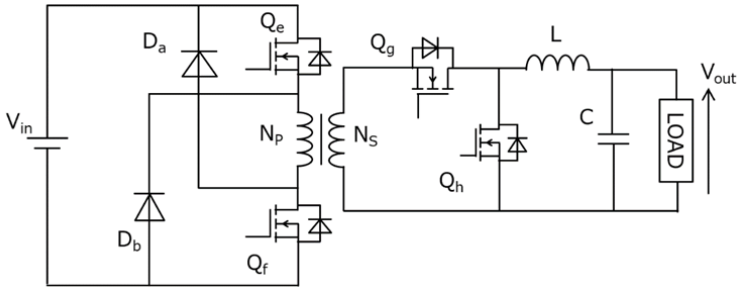

Fig. 3.7 TTF Circuit

【Mode 1】

Q_e and Q_f are on, and the input voltage V_{in} is applied to the N_P winding, transferring power to the secondary side.

The magnetizing current i_m increases by Δi_m during the on-time T_1 (= T_{on}) of Q_e and Q_f.

Assuming the magnetizing inductance is L_m, the increase in magnetizing current Δi_m is expressed as:

$$\Delta i_m = \frac{1}{L_m} \times V_{in} \times T_{on}$$

The secondary winding N_S induces a voltage of $V_{in} \times N_S/N_P$, and the parasitic diode D_g of Q_g conducts, supplying power to the secondary side.

The change in current Δi_L of the smoothing inductor L is expressed as:

$$\Delta i_L = \frac{1}{L} \times V_L \times T_{on} = \frac{1}{L} \times \left(V_{in} \times \frac{N_S}{N_P} - V_{out} \right) \times T_{on}$$

The current flowing through Q_e, Q_f, and N_P on the primary-side (i_{Qe}, i_{Qf}, i_{NP}) is the sum of the magnetizing current and the load current:

$$i_{Q1} = i_{Q2} = i_{NP} = \frac{N_S}{N_P} \times i_L + i_m$$

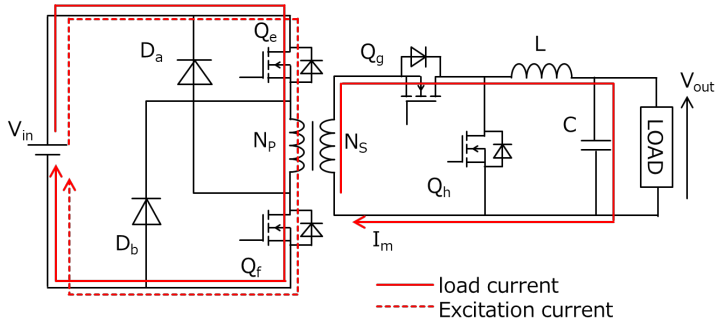

Fig. 3.8 Mode 1

【Mode 2】

Q_e and Q_f turn off. As the magnetizing current continues to flow, D_a and D_b conduct and return energy to the power source, as shown in Figure 3.9. The input voltage V_{in} is applied in reverse to the N_P winding, causing the magnetizing current to decrease and eventually reach 0A at time T_2.The decrease in magnetizing current Δi_m is expressed as:

$$\Delta i_m = \frac{1}{L_m} \times V_{NP} \times T_2 = \frac{1}{L_m} \times (-V_{in}) \times T_2$$

The current of the secondary-side smoothing inductor L circulates through the parasitic diode D_h of Q_h. Since V_{out} is applied in reverse to L, the change in i_L is as follows.

$$\Delta i_L = \frac{1}{L} \times V_L \times T_2 = \frac{1}{L} \times (-V_{out}) \times T_2$$

Also, the following equations hold:

$$i_{Da} = i_{Db} = i_{NP} = i_m$$
$$i_{Dh} = i_L$$

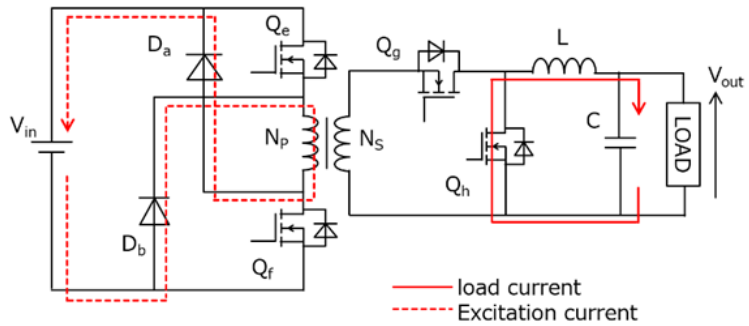

Fig. 3.9 Mode2 Circuit Operation

【Mode 3】

While the magnetizing current flows in Mode2, V_{in} is applied across the drain-source of Q_e and Q_f, charging their parasitic capacitances. In Mode3, the voltage ($2V_{in}$) of the charged parasitic capacitance is connected in series with the N_P winding in the reverse direction. As a result, $-V_{in}$ is applied to the N_P winding, and the magnetizing current flows in the negative direction and gradually increases, as shown in Figure 3.10. When the parasitic capacitance voltage of Q_e and Q_f discharges to V_{in} /2, the voltage applied to the N_P winding becomes positive.

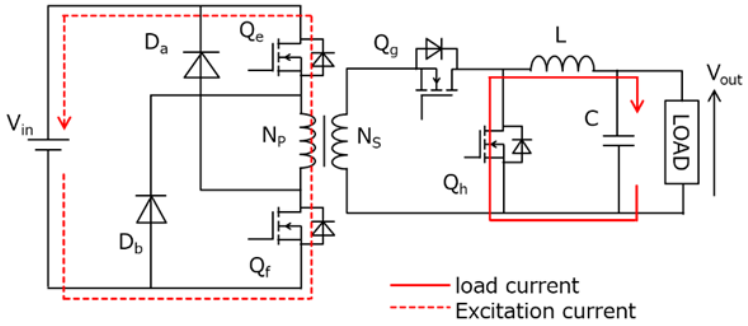

Fig. 3.10 Mode3 Circuit Operation

【Mode 4】

When the voltage applied to the N_P winding becomes positive, the synchronous rectifier Q_g on the secondary-side is forward-biased and conducts, transferring the magnetizing current to the N_S winding. Since the discharge of the parasitic capacitance of Q_e and Q_f is completed in Mode3, their voltages remain constant in Mode4.As both Q_g and Q_h conduct, $V_{NS} = V_{NP} = 0$, and the magnetizing current remains unchanged. If the magnetizing current flowing through the N_S winding is i_m and the magnetizing current at the end of Mode3 is $i_m(T_3)$, then:

$$I_{m4} = i_m(T_3) \times \frac{N_P}{N_S}$$

Afterward, Q_e and Q_f turn on again, transitioning back to Mode1.

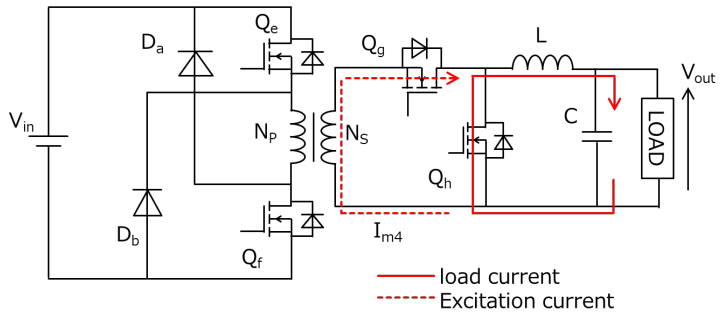

Fig. 3.11 Mode4 Circuit Operation

Since the magnetizing current i_m is smaller than the load current i_L, i_m is magnified in the waveform shown in Figure 3.12.

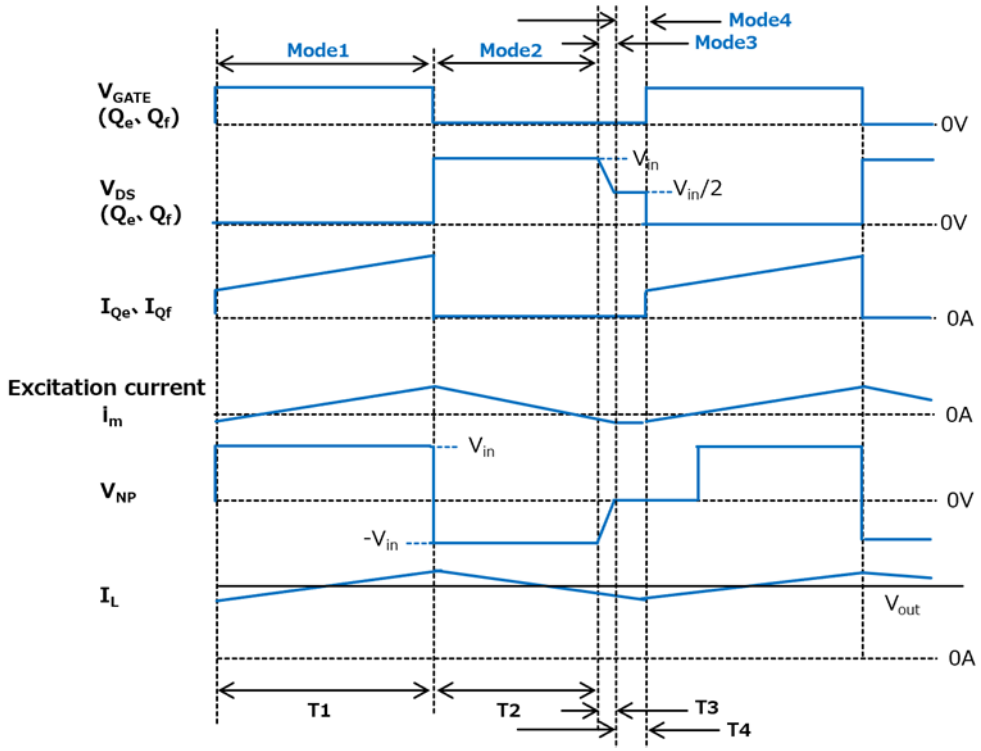

Fig. 3.12 TTF Current Waveforms

3.2.2. ITTF Circuit

An interleaved circuit is a configuration in which two or more circuits share certain components, such as smoothing capacitors, and operate synchronously with phase shifts.

Figure 3.13 shows the ITTF circuit. The two circuits (Circuit 1 and Circuit 2) are driven with a 180° phase shift. As a result, the output waveforms of each circuit overlap, reducing ripple current and effectively doubling the operating frequency. Switching losses are distributed, reducing the load on each switching device and simplifying thermal design. Additionally, the reduced ripple current and increased effective frequency allow for downsizing of the smoothing capacitors.

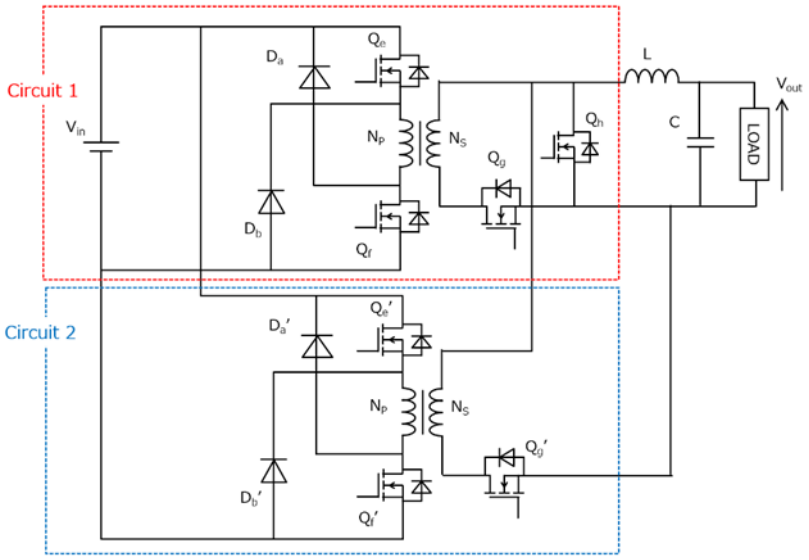

Fig. 3.13 ITTF Circuit

Figure 3.14 illustrates the turn-on timing of the switching devices and the output current waveform in the ITTF circuit. I_{L1} represents the output current from Circuit 1 in Figure 3.13, and I_{L2} represents the output current from Circuit 2. The total output current of the interleaved circuit is $I_{L1} + I_{L2}$, shown as I_L in Figure 3.14.

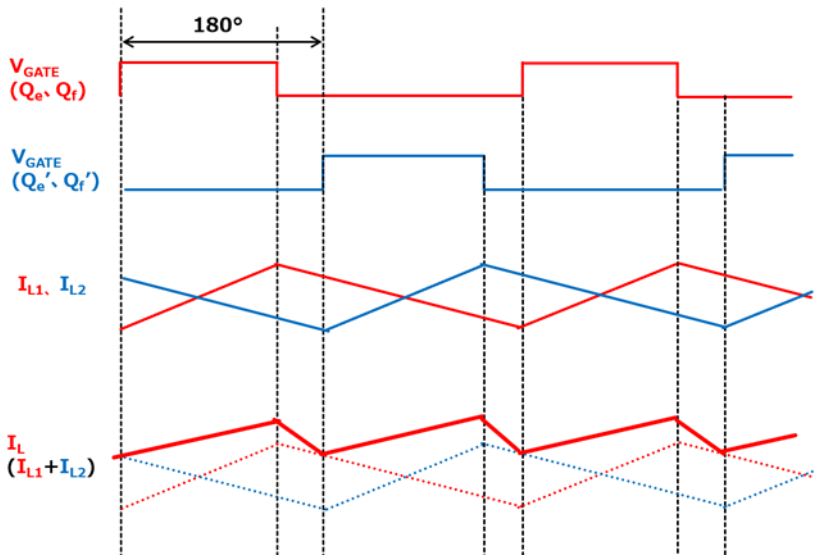

Fig. 3.14 ITTF Current Waveforms

3.3. ORing Circuit

Figure 3.15 shows the configuration of the ORing circuit.

The ORing circuit enables continuous system operation by connecting multiple power supplies in parallel, so that if one power unit fails, the others continue to supply power. It is used to increase output capacity and ensure redundancy.

When combining outputs from multiple power supply units into a single bus, it is necessary to prevent a failed unit from affecting the others. Therefore, power MOSFETs are used at the output of each power supply unit to prevent reverse current and ensure electrical isolation between units.

Although MOSFETs function as switches, in systems such as servers that require continuous operation, they are rarely turned off and operate almost always in the on-state, functioning as simple conductors during normal operation. Therefore, MOSFETs used in ORing circuits must have low conduction losses. Selecting MOSFETs with low on-resistance and fast switching capability improves system efficiency and reliability.

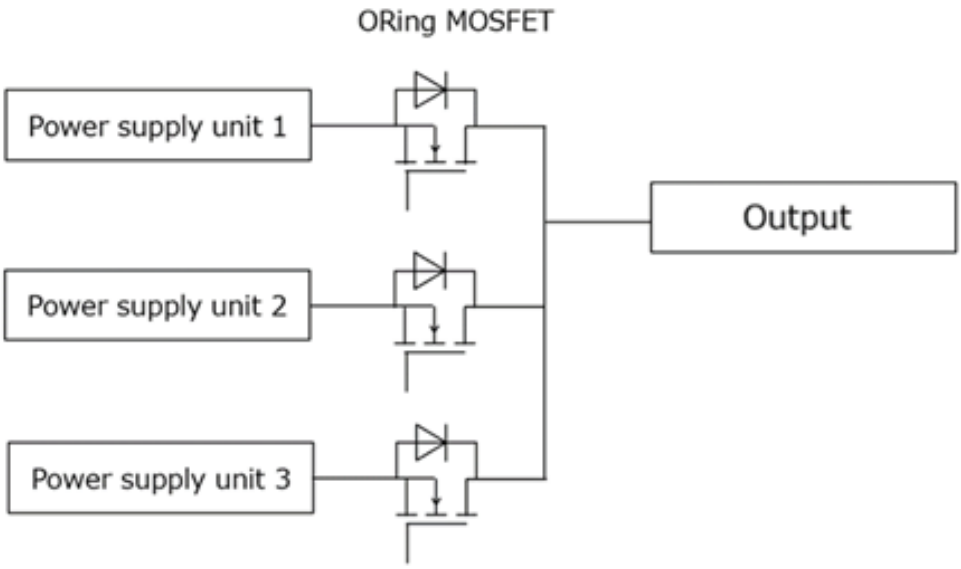

Fig. 3.15 ORing Circuit

4. 1.1kW ITTF AC-DC Converter for Servers

This chapter describes the configuration and circuit design overview of this design.Figure 4.1 shows the block diagram of the circuit.

The Totem-pole PFC and ITTF circuits are controlled by an MCU located on the primary-side. Each MOSFET on the secondary-side of the ITTF is driven via a digital isolator (DCL541A01).

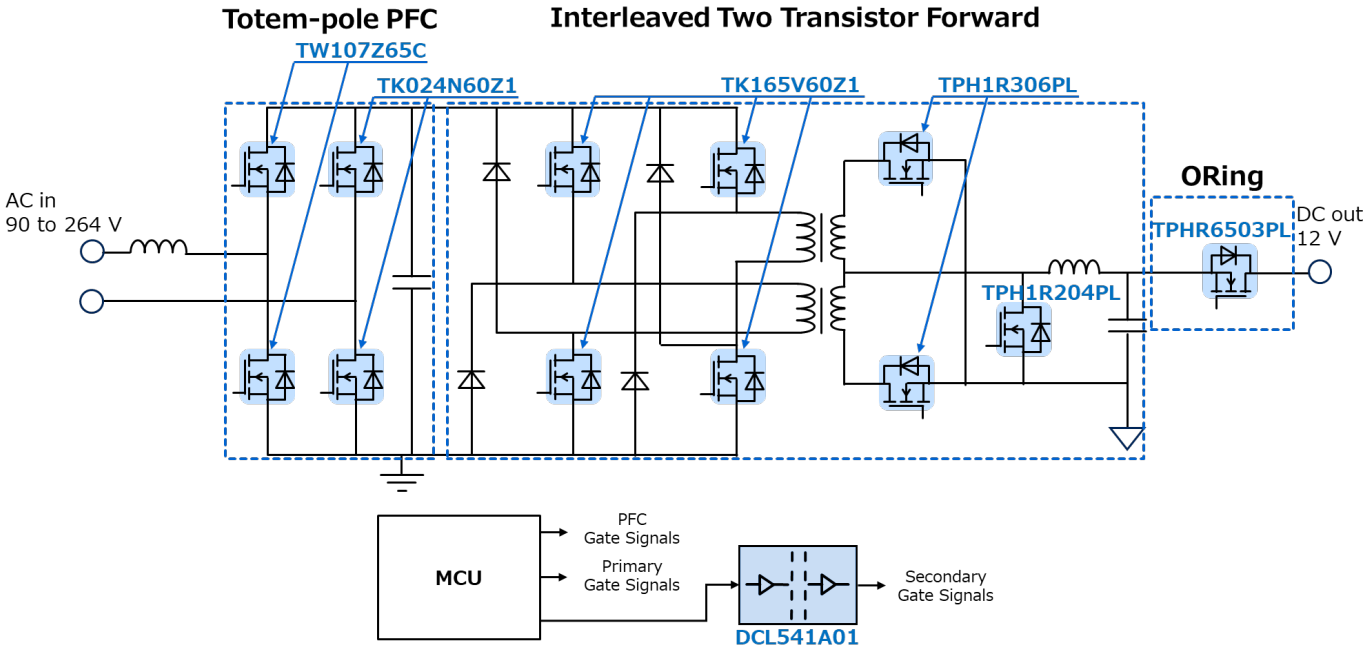

Fig. 4.1 Circuit Block Diagram

4.1. Specifications

Table 4.1 lists the main specifications of this design.

Table. 4.1 Specifications of This Design

Item	Conditions	Min.	Typ.	Max.	Unit
Input characteristics					
AC input voltage (rms)		90		264	V
AC input current (rms)	V_{in} = AC 90V, I_{out} = 92A			14	A
Input frequency		47		63	Hz
Internal characteristics (Interleaved PFC circuit)					
Output voltage			385		V
Maximum output power	V_{in} = AC 230V			1.2	kW
Switching frequency			65		kHz
Output characteristics (ITTF DC-DC Converter circuit)					
Output voltage		11.4	12	12.6	V
Output current				96.5	A
Maximum output power				1.1	kW
Switching frequency			80		kHz
Output ripple voltage	T_a = 25℃			240	mV
Other					
Protective functions	Output overvoltage protection, output overcurrent protection, and output short-circuit protection				
Board layer configuration	Main board: FR-4 4-layer structure, copper foil thickness 105μm Control board： FR-4 4-layer structure, copper foil thickness 35μm				

4.2. Totem-pole PFC Circuit

Figure 4.2 shows the circuit used in this design. TW107Z65C is used for the PWM switching elements (Q3, Q4), and TK024N60Z1 is used for the half-wave switching elements (Q1, Q2) of the input voltage.

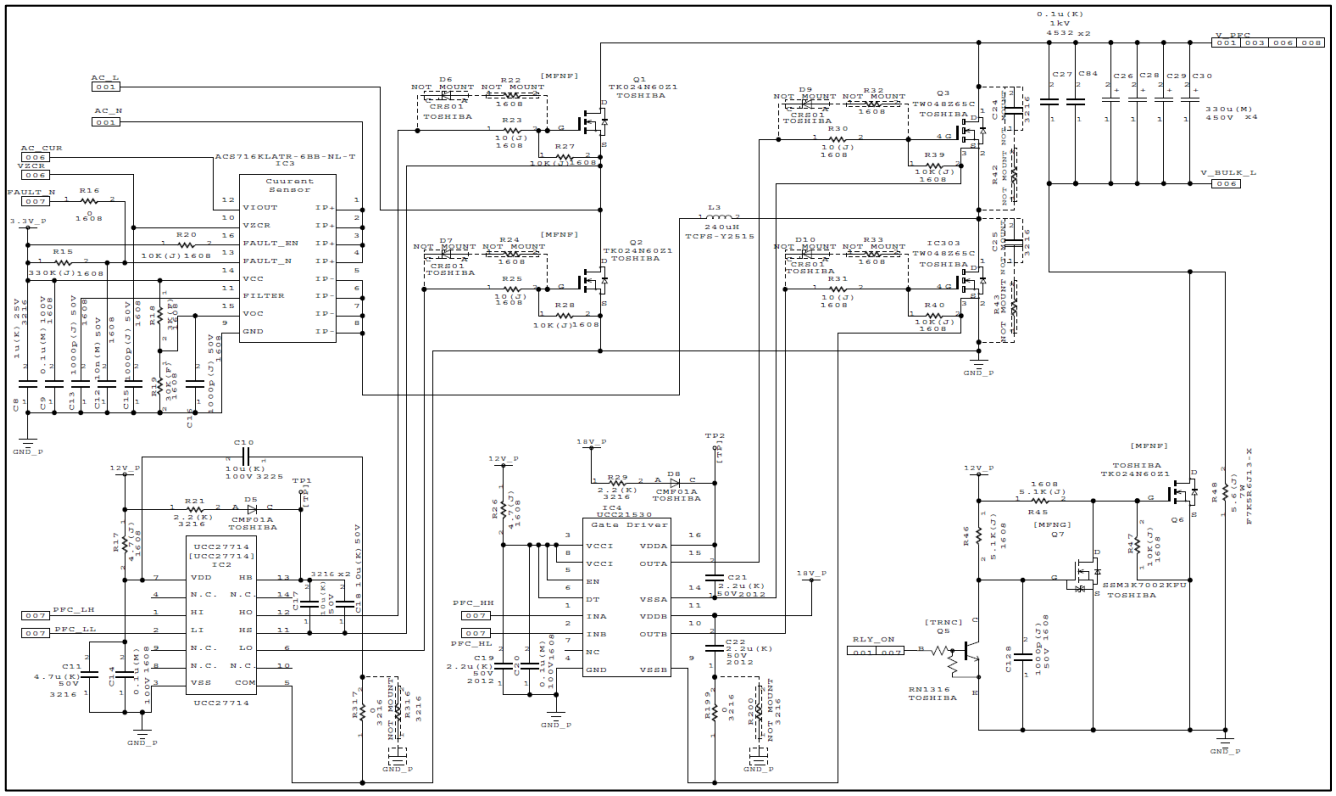

Fig. 4.2 Totem-pole PFC Circuit

4.3. ITTF Circuit

Figure 4.3 shows the primary-side circuit of the ITTF, and Figure 4.4 shows the secondary-side circuit. Figure 4.5 is a simplified diagram of Figure 4.4 for easier understanding of the circuit configuration.

In the primary-side ITTF circuit shown in Figure 4.3, TK165V60Z1 is used as the control MOSFET, and it is controlled via high-side/low-side gate driver ICs based on signals from the MCU. Circuit current is detected using a sense resistor and transmitted to the MCU via a differential amplifier circuit.

In the secondary-side rectifier circuit shown in Figure 4.4, two TPH1R204PL MOSFETs are used in parallel as control devices. Control signals are input to the low-side gate driver IC via a digital isolator (IC11 DCL541A01) from the MCU. Overvoltage detection signals from the forward converter output are also transmitted to the MCU via the digital isolator. Output voltage information from the forward converter is transferred to the primary-side via the isolation amplifier TLP7820 and detected by a differential amplifier circuit.

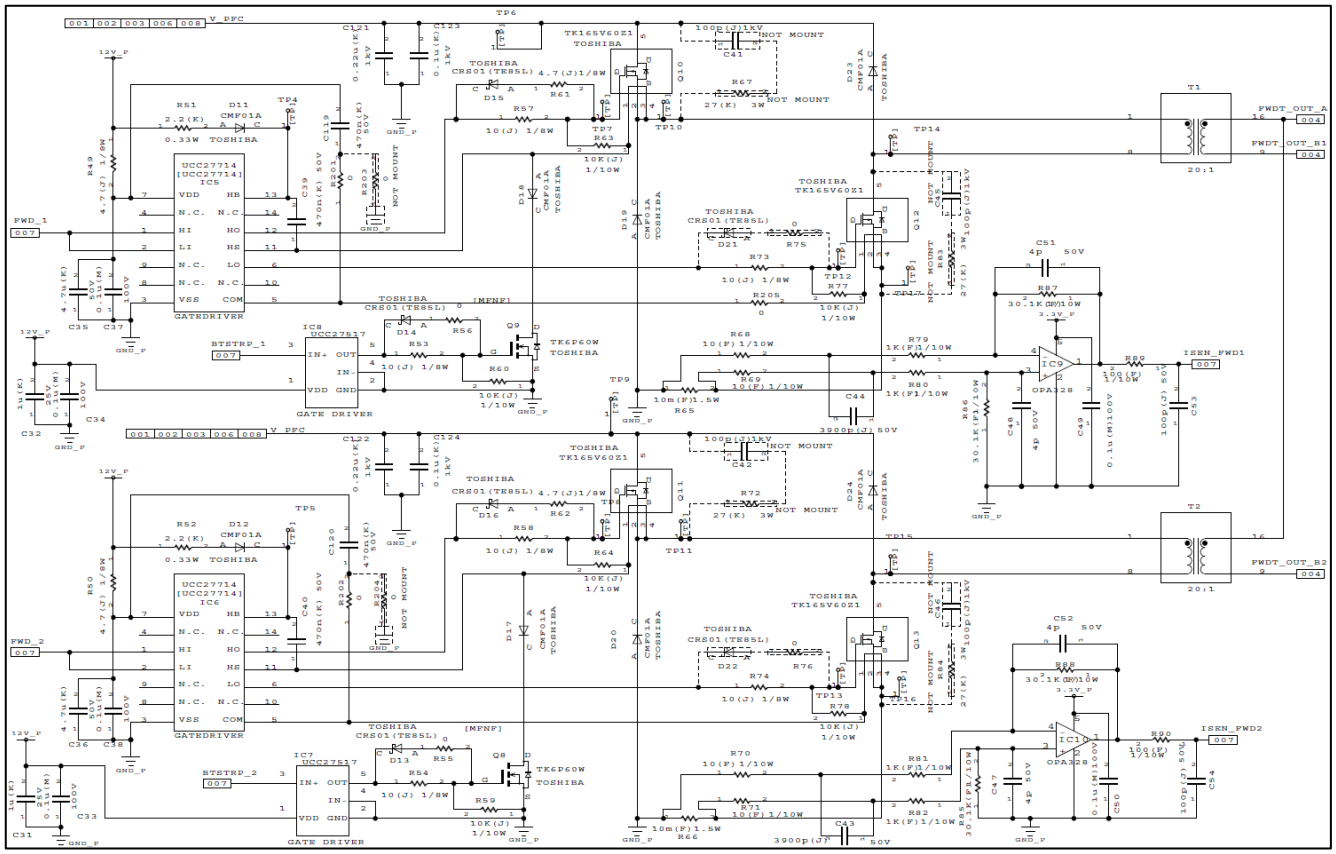

Fig. 4.3 ITTF Circuit (Primary Circuit)

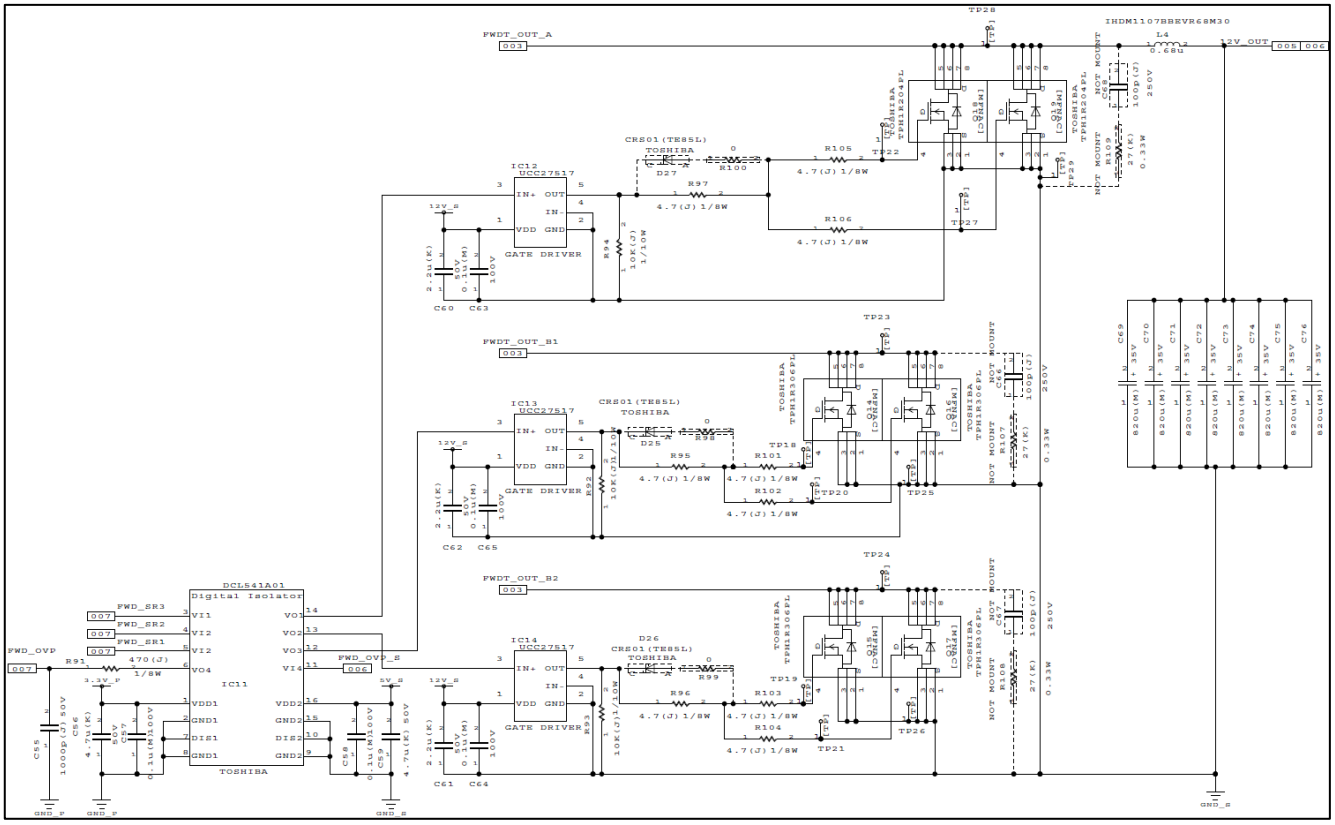

Fig. 4.4 ITTF Circuit (Secondary Circuit)

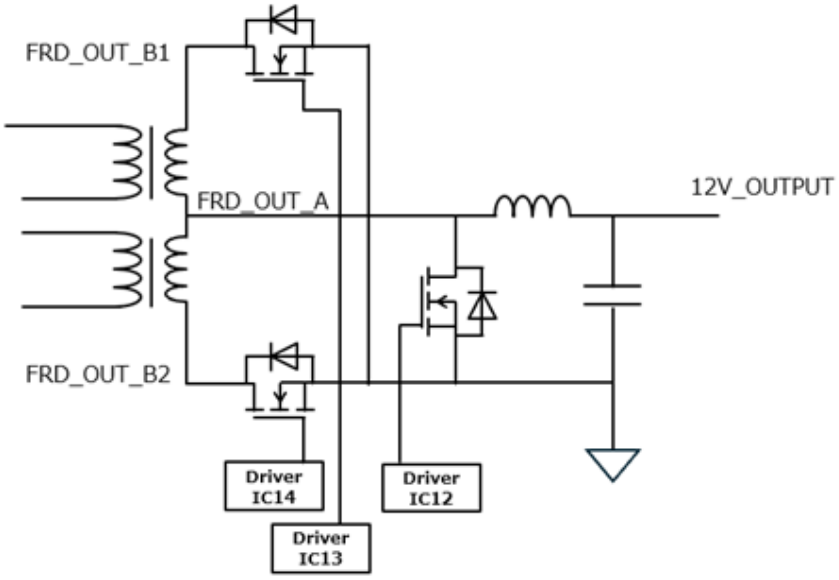

Fig. 4.5 Secondary Circuit Simplified Diagram

4.4. ORing Circuit

Figure 4.6 shows the ORing circuit used in this design. The power supply is not directly connected to the bus, but through the ORing circuit, enabling reverse current prevention during hot-plugging and output isolation during short circuits.

In this design, three TPHR6503PL MOSFETs are connected in parallel on the output line for ORing, and these MOSFETs are controlled by a hot-swap voltage controller IC (IC15 TPS2419D).

The voltage controller IC monitors the source-drain voltage $V_A - V_C$ of the MOSFET and controls the gate accordingly. When $V_A - V_C > 65mV$, the gate is driven high, turning the MOSFET on. If $V_A - V_C$ falls below the turn-off threshold set by the resistor connected to the RSET pin, the gate is pulled low (to GND).The gate drive voltage is referenced to V_A, and the gate is driven high only when $V_A > V_C$.

Additionally, if the bus voltage is higher than the forward converter output voltage, the MOSFET is turned off to prevent reverse current. Furthermore, gate control is enabled when the EN pin of the voltage controller IC is above 1.3V; if EN is low, the gate remains low.

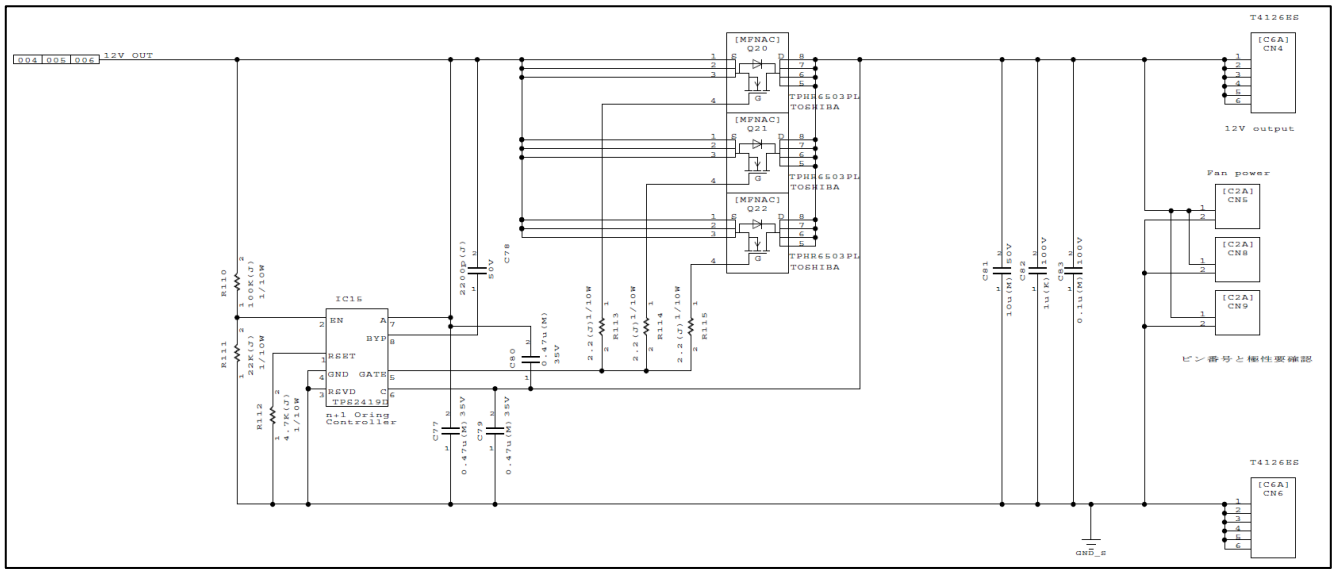

Fig. 4.6 ORing Circuit

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