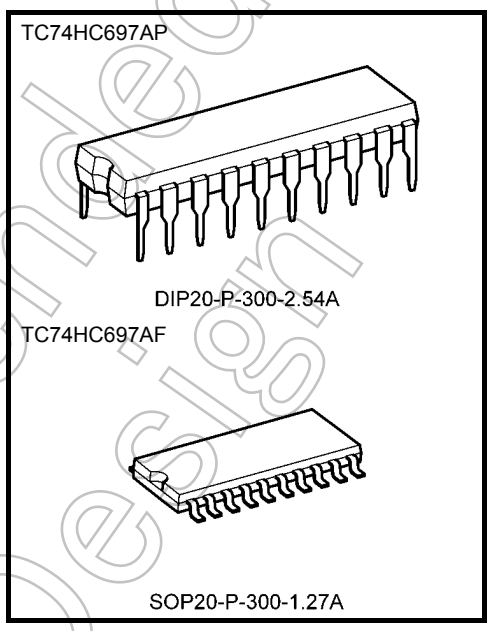
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC697AP, TC74HC697AF

Synchronous Presettable 4-Bit Binary Up/Down Counter with Output Register (multiplexed 3-state outputs)



Weight
DIP20-P-300-2.54A : 1.30 g (typ.)
SOP20-P-300-1.27A : 0.22 g (typ.)

The TC74HC697A is high speed CMOS UP/DOWN COUNTERS fabricated with silicon gate C^2MOS technology.

It achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It counts on the rising edge of the Counter Clock (CCK) input when "counter mode" is selected. If the up/down (U/$\overline{D}$) input is held high, the internal counter counts up. Conversely, if U/$\overline{D}$ is held low, it counts down.

The internal counters outputs are latched into the output registers on the rising edge of the Register Clock (RCK) input.

The outputs (QA~QD) are selected as either internal counter or registered outputs by the output select (R/$\overline{C}$) input. When high, the outputs are counter outputs and when low, they are registered outputs.

Two enable ($\overline{ENP}$, $\overline{ENT}$) inputs and a carry ($\overline{RCO}$) output are provided to enable cascading of the counters.

This facilitates easy implementation of n-bit counters without using external gates.

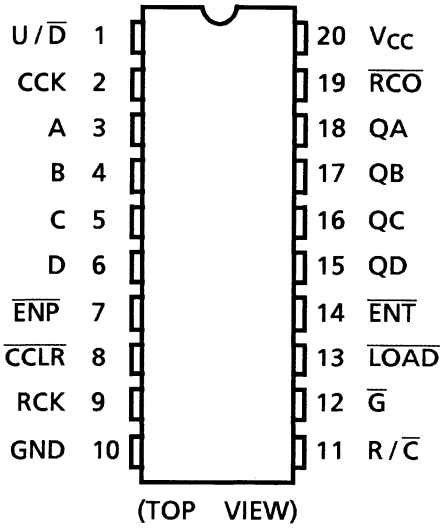
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

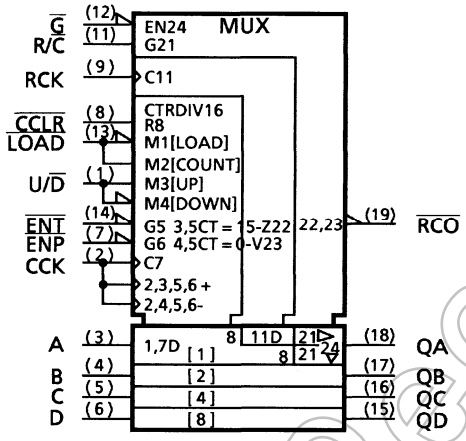
- High speed: f_{max} = 38 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Outputs drive capability: 15 LSTTL loads for QA~QD
  10 LSTTL loads for $\overline{RCO}$
- Symmetrical output impedance:
  $|I_{OH}| = I_{OL}$ = 6 mA (min) for QA~QD
  $|I_{OH}| = I_{OL}$ = 4 mA (min) for $\overline{RCO}$
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V
- Pin and function compatible with 74LS697

Start of commercial production
1988-11

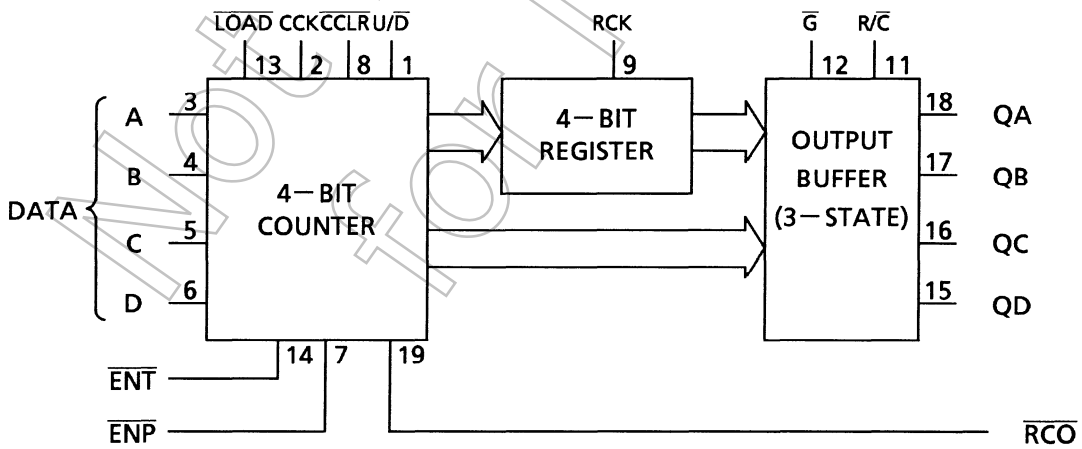
Pin Assignment



IEC Logic symbol



Block Diagram



Truth Table

Inputs									Outputs				Function
$\overline{CCLR}$	$\overline{LOAD}$	$\overline{ENP}$	$\overline{ENT}$	CCK	U/$\overline{D}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	L	L	L	L	L	L	Clear Counter
H	L	X	X	↑	X	X	L	L	a	b	c	d	Load Counter
H	H	H	X	↑	X	X	L	L	No Change				No Count
H	H	X	H	↑	X	X	L	L					
H	H	L	L	↑	H	X	L	L	Count Up				Count
H	H	L	L	↑	L	X	L	L	Count Down				Count
H	X	X	X	↓	X	X	L	L	No Change				No Count
X	X	X	X	X	X	↑	H	L	a'	b'	c'	d'	Load Register
X	X	X	X	X	X	↓	H	L	No Change				No Count

X: Don't care

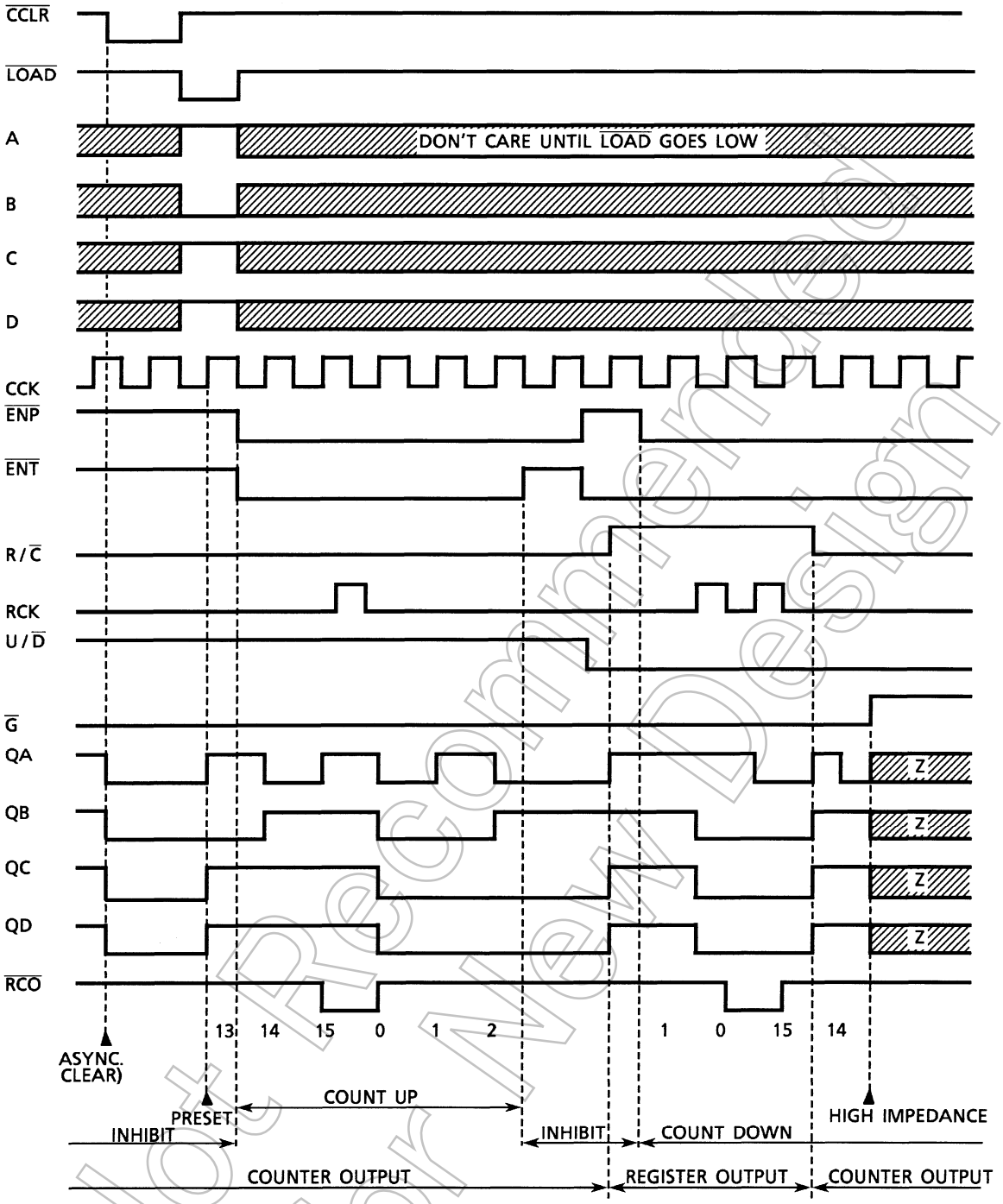
Z: High impedance

a~d: The level of steady state inputs at inputs A through D respectively.

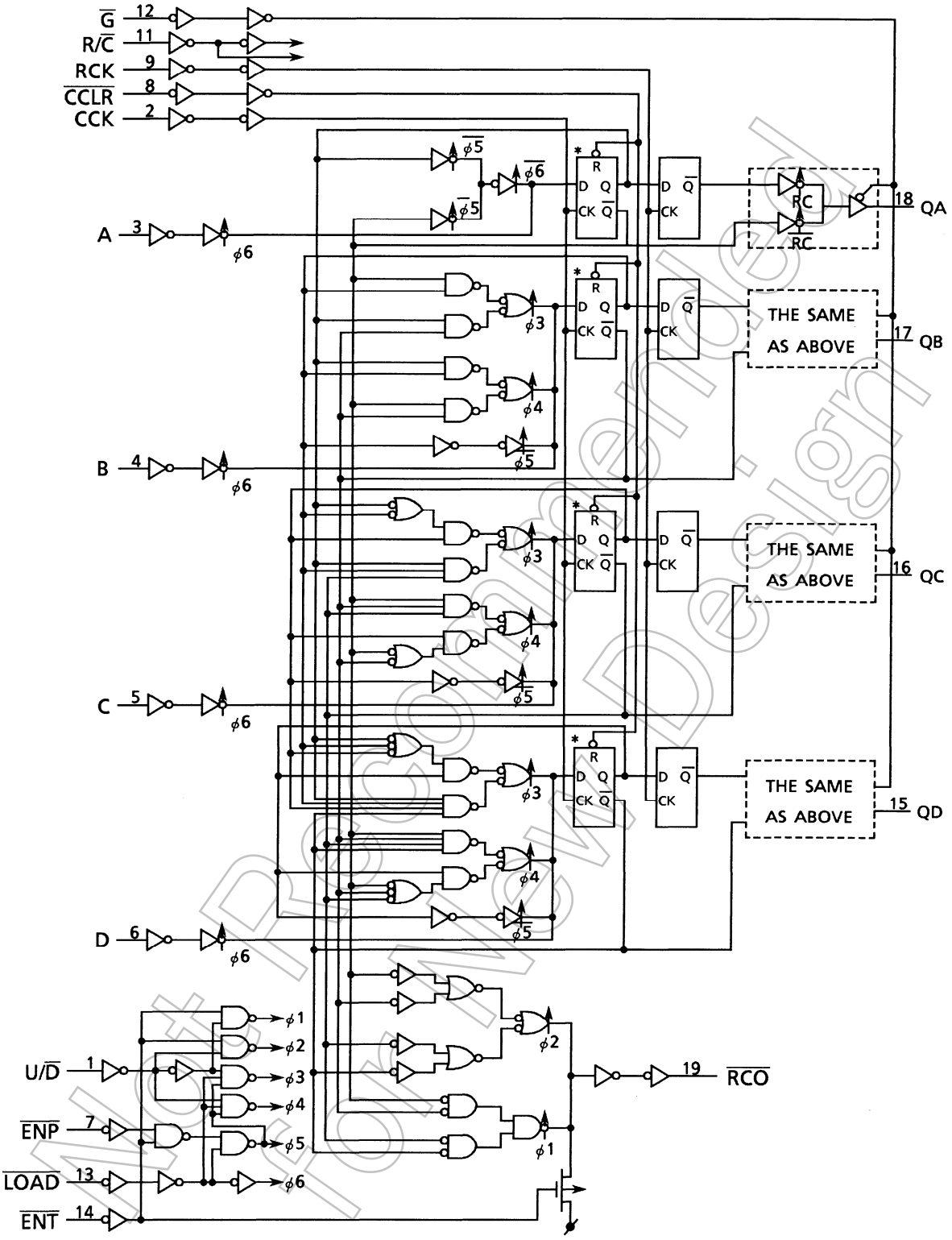
a'~d': The level of steady state outputs at internal counter outputs QA' through QD' respectively.

$$\overline{RCO} = (\overline{UP \cdot QA \cdot QB \cdot QC \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QB} \cdot \overline{QC} \cdot \overline{QD} \cdot ENT})$$

Timing Chart



System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current ($\overline{RCO}$)	I_{OUT}	±25	mA
DC output current (QA~QD)	I_{OUT}	±35	mA
DC V_{CC}/ground current	I_{CC}	±75	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	−65~150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 (V_{CC} = 2.0 V)	ns
		0 to 500 (V_{CC} = 4.5 V)	
		0 to 400 (V_{CC} = 6.0 V)	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition			V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—			2.0	1.50	—	—	1.50	—	V
					4.5	3.15	—	—	3.15	—	
					6.0	4.20	—	—	4.20	—	
Low-level input voltage	V_{IL}	—			2.0	—	—	0.50	—	0.50	V
					4.5	—	—	1.35	—	1.35	
					6.0	—	—	1.80	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}		I_{OH} = −20 μA	2.0	1.9	2.0	—	1.9	—	V
					4.5	4.4	4.5	—	4.4	—	
					6.0	5.9	6.0	—	5.9	—	
			$\overline{RCO}$	I_{OH} = −4 mA	4.5	4.18	4.31	—	4.13	—	
				I_{OH} = −5.2 mA	6.0	5.68	5.80	—	5.63	—	
			QA~QD	I_{OH} = −6 mA	4.5	4.18	4.31	—	4.13	—	
				I_{OH} = −7.8 mA	6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}		I_{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
					4.5	—	0.0	0.1	—	0.1	
					6.0	—	0.0	0.1	—	0.1	
			$\overline{RCO}$	I_{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
				I_{OL} = 5.2 mA	6.0	—	0.18	0.26	—	0.33	
			QA~QD	I_{OL} = 6 mA	4.5	—	0.17	0.26	—	0.33	
				I_{OL} = 7.8 mA	6.0	—	0.18	0.26	—	0.33	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND			6.0	—	—	±0.5	—	±5.0	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND			6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND			6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = −40 to 85°C	Unit
			V_{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (CCK, $\overline{RCK}$)	$t_{W(L)}$ $t_{W(H)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ($\overline{CCLR}$)	$t_{W(L)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time ($\overline{LOAD}$, $\overline{ENT}$, $\overline{ENP}$)	t_s	—	2.0	—	150	190	ns
			4.5	—	30	38	
			6.0	—	13	32	
Minimum set-up time (A, B, C, D)	t_s	—	2.0	—	50	65	ns
			4.5	—	10	13	
			6.0	—	9	11	
Minimum set-up time ($U/\overline{D}$)	t_s	—	2.0	—	100	125	ns
			4.5	—	20	25	
			6.0	—	17	21	
Minimum set-up time (CCK-RCK)	t_s	—	2.0	—	100	125	ns
			4.5	—	20	25	
			6.0	—	17	21	
Minimum hold time (A, B, C, D)	t_h	—	2.0	—	5	5	ns
			4.5	—	5	5	
			6.0	—	5	5	
Minimum hold time	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time	t_{rem}	—	2.0	—	5	5	ns
			4.5	—	5	5	
			6.0	—	5	5	
Clock frequency	f	—	2.0	—	5	4	MHz
			4.5	—	25	20	
			6.0	—	29	24	

AC Characteristics ($C_L = 15$ pF, $V_{CC} = 5$ V, Ta = 25°C, input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time ($\overline{RCO}$)	t_{TLH} t_{THL}	—	—	4	8	ns
Propagation delay time (CCK-$\overline{RCO}$)	t_{pLH} t_{pHL}	—	—	24	41	ns
Propagation delay time (ENT-$\overline{RCO}$)	t_{pLH} t_{pHL}	—	—	13	23	ns
Propagation delay time ($\overline{CCLR}$ - $\overline{RCO}$)	t_{pLH}	—	—	23	38	ns
Maximum clock frequency	f_{max}	—	25	38	—	MHz

AC Characteristics (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			CL (pF)	V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time (Qn)	t_{TLH} t_{THL}	—	50	2.0	—	25	60	—	75	ns
				4.5	—	7	12	—	15	
				6.0	—	6	10	—	13	
Output transition time ($\overline{RCO}$)	t_{pLH} t_{pHL}	—	50	2.0	—	30	75	—	95	ns
				4.5	—	8	15	—	19	
				6.0	—	7	13	—	16	
Propagation delay time (CCK-Q)	t_{pLH} t_{pHL}	—	50	2.0	—	90	195	—	245	ns
				4.5	—	26	39	—	49	
				6.0	—	19	33	—	42	
			150	2.0	—	103	235	—	295	
				4.5	—	31	47	—	59	
				6.0	—	23	40	—	50	
Propagation delay time (RCK-Q)	t_{pLH} t_{pHL}	—	50	2.0	—	82	180	—	225	ns
				4.5	—	24	36	—	45	
				6.0	—	18	31	—	38	
			150	2.0	—	95	220	—	275	
				4.5	—	29	44	—	55	
				6.0	—	22	37	—	47	
Propagation delay time (R/$\overline{C}$-Q)	t_{pLH} t_{pHL}	—	50	2.0	—	60	145	—	180	ns
				4.5	—	19	29	—	36	
				6.0	—	14	25	—	31	
			150	2.0	—	73	185	—	230	
				4.5	—	24	37	—	46	
				6.0	—	18	31	—	39	
Propagation delay time ($\overline{CCLR}$-Q)	t_{pHL}	—	50	2.0	—	89	195	—	245	ns
				4.5	—	26	39	—	49	
				6.0	—	20	33	—	42	
			150	2.0	—	102	235	—	295	
				4.5	—	31	47	—	59	
				6.0	—	24	40	—	50	
Propagation delay time (CCK-$\overline{RCO}$)	t_{pLH} t_{pHL}	—	50	2.0	—	108	235	—	295	ns
				4.5	—	31	47	—	59	
				6.0	—	23	40	—	50	
Propagation delay time ($\overline{ENT}$ - $\overline{RCO}$)	t_{pLH} t_{pHL}	—	50	2.0	—	63	135	—	170	ns
				4.5	—	18	27	—	34	
				6.0	—	14	23	—	29	
Propagation delay time ($\overline{CCLR}$ - $\overline{RCO}$)	t_{pLH}	—	50	2.0	—	98	220	—	275	ns
				4.5	—	29	44	—	55	
				6.0	—	23	37	—	47	

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			CL (pF)	V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output enable time ($\overline{G}$ -Q)	t_{pZL} t_{pZH}	R_L = 1 kΩ	50	2.0	—	45	115	—	145	ns
				4.5	—	15	23	—	29	
				6.0	—	12	20	—	25	
			150	2.0	—	58	155	—	195	
				4.5	—	20	31	—	39	
				6.0	—	16	26	—	33	
Output disable time ($\overline{G}$ -Q)	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	50	2.0	—	32	115	—	145	ns
				4.5	—	17	23	—	29	
				6.0	—	14	20	—	25	
Maximum clock frequency	f_{max}	—	50	2.0	5	11	—	4	—	MHz
				4.5	25	38	—	20	—	
				6.0	29	52	—	24	—	
Input capacitance	C_{IN}	—			—	5	10	—	10	pF
Output capacitance	C_{OUT}	—			—	13	—	—	—	pF
Power dissipation capacitance	C_{PD} (Note)	—			—	72	—	—	—	pF

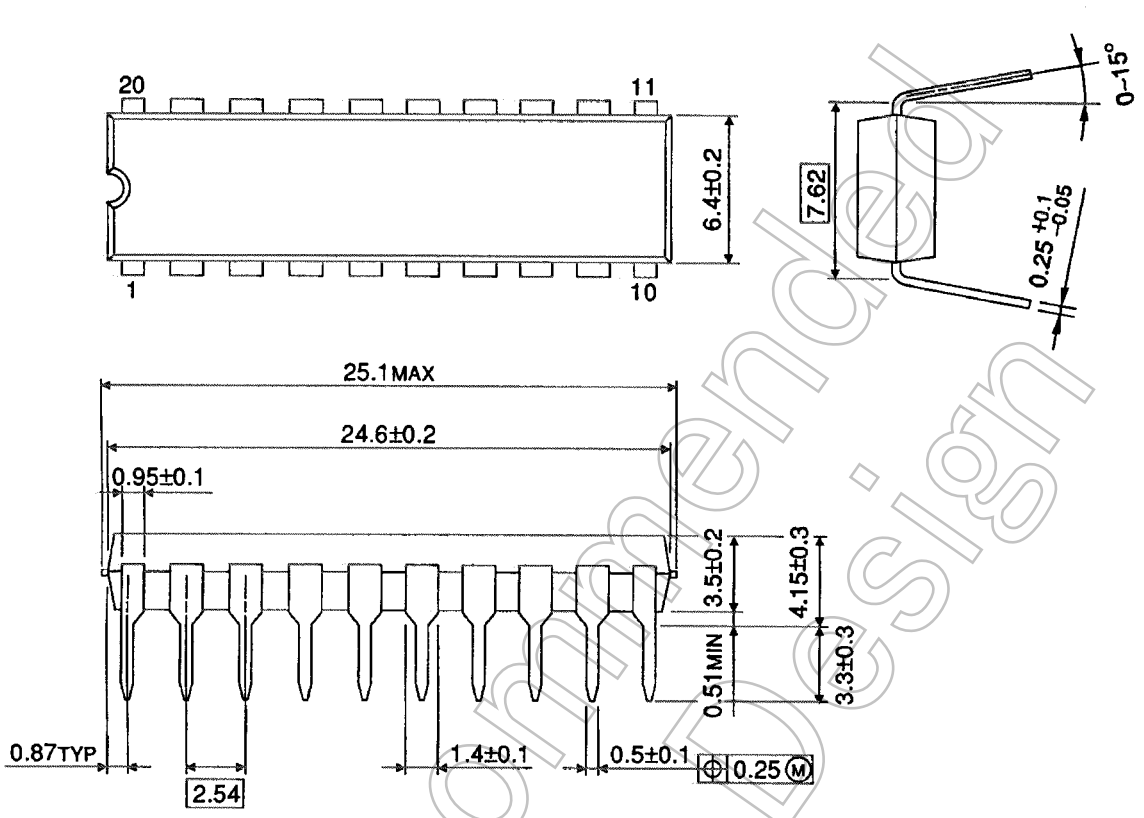
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions

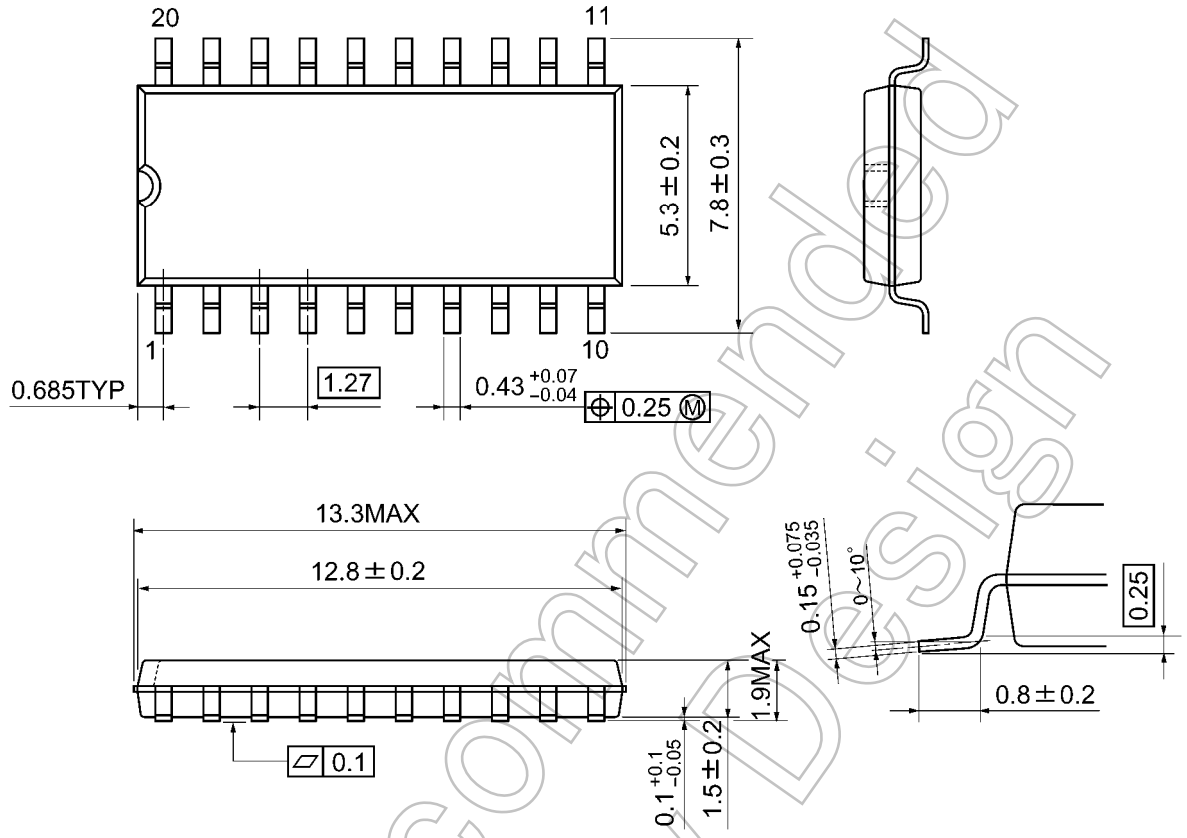
DIP20-P-300-2.54A Unit : mm



Weight: 1.30 g (typ.)

Package Dimensions

SOP20-P-300-1.27A Unit: mm



Weight: 0.22 g (typ.)

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