32-bit RISC Microcontroller
Reference Manual

12-bit Analog to Digital Converter (ADC-G)

Revision 1.4

2025-12

Toshiba Electronic Devices & Storage Corporation

Contents

List of Figures

List of Tables

Preface

Related Document

Document name
Input/Output Ports
Exception
Clock Control and Operation Mode
Product Information
Advanced Programmable Motor Control Circuit
Programmable Motor Control Circuit Plus

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-PMD	Advanced Programmable Motor Control Circuit
PMD+	Programmable Motor Control Circuit Plus
TRGSEL	Trigger Selection Circuit

1. Outlines

The 12-bit analog to digital converter (ADC) can convert multiple analog inputs (AINx00 to AINx24) to digital in each unit. The function list is shown as follows:

Function classification	Function	Operation explanation
AD conversion	Conversion resolution	12 bits
	Conversion time	4.5[V] ≤ AVDD5 ≤ 5.5[V]: 1.5[μs] at SCLK=20[MHz] 1.0[μs] at SCLK=30[MHz] 2.7[V] ≤ AVDD5 < 4.5[V]: 2.05[μs] at SCLK=20[MHz]
	Sampling time	Two types of sampling time can be set, and sampling time can be selected for each AIN channel.
	Store conversion result	24 conversion result storage registers.
Start conversion	Start-up by General Purpose Factor	Start-up factor can select software start-up (continuous conversion, single conversion) and general purpose trigger conversion. There is a conversion program (Note) that can perform AD conversions up to 24 with general purpose factor.
	Start-up by PMD trigger	Each of the twelve PMD triggers can select and execute one of eight PMD trigger programs (Note). Each PMD trigger program can perform up to 4 AD conversions at each conversion program.
Conversion status	Status flags	- Flag showing that the AD conversion is executing. - Flag showing that the program is executing (for each trigger). - Conversion result storage flag (for each conversion result storage register). - Conversion result overrun flag (for each conversion result storage register).
Interrupt	-	- PMD trigger program completion (2 interrupts). - General purpose trigger program completion. - Software single conversion program completion. - Software continuous conversion program completion. - Monitor function interrupt (2 interrupts).
DMA request	-	- DMA can be started at the end of a series of conversions by general purpose factors (per factor)
Monitor conversion result	AD monitor function	- Each ADC unit has 2 channels of monitor function. - Selectable conversion result storage register to be monitored. - Selectable detection method: Whether the target register value is larger or smaller than the comparison register. - Selectable number of detections. - Selectable continuous count and accumulated count.

Note: Conversion program can specify conversion channel (analog input) and enable / disable of interrupt. There are multiple programs. Each is started with the start-up factor / trigger.

Figure 1.1 shows the connection relationships with the peripheral functions that are linked with the ADC.

The AD conversion can be executed with the PMD trigger synchronized with the motor drive timing of "Programmable Motor Control Circuit Plus" or "Advanced Programmable Motor Control Circuit" (hereafter, abbreviated as PMD) and the general purpose timer trigger. Execution of the OVV protection in PMD and activation of general purpose timer are possible with the AD monitor function.

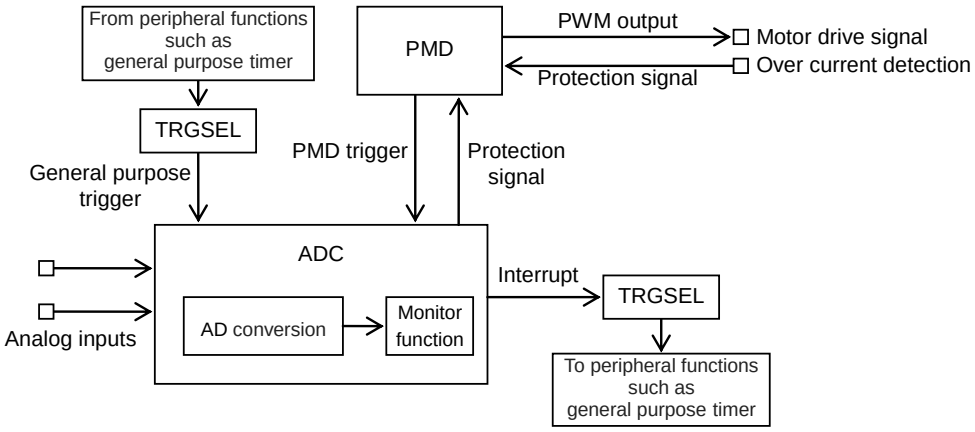


Figure 1.1 Related Figure of ADC and Another Peripheral Function

2. Configuration

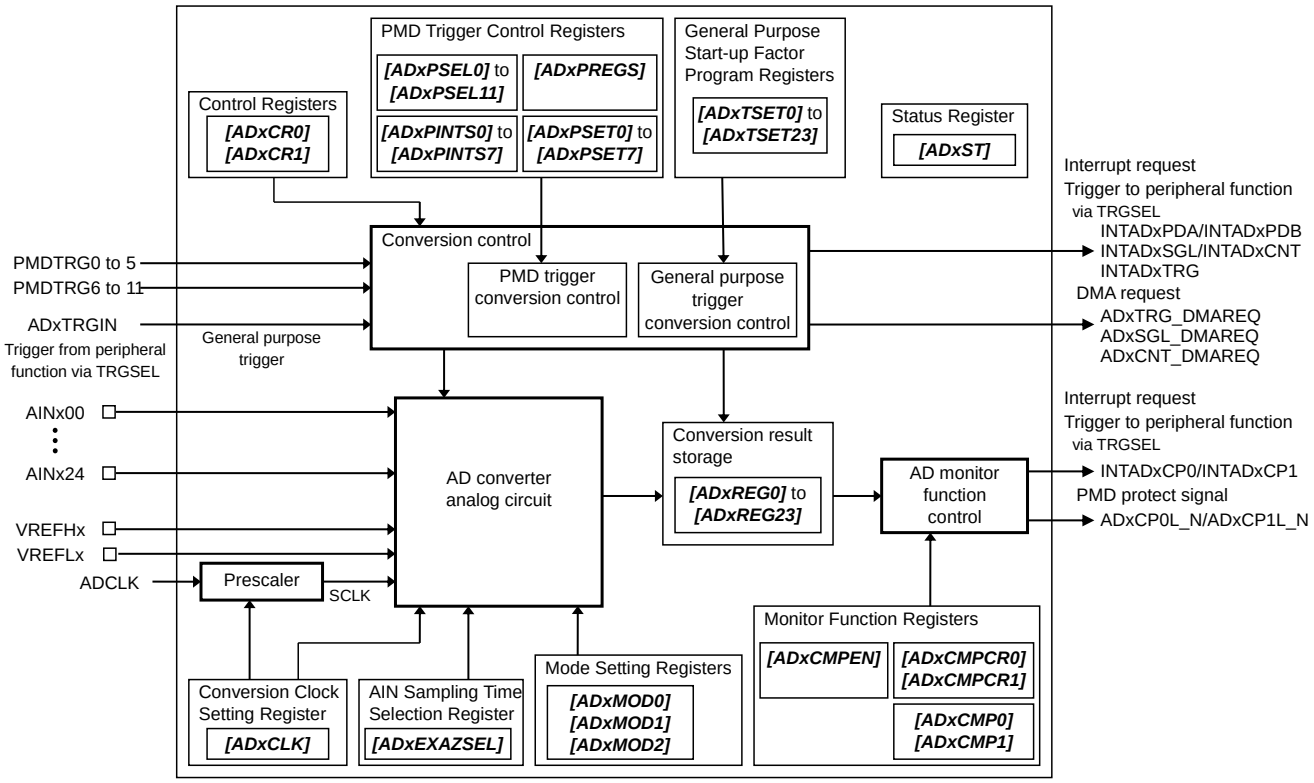


Figure 2.1 ADC Block Diagram

Table 2.1 List of Signals

No	Signal symbol	Signal name	I/O	Related reference manual
1	ADCLK	Conversion clock for ADC	Input	Clock Control and Operation Mode
2	AINx00 to AINx24	Analog input pin	Input	Product Information, Input/Output Ports
3	VREFHx	Reference power pin for analog	Input	Product Information
4	VREFLx	Reference GND pin for analog	Input	Product Information
5	PMDTRG0 to 5	PMD trigger	Input	Product Information
6	PMDTRG6 to 11	Trigger from PMD/peripheral function	Input	Product Information
7	ADxTRGIN	General purpose trigger	Input	Product Information
8	ADxCP0L_N	Monitor function0 output for PMD protect function	Output	Product Information
9	ADxCP1L_N	Monitor function1 output for PMD protect function	Output	Product Information
10	INTADxPDA	PMD trigger interrupt A	Output	Exception
11	INTADxPDB	PMD trigger interrupt B	Output	Exception
12	INTADxTRG	General purpose trigger interrupt	Output	Exception, Product Information
13	INTADxSGL	Single conversion interrupt	Output	Exception, Product Information
14	INTADxCNT	Continuous conversion interrupt	Output	Exception, Product Information
15	INTADxCP0	Monitor function0 interrupt	Output	Exception, Product Information
16	INTADxCP1	Monitor function1 interrupt	Output	Exception, Product Information
17	ADxTRG_DMAREQ	General purpose trigger DMA request	Output	Product Information
18	ADxSGL_DMAREQ	Single conversion DMA request	Output	Product Information
19	ADxCNT_DMAREQ	Continuous conversion DMA request	Output	Product Information

3. Function and Operation

The ADC is triggered to start the conversion by the software start-up (Software trigger) or the trigger signal from PMD, a timer, and others.

3.1. Clock Supply

When using ADC, set an applicable clock enable bit to "1" (clock supply) in Clock supply and stop register A for fsys (***[CGFSYSENA]***, ***[CGFSYSMENA]***), Clock supply and stop register B for fsys (***[CGFSYSENB]***, ***[CGFSYSMENB]***), Clock supply and stop register C for fsys (***[CGFSYSMENC]***), and Clock supply and stop register for fc (***[CGFCEN]***). Set the ADC conversion clock enable bit to "1" in Clock supply and stop register for ADC and Debug circuit (***[CGSPCLKEN]***).

An applicable register and the bit position vary according to a product. Therefore, the register may not exist with the product. Please refer to the reference manual "Clock Control and Operation Mode" for the details.

When stopping the clock supply, check that AD conversion has stopped. And when changing the operation mode to STOP1/STOP2, check that AD conversion has stopped.

3.2. Conversion Operation by General Purpose Start-up Factor

The factor of the general purpose start-up is the general purpose trigger input or the software start-up factor. The software start-up is the single conversion or the continuous conversion.

3.2.1. Operation

When the conversion is triggered by the general purpose start-up factor, the conversion executes according to the setting in the general purpose start-up factor program register which is prepared for each conversion result register.

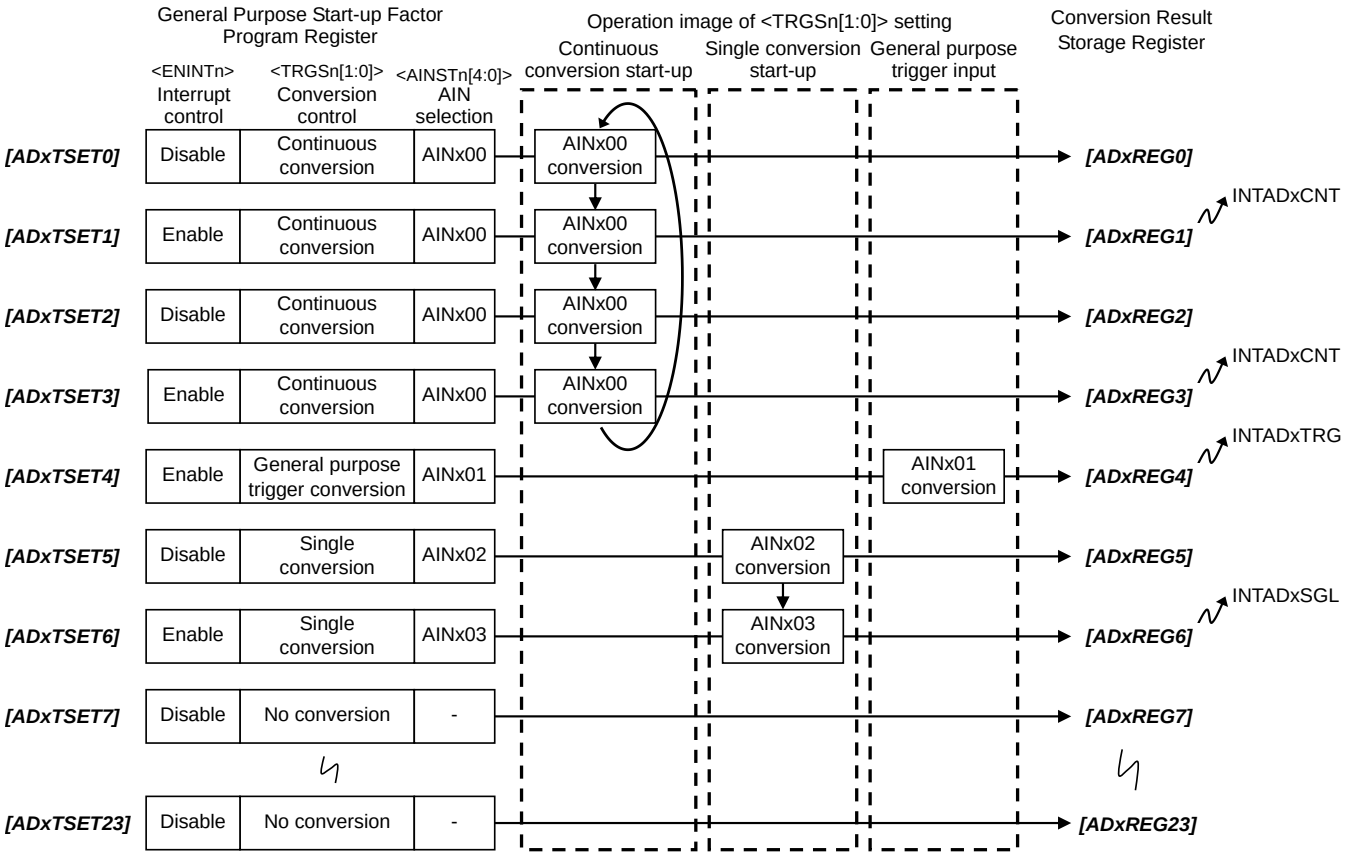


Figure 3.1 General Purpose Start-up Factor and Its Corresponding Operation

The general purpose start-up factor selection (Conversion control)<TRGSn[1:0]>, the AIN selection <AINSTn[4:0]>, and the interrupt enable or disable (Interrupt control)<ENINTn> are programmed to the general purpose start-up factor program register (***[ADxTSETn]***). When the start-up factor occurs, the specified conversions are executed from the smallest number of the general purpose start-up factor program registers.

The continuous conversion repeats the specified conversion. The single conversion executes the specified conversion only once. The general purpose trigger conversion executes the specified conversion once when the general purpose trigger is received.

With a general purpose start-up, when the conversion of the interrupt specified by ***[ADxTSETn]***<ENINTn> ends, different interrupts (INTADxTRG, INTADxSGL, INTADxCNT) are generated for each start-up factor (general purpose trigger conversion, single conversion, continuous conversion).

A DMA request can be generated for each general purpose start-up factor at the end of a series of conversions. To enable DMA requests, set ***[ADxCR1]***<CNTDMEN>, <SGLDMEN>, and/or <TRGDMEN> to "1".

In general purpose trigger and single conversion, if an interrupt is enabled for the last conversion in a series of conversions, a DMA request is generated at the same time as the interrupt generation.

In continuous conversion, the conversion being performed when ***[ADxCR0]***<CNT> is set to "0" (stop) is the last conversion. If an interrupt is enabled for the last conversion, a DMA request is generated at the same time as the interrupt generation.

Table 3.1 Start-up Factor and Interrupt / DMA Request

Start-up factor	Interrupt	DMA request
General purpose trigger conversion	General purpose trigger interrupt (INTADxTRG)	General purpose trigger DMA request (ADxTRG_DMAREQ)
Single conversion	Single conversion interrupt (INTADxSGL)	Single conversion DMA request (ADxSGL_DMAREQ)
Continuous conversion	Continuous conversion interrupt (INTADxCNT)	Continuous conversion DMA request (ADxCNT_DMAREQ)

3.2.2. Control Registers

- General purpose start-up factor program register (***[ADxTSET0]*** to ***[ADxTSET23]***)

  The general purpose start-up factor program register is prepared for each conversion result storage register.

  The AIN select <AINSTn[4:0]>, the conversion control <TRGSn[1:0]>, and the interrupt control <ENINTn> of ***[ADxTSETn]*** are set.

- Mode setting register0 (***[ADxMOD0]***)

  When using the ADC, set ***[ADxMOD0]***<DACON> to "1". And the interval of 3[µs] are necessary for the stabilization.

- Control register0 (***[ADxCR0]***)

  When the AD conversion can be started, after setting, ***[ADxCR0]***<ADEN> should be set to "1".

  The software single conversion or the software continuous conversion is enabled by setting ***[ADxCR0]*** <SGL> or <CNT> to "1". When the continuous conversion should be stopped, <CNT> is set to "0".

- Control register1 (***[ADxCR1]***)

  [ADxCR1]<TRGEN> enables the trigger, and then the program start-up is done by the general purpose trigger. The conversion starts when a trigger is received.

  [ADxCR1]<SGLDMEN>, <CNTDMEN>, <TRGDMEN> are set to "1" to enable the DMA request generation.

  Note: ***[ADxCR1]*** register must be set while ***[ADxCR0]***<ADEN> = 0.

For start AD conversion by the general purpose start-up factor, please set up as below sequence.

- Single conversion
  (1) Set interrupt to use INTADxSGL.
  (2) Set ***[ADxMOD0]***<DACON> to "1".
  (3) Wait at least 3[µs].
  (4) Set ***[ADxTSETn]***. AIN selection <AINSTn[4:0]> = arbitrary, conversion control <TRGSn[1:0]> = 10, interrupt control <ENINTn> = 1.
  (5) To perform the single conversion using multiple channels, set (4) with another AIN selection again.
  (6) Set ***[ADxCR0]***<ADEN> to "1".
  (7) Set ***[ADxCR0]***<SGL> to "1", starts the conversion.
  (8) When conversion is complete, INTADxSGL will be generated. Read ***[ADxREGn]*** in the interrupt service routine.
  (9) Repeat steps (7) to (8).

- Continuous conversion
  (1) Set interrupt to use INTADxCNT.
  (2) Set ***[ADxMOD0]***<DACON> to "1".
  (3) Wait at least 3[μs].
  (4) Set ***[ADxTSETn]***. AIN selection <AINSTn[4:0]> = arbitrary, conversion control <TRGSn[1:0]> = 01, interrupt control <ENINTn> = 1.
  (5) To perform the continuous conversion using multiple channels, set (4) with another AIN selection again.
  (6) Set ***[ADxCR0]***<ADEN> to "1".
  (7) Set ***[ADxCR0]***<CNT> to "1", starts the conversion.
  (8) When conversion is complete, INTADxCNT will be generated. Read ***[ADxREGn]*** in the interrupt service routine.
  (9) Repeat steps (8).

- General purpose trigger conversion
  (1) Set interrupt to use INTADxTRG.
  (2) Set ***[ADxMOD0]***<DACON> to "1".
  (3) Wait at least 3[μs].
  (4) Set ***[ADxCR1]***<TRGEN> to "1".
  (5) Sets which trigger to use for the general purpose trigger (ADxTRGIN). (Note)
  (6) Set ***[ADxTSETn]***. AIN selection <AINSTn[4:0]> = arbitrary, conversion control <TRGSn[1:0]> = 11, interrupt control <ENINTn> = 1.
  (7) To activate the general purpose trigger conversion using multiple channels, set (4) with another AIN selection again.
  (8) Set ***[ADxCR0]***<ADEN> to "1".
  (9) When you input a trigger, conversion starts.
  (10) When conversion is complete, INTADxTRG will be generated. Read ***[ADxREGn]*** in the interrupt service routine.
  (11) Repeat steps (9) to (10).

  Note: For details of the signal connected to the general purpose trigger (ADxTRGIN), refer to the reference manual "Product Information".

3.3. Conversion Operation by PMD Trigger

3.3.1. Operation

The conversion is started by the PMDTRGn (n=0 to 11). PMDTRGn are triggered from the PMD and the other peripheral function. (Note1)(Note2)

The programmed conversion operation is executed by the PMDTRGn. Each PMDTRGn selects one program from among 8 programs available.

One program can execute 4-time conversions at maximum. The conversion result is stored to the selected register group in units of 4 registers.

Either the INTADxPDA interrupt or the INTADxPDB interrupt can be generated at the program completion.

Note1: For details of the PMD, refer to the reference manual "Advanced Programmable Motor Control Circuit" or "Programmable Motor Control Circuit Plus".

Note2: For the connections of each product, refer to the reference manual "Product Information".

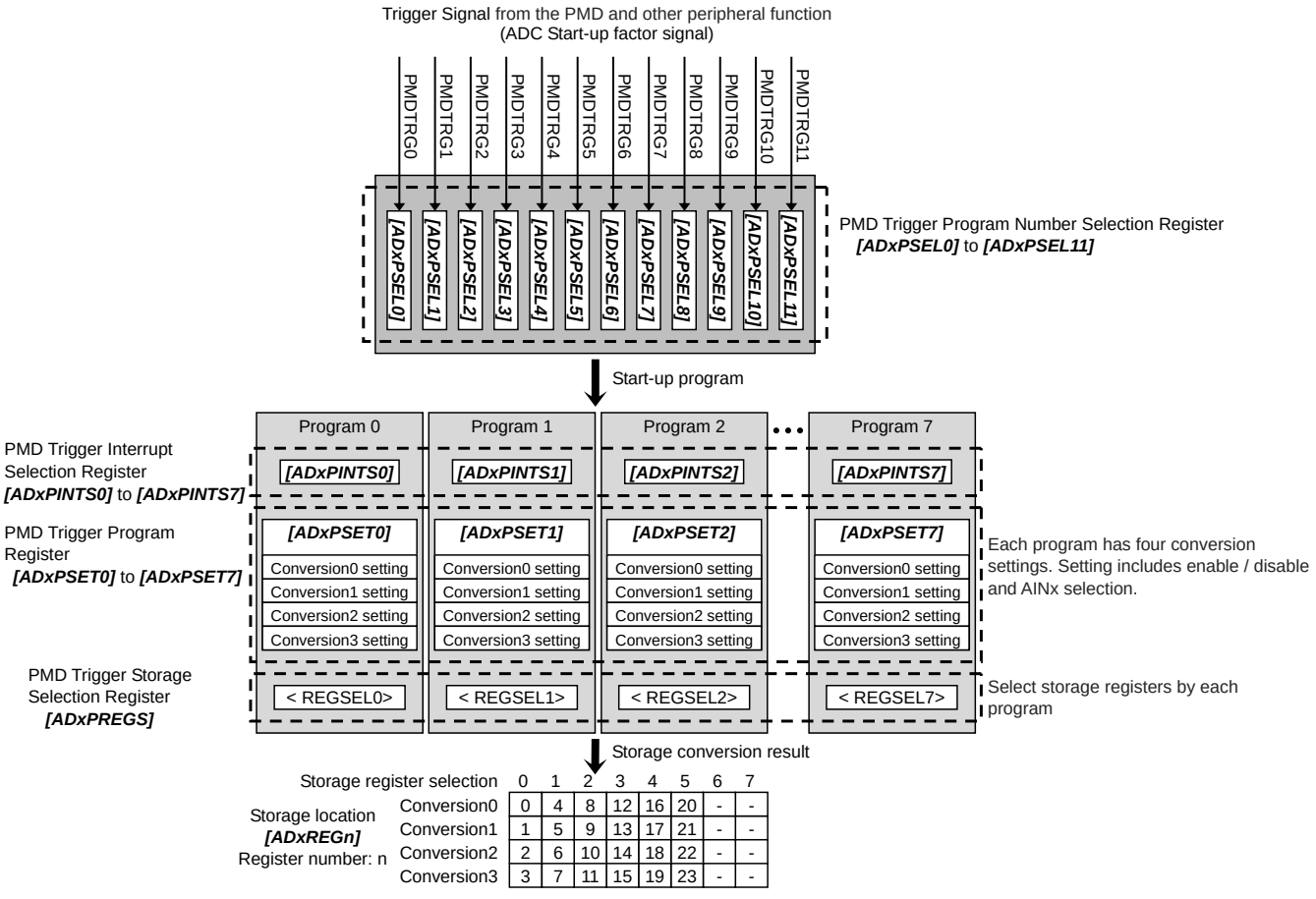


Figure 3.2 PMD Start-up Factor and Its Operation

3.3.2. Control Registers

The following registers should be set for the conversion started by the PMD trigger.

- Mode setting register0 (***[ADxMOD0]***)
  When using the ADC, set ***[ADxMOD0]***<DACON> to "1". And the interval of 3[μs] are necessary for the stabilization.

- PMD trigger program number selection register (***[ADxPSEL0]*** to ***[ADxPSEL11]***)
  Each register sets the trigger enable/disable and the specified program number (0 to 7) for one corresponding trigger out of 12 triggers.
  12 registers (***[ADxPSEL0]*** to ***[ADxPSEL11]***) are prepared for the 12 PMD triggers (PMDTRG0 to PMDTRG11), respectively.

- PMD trigger program register (***[ADxPSET0]*** to ***[ADxPSET7]***)
  These registers are set for each program. The setting items are the enable or disable of conversion, and the analog input channel to be converted. Each program can be set to 4-time conversions at maximum.

- PMD trigger interrupt selection register (***[ADxPINTS0]*** to ***[ADxPINTS7]***)
  An interrupt can be generated at the program completion. The PMD trigger interrupt selection register selects the interrupt enable or disable, and the interrupt INTADxPDA or INTADxPDB.
  8 registers (***[ADxPINTS0]*** to ***[ADxPINTS7]***) are prepared for the 8 programs.

- PMD trigger storage selection register (***[ADxPREGS]***)
  The storage destination of the conversion result of each program can be selected. The storage destination is selected from among the group of the conversion result storage register 0 to 3, 4 to 7, 8 to 11, 12 to 15, 16 to 19, and 20 to 23.

- Control register0 (***[ADxCR0]***)
  When the AD conversion can be started, after setting, ***[ADxCR0]***<ADEN> should be set to "1".

For start AD conversion by PMD trigger, please set up as below sequence.

(1) Set interrupt to use INTADxPDA or INTADxPDB.
(2) Set ***[ADxMOD0]***<DACON> to "1".
(3) Wait at least 3[μs].
(4) Set ***[ADxPSELm]***. Trigger control <PENSm> = 1, Program number <PMDSm[2:0]> = arbitrary.
(5) Set ***[ADxPSETn]***. AIN selection <AINSPn[4:0]> = arbitrary, conversion control <ENSPn> = 1.
(6) Set ***[ADxPINTSn]***. Interrupt selection <INTSELn[1:0]> = INTADxPDA or INTADxPDB.
(7) Set ***[ADxPREGS]***. Register selection <REGSELn[2:0]> = arbitrary.
(8) Set ***[ADxCR0]***<ADEN> to "1".
(9) Conversion starts by the trigger (PMDTRGm) that is PMD generated.
(10) When conversion program is complete, the interrupt (INTADxPDA or INTADxPDB) will be generated. Read ***[ADxREGi]*** to ***[ADxREGi+3]*** in the interrupt service routine.
(11) Repeat steps (9) to (10).

3.4. Conversion Stop

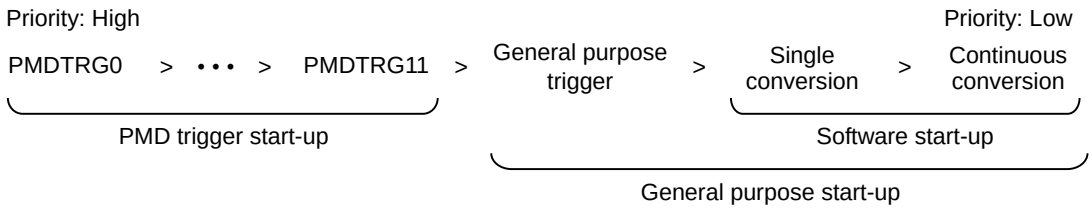
When ***[ADxCR0]***<ADEN> is set to "0", the conversion stops immediately. If the continuous conversion is enabled, ***[ADxCR0]***<CNT> should be also set to "0".

When the conversion stops completely, all bits in ***[ADxST]*** become "0". The registers other than ***[ADxST]*** keep their data, as well as the conversion result registers. Before the next conversion is enabled, the conversion result registers should be read to clear the corresponding flags.

When stopping ADCLK, AD conversion stop processing should be performed. Please confirm that ***[ADxST]*** <CNTF>, <SNGF>, <TRGF>, <PMDF> become all "0" and stop ADCLK.

3.5. Start-up Priority

The start-up factors are prioritized as follows:



If multiple start-up factors occur at the same time, the conversion program with the highest priority start-up factor is executed and other start-up factors are suspended.

Once a PMD trigger conversion program starts to execute, it is never suspended. Even though a higher priority PMD trigger is generated, it can execute after the currently executed conversion program completes.

The situation is different for the conversion programs of the general purpose trigger, the single conversion, and continuous conversion. When a higher priority start-up factor occurs, the current conversion program execution is suspended and the conversion program of the higher priority start-up factor executes. When a lower priority start-up factor occurs, it waits for execution.

The conversion programs of suspended general purpose trigger, single conversion, and continuous conversion restarts from suspended conversion when they become executable.

When the start-up factor occurs again during execution of the conversion program of the same start-up factor, the factor is ignored. The execution status of the conversion program can be checked by ***[ADxST]***<CNTF>, <SNGF>, <TRGF>, <PMDF>. For the software start-up factors, it should be confirmed whether the corresponding flags are "0". Then, the start-up is certainly executed.

Table 3.2 Operation when Start-up Factor Occurs During Conversion

		Later start-up factor			
		PMDTRGn (Note1)	**General purpose trigger**	**Software single conversion**	**Software continuous conversion**
Current start-up factor during conversion	PMDTRGm (Note1)	Continue current factor (Note2)	Continue current factor (Note3)	Continue current factor (Note3)	Continue current factor (Note3)
	General purpose trigger	Start later factor (Note5)	Continue current factor (Note4)	Continue current factor (Note3)	Continue current factor (Note3)
	Software single conversion	Start later factor (Note5)	Start later factor (Note5)	Continue current factor (Note4)	Continue current factor (Note3)
	Software continuous conversion	Start later factor (Note5)	Start later factor (Note5)	Start later factor (Note5)	Continue current factor (Note4)

Note1: m, n = 0 to 11

Note2: In the case of m = n, the later start-up factor is ignored.
In the case of m<>n, the later start-up factor is performed after the current factor is completed.

Note3: The later start-up factor is performed after the current factor is completed.

Note4: The later start-up factor is ignored.

Note5: The current start-up factor is suspended, and the later start-up factor is executed. After the later start-up factor completed, the current start-up factor is restarted.

3.6. AD Monitor Function

The AD monitor function generates an interrupt if the AD conversion result is larger than or smaller than the set value. It is possible to detect whether the AD conversion result is within the range of two set values or to detect whether the AD conversion result is out of the range by using this function simultaneously in two channels.

When ***[ADxCMPEN]***<CMP0EN> or <CMP1EN> is set to "1", the corresponding AD monitor function is enabled. The two monitor functions can be enabled simultaneously.

The following description is for ***[ADxCMPCR0]*** (The same for ***[ADxCMPCR1]***).

[ADxCMPCR0]<REGS0[4:0]> sets the conversion result storage register which value should be compared. <ADBIG0> sets the determination condition (larger or smaller). <CMPCND0> sets the determination count condition. And <CMPCNT0[3:0]> sets the determination count value.

Whenever a conversion result is stored to the target conversion result storage register, the result is compared (larger or smaller). If the comparison result is the same as the <ADBIG0> setting, the determination counter increments.

The determination count condition is either the continuous count or the accumulated count.

The continuous count condition is as follows: when the status set in <ADBIG0> continues the count times set in <CMPCNT0[3:0]>, the AD monitor function interrupt (INTADxCP0) and the protect signal for the PMD are generated. When it continues exceeding the set-up count number, nothing occurs. If the status is different from the <ADBIG0> status, the counter is cleared.

The accumulated count condition is as follows: when the count of the status set in <ADBIG0> is accumulated and the accumulated value reaches the value set in <CMPCNT0[3:0]>, the AD monitor function interrupt (INTADxCP0) and the protect signal for the PMD are generated, and the counter is cleared. Even when the status is different from the status set in <ADBIG0>, the counter value is maintained. When the value in the conversion result storage register specified by the ***[ADxCMPCR0]*** register is equal to the value in the conversion result comparison register, the counter does not increment and the AD monitor function interrupt and the trigger are not generated.

Table 3.3 Monitor Function and Interrupt

Monitor function	Interrupt
Monitor function Setting Register0 (***[ADxCMPCR0]***)	Monitor function0 Interrupt (INTADxCP0)
Monitor function Setting Register1 (***[ADxCMPCR1]***)	Monitor function1 Interrupt (INTADxCP1)

When the AD monitor function is used, the overrun flag ***[ADxREGn]***<ADOVRFn> and the conversion result storage flag ***[ADxREGn]***<ADRFn> are set because the storage register is not read by the software. So, when the AD monitor function is executing, the flags of the corresponding conversion result storage registers should not be used.

Note: The monitor function registers must be set while ***[ADxCR0]***<ADEN> = 0.

(1) Determination by Continuous count

- Monitor function setting register0 (***[ADxCMPCR0]*** = 0x00000200)

  Conversion result storage register (Comparison target): ***[ADxREG0]***
  Magnitude determination: ***[ADxREG0]***<ADR0[11:0]> > ***[ADxCMP0]***<AD0CMP0[11:0]>
  (Larger than the comparison register.)
  Determination count condition: Continuous count
  Magnitude determination count: 3 counts
- AD conversion result comparison register0 (***[ADxCMP0]***<AD0CMP0[11:0]> = 0x888)
- Monitor function enable register (***[ADxCMPEN]*** = 0x00000001)

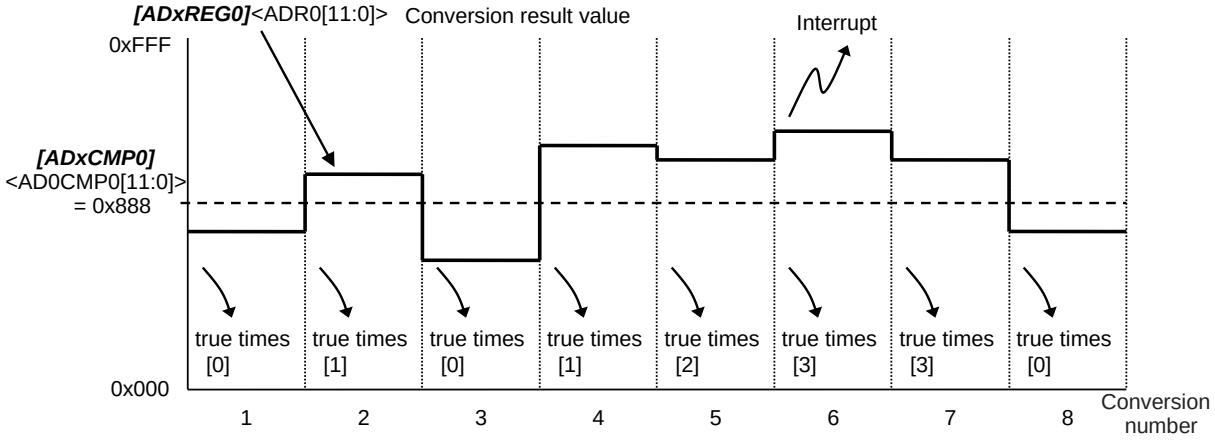


Figure 3.3 AD Monitor Function (Determination Condition: Continuous Count)

(2) Determination by Accumulated count

- Monitor function setting register0 (***[ADxCMPCR0]*** = 0x00000240)

  Conversion result storage register (Comparison target): ***[ADxREG0]***
  Magnitude determination: ***[ADxREG0]***<ADR0[11:0]> > ***[ADxCMP0]***<AD0CMP0[11:0]>
  (Larger than the comparison register.)
  Determination count condition: Accumulated count
  Magnitude determination count: 3 counts
- AD conversion result comparison register0 (***[ADxCMP0]***<AD0CMP0[11:0]> = 0x888)
- Monitor function enable register (***[ADxCMPEN]*** = 0x00000001)

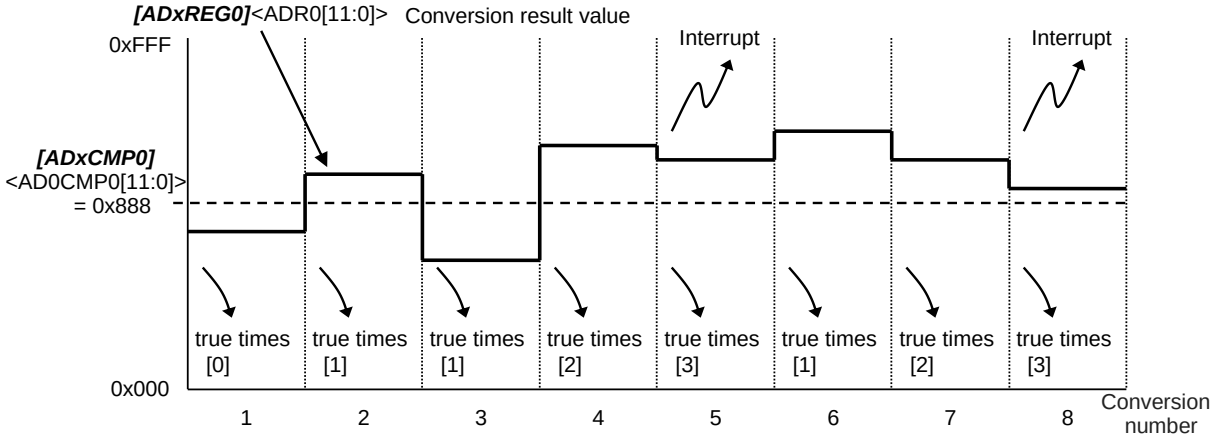


Figure 3.4 AD Monitor Function (Determination Condition: Accumulated Count)

3.7. Analog Reference Voltage

Analog reference voltage pins (VREFHx and VREFLx) in the ADC unit are connected to a High level and a Low level, respectively. When ***[ADxMOD0]***<RCUT> is set to "1", the switch between VREFHx and VREFLx is turned on only during the conversion to reduce the power consumption.

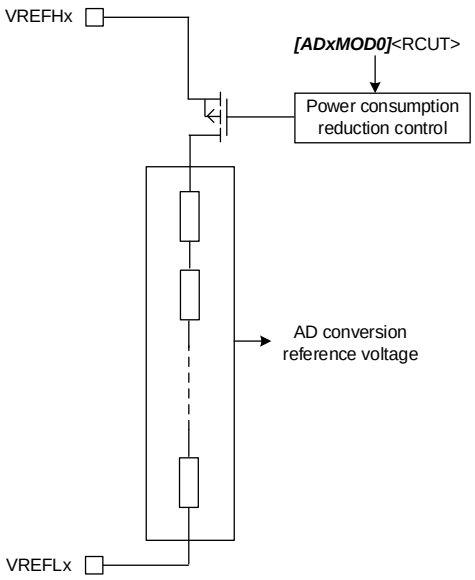


Figure 3.5 Configuration of Analog Reference Voltage

3.8. Conversion Time

3.8.1. Conversion Timing

Conversion timing is shown in Figure 3.6.

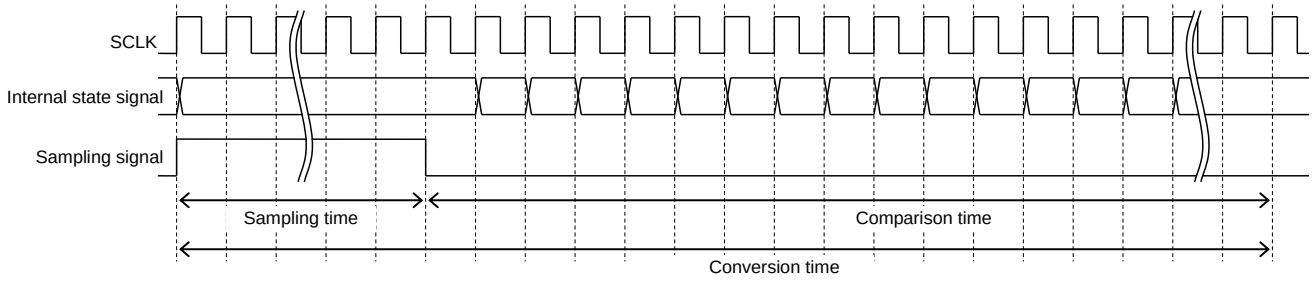


Figure 3.6 Example of Conversion Timing

3.8.2. Setting of Sampling Time

The sampling time is set with ***[ADxCLK]***<EXAZ0[3:0]> or <EXAZ1[3:0]>, <VADCLK[2:0]>, and ***[ADxMOD1]***<MOD1[31:0]>. Two types of AIN sampling time setting (<EXAZ0[3:0]>, <EXAZ1[3:0]>) can be set, and AIN sampling time setting can be selected for each AIN channel.

Sampling time = SCLK period × m × n
(m: <MOD1[31:0]> setting, n: <EXAZ0[3:0]> or <EXAZ1[3:0]> setting)

For the value of "m", refer to "5.2.6. ***[ADxMOD1]*** (Mode Setting Register1)".
For the value of "n", refer to "5.2.4. ***[ADxCLK]*** (Conversion Clock Setting Register)".

The sampling time varies depending on the power supply voltage and SCLK frequency to be used.

(1) 4.5[V] ≤ AVDD5 ≤ 5.5[V]:
SCLK = 20[MHz]: 0.4[µs] to 15.2[µs]
SCLK = 30[MHz]: 0.27[µs] to 10.13[µs]

(2) 2.7[V] ≤ AVDD5 < 4.5[V]:
SCLK = 20[MHz]: 0.6[µs] to 15.2[µs]

Table 3.4 to Table 3.6 show examples of sampling time settings.

Table 3.4 Example of Setting of Sampling Time (1) (SCLK = 20[MHz], 4.5[V] ≤ AVDD5 ≤ 5.5[V], Unit: μs)

[ADxMOD1] <MOD1[31:0]>	*[ADxCLK]*<EXAZ0[3:0]>, <EXAZ1[3:0]>				
	0000	0001	0010	0011	0101
0x00000000	-	0.4	0.6	0.8	3.2
0x00001000	-	0.5	0.75	1.0	4.0
0x00002000	-	0.6	0.9	1.2	4.8
0x00003000	-	0.7	1.05	1.4	5.6
0x00004000	0.4	0.8	1.2	1.6	6.4
0x00005000	0.45	0.9	1.35	1.8	7.2
0x00006000	0.5	1.0	1.5	2.0	8.0
0x00007000	0.55	1.1	1.65	2.2	8.8
0x00008000	0.6	1.2	1.8	2.4	9.6
0x00009000	0.65	1.3	1.95	2.6	10.4
0x0000A000	0.7	1.4	2.1	2.8	11.2
0x0000B000	0.75	1.5	2.25	3.0	12.0
0x0000C000	0.8	1.6	2.4	3.2	12.8
0x0000D000	0.85	1.7	2.55	3.4	13.6
0x0000E000	0.9	1.8	2.7	3.6	14.4
0x0000F000	0.95	1.9	2.85	3.8	15.2

Note: "-" setting can not be used.

Table 3.5 Example of Setting of Sampling Time (2) (SCLK = 20[MHz], 2.7[V] ≤ AVDD5 < 4.5[V], Unit: μs)

[ADxMOD1] <MOD1[31:0]>	*[ADxCLK]*<EXAZ0[3:0]>, <EXAZ1[3:0]>				
	0000	0001	0010	0011	0101
0x00000001	-	-	0.6	0.8	3.2
0x00001001	-	-	0.75	1.0	4.0
0x00002001	-	0.6	0.9	1.2	4.8
0x00003001	-	0.7	1.05	1.4	5.6
0x00004001	-	0.8	1.2	1.6	6.4
0x00005001	-	0.9	1.35	1.8	7.2
0x00006001	-	1.0	1.5	2.0	8.0
0x00007001	-	1.1	1.65	2.2	8.8
0x00008001	0.6	1.2	1.8	2.4	9.6
0x00009001	0.65	1.3	1.95	2.6	10.4
0x0000A001	0.7	1.4	2.1	2.8	11.2
0x0000B001	0.75	1.5	2.25	3.0	12.0
0x0000C001	0.8	1.6	2.4	3.2	12.8
0x0000D001	0.85	1.7	2.55	3.4	13.6
0x0000E001	0.9	1.8	2.7	3.6	14.4
0x0000F001	0.95	1.9	2.85	3.8	15.2

Note: "-" setting can not be used.

Table 3.6 Example of Setting of Sampling Time (3) (SCLK = 30[MHz], 4.5[V] ≤ AVDD5 ≤ 5.5[V], Unit: μs)

[ADxMOD1] <MOD1[31:0]>	*[ADxCLK]*<EXAZ0[3:0]>, <EXAZ1[3:0]>				
	0000	0001	0010	0011	0101
0x00000000	-	0.27	0.40	0.53	2.13
0x00001000	-	0.33	0.50	0.67	2.67
0x00002000	-	0.40	0.60	0.80	3.20
0x00003000	-	0.47	0.70	0.93	3.73
0x00004000	0.27	0.53	0.80	1.07	4.27
0x00005000	0.30	0.60	0.90	1.20	4.80
0x00006000	0.33	0.67	1.00	1.33	5.33
0x00007000	0.37	0.73	1.10	1.47	5.87
0x00008000	0.40	0.80	1.20	1.60	6.40
0x00009000	0.43	0.87	1.30	1.73	6.93
0x0000A000	0.47	0.93	1.40	1.87	7.47
0x0000B000	0.50	1.00	1.50	2.00	8.00
0x0000C000	0.53	1.07	1.60	2.13	8.53
0x0000D000	0.57	1.13	1.70	2.27	9.07
0x0000E000	0.60	1.20	1.80	2.40	9.60
0x0000F000	0.63	1.27	1.90	2.53	10.13

Note: "-" setting can not be used.

3.8.2.1. Selection of Sampling Time

Select the sampling time set by ***[ADxCLK]***<EXAZ0[3:0]> or <EXAZ1[3:0]> for each AIN channel with the AIN sampling time selection register (***[ADxEXAZSEL]***).

3.8.3. Setting of Conversion Time

The conversion time can be obtained by the following formula.

Conversion time = Sampling time + Comparison time

(1) 4.5[V] ≤ AVDD5 ≤ 5.5[V]
SCLK = 20[MHz]: Conversion time = Sampling time + 1.1[μs]
SCLK = 30[MHz]: Conversion time = Sampling time + 0.73[μs]

Note: Refer to Table 3.4 and Table 3.6 for sampling time.

(2) 2.7[V] ≤ AVDD5 < 4.5[V]
SCLK = 20[MHz]: Conversion time = Sampling time + 1.45[μs]

Note: Refer to Table 3.5 for sampling time.

Table 3.7 to Table 3.9 show examples of conversion time settings.

Table 3.7 Example of Setting of Conversion Time (1) (SCLK = 20[MHz], 4.5[V] ≤ AVDD5 ≤ 5.5[V], Unit: μs)

[ADxMOD1] <MOD1[31:0]>	*[ADxCLK]*<EXAZ0[3:0]> , <EXAZ1[3:0]>				
	0000	0001	0010	0011	0101
0x00000000	-	1.5	1.7	1.9	4.3
0x00001000	-	1.6	1.85	2.1	5.1
0x00002000	-	1.7	2.0	2.3	5.9
0x00003000	-	1.8	2.15	2.5	6.7
0x00004000	1.5	1.9	2.3	2.7	7.5
0x00005000	1.55	2.0	2.45	2.9	8.3
0x00006000	1.6	2.1	2.6	3.1	9.1
0x00007000	1.65	2.2	2.75	3.3	9.9
0x00008000	1.7	2.3	2.9	3.5	10.7
0x00009000	1.75	2.4	3.05	3.7	11.5
0x0000A000	1.8	2.5	3.2	3.9	12.3
0x0000B000	1.85	2.6	3.35	4.1	13.1
0x0000C000	1.9	2.7	3.5	4.3	13.9
0x0000D000	1.95	2.8	3.65	4.5	14.7
0x0000E000	2.0	2.9	3.8	4.7	15.5
0x0000F000	2.05	3.0	3.95	4.9	16.3

Note: "-" setting can not be used.

Table 3.8 Example of Setting of Conversion Time (2) (SCLK = 20[MHz], 2.7[V] ≤ AVDD5 < 4.5[V], Unit: μs)

[ADxMOD1] <MOD1[31:0]>	*[ADxCLK]*<EXAZ0[3:0]> , <EXAZ1[3:0]>				
	0000	0001	0010	0011	0101
0x00000001	-	-	2.05	2.25	4.65
0x00001001	-	-	2.20	2.45	5.45
0x00002001	-	2.05	2.35	2.65	6.25
0x00003001	-	2.15	2.50	2.85	7.05
0x00004001	-	2.25	2.65	3.05	7.85
0x00005001	-	2.35	2.80	3.25	8.65
0x00006001	-	2.45	2.95	3.45	9.45
0x00007001	-	2.55	3.1	3.65	10.25
0x00008001	2.05	2.65	3.25	3.85	11.05
0x00009001	2.10	2.75	3.4	4.05	11.85
0x0000A001	2.15	2.85	3.55	4.25	12.65
0x0000B001	2.20	2.95	3.7	4.45	13.45
0x0000C001	2.25	3.05	3.85	4.65	14.25
0x0000D001	2.30	3.15	4.0	4.85	15.05
0x0000E001	2.35	3.25	4.15	5.05	15.85
0x0000F001	2.40	3.35	4.3	5.25	16.65

Note: "-" setting can not be used.

Table 3.9 Example of Setting of Conversion Time (3) (SCLK = 30[MHz], 4.5[V] ≤ AVDD5 ≤ 5.5[V], Unit: μs)

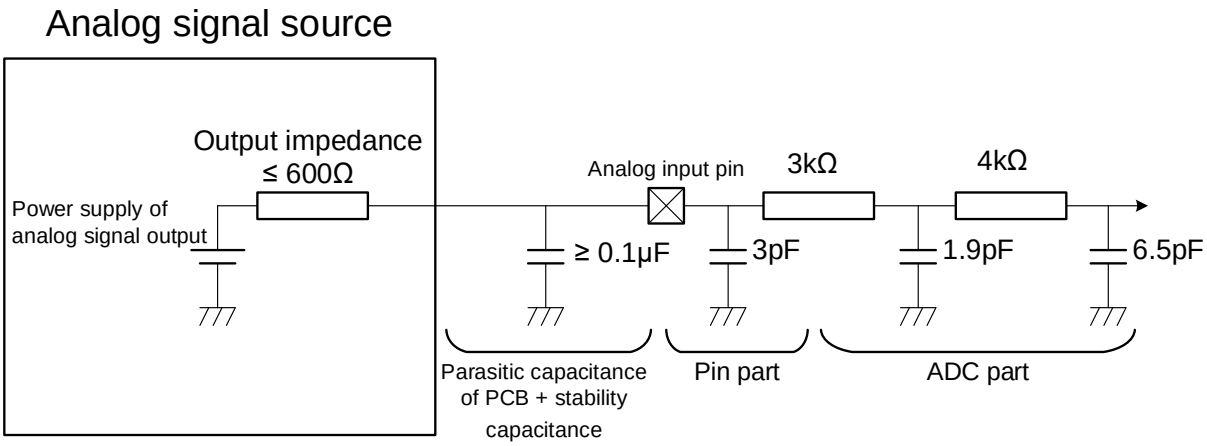
[ADxMOD1] **<MOD1[31:0]>**	***[ADxCLK]*<EXAZ0[3:0]>, <EXAZ1[3:0]>**				
	0000	**0001**	**0010**	**0011**	**0101**
0x00000000	-	1.00	1.13	1.27	2.87
0x00001000	-	1.07	1.23	1.40	3.40
0x00002000	-	1.13	1.33	1.53	3.93
0x00003000	-	1.20	1.43	1.67	4.47
0x00004000	1.00	1.27	1.53	1.80	5.00
0x00005000	1.03	1.33	1.63	1.93	5.53
0x00006000	1.07	1.40	1.73	2.07	6.07
0x00007000	1.10	1.47	1.83	2.20	6.60
0x00008000	1.13	1.53	1.93	2.33	7.13
0x00009000	1.17	1.60	2.03	2.47	7.67
0x0000A000	1.20	1.67	2.13	2.60	8.20
0x0000B000	1.23	1.73	2.23	2.73	8.73
0x0000C000	1.27	1.80	2.33	2.87	9.27
0x0000D000	1.30	1.87	2.43	3.00	9.80
0x0000E000	1.33	1.93	2.53	3.13	10.33
0x0000F000	1.37	2.00	2.63	3.27	10.87

Note: "-" setting can not be used.

4. Equivalent Circuit

Equivalent circuit of analog input pin is shown in Figure 4.1. Each constant is the design value.

1. Condition 1
   - AVDD5 = 4.5 to 5.5V
   - Load resistor of analog input pin: ≤ 600Ω
   - Load capacitance of analog input pin: ≥ 0.1μF
   - Conversion time: ≥ 1.00μs



2. Condition 2
   - AVDD5 = 2.7 to 4.5V
   - Load resistor of analog input pin: ≤ 600Ω
   - Load capacitance of analog input pin: ≥ 0.1μF
   - Conversion time: ≥ 2.05μs

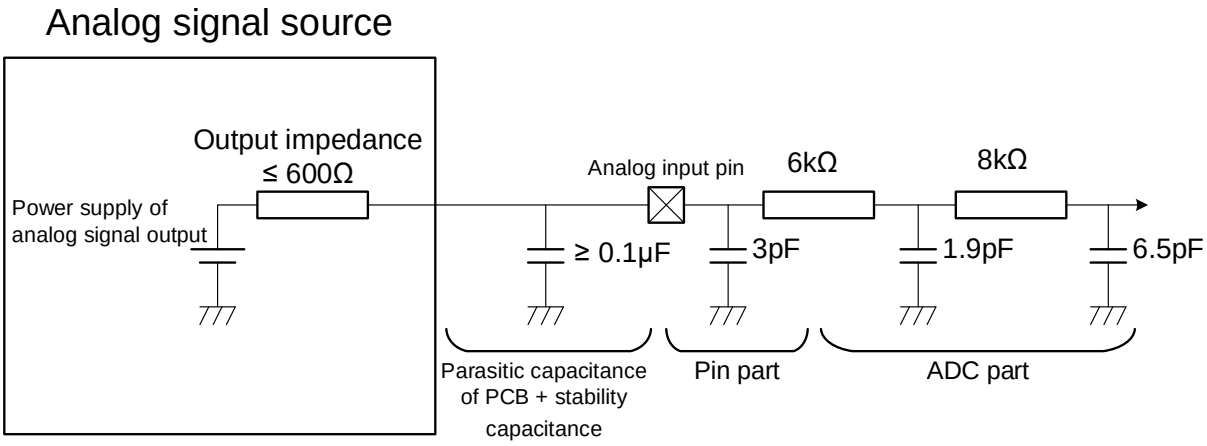


Figure 4.1 Equivalent Circuit of Analog Input Pin

5. Registers

5.1. List of Registers

The control registers and their addresses are shown as follows:

Peripheral function		Channel/unit	Base address		
			TYPE1	TYPE2	TYPE3
12-bit Analog to Digital Converter	ADC	Unit A	0x400B8800	0x400BA000	0x4005A000
		Unit B	0x400B8C00	0x400BA400	0x4005A400

Note: The Channel/Unit and Base address type are different by products. Please refer to the reference manual "Product Information" for the details.

Register name		Address (Base+)
Control Register0	***[ADxCR0]***	0x0000
Control Register1	***[ADxCR1]***	0x0004
Status Register	***[ADxST]***	0x0008
Conversion Clock Setting Register	***[ADxCLK]***	0x000C
Mode Setting Register0	***[ADxMOD0]***	0x0010
Mode Setting Register1	***[ADxMOD1]***	0x0014
Mode Setting Register2	***[ADxMOD2]***	0x0018
Monitor function Enable Register	***[ADxCMPEN]***	0x0020
Monitor function Setting Register0	***[ADxCMPCR0]***	0x0024
Monitor function Setting Register1	***[ADxCMPCR1]***	0x0028
Conversion Result Comparison Register0	***[ADxCMP0]***	0x002C
Conversion Result Comparison Register1	***[ADxCMP1]***	0x0030
PMD Trigger Program Number Selection Register0	***[ADxPSEL0]***	0x0040
PMD Trigger Program Number Selection Register1	***[ADxPSEL1]***	0x0044
PMD Trigger Program Number Selection Register2	***[ADxPSEL2]***	0x0048
PMD Trigger Program Number Selection Register3	***[ADxPSEL3]***	0x004C
PMD Trigger Program Number Selection Register4	***[ADxPSEL4]***	0x0050
PMD Trigger Program Number Selection Register5	***[ADxPSEL5]***	0x0054
PMD Trigger Program Number Selection Register6	***[ADxPSEL6]***	0x0058
PMD Trigger Program Number Selection Register7	***[ADxPSEL7]***	0x005C
PMD Trigger Program Number Selection Register8	***[ADxPSEL8]***	0x0060
PMD Trigger Program Number Selection Register9	***[ADxPSEL9]***	0x0064
PMD Trigger Program Number Selection Register10	***[ADxPSEL10]***	0x0068
PMD Trigger Program Number Selection Register11	***[ADxPSEL11]***	0x006C
PMD Trigger Interrupt Selection Register0	***[ADxPINTS0]***	0x0070
PMD Trigger Interrupt Selection Register1	***[ADxPINTS1]***	0x0074
PMD Trigger Interrupt Selection Register2	***[ADxPINTS2]***	0x0078
PMD Trigger Interrupt Selection Register3	***[ADxPINTS3]***	0x007C
PMD Trigger Interrupt Selection Register4	***[ADxPINTS4]***	0x0080
PMD Trigger Interrupt Selection Register5	***[ADxPINTS5]***	0x0084
PMD Trigger Interrupt Selection Register6	***[ADxPINTS6]***	0x0088
PMD Trigger Interrupt Selection Register7	***[ADxPINTS7]***	0x008C

Register name		Address (Base+)
PMD Trigger Storage Selection Register	***[ADxPREGS]***	0x0090
Trimming Setting Register	***[ADxTRM]***	0x0094
AIN sampling time selection Register	***[ADxEXAZSEL]***	0x009C
PMD Trigger Program Register0	***[ADxPSET0]***	0x00A0
PMD Trigger Program Register1	***[ADxPSET1]***	0x00A4
PMD Trigger Program Register2	***[ADxPSET2]***	0x00A8
PMD Trigger Program Register3	***[ADxPSET3]***	0x00AC
PMD Trigger Program Register4	***[ADxPSET4]***	0x00B0
PMD Trigger Program Register5	***[ADxPSET5]***	0x00B4
PMD Trigger Program Register6	***[ADxPSET6]***	0x00B8
PMD Trigger Program Register7	***[ADxPSET7]***	0x00BC
General Purpose Start-up Factor Program Register0	***[ADxTSET0]***	0x00C0
General Purpose Start-up Factor Program Register1	***[ADxTSET1]***	0x00C4
General Purpose Start-up Factor Program Register2	***[ADxTSET2]***	0x00C8
General Purpose Start-up Factor Program Register3	***[ADxTSET3]***	0x00CC
General Purpose Start-up Factor Program Register4	***[ADxTSET4]***	0x00D0
General Purpose Start-up Factor Program Register5	***[ADxTSET5]***	0x00D4
General Purpose Start-up Factor Program Register6	***[ADxTSET6]***	0x00D8
General Purpose Start-up Factor Program Register7	***[ADxTSET7]***	0x00DC
General Purpose Start-up Factor Program Register8	***[ADxTSET8]***	0x00E0
General Purpose Start-up Factor Program Register9	***[ADxTSET9]***	0x00E4
General Purpose Start-up Factor Program Register10	***[ADxTSET10]***	0x00E8
General Purpose Start-up Factor Program Register11	***[ADxTSET11]***	0x00EC
General Purpose Start-up Factor Program Register12	***[ADxTSET12]***	0x00F0
General Purpose Start-up Factor Program Register13	***[ADxTSET13]***	0x00F4
General Purpose Start-up Factor Program Register14	***[ADxTSET14]***	0x00F8
General Purpose Start-up Factor Program Register15	***[ADxTSET15]***	0x00FC
General Purpose Start-up Factor Program Register16	***[ADxTSET16]***	0x0100
General Purpose Start-up Factor Program Register17	***[ADxTSET17]***	0x0104
General Purpose Start-up Factor Program Register18	***[ADxTSET18]***	0x0108
General Purpose Start-up Factor Program Register19	***[ADxTSET19]***	0x010C
General Purpose Start-up Factor Program Register20	***[ADxTSET20]***	0x0110
General Purpose Start-up Factor Program Register21	***[ADxTSET21]***	0x0114
General Purpose Start-up Factor Program Register22	***[ADxTSET22]***	0x0118
General Purpose Start-up Factor Program Register23	***[ADxTSET23]***	0x011C
Conversion Result Storage Register0	***[ADxREG0]***	0x0140
Conversion Result Storage Register1	***[ADxREG1]***	0x0144
Conversion Result Storage Register2	***[ADxREG2]***	0x0148
Conversion Result Storage Register3	***[ADxREG3]***	0x014C
Conversion Result Storage Register4	***[ADxREG4]***	0x0150
Conversion Result Storage Register5	***[ADxREG5]***	0x0154
Conversion Result Storage Register6	***[ADxREG6]***	0x0158
Conversion Result Storage Register7	***[ADxREG7]***	0x015C
Conversion Result Storage Register8	***[ADxREG8]***	0x0160
Conversion Result Storage Register9	***[ADxREG9]***	0x0164
Conversion Result Storage Register10	***[ADxREG10]***	0x0168
Conversion Result Storage Register11	***[ADxREG11]***	0x016C

Register name		Address (Base+)
Conversion Result Storage Register12	***[ADxREG12]***	0x0170
Conversion Result Storage Register13	***[ADxREG13]***	0x0174
Conversion Result Storage Register14	***[ADxREG14]***	0x0178
Conversion Result Storage Register15	***[ADxREG15]***	0x017C
Conversion Result Storage Register16	***[ADxREG16]***	0x0180
Conversion Result Storage Register17	***[ADxREG17]***	0x0184
Conversion Result Storage Register18	***[ADxREG18]***	0x0188
Conversion Result Storage Register19	***[ADxREG19]***	0x018C
Conversion Result Storage Register20	***[ADxREG20]***	0x0190
Conversion Result Storage Register21	***[ADxREG21]***	0x0194
Conversion Result Storage Register22	***[ADxREG22]***	0x0198
Conversion Result Storage Register23	***[ADxREG23]***	0x019C

5.2. Details of Registers

5.2.1. *[ADxCR0] (Control Register0)*

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0".
7	ADEN	0	R/W	ADC control 0: Disabled 1: Enabled When this bit is set to "1", the conversion is enabled. When this bit is set to "0", the conversion stops.
6:2	-	0	R	Read as "0".
1	SGL	0	W	Single conversion control 0: Don't care. 1: Conversion start. When this bit is set to "1", the single conversion program starts to execute. If this bit is read, "0" is returned.
0	CNT	0	R/W	Continuous conversion control 0: Disabled 1: Enabled When this bit is set to "1", the continuous conversion starts to execute. This bit should be set to "1" while ***[ADxST]***<CNTF> is "0" (a continuous conversion program does not execute).

5.2.2. *[ADxCR1]* (Control Register1)

Bit	Bit symbol	After reset	Type	Function
31:7	-	0	R	Read as "0".
6	CNTDMEN	0	R/W	Continuous conversion DMA request control 0: Disabled 1: Enabled
5	SGLDMEN	0	R/W	Single conversion DMA request control 0: Disabled 1: Enabled
4	TRGDMEN	0	R/W	General purpose trigger DMA request control 0: Disabled 1: Enabled
3:1	-	0	R	Read as "0".
0	TRGEN	0	R/W	General purpose trigger start-up control 0: Disabled 1: Enabled

Note: This register must be set while ***[ADxCR0]***<ADEN> = 0.

5.2.3. *[ADxST]* (Status Register)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0".
7	ADBF	0	R	AD operation flag 0: Stop (ADCLK can be stopped.) 1: Executing (ADCLK cannot be stopped.) Before ADCLK is stopped, this bit should be confirmed to be "0".
6:4	-	0	R	Read as "0".
3	CNTF	0	R	Continuous conversion program flag 0: Stop 1: Executing When the request is received, this bit becomes "1". When the last conversion result is stored, this bit becomes "0".
2	SNGF	0	R	Single conversion program flag 0: Stop 1: Executing (Note) When the request is received, this bit becomes "1". When the last conversion result is stored, this bit becomes "0".
1	TRGF	0	R	General purpose trigger program flag 0: Stop 1: Executing When the request is received, this bit becomes "1". When the last conversion result is stored, this bit becomes "0".
0	PMDF	0	R	PMD trigger program flag 0: Stop 1: Executing When the request is received, this bit becomes "1". When the last conversion result is stored, this bit becomes "0".

Note: After ***[ADxCR0]***<SGL> is set to "1", it changes after up to 5 SCLK clocks.

5.2.4. *[ADxCLK]* (Conversion Clock Setting Register)

Bit	Bit symbol	After reset	Type	Function
31:12	-	0	R	Read as "0".
11:8	EXAZ1[3:0]	0000	R/W	AIN sampling time setting 1 (Note2) 0000: SCLK period × n (m = 1) 0001: SCLK period × 2n (m = 2) 0010: SCLK period × 3n (m = 3) 0011: SCLK period × 4n (m = 4) 0101: SCLK period × 16n (m = 16) Others: Reserved Please refer to ”5.2.6. *[ADxMOD1]* (Mode Setting Register1)” for the value of "n".
7	-	0	R	Read as "0".
6:3	EXAZ0[3:0]	0000	R/W	AIN sampling time setting 0 (Note2) 0000: SCLK period × n (m = 1) 0001: SCLK period × 2n (m = 2) 0010: SCLK period × 3n (m = 3) 0011: SCLK period × 4n (m = 4) 0101: SCLK period × 16n (m = 16) Others: Reserved Please refer to ”5.2.6. *[ADxMOD1]* (Mode Setting Register1)” for the value of "n".
2:0	VADCLK[2:0]	000	R/W	AD prescaler output (SCLK) selection 000: ADCLK/2 001: ADCLK/4 010: ADCLK/8 011: ADCLK/16 100: ADCLK/3 101: ADCLK/5 110: ADCLK/6 111: ADCLK/10 This bit should be set so that SCLK frequency is as follows: 4.5V ≤ AVDD5 ≤ 5.5V: 30MHz or less 2.7V ≤ AVDD5 < 4.5V: 20MHz or less

Note1: This register must be set while ***[ADxCR0]***<ADEN> = 0.

Note2: Select the AIN sampling time setting with ***[ADxEXAZSEL]***.

5.2.5. *[ADxMOD0]* (Mode Setting Register0)

Bit	Bit symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1	RCUT	1	R/W	Low power mode selection 0: Normal operation 1: Low power operation (Energized between VREFHx and VREFLx only during the conversion)
0	DACON	0	R/W	DAC control (Note2) 0: OFF 1: ON When the ADC is used, <DACON> should be set to "1".

Note1: This register must be set while ***[ADxCR0]***<ADEN> = 0.

Note2: After ***[ADxMOD0]***<DACON> is set to "1", the interval of 3[μs] are necessary for the stabilization.

5.2.6. *[ADxMOD1]* (Mode Setting Register1)

Bit	Bit symbol	After reset	Type	Function
31:0	MOD1[31:0]	0x00004000	R/W	"n" value setting for sampling time 4.5[V] ≤ AVDD5 ≤ 5.5[V] 0x00000000: 4 0x00001000: 5 0x00002000: 6 0x00003000: 7 0x00004000: 8 0x00005000: 9 0x00006000: 10 0x00007000: 11 0x00008000: 12 0x00009000: 13 0x0000A000: 14 0x0000B000: 15 0x0000C000: 16 0x0000D000: 17 0x0000E000: 18 0x0000F000: 19 Others: reserved 2.7[V] ≤ AVDD5 < 4.5[V] 0x00000001: 4 0x00001001: 5 0x00002001: 6 0x00003001: 7 0x00004001: 8 0x00005001: 9 0x00006001: 10 0x00007001: 11 0x00008001: 12 0x00009001: 13 0x0000A001: 14 0x0000B001: 15 0x0000C001: 16 0x0000D001: 17 0x0000E001: 18 0x0000F001: 19 Others: reserved Please refer to “3.8.2. Setting of Sampling Time” for setting range of sampling time.

Note: This register must be set while ***[ADxCR0]***<ADEN> = 0.

5.2.7. *[ADxMOD2]* (Mode Setting Register2)

Bit	Bit symbol	After reset	Type	Function
31:0	MOD2[31:0]	0x00000000	R/W	The setting value of this register varies depending on the product. For the setting value, refer to the reference manual "Product Information".

Note: This register must be set while ***[ADxCR0]***<ADEN> = 0.

5.2.8. *[ADxCMPEN]* (Monitor function Enable Register)

Bit	Bit symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1	CMP1EN	0	R/W	AD monitor function1 operation 0: Disabled. 1: Enabled.
0	CMP0EN	0	R/W	AD monitor function0 operation 0: Disabled. 1: Enabled.

5.2.9. *[ADxCMPCR0]* (Monitor function Setting Register0)

Bit	Bit symbol	After reset	Type	Function
31:12	-	0	R	Read as "0".
11:8	CMPCNT0[3:0]	0000	R/W	Comparison count 0000: 1 1000: 9 0001: 2 1001: 10 0010: 3 1010: 11 0011: 4 1011: 12 0100: 5 1100: 13 0101: 6 1101: 14 0110: 7 1110: 15 0111: 8 1111: 16
7	-	0	R	Read as "0".
6	CMPCND0	0	R/W	Determination condition 0: Continuous count 1: Accumulated count
5	ADBIG0	0	R/W	Magnitude determination setting 0: Conversion result specified by <REGS0[4:0]> > ***[ADxCMP0]*** 1: Conversion result specified by <REGS0[4:0]> < ***[ADxCMP0]***
4:0	REGS0[4:0]	00000	R/W	Compared conversion result storage register 00000: ADxREG0 01000: ADxREG8 10000: ADxREG16 00001: ADxREG1 01001: ADxREG9 10001: ADxREG17 00010: ADxREG2 01010: ADxREG10 10010: ADxREG18 00011: ADxREG3 01011: ADxREG11 10011: ADxREG19 00100: ADxREG4 01100: ADxREG12 10100: ADxREG20 00101: ADxREG5 01101: ADxREG13 10101: ADxREG21 00110: ADxREG6 01110: ADxREG14 10110: ADxREG22 00111: ADxREG7 01111: ADxREG15 10111: ADxREG23 11000 to 11111: Inhibited setting

Note: This register must be set while ***[ADxCMPEN]***<CMP0EN> = 0.

5.2.10. *[ADxCMPCR1]* (Monitor function Setting Register1)

Bit	Bit symbol	After reset	Type	Function
31:12	-	0	R	Read as "0".
11:8	CMPCNT1[3:0]	0000	R/W	Comparison count 0000: 1 1000: 9 0001: 2 1001: 10 0010: 3 1010: 11 0011: 4 1011: 12 0100: 5 1100: 13 0101: 6 1101: 14 0110: 7 1110: 15 0111: 8 1111: 16
7	-	0	R	Read as "0".
6	CMPCND1	0	R/W	Determination condition 0: Continuous count 1: Accumulated count
5	ADBIG1	0	R/W	Magnitude determination setting 0: Conversion result specified by <REGS1[4:0]> > ***[ADxCMP1]*** 1: Conversion result specified by <REGS1[4:0]> < ***[ADxCMP1]***
4:0	REGS1[4:0]	00000	R/W	Compared conversion result storage register 00000: ADxREG0 01000: ADxREG8 10000: ADxREG16 00001: ADxREG1 01001: ADxREG9 10001: ADxREG17 00010: ADxREG2 01010: ADxREG10 10010: ADxREG18 00011: ADxREG3 01011: ADxREG11 10011: ADxREG19 00100: ADxREG4 01100: ADxREG12 10100: ADxREG20 00101: ADxREG5 01101: ADxREG13 10101: ADxREG21 00110: ADxREG6 01110: ADxREG14 10110: ADxREG22 00111: ADxREG7 01111: ADxREG15 10111: ADxREG23 11000 to 11111: Inhibited setting

Note: This register must be set while ***[ADxCMPEN]***<CMP1EN> = 0.

5.2.11. *[ADxCMP0]* (Conversion Result Comparison Register0)

Bit	Bit symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:4	AD0CMP0[11:0]	0x000	R/W	AD conversion result comparison value storage The value compared with the AD conversion result is set.
3:0	-	0	R	Read as "0".

Note: This register must be set while ***[ADxCMPEN]***<CMP0EN> = 0.

5.2.12. *[ADxCMP1]* (Conversion Result Comparison Register1)

Bit	Bit symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:4	AD0CMP1[11:0]	0x000	R/W	AD conversion result comparison value storage The value compared with the AD conversion result is set.
3:0	-	0	R	Read as "0".

Note: This register must be set while ***[ADxCMPEN]***<CMP1EN> = 0.

5.2.13. *[ADxEXAZSEL]* (AIN sampling time selection Register)

Bit	Bit symbol	After reset	Type	Function
31:0	EXAZSEL[31:0]	0x00000000	R/W	Selection of AIN sampling time setting 0: ***[ADxCLK]***<EXAZ0[3:0]> setting is used 1: ***[ADxCLK]***<EXAZ1[3:0]> setting is used Please select which one of <EXAZ0[3:0]> or <EXAZ1[3:0]> is used for each AIN channel. Each bit corresponds to the AIN channel. EXAZSEL[24]: AIN sampling time setting selection of AINx24 EXAZSEL[23]: AIN sampling time setting selection of AINx23 . . EXAZSEL[0]: AIN sampling time setting selection of AINx00 Others: Reserved

Note: This register must be set while ***[ADxCR0]***<ADEN> = 0.

5.2.14. *[ADxTRM]* (Trimming Setting Register)

Bit	Bit symbol	After reset	Type	Function
31:0	TRM[31:0]	0x00000000	R/W	The setting value of this register varies depending on the product. For the setting value, refer to the reference manual "Product Information".

Note: This register must be set while ***[ADxCR0]***<ADEN> = 0.

5.2.15. PMD Trigger Control Registers

5.2.15.1. *[ADxPSEL0]* (PMD Trigger Program Number Selection Register0)

The following is an example of ***[ADxPSEL0]***. ***[ADxPSEL1]*** to ***[ADxPSEL11]*** have the same configuration.

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0".
7	PENS0	0	R/W	PMDTRG0 trigger control (Note2) 0: Disabled. 1: Enabled.
6:3	-	0	R	Read as "0".
2:0	PMDS0[2:0]	000	R/W	Program number selection 000: Program 0 001: Program 1 010: Program 2 011: Program 3 100: Program 4 101: Program 5 110: Program 6 111: Program 7

Note1: This register must be set while ***[ADxCR0]***<ADEN> = 0.

Note2: For details of the PMD, refer to the reference manual "Advanced Programmable Motor Control Circuit" or "Programmable Motor Control Circuit Plus".

5.2.15.2. *[ADxPINTS0]* (PMD Trigger Interrupt Selection Register0)

The following is an example of ***[ADxPINTS0]***. ***[ADxPINTS1]*** to ***[ADxPINTS7]*** have the same configuration.

Bit	Bit symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1:0	INTSEL0[1:0]	00	R/W	Interrupt selection 00: No interrupts 01: INTADxPDA 10: INTADxPDB 11: Reserved This field selects an interrupt for the program 0.

Note: This register must be set while ***[ADxCR0]***<ADEN> = 0.

5.2.15.3. *[ADxPREGS]* (PMD Trigger Storage Selection Register)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as "0".
30:28	REGSEL7[2:0]	000	R/W	Program 7 conversion result storage register selection 000: ADxREG0 to 3 100: ADxREG16 to 19 001: ADxREG4 to 7 101: ADxREG20 to 23 010: ADxREG8 to 11 110: Inhibited setting. 011: ADxREG12 to 15 111: Inhibited setting.
27	-	0	R	Read as "0".
26:24	REGSEL6[2:0]	000	R/W	Program 6 conversion result storage register selection 000: ADxREG0 to 3 100: ADxREG16 to 19 001: ADxREG4 to 7 101: ADxREG20 to 23 010: ADxREG8 to 11 110: Inhibited setting. 011: ADxREG12 to 15 111: Inhibited setting.
23	-	0	R	Read as "0".
22:20	REGSEL5[2:0]	000	R/W	Program 5 conversion result storage register selection 000: ADxREG0 to 3 100: ADxREG16 to 19 001: ADxREG4 to 7 101: ADxREG20 to 23 010: ADxREG8 to 11 110: Inhibited setting. 011: ADxREG12 to 15 111: Inhibited setting.
19	-	0	R	Read as "0".
18:16	REGSEL4[2:0]	000	R/W	Program 4 conversion result storage register selection 000: ADxREG0 to 3 100: ADxREG16 to 19 001: ADxREG4 to 7 101: ADxREG20 to 23 010: ADxREG8 to 11 110: Inhibited setting. 011: ADxREG12 to 15 111: Inhibited setting.
15	-	0	R	Read as "0".
14:12	REGSEL3[2:0]	000	R/W	Program 3 conversion result storage register selection 000: ADxREG0 to 3 100: ADxREG16 to 19 001: ADxREG4 to 7 101: ADxREG20 to 23 010: ADxREG8 to 11 110: Inhibited setting. 011: ADxREG12 to 15 111: Inhibited setting.
11	-	0	R	Read as "0".
10:8	REGSEL2[2:0]	000	R/W	Program 2 conversion result storage register selection 000: ADxREG0 to 3 100: ADxREG16 to 19 001: ADxREG4 to 7 101: ADxREG20 to 23 010: ADxREG8 to 11 110: Inhibited setting. 011: ADxREG12 to 15 111: Inhibited setting.
7	-	0	R	Read as "0".
6:4	REGSEL1[2:0]	000	R/W	Program 1 conversion result storage register selection 000: ADxREG0 to 3 100: ADxREG16 to 19 001: ADxREG4 to 7 101: ADxREG20 to 23 010: ADxREG8 to 11 110: Inhibited setting. 011: ADxREG12 to 15 111: Inhibited setting.
3	-	0	R	Read as "0".
2:0	REGSEL0[2:0]	000	R/W	Program 0 conversion result storage register selection 000: ADxREG0 to 3 100: ADxREG16 to 19 001: ADxREG4 to 7 101: ADxREG20 to 23 010: ADxREG8 to 11 110: Inhibited setting. 011: ADxREG12 to 15 111: Inhibited setting.

Note: This register must be set while ***[ADxCR0]***<ADEN> = 0.

5.2.15.4. *[ADxPSET0]* (PMD Trigger Program Register0)

The following is an example of ***[ADxPSET0]***. ***[ADxPSET1]*** to ***[ADxPSET7]*** have the same configuration.

Bit	Bit symbol	After reset	Type	Function
31	ENSP03	0	R/W	Conversion 3 setting: Conversion control 0: Disabled. 1: Enabled.
30:29	-	00	R/W	Write as "00".
28:24	AINSP03[4:0]	00000	R/W	Conversion 3 setting: AIN selection (Note2) 00000: AINx00 01000: AINx08 10000: AINx16 11000: AINx24 00001: AINx01 01001: AINx09 10001: AINx17 00010: AINx02 01010: AINx10 10010: AINx18 00011: AINx03 01011: AINx11 10011: AINx19 00100: AINx04 01100: AINx12 10100: AINx20 00101: AINx05 01101: AINx13 10101: AINx21 00110: AINx06 01110: AINx14 10110: AINx22 00111: AINx07 01111: AINx15 10111: AINx23 Others: Inhibited setting
23	ENSP02	0	R/W	Conversion 2 setting: Conversion control 0: Disabled. 1: Enabled.
22:21	-	00	R/W	Write as "00".
20:16	AINSP02[4:0]	00000	R/W	Conversion 2 setting: AIN selection (Note2) 00000: AINx00 01000: AINx08 10000: AINx16 11000: AINx24 00001: AINx01 01001: AINx09 10001: AINx17 00010: AINx02 01010: AINx10 10010: AINx18 00011: AINx03 01011: AINx11 10011: AINx19 00100: AINx04 01100: AINx12 10100: AINx20 00101: AINx05 01101: AINx13 10101: AINx21 00110: AINx06 01110: AINx14 10110: AINx22 00111: AINx07 01111: AINx15 10111: AINx23 Others: Inhibited setting
15	ENSP01	0	R/W	Conversion 1 setting: Conversion control 0: Disabled. 1: Enabled.
14:13	-	00	R/W	Write as "00".
12:8	AINSP01[4:0]	00000	R/W	Conversion 1 setting: AIN selection (Note2) 00000: AINx00 01000: AINx08 10000: AINx16 11000: AINx24 00001: AINx01 01001: AINx09 10001: AINx17 00010: AINx02 01010: AINx10 10010: AINx18 00011: AINx03 01011: AINx11 10011: AINx19 00100: AINx04 01100: AINx12 10100: AINx20 00101: AINx05 01101: AINx13 10101: AINx21 00110: AINx06 01110: AINx14 10110: AINx22 00111: AINx07 01111: AINx15 10111: AINx23 Others: Inhibited setting
7	ENSP00	0	R/W	Conversion 0 setting: Conversion control 0: Disabled. 1: Enabled.
6:5	-	00	R/W	Write as "00".

Bit	Bit symbol	After reset	Type	Function
4:0	AINSP00[4:0]	00000	R/W	Conversion 0 setting: AIN selection (Note2) 00000: AINx00 01000: AINx08 10000: AINx16 11000: AINx24 00001: AINx01 01001: AINx09 10001: AINx17 00010: AINx02 01010: AINx10 10010: AINx18 00011: AINx03 01011: AINx11 10011: AINx19 00100: AINx04 01100: AINx12 10100: AINx20 00101: AINx05 01101: AINx13 10101: AINx21 00110: AINx06 01110: AINx14 10110: AINx22 00111: AINx07 01111: AINx15 10111: AINx23 Others: Inhibited setting

Note1: This register must be set while ***[ADxCR0]***<ADEN> = 0.

Note2: The AIN which the product does not have is inhibited to be set (refer to the reference manual "Product Information").

5.2.16. *[ADxTSET0]* (General Purpose Start-up Factor Program Register0)

The following is an example of ***[ADxTSET0]***. ***[ADxTSET1]*** to ***[ADxTSET23]*** have the same configuration.

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0".
7	ENINT0	0	R/W	Conversion Result Storage Register0 setting: Interrupt control 0: Disabled. 1: Enabled.
6:5	TRGS0[1:0]	00	R/W	Conversion Result Storage Register0 setting: Conversion control 00: No conversion 01: Continuous conversion 10: Single conversion 11: General purpose trigger conversion
4:0	AINST0[4:0]	00000	R/W	Conversion Result Storage Register0 setting: AIN selection (Note2) 00000: AINx00 01000: AINx08 10000: AINx16 11000: AINx24 00001: AINx01 01001: AINx09 10001: AINx17 00010: AINx02 01010: AINx10 10010: AINx18 00011: AINx03 01011: AINx11 10011: AINx19 00100: AINx04 01100: AINx12 10100: AINx20 00101: AINx05 01101: AINx13 10101: AINx21 00110: AINx06 01110: AINx14 10110: AINx22 00111: AINx07 01111: AINx15 10111: AINx23 Others: Inhibited setting

Note1: This register must be set while ***[ADxCR0]***<ADEN> = 0.

Note2: The AIN which the product does not have is inhibited to be set (refer to the reference manual "Product Information").

5.2.17. *[ADxREG0]* (Conversion Result Storage Register0)

The following is an example of ***[ADxREG0]***. ***[ADxREG1]*** to ***[ADxREG23]*** have the same configuration.

Bit	Bit symbol	After reset	Type	Function
31:30	-	0	R	Read as "0".
29	ADOVR_M0	0	R	Mirror bit of overrun flag <ADOVRF0>
28	ADRF_M0	0	R	Mirror bit of AD conversion result storage flag <ADRF0>
27:16	ADR_M0[11:0]	0x000	R	Mirror field of AD conversion result <ADR0[11:0]>. The AD conversion result is read from the lower 12 bits in the upper half word of ***[ADxREG0]*** register.
15:4	ADR0[11:0]	0x000	R	AD conversion result is stored. The AD conversion result is read from the upper 12 bits in the lower half word of ***[ADxREG0]*** register.
3:2	-	0	R	Read as "0".
1	ADOVRF0	0	R	Overrun flag 0: Not occurred. 1: Occurred. This flag is set to "1", when an AD conversion result is overwritten before the ***[ADxREG0]*** register is read. This flag is cleared to "0" when it is read.
0	ADRF0	0	R	AD conversion result storage flag 0: No conversion results are stored. 1: A conversion result is stored. This flag is set to "1" when an AD conversion value is stored. This flag is cleared to "0" when it is read.

6. Example of Usage

6.1. Single Conversion

The single conversion is started by software and enable more than one conversion.

In the following setting example, the conversion results of the two analog inputs (AINx02, AINx03) are saved in two result storage registers (***[ADxREG4]***, ***[ADxREG5]***), and a single conversion interrupt INTADxSGL is generated at the end of the second conversion.

- Initial setting
  - ***[ADxMOD0]*** = 0x00000001
    DAC ON: <DACON> = 1
    Normal operation: <RCUT> = 0
  - ***[ADxCLK]*** = 0x00000000
    Conversion Clock setting: Conversion time 1.5[µs] at 4.5[V] ≤ AVDD5 ≤ 5.5[V] / ADCLK = 40[MHz], SCLK = 20[MHz]
  - ***[ADxMOD1]*** = 0x00004000
    MODE setting 1: Conversion time 1.5[µs] at 4.5[V] ≤ AVDD5 ≤ 5.5[V] / ADCLK = 40[MHz], SCLK=20[MHz]
  - ***[ADxMOD2]*** = 0x00000300
    [ADxTRM] = 0x00034000

    Note: The setting value varies depending on the product. For the setting value, refer to the reference manual "Product Information".

- Conversion program setting
  - ***[ADxTSET4]*** = 0x00000042
    Single conversion: <TRGS4[1:0]> = 10
    AINx02: <AINST4[4:0]> = 00010
    Disable interrupt output: <ENINT4> = 0
  - ***[ADxTSET5]*** = 0x000000C3
    Single conversion: <TRGS5[1:0]> = 10
    AINx03: <AINST5[4:0]> = 00011
    Enable interrupt output: <ENINT5> = 1

- Conversion start setting
  - ***[ADxCR1]*** = 0x00000000
    Disable DMA request
  - ***[ADxCR0]*** = 0x00000082
    Enable ADC: <ADEN> = 1
    Disable continuous conversion: <CNT> = 0
    Enable single conversion: <SGL> = 1 ; Conversion start

6.2. PMD Trigger Conversion

6.2.1. PMD (3-shunt), ADC × 1

The following shows the connection diagram in which PMD channel 0 and ADC unit A are used in 3-shunt.

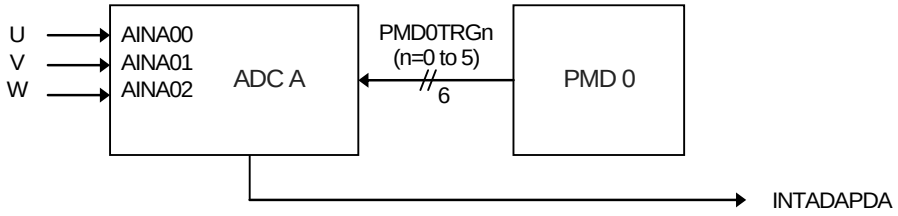


Figure 6.1 3-shunt Example

The setting example for the ADC is as follows in this case:

Table 6.1 ADC Setting in 3-shunt

Program	0	1	2	3	4	5
Reg0	U	V	W	V	W	U
Reg1	V	W	U	U	V	W
INT	INTADAPDA	INTADAPDA	INTADAPDA	INTADAPDA	INTADAPDA	INTADAPDA

The 6 trigger inputs PMD0TRG0 to 5 are assigned to the programs 0 to 5 by ***[ADAPSEL0]*** to ***[ADAPSEL5]***. Reg0 and Reg1 in the table represent ***[ADAPSETn]***[7:0] and ***[ADAPSETn]***[15:8] (n: Program number), respectively. U, V, and W in the table are the motor phases. The corresponding AIN input should be selected for each phase.

When the trigger is received, the AD conversion starts and the execution is done in the order of Reg0 and Reg1. Each conversion result is stored to the conversion result storage register, and the INTADAPDA interrupt is generated.

6.2.2. PMD (1-shunt), ADC × 1

The following shows the connection diagram in which PMD channel 0 and ADC unit A are used in 1-shunt.

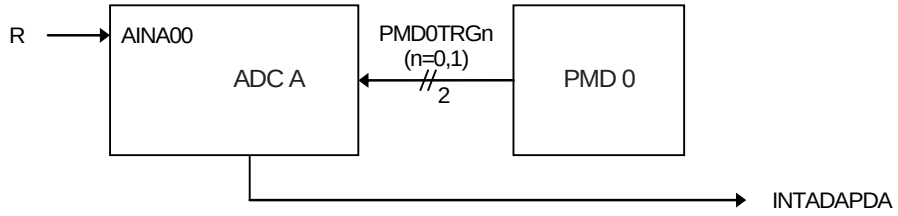


Figure 6.2 1-shunt Example

The setting example for the ADC is as follows in this case:

Table 6.2 ADC Setting in 1-shunt

Trigger	PMD0	PMD0
	0	1
Program	0	1
Reg0	R	-
Reg1	-	R
INT	-	INTADAPDA

The two trigger signals from PMD0 are assigned to the program numbers.

Reg0 and Reg1 in the table represent ***[ADAPSETn]***[7:0] and ***[ADAPSETn]***[15:8] (n: Program number), respectively. R in the table is a resistor. It is connected to the corresponding AIN.

When the trigger is received, ADC unit A starts and the conversion result is stored to the conversion result storage register0 and 1. The conversion executes in the order of the program0 and 1. The INTADAPDA interrupt is generated at the conversion completion.

7. Precaution

- The AD conversion result may have some variation due to the fluctuation of the power supply and surrounding noises. The data of the output pins should not be changed during AD conversion to prevent from degrading the AD conversion accuracy. The AD conversion accuracy may degrade if the signal on the shared pin with the AD input/output changes or other output pin changes its output during the AD conversion. In the above case, the AD conversion result should be acquired with the mean value of multiple conversion results and other countermeasures.

- Measures should be taken to prevent digital noise from mixing into the analog power supply pins (AVDD5, AVSS) and the reference voltage pins (VREFHx, VREFLx) of the ADC.

  – Insert a bypass capacitor between AVDD5 and AVSS pins, the VREFHx and VREFLx pins. Place the capacitor as close to the terminal as possible.

8. Revision History

Table 8.1 Revision History

Revision	Date	Description
1.0	2021-01-15	- First release
1.1	2021-03-22	- 3.8.2. Setting of Sampling time Modified description. - Corrected Figure 4.1. - 5.1. List of Registers Added Trimming Setting Register (***[ADxTRM]***) - 5.2.14. ***[ADxTRM]*** (Trimming Setting Register) Added this section. - 6.1. Single conversion Added ***[ADxTRM]*** setting in initial setting.
1.2	2021-05-28	- Outlines Corrected description. - Figure 2.1 ADC block diagram Added AINx27. - Table 2.1 List of Signals AINx27 is added in Signal symbol column of No.2. - 5.2.13. ***[ADxEXAZSEL]*** (AIN sampling time selection Register) Added EXAZSEL[27]. - ***[ADxTSET0]*** (General Purpose Start-up Factor Program Register0) Added the value 11011 in AINST0[4:0].
1.3	2023-01-17	- 1. Outline Deleted AINx27. Corrected from AINx23 to AINx24. - Figure 2.1 ADC block diagram Deleted AINx27. Corrected from AINx23 to AINx24. - Table 2.1 List of Signals AINx27 is deleted in Signal symbol column of No.2. Corrected from AINx23 to AINx24 in Signal symbol column of No.2. - 5.2.13. ***[ADxEXAZSEL]*** (AIN sampling time selection Register) Deleted EXAZSEL[27]. Added EXAZSEL[24]. - 5.2.15.4. ***[ADxPSET0]*** (PMD Trigger Program Register0) Added AINx24. - 5.2.16. ***[ADxTSET0]*** (General Purpose Start-up Factor Program Register0) Corrected from "11011:AINx27" to "11000:AINx24" in AINST0[4:0].
1.4	2025-12-05	- Appearance update - 1. Outlines Changed table - 3.2.1. Operation Changed description

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as "TOSHIBA".
Hardware, software and systems described in this document are collectively referred to as "Product".

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**