

# TC74HC74AP, TC74HC74AF

## Dual D-Type Flip Flop Preset and Clear

The TC74HC74A is a high speed CMOS D FLIP FLOP fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CLOCK pulse.

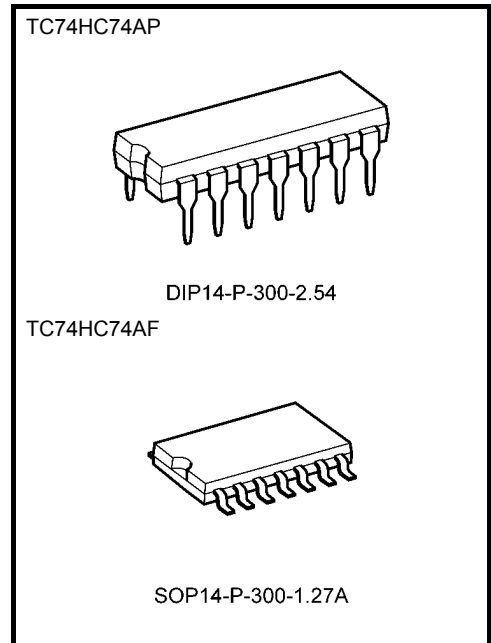
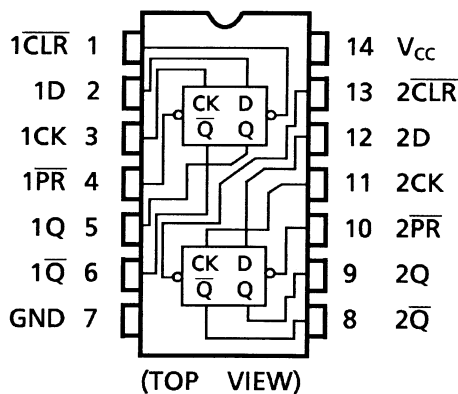
$\overline{\text{CLEAR}}$  and  $\overline{\text{PRESET}}$  are independent of the CLOCK and are accomplished by setting the appropriate input to an "L" level.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

- High speed:  $f_{\text{max}} = 77 \text{ MHz (typ.)}$  at  $V_{\text{CC}} = 5 \text{ V}$
- Low power dissipation:  $I_{\text{CC}} = 2 \mu\text{A (max)}$  at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}} \text{ (min)}$
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance:  $|I_{\text{OH}}| = I_{\text{OL}} = 4 \text{ mA (min)}$
- Balanced propagation delays:  $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide operating voltage range:  $V_{\text{CC}} \text{ (opr)} = 2 \text{ to } 6 \text{ V}$
- Pin and function compatible with 74LS74

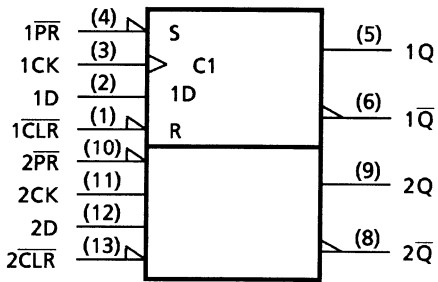
### Pin Assignment



Weight	
DIP14-P-300-2.54	: 0.96 g (typ.)
SOP14-P-300-1.27A	: 0.18 g (typ.)

Start of commercial production  
1986-05

## IEC Logic Symbol

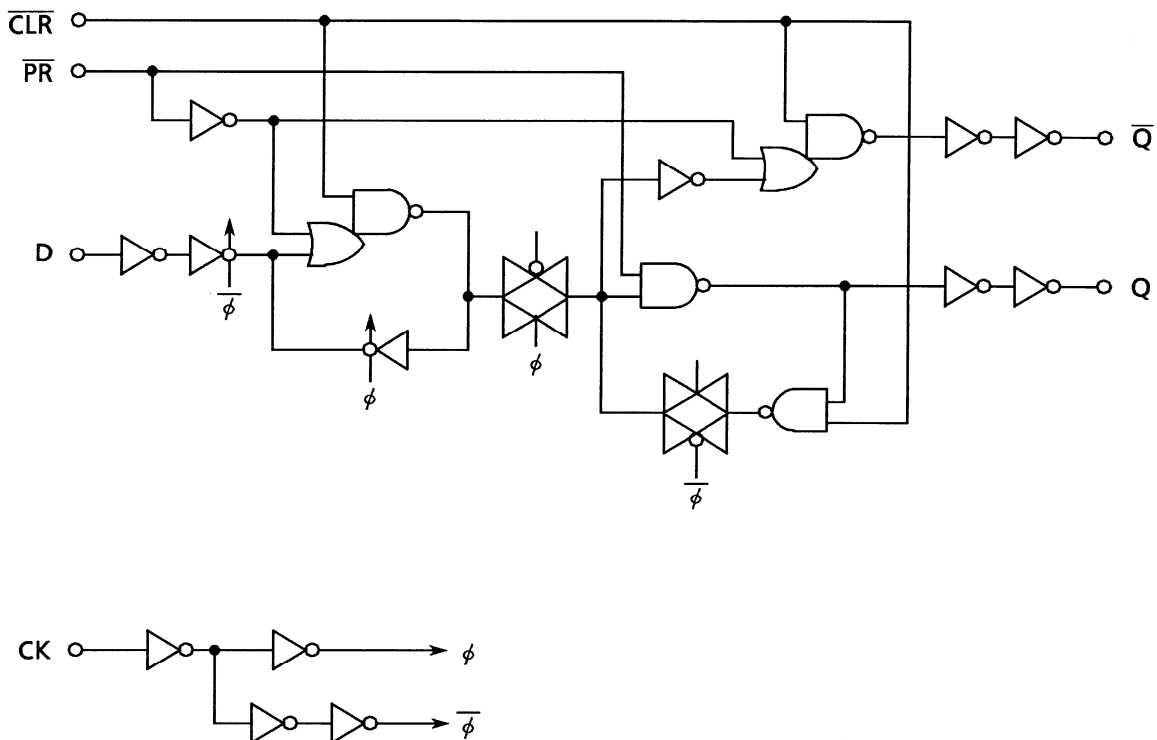


## Truth Table

Inputs				Outputs		Function
CLR	PR	D	CK	Q	Q-bar	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q <sub>n</sub>	Q <sub>n</sub> -bar	No Change

X: Don't care

## System Diagram



## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 50$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^{\circ}C$ . From  $T_a = 65$  to  $85^{\circ}C$  a derating factor of  $-10$  mW/ $^{\circ}C$  shall be applied until 300 mW.

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2 to 6	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}C$
Input rise and fall time	$t_r, t_f$	0 to 1000 ( $V_{CC} = 2.0$ V) 0 to 500 ( $V_{CC} = 4.5$ V) 0 to 400 ( $V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit		
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max	
High-level input voltage	V <sub>IH</sub>	—		2.0	1.50	—	—	1.50	—	V	
				4.5	3.15	—	—	3.15	—		
				6.0	4.20	—	—	4.20	—		
Low-level input voltage	V <sub>IL</sub>	—		2.0	—	—	0.50	—	0.50	V	
				4.5	—	—	1.35	—	1.35		
				6.0	—	—	1.80	—	1.80		
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2.0	1.9	2.0	—	1.9	—	V	
				4.5	4.4	4.5	—	4.4	—		
				6.0	5.9	6.0	—	5.9	—		
			I <sub>OH</sub> = -4 mA	4.5	4.18	4.31	—	4.13	—		
				6.0	5.68	5.80	—	5.63	—		
				I <sub>OH</sub> = -5.2 mA	4.5	—	0.0	0.1	—		0.1
6.0	—	0.0	0.1		—	0.1					
6.0	—	0.0	0.1		—	0.1					
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2.0	—	0.0	0.1	—	0.1	V	
				4.5	—	0.0	0.1	—	0.1		
				6.0	—	0.0	0.1	—	0.1		
			I <sub>OL</sub> = 4 mA	4.5	—	0.17	0.26	—	0.33		
				6.0	—	0.18	0.26	—	0.33		
				I <sub>OL</sub> = 5.2 mA	4.5	—	—	—	—		—
6.0	—	—	—		—	—					
6.0	—	—	—		—	—					
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	2.0	—	20.0	μA	

### Timing Requirements (input: $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Unit	
			V <sub>CC</sub> (V)	Typ.	Limit		Limit
Minimum pulse width (CK)	$t_W$ (L) $t_W$ (H)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ )	$t_W$ (L)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time	$t_s$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum hold time	$t_h$	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ )	$t_{\text{rem}}$	—	2.0	—	25	30	ns
			4.5	—	5	6	
			6.0	—	4	5	
Clock frequency	f	—	2.0	—	6	5	MHz
			4.5	—	31	25	
			6.0	—	36	29	

### AC Characteristics (C<sub>L</sub> = 15 pF, V<sub>CC</sub> = 5 V, Ta = 25°C, input: $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{\text{TLH}}$	—	—	6	12	ns
	$t_{\text{THL}}$					
Propagation delay time (CK-Q, $\overline{\text{Q}}$ )	$t_{\text{pLH}}$	—	—	13	26	ns
	$t_{\text{pHL}}$					
Propagation delay time ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ -Q, $\overline{\text{Q}}$ )	$t_{\text{pLH}}$	—	—	14	26	ns
	$t_{\text{pHL}}$					
Maximum clock frequency	$f_{\text{max}}$	—	36	77	—	MHz

### AC Characteristics (C<sub>L</sub> = 50 pF, input: t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to 85°C		Unit
				Min	Typ.	Max	Min	Max	
Output transition time	t <sub>TLH</sub> t <sub>THL</sub>	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (CK-Q, $\bar{Q}$ )	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	48	150	—	190	ns
			4.5	—	16	30	—	38	
			6.0	—	13	26	—	32	
Propagation delay time ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ -Q, $\bar{Q}$ )	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	51	150	—	190	ns
			4.5	—	17	30	—	38	
			6.0	—	15	26	—	32	
Maximum clock frequency	f <sub>max</sub>	—	2.0	6	21	—	5	—	MHz
			4.5	31	63	—	25	—	
			6.0	36	67	—	29	—	
Input capacitance	C <sub>IN</sub>	—	—	5	10	—	10	pF	
Power dissipation capacitance	C <sub>PD</sub>	(Note)	—	34	—	—	—	pF	

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

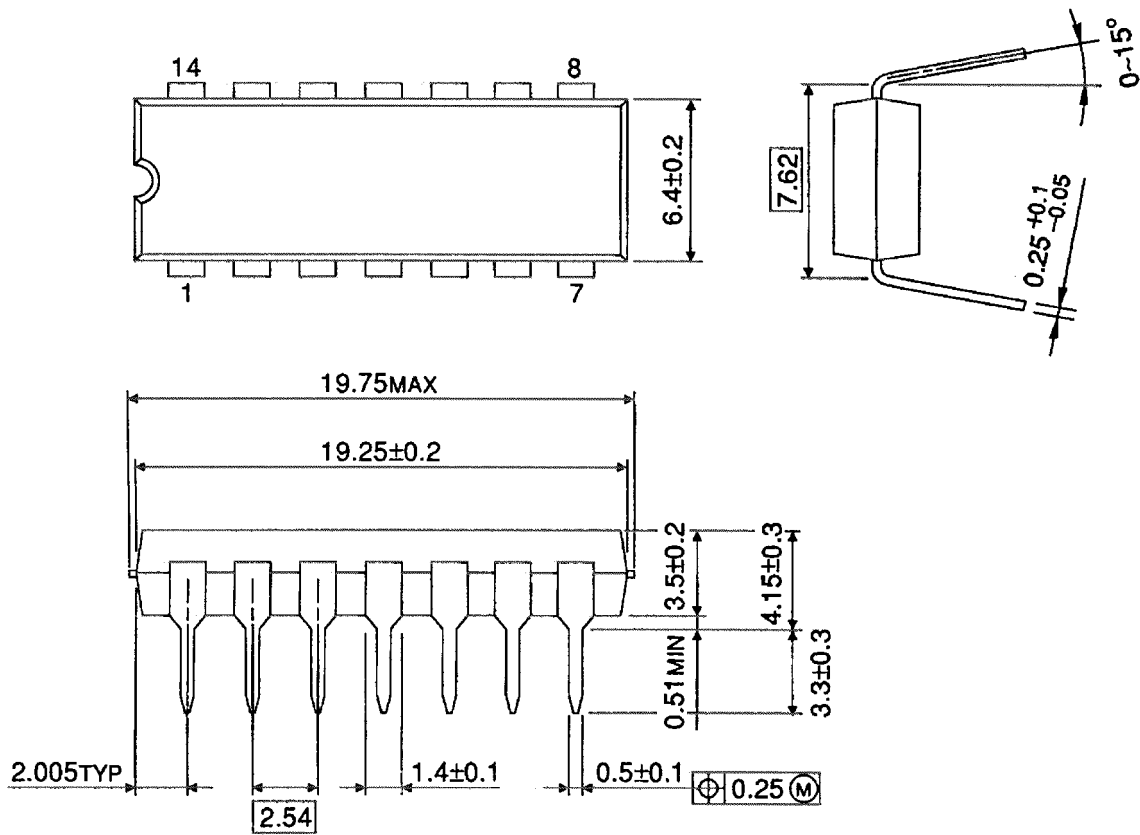
Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

## Package Dimensions

DIP14-P-300-2.54

Unit : mm

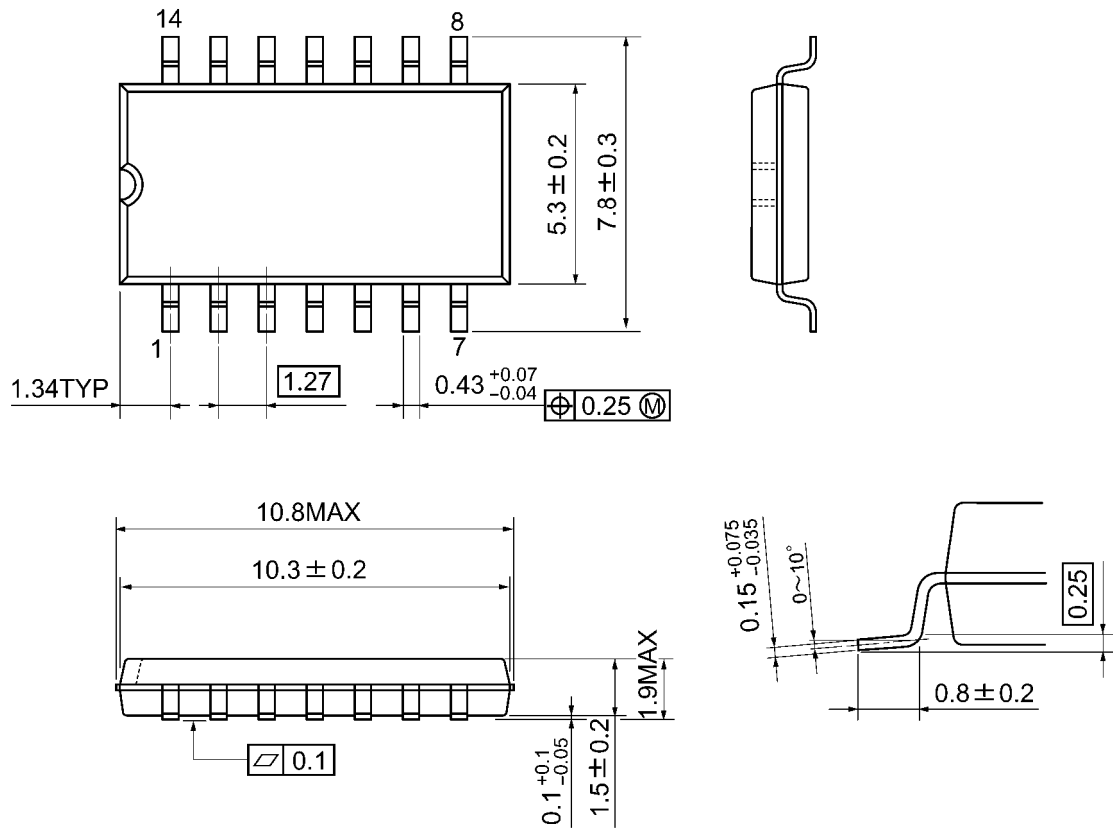


Weight: 0.96 g (typ.)

## Package Dimensions

SOP14-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

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