

MOSFETs Silicon N-Channel MOS (DTMOSVI)

# TK058V60Z5

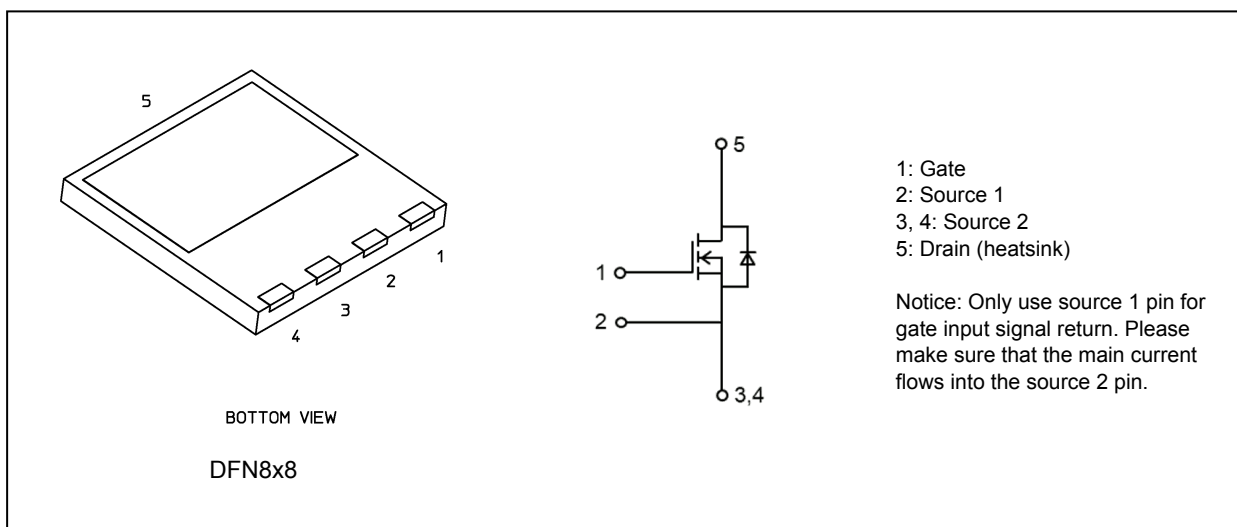
## 1. Applications

- Switching Voltage Regulators

## 2. Features

- (1) Fast reverse recovery time:  $t_{rr} = 140 \text{ ns}$  (typ.)
- (2) Low drain-source on-resistance:  $R_{DS(ON)} = 0.050 \Omega$  (typ.)
- (3) High-speed switching properties with the lower capacitance.
- (4) Enhancement mode:  $V_{th} = 3.5 \text{ to } 4.5 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 1.69 \text{ mA}$ )

## 3. Packaging and Internal Circuit



Start of commercial production  
2025-12

## 4. Absolute Maximum Ratings (Note) ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	600	V
Gate-source voltage	$V_{GSS}$	$\pm 30$	
Drain current (DC) (Note 1)	$I_D$	40	A
Drain current (pulsed) (Note 1)	$I_{DP}$	160	
Power dissipation ( $T_c = 25\text{ }^\circ\text{C}$ )	$P_D$	270	W
Single-pulse avalanche energy (Note 2)	$E_{AS}$	901	mJ
Single-pulse avalanche current	$I_{AS}$	6	A
Reverse drain current (DC) (Note 1)	$I_{DR}$	40	
Reverse drain current (pulsed) (Note 1)	$I_{DRP}$	160	
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## 5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	0.462	$^\circ\text{C/W}$

Note 1: Ensure that the channel temperature does not exceed  $150\text{ }^\circ\text{C}$ .

Note 2:  $V_{DD} = 90\text{ V}$ ,  $T_{ch} = 25\text{ }^\circ\text{C}$  (initial),  $L = 44.3\text{ mH}$ ,  $I_{AS} = 6\text{ A}$

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

## 6. Electrical Characteristics

### 6.1. Static Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$ , $V_{DS} = 0\text{ V}$	—	—	$\pm 1$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = 600\text{ V}$ , $V_{GS} = 0\text{ V}$	—	—	100	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}$ , $V_{GS} = 0\text{ V}$	600	—	—	V
Gate threshold voltage	$V_{th}$	$V_{DS} = 10\text{ V}$ , $I_D = 1.69\text{ mA}$	3.5	—	4.5	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}$ , $I_D = 15\text{ A}$	—	0.050	0.058	$\Omega$

## 6.2. Dynamic Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = 300\text{ V}, V_{GS} = 0\text{ V}, f = 100\text{ kHz}$	—	3750	—	pF
Reverse transfer capacitance	$C_{rss}$		—	3.2	—	
Output capacitance	$C_{oss}$		—	85	—	
Effective output capacitance (energy related) (Note 3)	$C_{o(er)}$	$V_{DS} = 0\text{ to }400\text{ V}, V_{GS} = 0\text{ V}$	—	140	—	
Effective output capacitance (time related) (Note 4)	$C_{o(tr)}$		—	1020	—	
Gate resistance	$r_g$	$V_{DS} = \text{OPEN}, f = 1\text{ MHz}$	—	2.6	—	$\Omega$
Switching time (rise time)	$t_r$	See Fig. 6.2.1	—	24	—	ns
Switching time (turn-on time)	$t_{on}$		—	61	—	
Switching time (fall time)	$t_f$		—	4.3	—	
Switching time (turn-off time)	$t_{off}$		—	110	—	
MOSFET dv/dt ruggedness	dv/dt	$V_{DS} \leq V_{DSS}, I_D \leq 20\text{ A}$	110	—	—	V/ns

Note 3:  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to 400 V.

Note 4:  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to 400 V.

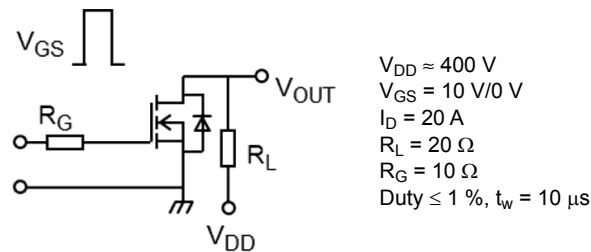


Fig. 6.2.1 Switching Time Test Circuit

## 6.3. Gate Charge Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} \approx 400\text{ V}, V_{GS} = 10\text{ V}, I_D = 40\text{ A}$	—	66	—	nC
Gate-source charge 1	$Q_{gs1}$		—	23	—	
Gate-drain charge	$Q_{gd}$		—	20	—	

## 6.4. Source-Drain Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage	$V_{DSF}$	$I_{DR} = 40\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.7	V
Reverse recovery time (Note 5)	$t_{rr}$	$V_{DD} = 400\text{ V},$ $I_{DR} = 20\text{ A}, V_{GS} = 0\text{ V}$ $-dI_{DR}/dt = 100\text{ A}/\mu\text{s}$	—	140	224	ns
Reverse recovery charge	$Q_{rr}$		—	0.87	—	$\mu\text{C}$
Peak reverse recovery current	$I_{rr}$		—	12.5	—	A
Diode dv/dt ruggedness	dv/dt	$V_{DD} \leq 400\text{ V}, I_{DR} \leq 20\text{ A}, V_{GS} = 0\text{ V}$	70	—	—	V/ns

Note 5: Defined by design.

## 7. Marking

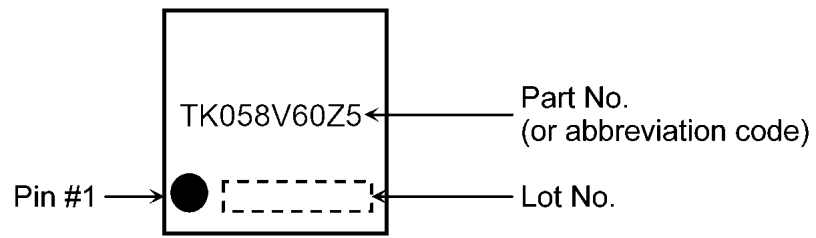


Fig. 7.1 Marking

## 8. Characteristics Curves (Note)

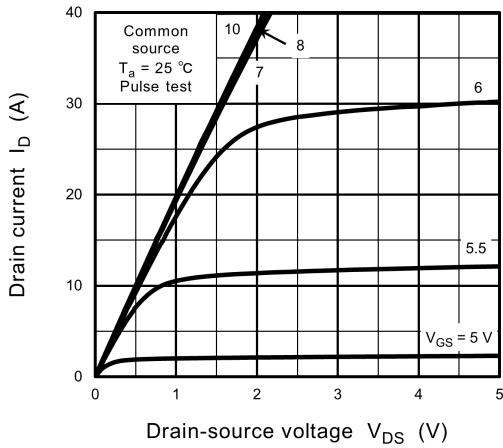


Fig. 8.1  $I_D - V_{DS}$

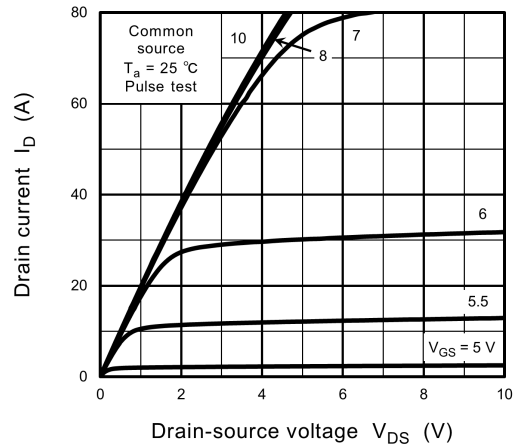


Fig. 8.2  $I_D - V_{DS}$

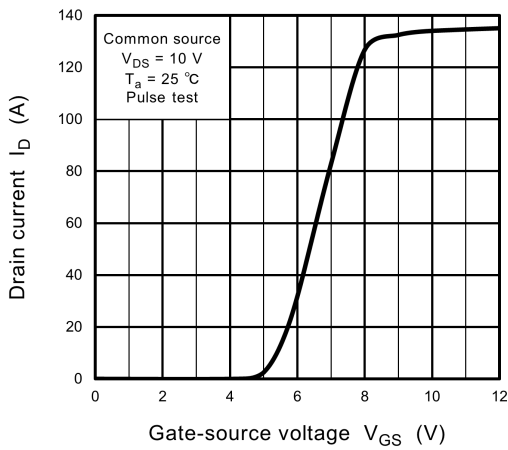


Fig. 8.3  $I_D - V_{GS}$

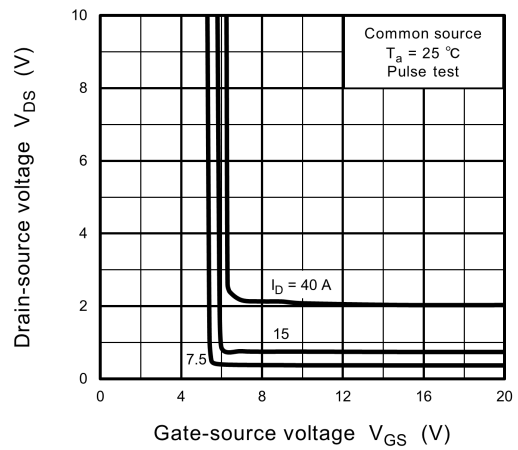


Fig. 8.4  $V_{DS} - V_{GS}$

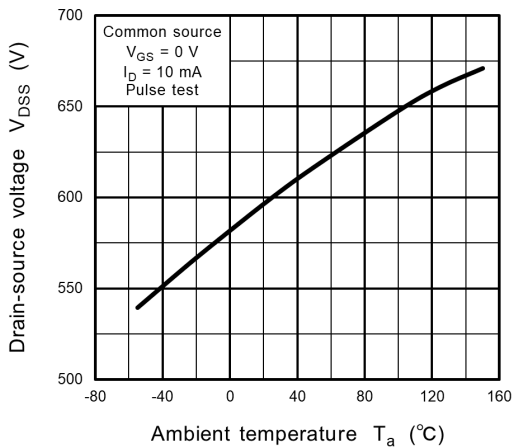


Fig. 8.5  $V_{DSS} - T_a$

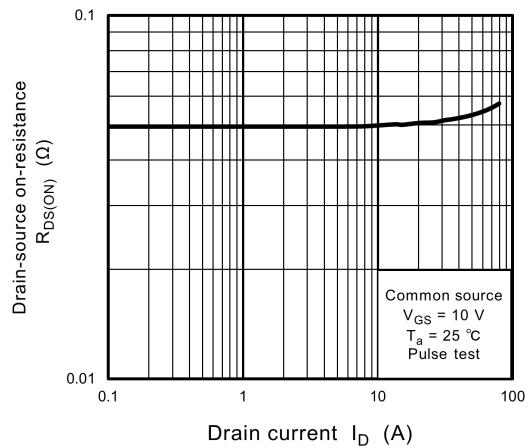
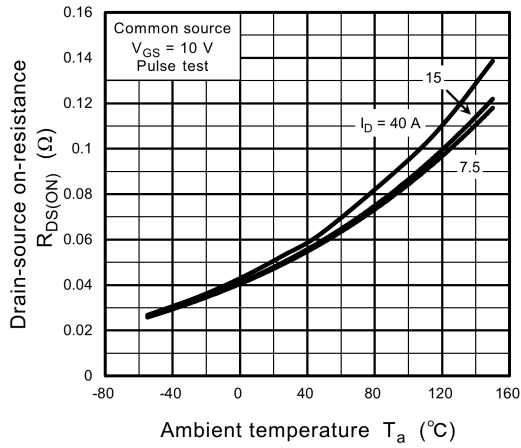
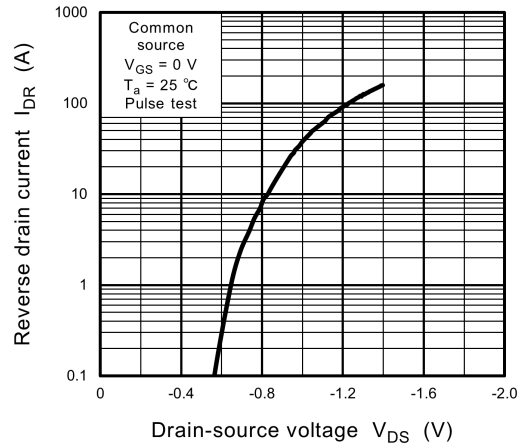


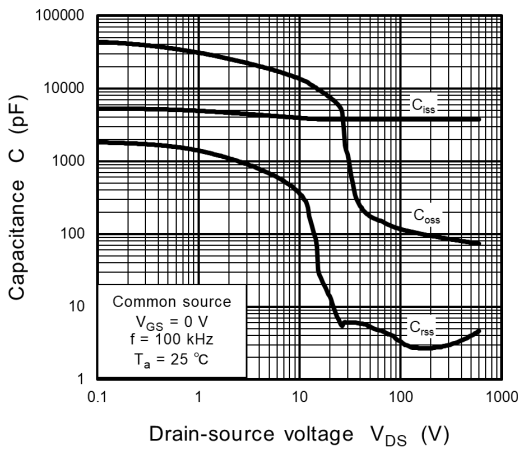
Fig. 8.6  $R_{DS(ON)} - I_D$



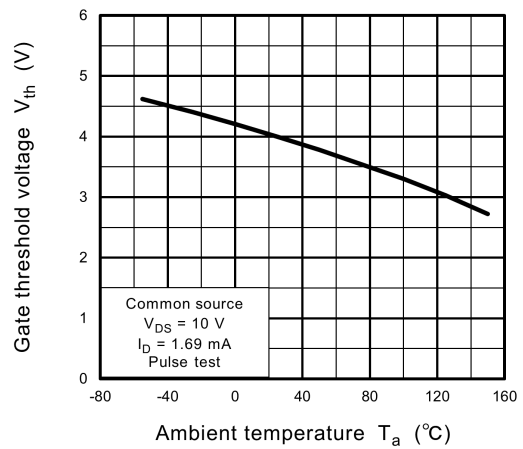
**Fig. 8.7**  $R_{DS(ON)} - T_a$



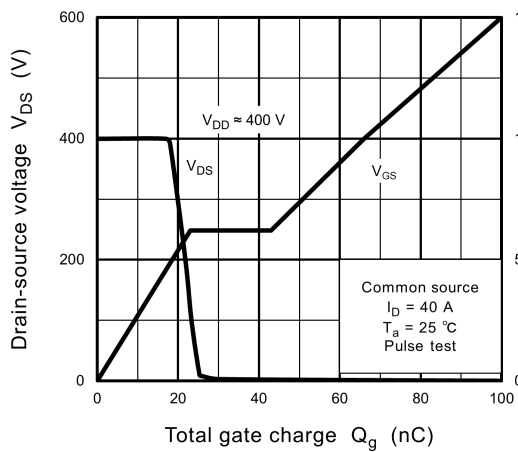
**Fig. 8.8**  $I_{DR} - V_{DS}$



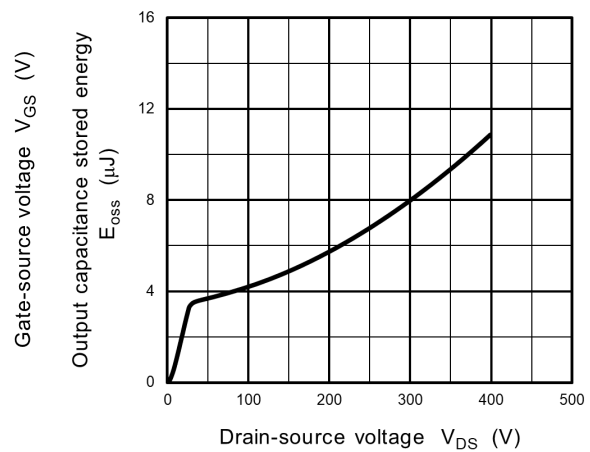
**Fig. 8.9**  $C - V_{DS}$



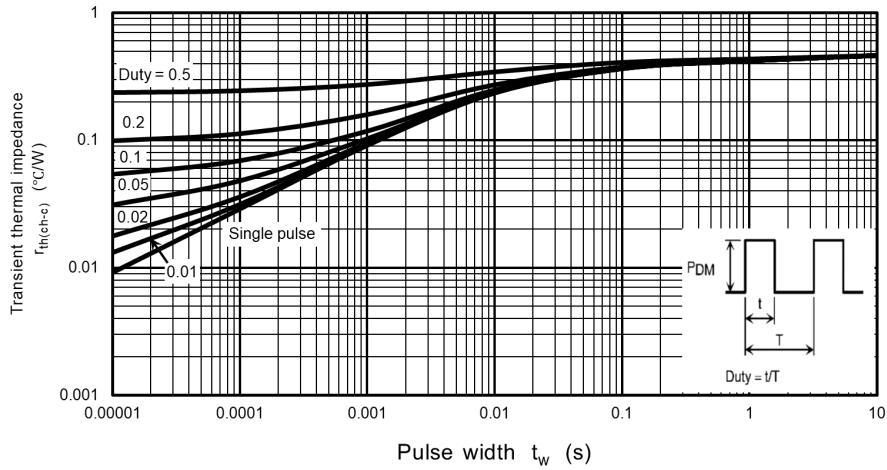
**Fig. 8.10**  $V_{th} - T_a$



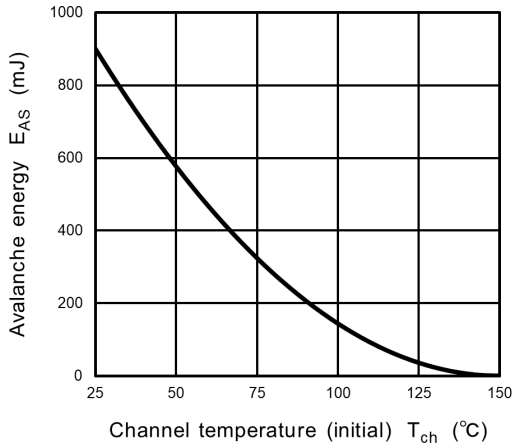
**Fig. 8.11** Dynamic Input/Output Characteristics



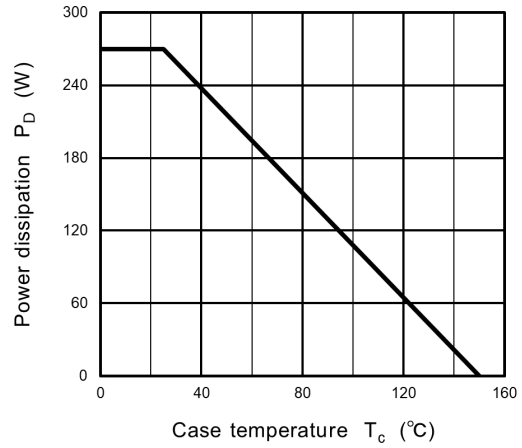
**Fig. 8.12**  $E_{oss} - V_{DS}$



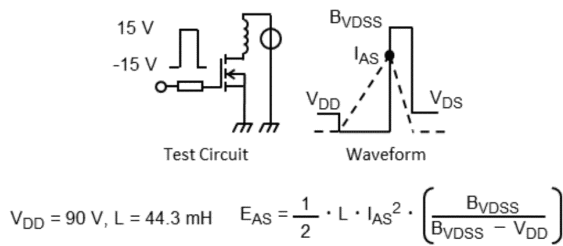
**Fig. 8.13  $r_{th} - t_w$**   
(Guaranteed Maximum)



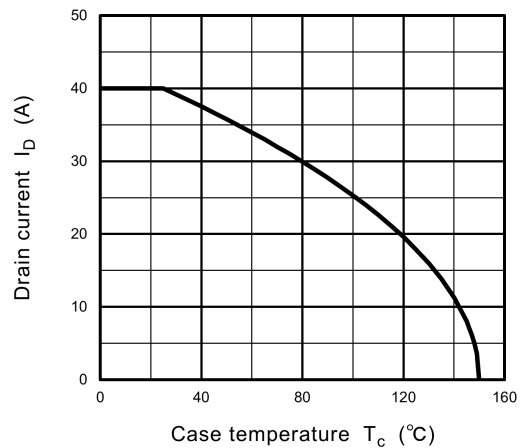
**Fig. 8.14  $E_{AS} - T_{ch}$**   
(Guaranteed Maximum)



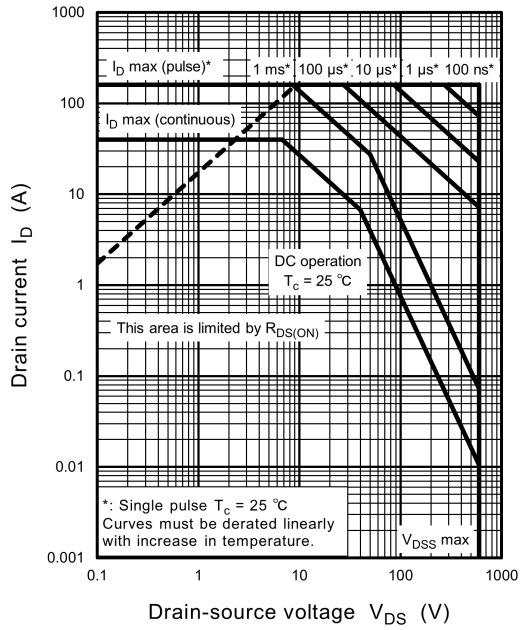
**Fig. 8.15  $P_D - T_c$**   
(Guaranteed Maximum)



**Fig. 8.16 Test Circuit/Waveform**



**Fig. 8.17  $I_D - T_c$**   
(Guaranteed Maximum)



**Fig. 8.18 Safe Operating Area (Guaranteed Maximum)**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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