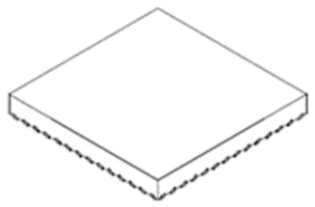
Bi-CMOS Linear Integrated Circuit Silicon Monolithic

TB9M001FTG

Automotive IC for DC motors with integrated microcontroller.

1. Description

The TB9M001FTG is an integrated IC with a microcontroller unit (MCU) for automotive applications, which incorporates an Arm® Cortex®-M0 Processor, a relay driver, and a LIN transceiver. This IC features a power supply system that operates at vehicle battery voltage levels, making it suitable for DC motor applications using external relays.It also includes large-capacity code flash and data flash memory, allowing it to function as a LIN-controlled secondary device.The TB9M001FTG can be configured to transition to Standby mode in the idle state to reduce power consumption.



P-VQFN48-0707-0.50-005

Weight: 0.13 g (typ.)

2. Applications

For automotive (electric sunroof, electric wiper, power window, power seat) LIN-controlled secondary device applications.

3. Features

- Integrated MCU, relay drivers, and automotive power supply system enable downsizing of the system
- Built-in LIN transceiver

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Start of commercial production
2025-12

4. Functions

- Arm® Cortex®-M0 Processor
  - SerialWireDebugSupport
  - 32ch Interrupt Controller
  - 1 cycle multiplier
  - Up to 40MHz clock frequency
- 12KBytes ROM (BootLoader, Flash API) (incECCSEC/DED)
- 192KBytes Code Flash (incECCSEC/DED)
- 16KBytes Data Flash (incECCSEC/DED)
- 32-bit Compare timers (DTIMER)
- 28-bit Capture timer (8 inputs, 6 measurement)
- WATCHDOG
- Power saving modes (CPU Sleep, Standby, CWU)
- 4 Legacy PWM Generator
- 14 General-purpose I/O Ports (GPIO)
- 10-bit A/D Converter (GADC) with 13 analog inputs (ADIN0-7、SWIN0-4) + internal temperature, VB, VCC
- 4 Low Side Drivers (LSD0-3)
- High Side Drivers (HSD0, HSD1)
- 9 High Voltage Input (SWIN0-4 + HPIN0-3)
- LDOs (LDO5V, LDO15V)
- Power On Reset (POR5V, PORL)
- 2 on-chip OSCs (IOSCH, IOSCL)
- External OSC
- PLL
- LIN ISO17987/SAEJ2602 transceiver + controller
- 2 full duplex serial interfaces (UART1, UART2), UART1 with LIN support
- SPI-I/F
- Thermal Shutdown (TSD)
- Package P-VQFN48-0707-0.50
- Single power supply from 6.0V to 18V
- Temperature Range Tj: -40 up to 150°C
- Green package (RoHS compliant)
- AEC-Q100 grade 1 Qualified

5. Block Diagram

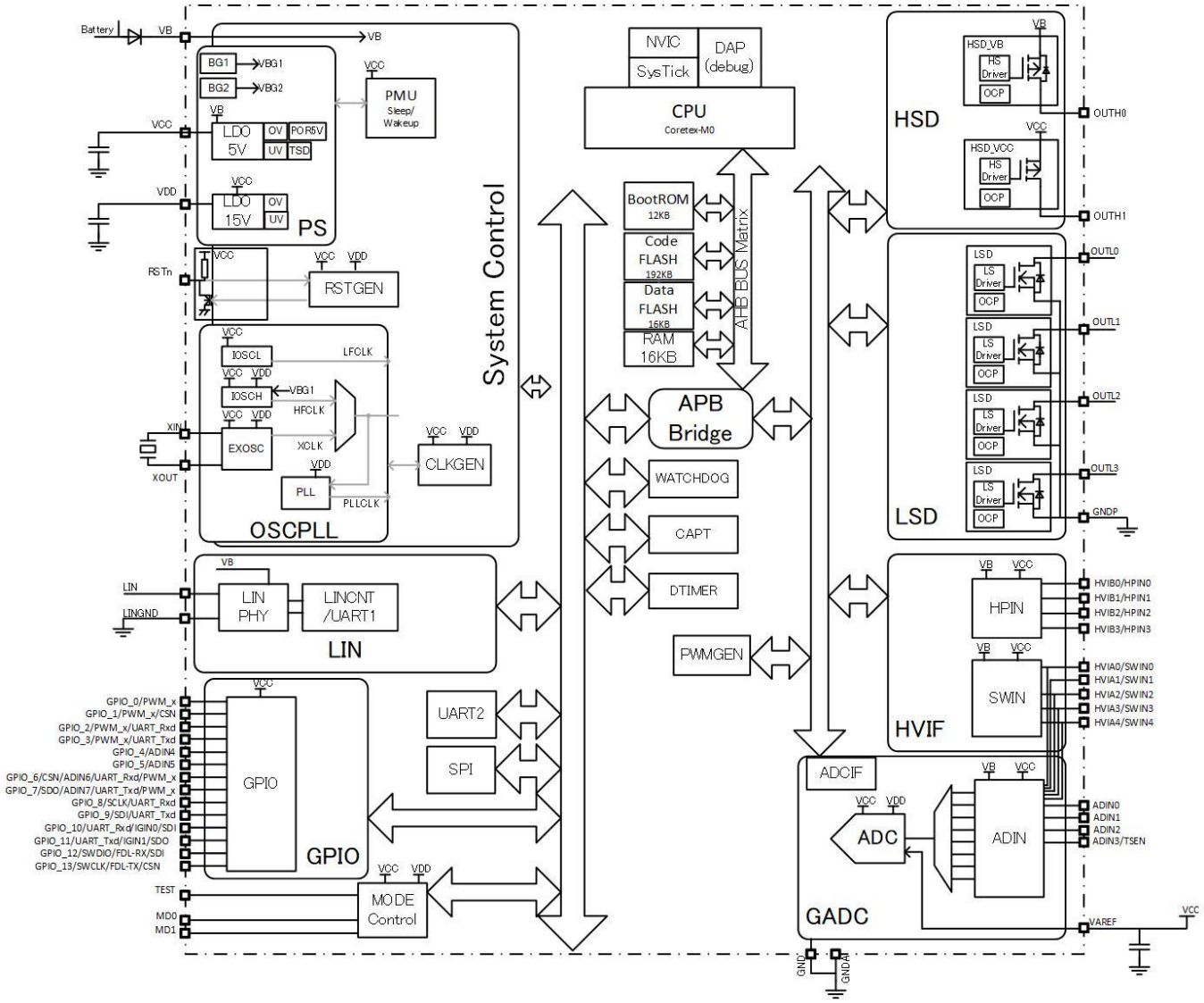


Figure 5.1 Block Diagram

6. Pin Assignments

(Top view)

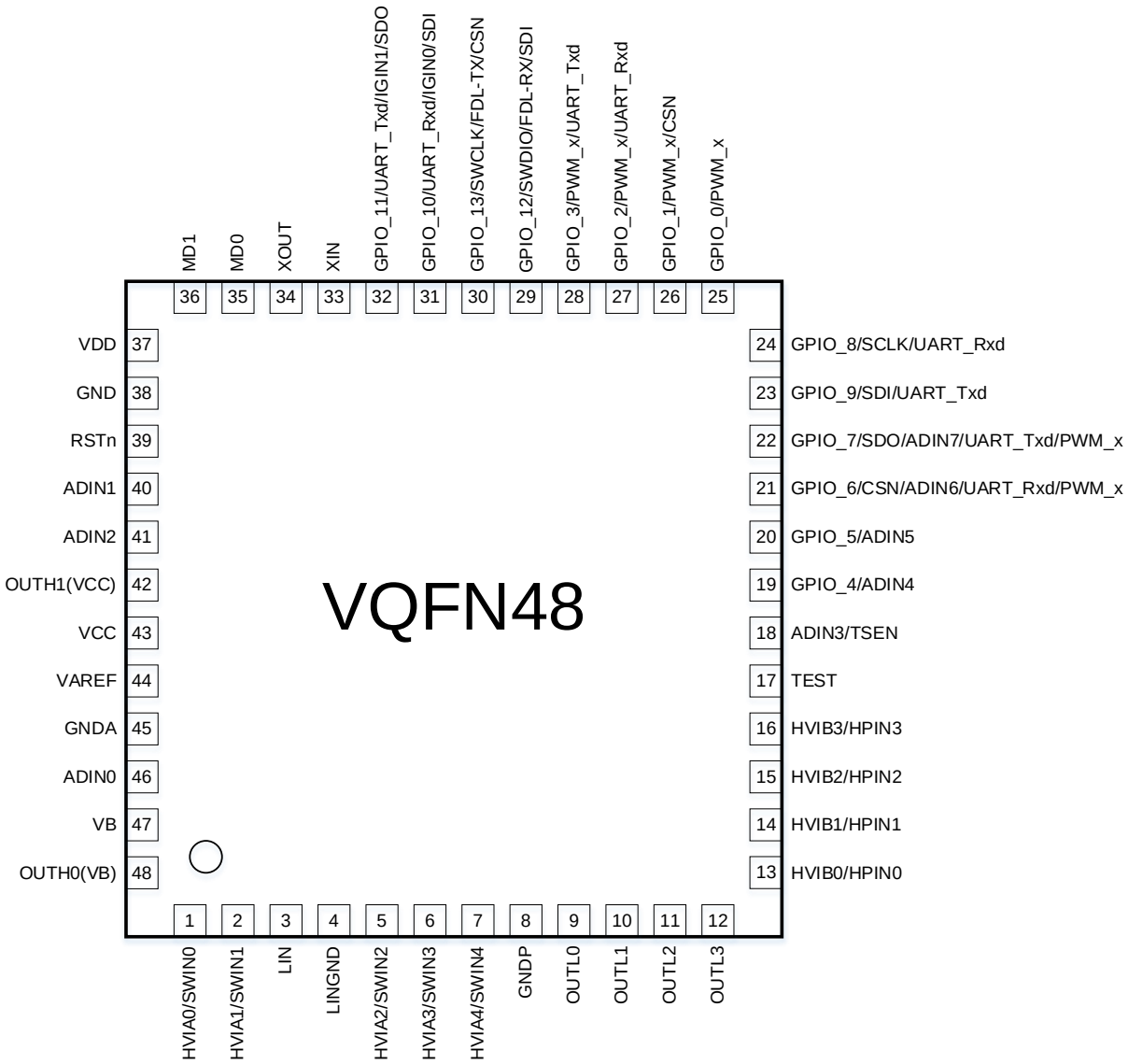


Figure 6.1 Pin Assignment Diagram

7. Pin Description

Table 7.1 Pin Description

Pin No.	Pin Name	I/O	Description
1	HVIA0/SWIN0	I	High-voltage logic input/switch input
2	HVIA1/SWIN1	I	High-voltage logic input/switch input
3	LIN	I/O	LIN communication pin
4	LINGND	-	LIN ground
5	HVIA2/SWIN2	I	High-voltage logic input/switch input
6	HVIA3/SWIN3	I	High-voltage logic input/switch input
7	HVIA4/SWIN4	I	High-voltage logic input/switch input
8	GNDP	-	Ground (for LSD)
9	OUTL0	O	Low-side driver output
10	OUTL1	O	Low-side driver output
11	OUTL2	O	Low-side driver output
12	OUTL3	O	Low-side driver output
13	HVIB0/HPIN0	I	High-voltage logic input/hall sensor input
14	HVIB1/HPIN1	I	High-voltage logic input/hall sensor input
15	HVIB2/HPIN2	I	High-voltage logic input/hall sensor input
16	HVIB3/HPIN3	I	High-voltage logic input/hall sensor input
17	TEST	I	Test mode select
18	ADIN3/TSEN	I	ADC input/temperature monitor
19	GPIO_4/ADIN4	I/O	General-purpose I/O port
20	GPIO_5/ADIN5	I/O	General-purpose I/O port
21	GPIO_6/CSN/ADIN6/UART_Rxd/PWM_x	I/O	General-purpose I/O port
22	GPIO_7/SDO/ADIN7/UART_Txd/PWM_x	I/O	General-purpose I/O port
23	GPIO_9/SDI/UART_Txd	I/O	General-purpose I/O port
24	GPIO_8/SCLK/UART_Rxd	I/O	General-purpose I/O port
25	GPIO_0/PWM_x	I/O	General-purpose I/O port
26	GPIO_1/PWM_x/CSN	I/O	General-purpose I/O port
27	GPIO_2/PWM_x/UART_Rxd	I/O	General-purpose I/O port
28	GPIO_3/PWM_x/UART_Txd	I/O	General-purpose I/O port
29	GPIO_12/SWDIO/FDL-RX/SDI	I/O	General-purpose I/O port
30	GPIO_13/SWCLK/FDL-TX/CSN	I/O	General-purpose I/O port
31	GPIO_10/UART_Rxd/IGIN0/SDI	I/O	General-purpose I/O port
32	GPIO_11/UART_Txd/IGIN1/SDO	I/O	General-purpose I/O port
33	XIN	I	External oscillator connection
34	XOUT	O	External oscillator connection
35	MD0	I	Mode selects
36	MD1	I	Mode selects
37	VDD	-	1.5-volt regulator output
38	GND	-	Ground
39	RSTn	I/O	Reset I/O
40	ADIN1	I	ADC input
41	ADIN2	I	ADC input
42	OUTH1(VCC)	O	High-side driver output (VCC)
43	VCC	-	5-volt regulator output
44	VAREF	I	ADC reference voltage input
45	GNDA	-	Ground
46	ADIN0	I	ADC input
47	VB	-	Battery input
48	OUTH0(VB)	O	High-side driver output (VCC)
-	EP	-	Exposed pad to be connected to GND
-	Corner pin	-	Corner pin to be connected to GND

8. I/O Equivalent Circuits

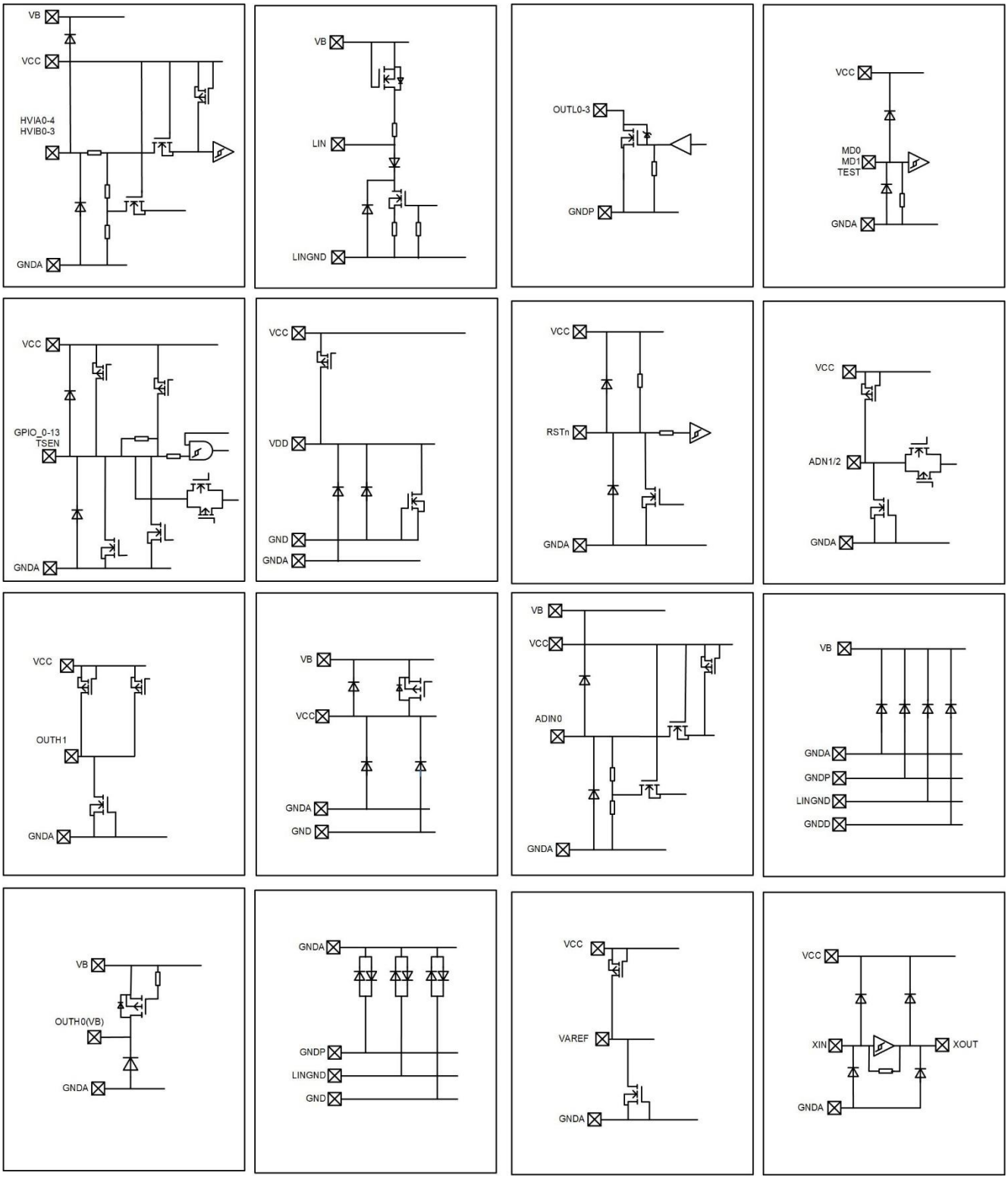


Figure 8.1 I/O Equivalent Circuit Diagrams

9. Functional Description

9.1. CPU

- This product contains a high-performance, low-power 32-bit (Arm® Cortex®-M0 processor).
- This section provides information specific to the product.

9.1.1. Overview

9.1.2. Arm® Cortex®-M0 Processor

- The revision of the Arm® Cortex®-M0 Processor incorporated in this product is as follows.
- For details on the CPU core and its architecture, see the documentation set for the Arm® Cortex®-M0 Processor, which is available at:
  http://infocenter.arm.com/help/index.jsp
  Armv6-M Architecture Reference Manual Issue.
  Cortex-M0 Devices Generic User Guide Issue.
  Cortex-M0 Technical Reference Manual Issue.

Arm processor name	Core Vision
Arm® Cortex®-M0 Processor	r0p0-03

9.1.3. Configurable Options

- The Arm® Cortex®-M0 Processor allows selection of whether to implement some of the functional blocks.
- The following table shows the Arm® Cortex®-M0 Processor implementation in this product.

Configurable Option	Implementation
Number of interrupts	32
Endianness	Little-endian
SysTick timer	Implemented
Number of watchpoint comparators	2
Number of breakpoint comparators	4
Halt Debug	Implemented
WIC	None
Debug port	Serial wire
Multiplier	High-speed

- The Arm® Cortex®-M0 Processor incorporates a system timer called SysTick, which can generate a SysTick exception.

9.1.4. External Signals

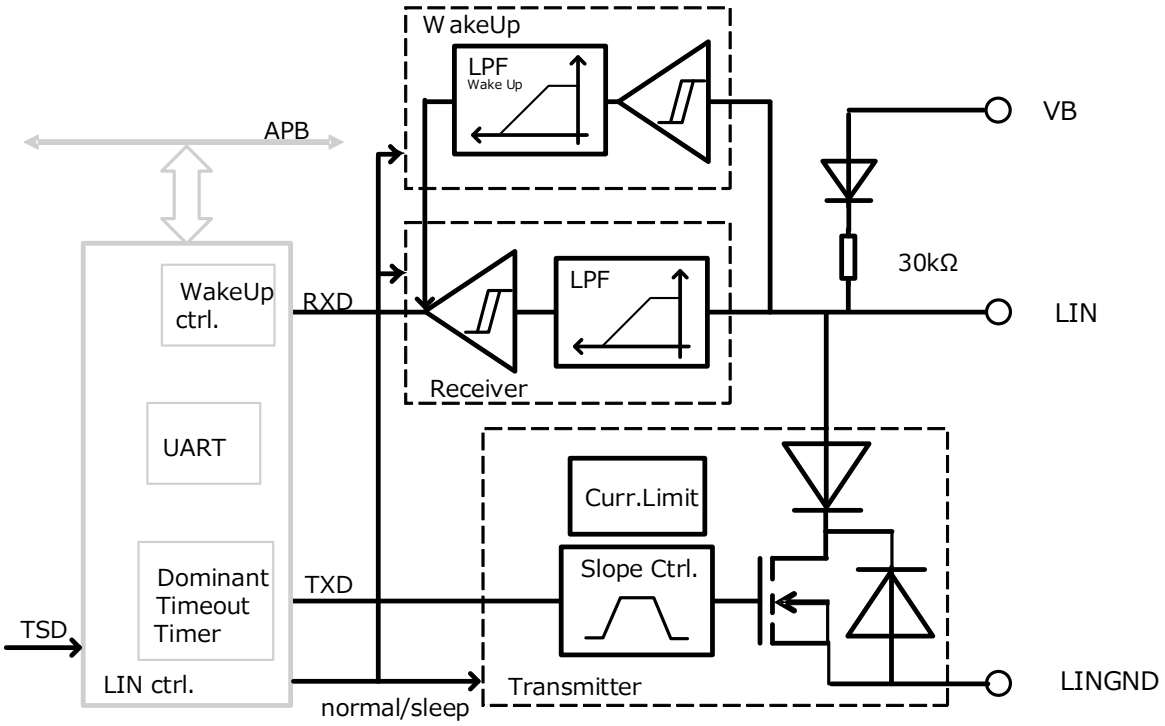
The Arm® Cortex®-M0 Processor provides supports a two-wire Serial Wire Debug (SWD) interface for debugging.

9.1.5. Module Organization

This product incorporates a 32-bit Arm RISC Arm® Cortex®-M0 Processor CPU.

9.2. LINPHY

- Single responder-only LIN Phy channel
- Compliant with the ISO 17987-4, ISO 17987-7 12 V electrical physical layer (EPL), and SAE J2602 standards
- Withstands an ESD of ±6 kV (IEC 61000-4-2:2008, contact discharge, 150 pF, 330 Ω)
- Output slope control to reduce conducted EMI noise
- Programmable slew rate (Low Slope mode<10kbps>, Normal Slope mode<20kbps>, Fast Baud Rate mode<250kbps>) The values enclosed in < > indicate approximate baud rates.
- The figures enclosed between parentheses above are estimated baud rates.
- Output driver with a current limiter
- Thermal shutdown (TSD) circuit in the vicinity of the output driver
- A circuit that detects a wake-up request pulse from the LIN bus and notifies a system controller, PMU, etc. of the wake-up request
- Maximum pulse width of a wake-up request: 150 μs as specified by the LIN Specification
  The system controller, PMU, and other components perform the wake-up process upon receiving this notification, transition from low-power mode to Active mode, and issue an interrupt request to the CPU.



9.2.1 LINPHY Block Diagram

9.3. LINCNT/UART1

- Compliant with ISO 17987:2016 LIN standard
- Dedicated for responder use for LIN
- BREAK field detection function
  - Configurable BREAK width detection (9.5Tbit/10.5Tbit for fixed baud rate mode, 10Tbit/11Tbit for auto baud rate mode)
- Baud rate adjustment functions (selectable from two modes)
  - Fixed baud rate mode
  - Auto baud rate mode using Sync field
  - Baud rate change function
- Wake-up functions
  - Wake-up transmission function
  - Wake-up reception function (measures RXD low duration)
- Built-in checksum calculation accelerator for transmit/receive support
- LIN bus idle time detection function
- Dominant timeout function
- Programmable response space interval (0 to 7 Tbits)
- Programmable inter-byte space interval (0 to 3 Tbits)
  - Configurable number of data bytes in response field (1 to 8 bytes)
- Timer functions
  - RXD low duration measurement
  - Frame timeout function
  - TXD low duration measurement
  - RXD high duration measurement
- Interrupt functions
  - Receive interrupt
    - LIN break field receive interrupt
    - LIN sync field receive interrupt
    - LIN receive-complete interrupt
  - Transmit interrupt
    - LIN transmit-complete interrupt
  - Status interrupt
    - LIN framing error interrupt
    - LIN RXD low-period interrupt
    - LIN frame timeout interrupt
    - LIN sync field error interrupt
    - LIN bit error interrupt
    - LIN TXD low-period timeout interrupt
    - LIN bus high-period timeout interrupt

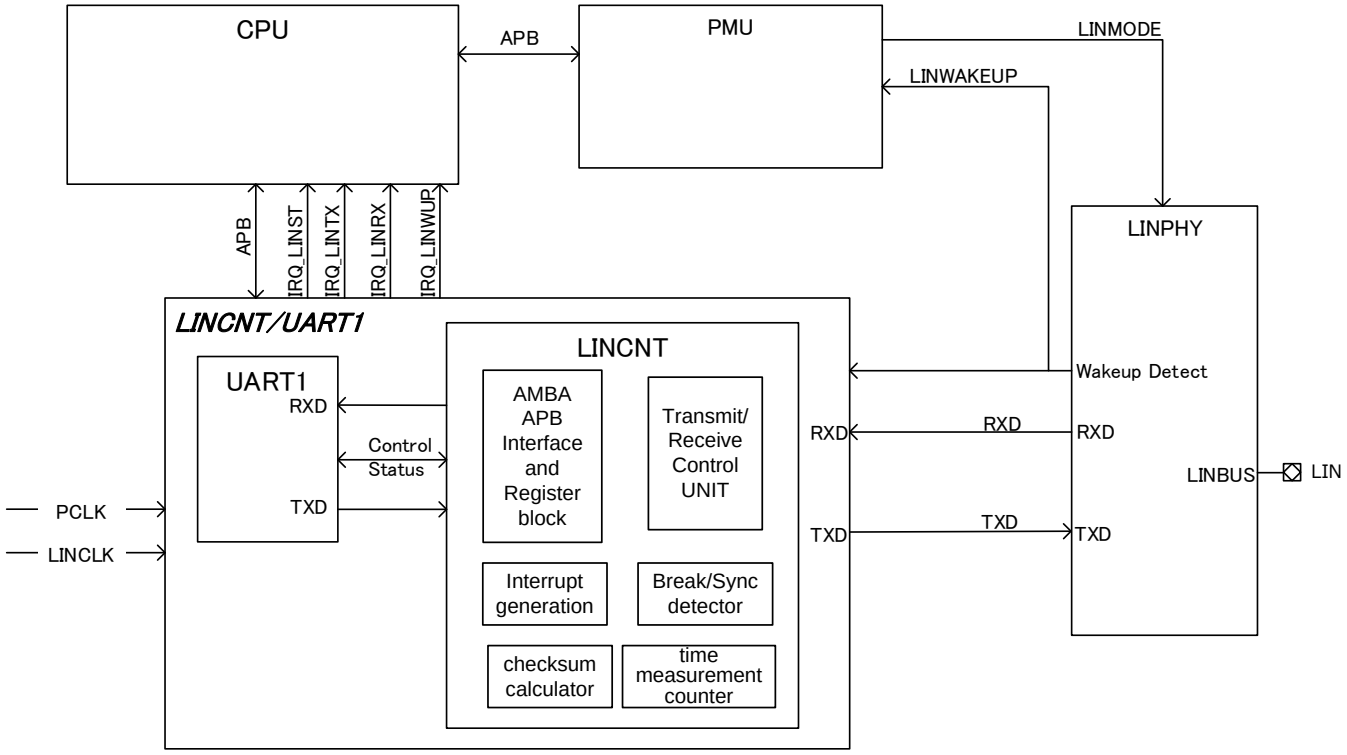


Figure 9.3.1 LINCNT/UART1 Block Diagram

9.4. SPI

9.4.1. External Signals

The external connection is made via GPIO.

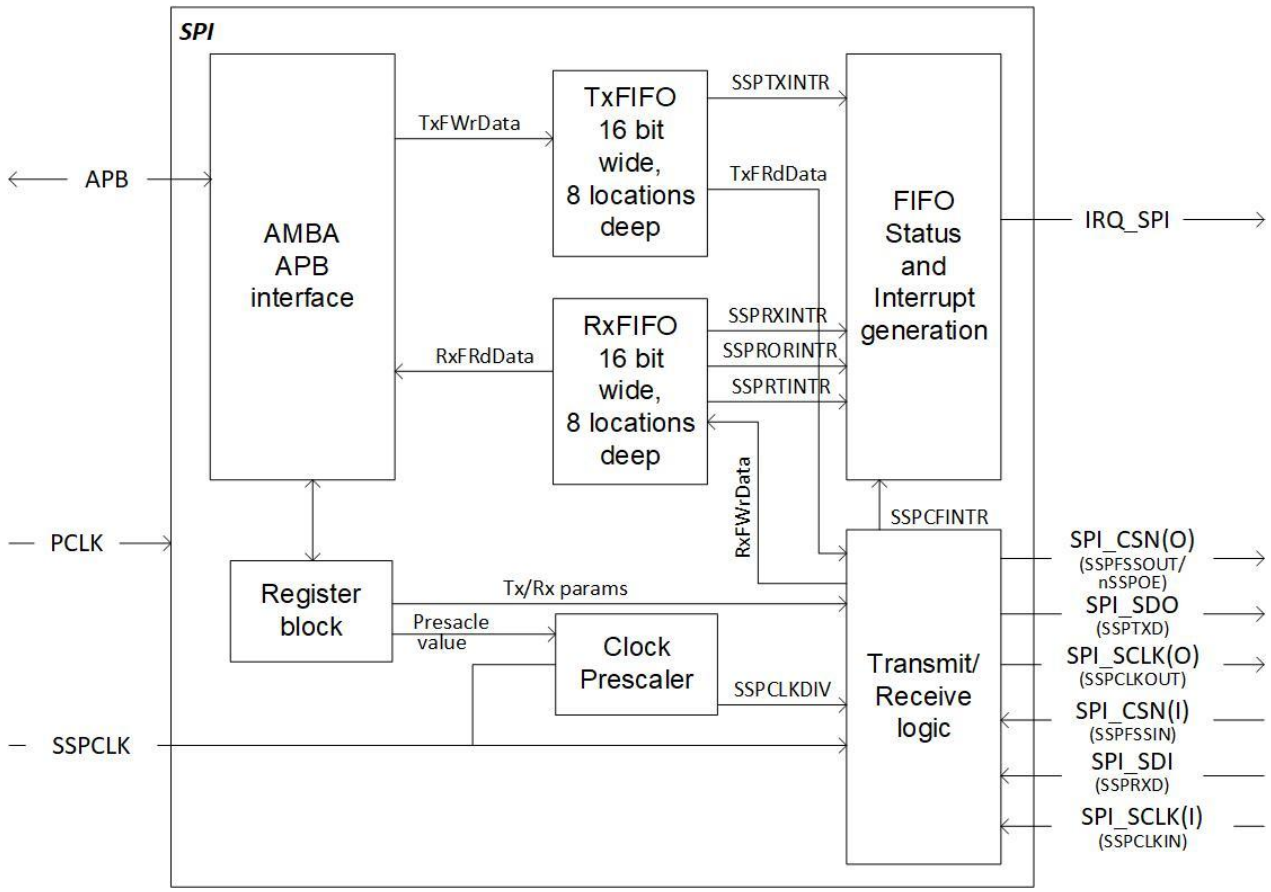


Figure 9.4.1 SPI Block Diagram

9.5. GPIO

- This product provides 14 general-purpose I/O (GPIO) ports.
  – All the GPIO ports can be configured with pull-up or pull-down
  – Two GPIO ports can be used as a source of wake-up from the Standby mode.
  – These wake-up ports can be programmed to generate an interrupt.
- Four GPIO ports accept analog inputs.
- Several GPIO ports can be configured as UART or SPI ports.
- Six GPIO ports can be configured as PWM outputs.
- Six GPIO ports can be configured as capture trigger inputs for the CAPT.
- Two GPIO ports can be configured to accept wake-up or interrupt inputs.
- Several GPIO ports can be configured as debug ports of the SWD.

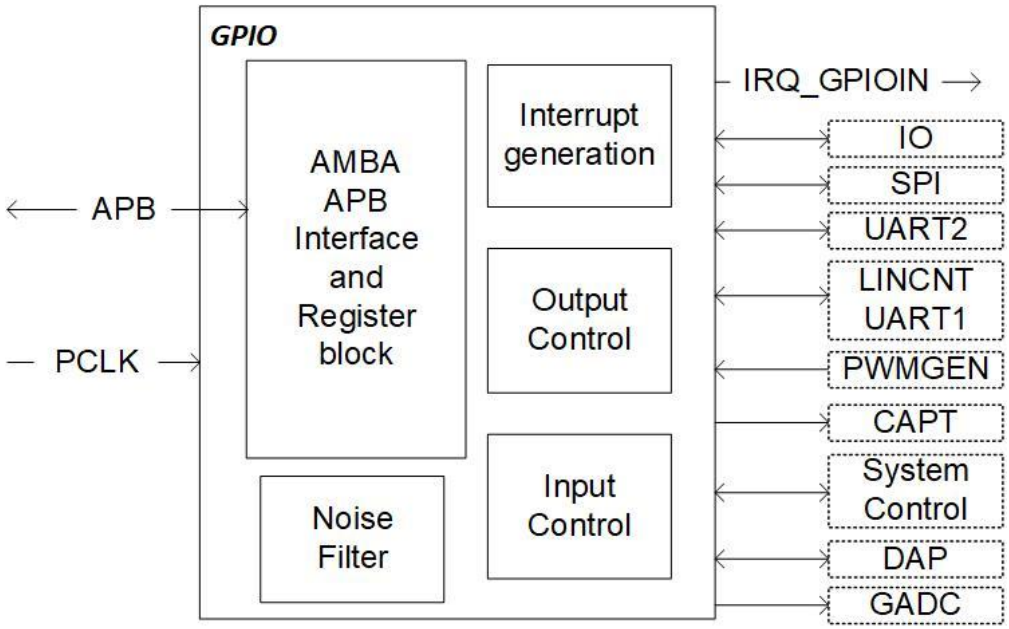


Figure 9.5.1 GPIO Block Diagram

9.6. 10bit Analog Digital Converter (GADC)

- This product provides a 10-bit successive-approximation analog-digital converter (GADC).
- The GADC is capable of measuring 24 analog inputs.
- It supports 12 measurement channels.
- Of these channels, four channels allow the upper and lower limit thresholds to be programmed and can be configured to generate an interrupt when the measurement result is outside the programmed range.
- The GADC provides three measurement modes:
  - Command trigger Single mode: The GADC starts by command trigger via a register writing, stops after performing a sequence of measurements as programmed.
  - Command trigger Cyclic mode: The GADC starts by command trigger via a register writing, repeats a sequence of the programmed measurements.
  - Timer trigger Cyclic mode: The GADC starts by trigger via a timer (TIMER2), repeats a sequence of the programmed measurements.
    * TIMER1 cannot be used as a trigger for ADC measurement.
- The GADC can be configured to generate an interrupt upon completion of measurement.
- For the input from ADIN0, the direct path (x1) or the divided path (x0.45) can be selected.
- Each ADINx pin has a 500kΩ (Min) resistor to GND for division as shown in the Figure 8.1 I/O Equivalent Circuits. (This resistor is not disconnected when x1 is selected.)

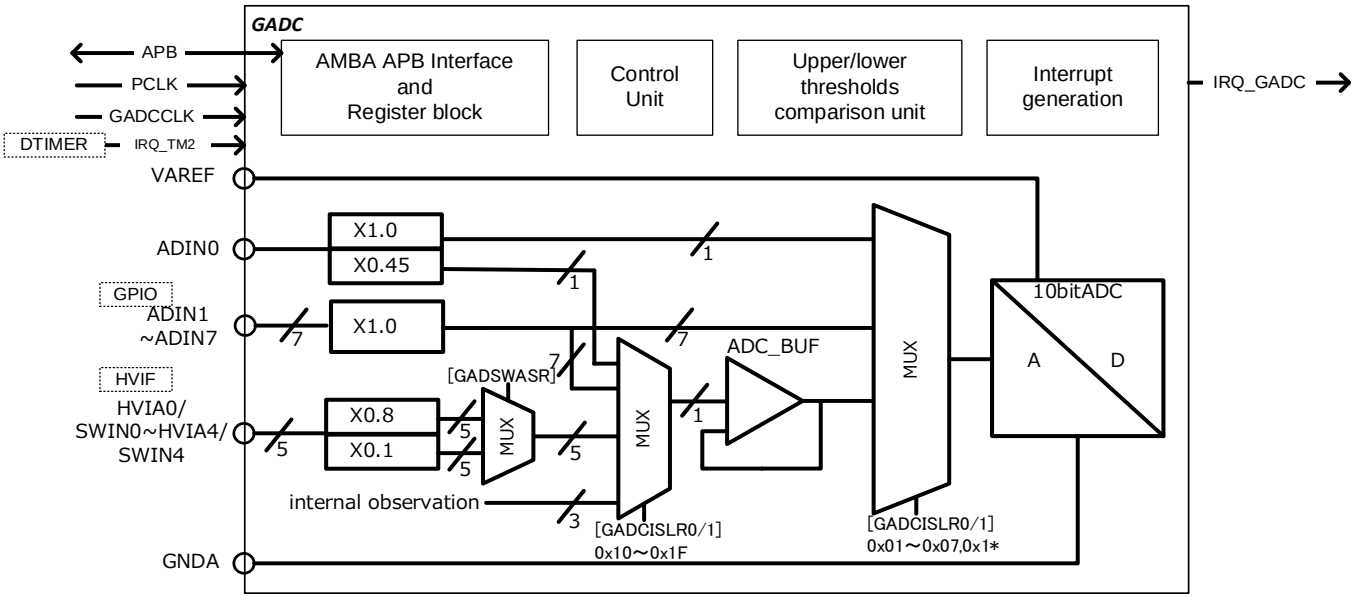


Figure 9.6.1 GADC Block Diagram

9.7. Low Side Drivers (LSD)

- The LSD module incorporates four channels of low-side drivers for relays.
- Each channel provides overcurrent detection. The output of a channel with an overcurrent condition is shut down.
- Each channel incorporates an active clamp circuit to suppress a rise in voltage when its output is shut down.
- All the LSD channels can be configured for register or PWM control.

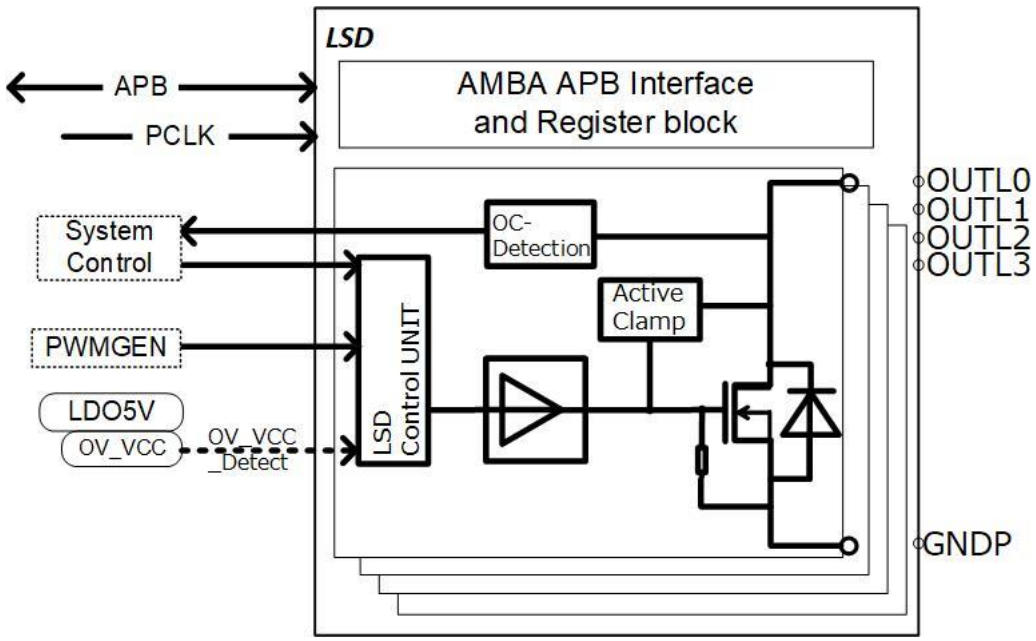


Figure 9.7.1 LSD Block Diagram

9.8. High Side Drivers (HSD)

- This product incorporates two channels of high-side drivers: HSD_VB and HD_VCC. HSD_VB (Channel 0) is powered from VB (12 V) whereas HSD_VCC (Channel 1) is powered from VCC (5 V).
- Both the HSD channels provide overcurrent detection.
- Both the HSD channels can be configured for register or PWM control.

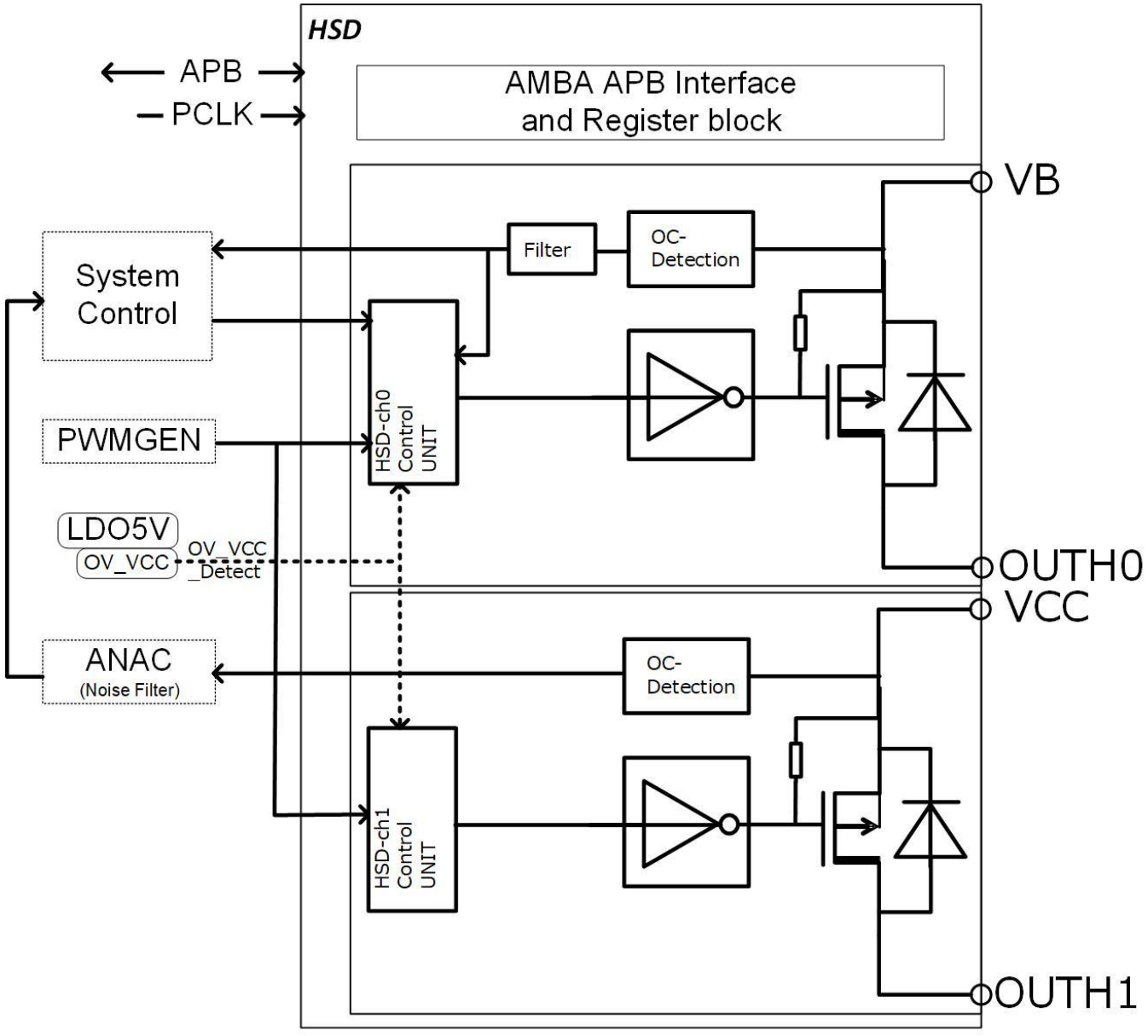


Figure 9.8.1 HSD Block Diagram

9.9. High Voltage Inputs (HVIF)

- Five switch inputs
- Four Hall sensor inputs
- Noise reduction using digital noise filters
  - Four types of settings for a group of five switch inputs
  - Four types of settings for a group of four Hall sensor inputs
- Since SWIN0-SWIN4 and HPIN0 to HPIN3 are high-voltage inputs powered from VB, they incorporate a pull-down resistor and a clamp circuit for internal circuit protection.

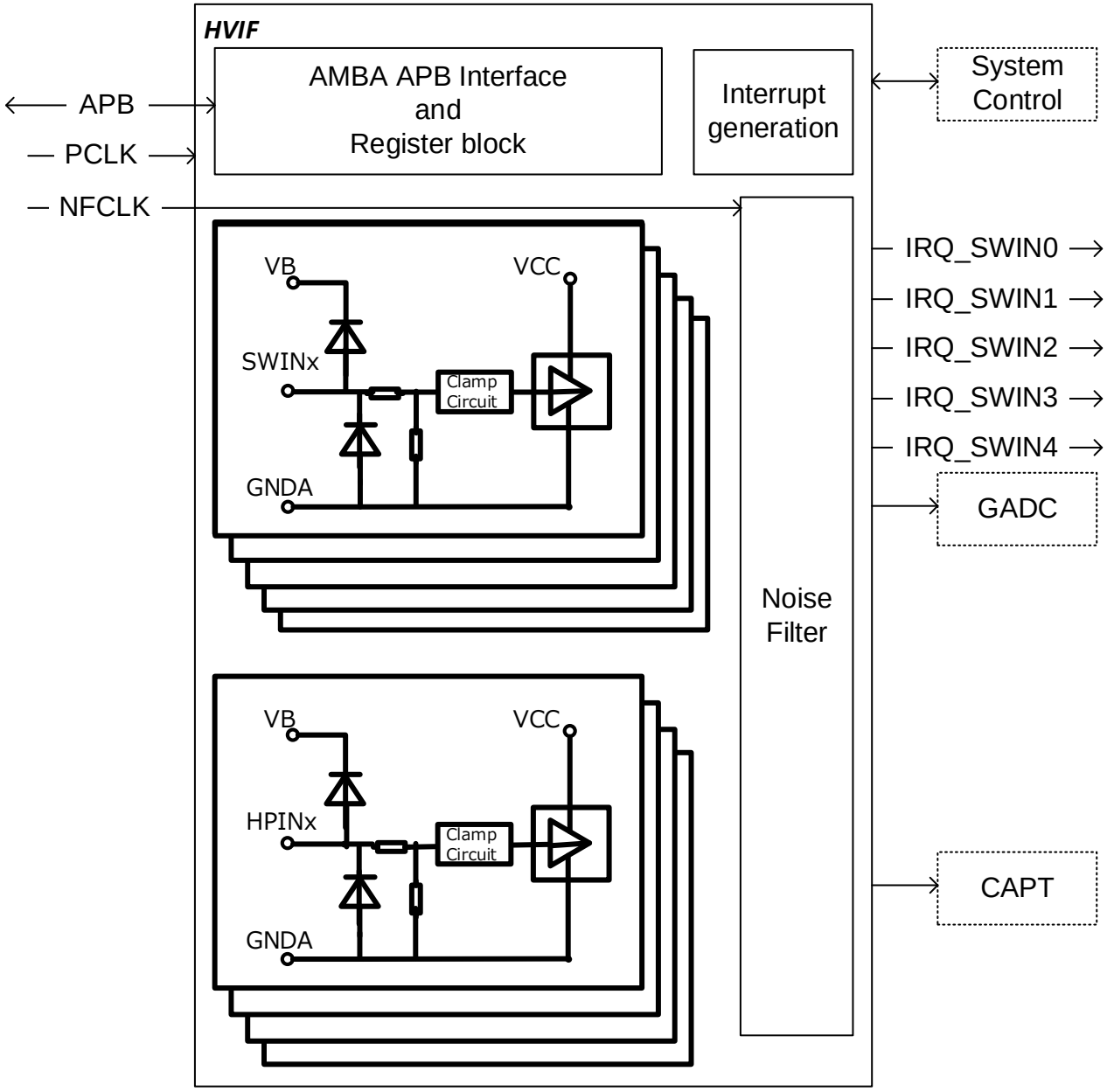


Figure 9.9.1 High Voltage Inputs Block

9.10. Memory Map

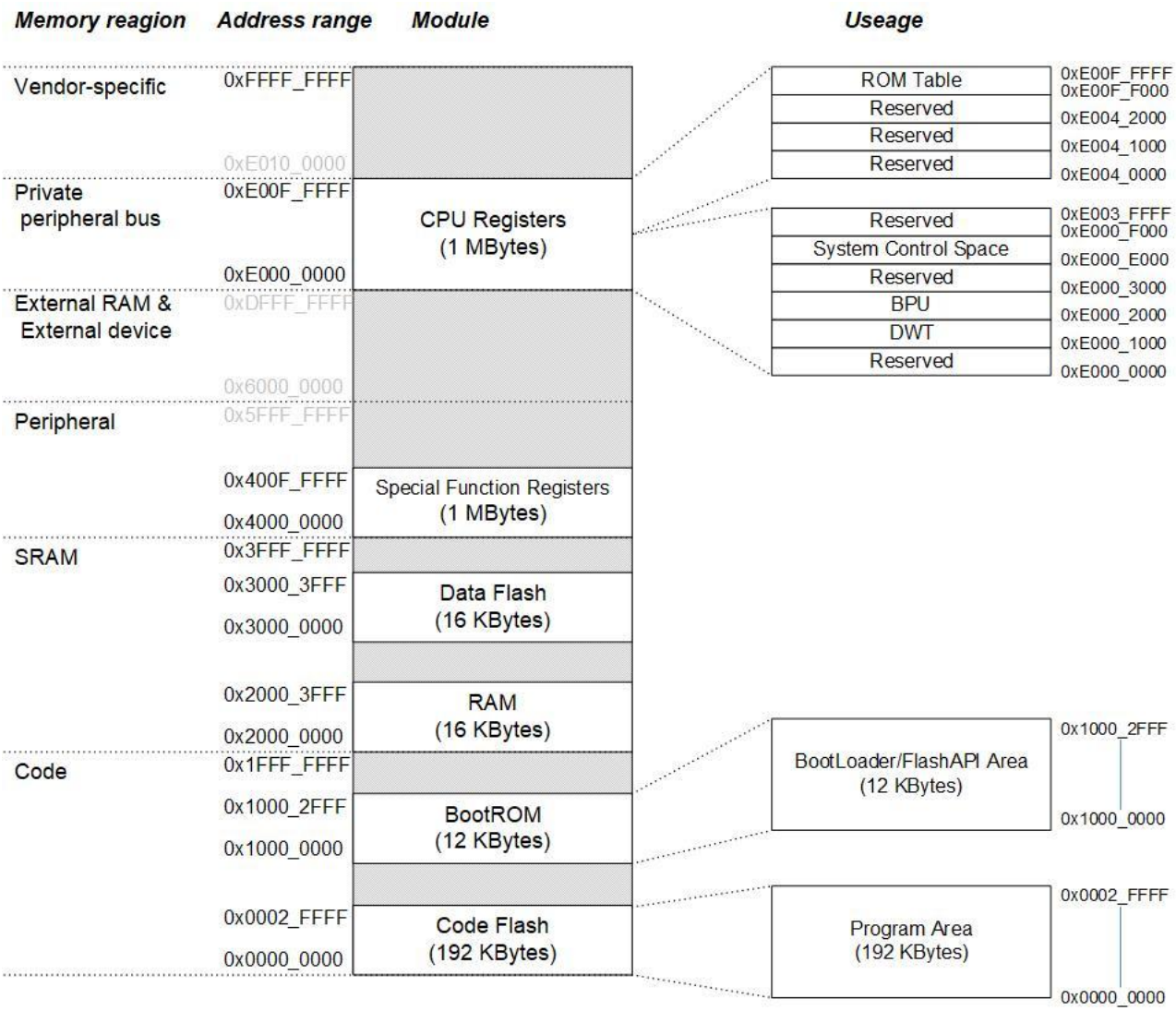


図 9.10.1 Memory Map (Normal and Debug Modes)

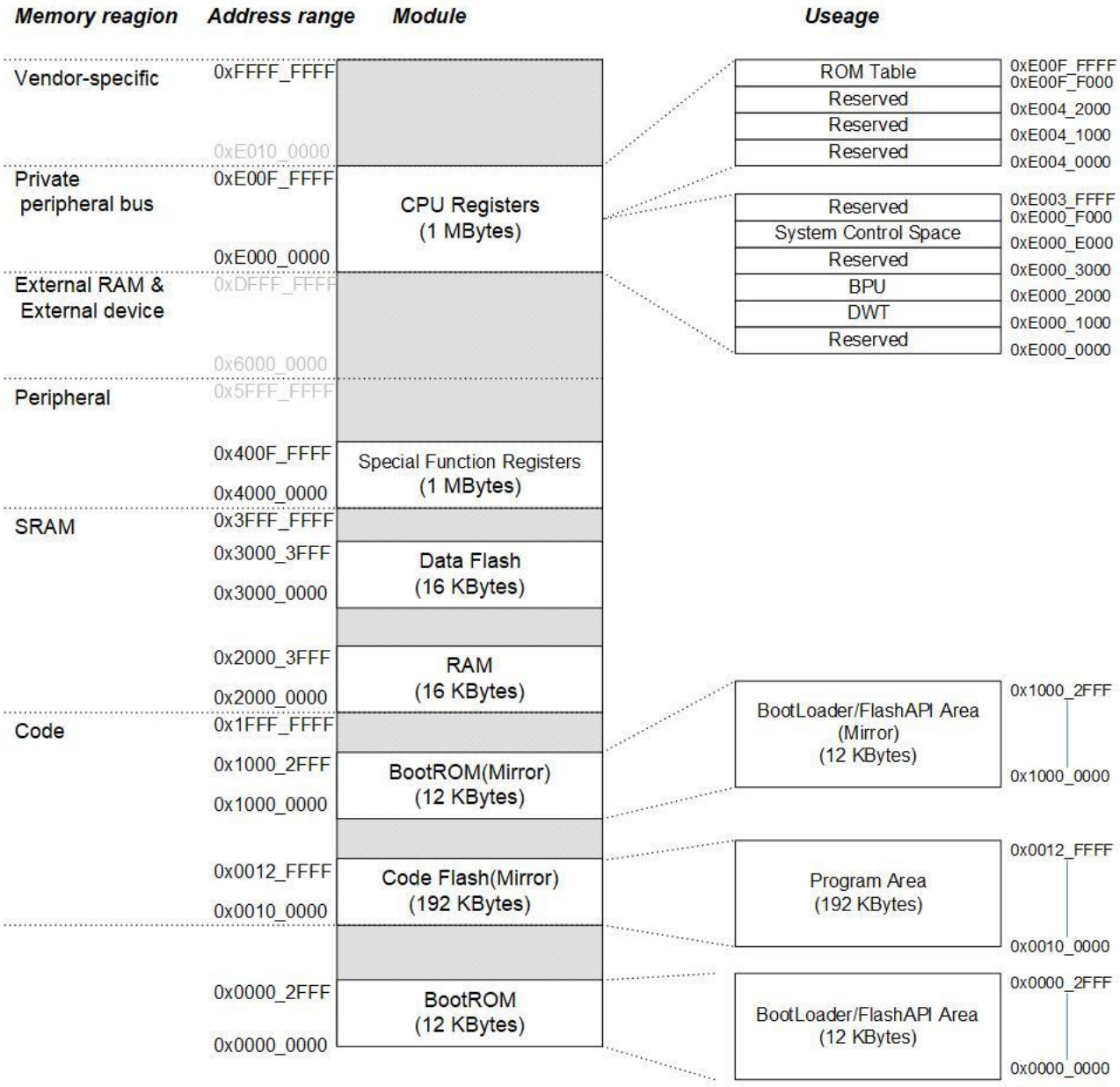


図 9.10.2 Memory Map (Flash Download Mode)

10. Electrical Characteristics

10.1. Absolute Maximum Ratings

Table 10.1 Absolute Maximum Ratings

Characteristic	Symbol	Pin	Test Conditions	Rating	Unit
Supply voltage 1	VB1	VB		-0.3 to 40	V
Supply voltage 2	VVCC	VCC		-0.3 to 6.0	V
Supply voltage 3	VVDD	VDD		-0.3 to 2.1	V
Pin-to-pin voltage	VGND	See test conditions	LINGND, GNDP, GND, GNDA	-0.3 to 0.3	V
Input voltage 1	VLIN	LIN	When VB1 = 6 to 18 V	-27 to 40	V
Input voltage 2	VIN2	See test conditions	HVIA0 to HVIA4 HVIB0 to HVIB3, ADIN0	-0.3 to VB1+0.3 (Max 40V)	V
Input voltage 3	VIN3	See test conditions	GPIO_0 to GPIO_13, MD0, MD1, ADIN1 to ADIN3, VAREF, RSTn, XIN	-0.3 to VVCC+0.3 (Max 6V)	V
Output voltage 1	VOUT1	LIN	When VB1 = 6 to 18 V	-27 to 40	V
Output voltage 2	VOUT2	OUTH0		-0.3 to VB1+0.3 (Max 40V)	V
Output voltage 3	VOUT3	See test conditions	GPIO_0 to GPIO_13, RSTn, OUTH1, XOUT	-0.3 to VVCC+0.3 (Max 6V)	V
Input current 1	IIN1	See test conditions	OUTL0 to OUTL3	0 to 0.8	A
Operating temperature	Ta	—	—	-40 to 90	°C
Storage temperature	Tstg	—	—	-55 to 150	°C

Note:

None of the absolute maximum ratings must be exceeded even instantaneously. Exposure to stress exceeding absolute maximum ratings might cause permanent destruction or degradation of an IC and adversely affect other components. Ensure that none of the absolute maximum ratings is exceeded under any operating conditions.

At above ±18 V, there is a limit to the period during which this product may be exposed to such conditions: ≤ 90 minutes at 18 to 28 V and ≤ 400ms at 28 to 40 V

10.2. Operating Ranges

Table 10.2 Operating Ranges

Characteristic	Symbol	Rating	Unit	Remarks
Supply voltage	VB1	18 to 27	V	The electrical characteristics are not satisfied.
		6 to 18		-
		4.8 to 6		The electrical characteristics are not satisfied.
Operating temperature	Topr	-40 to 90	°C	Ambient temperature, Ta
		-40 to 150		Junction temperature, Tj

10.3. Overall Electrical Characteristics

Table 10.3.1 Electrical Characteristics

(VB=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 150°C unless otherwise noted)

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
Standby current 1 (Standby mode)	Istby1	-	VB=12.0 V, 25°C	-	-	20	μA
Standby current 2 (Standby mode) (Guaranteed by design)	Istby2	-	VB=13.5 V, Ta<50°C	-	-	50	μA
Standby current 1 (CWU mode)	Istby3	-	VB=12 V, 25°C Sleep state: 51ms, PWU state: Average current when the periodic wake-up cycle is programmed to be 125μs	-	-	80	μA

Reference information:

When VB=12V, normal temperature, EXOSC use, SYSCLK=40MHz, LIN, ADC only operating condition, no IC external loading, the current consumption (evaluated) is approximately 11mA.

The current consumption varies depending on the usage conditions. For example, CPU loads and operating frequency.

10.4. 5-V/1.5-V Regulator (LDO5V/LDO15V)

Table 10.4.1 Electrical Characteristics

(VB=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 150°C unless otherwise noted)

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
Output voltage	Vcc	VCC (Note1)	Io =-10μA to -135mA (sum of the maximum VCC/VDD supply current inside TB9M001FTG and OUTH1 (65mA max))	4.8	5	5.2	V
Limit current 1	Icc_lim1		VCC ≥ (4.0V)	-850	-475	-250	mA
Limit current 2 (Note3)	Icc_lim2		VCC ≤ (3.0V)	-250	-115	-10	mA
Drop voltage (Guaranteed by design)	Vdrop		VB – VCC under the following conditions: VB = 4.5V and Io =-10μA to -135mA (sum of the maximum VCC/VDD supply current inside TB9M001FTG and OUTH1 (65mA max))	-	-	0.5	V
Under release voltage1(VCC)	Vccuvrel		VCC rising (UV_VCC)	4.20	-	4.75	V
Under detect voltage1(VCC)	Vccuvdet		VCC falling (UV_VCC)	4.00	-	4.35	V
Over detect/ release voltage (VCC)	Vccovdet			5.28	-	5.72	V
Under release voltage2 (VCC)	Vccporrel		VCC rising (POR5V)	3.22	3.60	3.98	V
Under detect voltage2 (VCC)	Vccpordet		VCC falling (POR5V)	3.07	3.45	3.83	V
Output voltage 2	Vdd	VDD (Note2)	Io = -10μA to -60mA (maximum VDD supply current inside TB9M001FTG)	1.45	1.5	1.55	V
Under release voltage (VDD)	Vddporrel		VDD rising	1.35	-	1.45	V
Limit current	Idd_lim3			-250	-150	-70	mA
Under detect voltage (VDD)	Vddpordet		VDD falling	1.30	-	1.40	V
Over detect/ release voltage (VDD)	Vddovdet			1.55	-	1.65	V
Detection temperature (Specified by design)	tsd	-		150	170	190	°C
Release temperature (Guaranteed by design)	tsrel	-		135	-	175	°C

Note1: Connect a capacitor of 1.0μF or more as close as possible to the VCC pin.
Note2: Connect a capacitor of 2.2μF or more as close as possible to the VDD pin.
Fully evaluate electrical characteristics with a unit board in the usage environment to determine the values of external components.
Note3: The current limit at VCC in Standby/CWU mode is Current Limit 2.

10.5. Switch and Hall Sensor IC Inputs（High Voltage Inputs）

Table 10.5.1 Electrical Characteristics

(VB=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 150°C unless otherwise noted)

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
Input voltage range	Irange	SWINx, HPINx	Voltage at the opposite end of a 10kΩ resistor connected to the input pin The comparator output shall not invert up to the High-level or Low-level threshold.	-1	-	18	V
High-level threshold	VIH	SWINx, HPINx	SWINx, HPINx = L→H Input resistor = 10kΩ	0.65 ×VCC	-	-	V
Low-level threshold	VIL	SWINx, HPINx	SWINx, HPINx = H→L Input resistor = 10kΩ	-	-	0.35 ×VCC	V
Input current 3	IIH	SWINx, HPINx	SWINx, HPINx = 0V	-100	-	1000	nA
Input NF	Tnf	SWINx, HPINx	Filter setting = 1.2μs	1.14	1.2	1.26	μs
Pull-down resistor	Rpd	SWINx, HPINx		500	-	-	kΩ

10.6. Oscillator

Table 10.6.1 Electrical Characteristics

(VB=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 150°C unless otherwise noted)

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
IOSCH Frequency (HFCLK)	Fhclk	-		19.0	20	21.0	MHz
IOSCL Frequency (LFCLK)	Flclk	-		27.2	32	36.8	kHz
External osc (Note1) Frequency	Exosc	XIN, XOUT	Values of a usable external CERALOCK ceramic resonator or crystal	16	-	20	MHz

Note1:

Contact the manufacturer of external components for the matching with EXOSC.
Toshiba has tested the CSTNE16M0VH3C000R0 and CSTNE20M0VH3C000R0 and confirmed that they operate with the EXOSC properly.
The tolerance of external components should be ±0.2% or less.

10.7. Reset Generator and Standby Time

Table 10.7.1 Electrical Characteristics

(VB=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 150°C unless otherwise noted)

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
Low-level output voltage	VOL	RSTn (output)	Io = +5mA	0	-	0.4	V
Analog NF	Tnf	RSTn (input)		10	20	40	μs
WATCHDOG reset time	Trst_wdt	-	Time from a WATCHDOG reset request to an internal reset release (except when the flash memory is busy)	-	70	-	μs
Boot standby time 1	trst1	-	Time from recovery from VCC undervoltage 1 to a CPU reset release	-	-	8	ms
Boot standby time 2	trst2	-	Time from when a wake-up request is detected to when a CPU reset is released after LDO15V stabilizes	-	-	2	ms
External oscillator settling time	Twait_exosc	-	Time from when the oscillator is started by software to when it settles to a steady state (when the CSTNE16M0VH3C000R0, a 16-MHz CERALOCK ceramic resonator from Murata, is used)	-	-	1	ms
PLL settling time	Twait_pll	-		-	-	140	μs
Pull-up resistor	Rpu	RSTn	Between the VCC and RSTn pins	30	50	100	kΩ
RSTn input voltage	VIH	RSTn (input)		0.75 ×VCC	-	-	V
RSTn input voltage	VIL	RSTn (input)		-	-	0.25 ×VCC	V

10.8. Data Flash

Table 10.8.1 Electrical Characteristics

(VB=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 150°C unless otherwise noted)

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
Bus frequency (Note1)	FbusDT	-		-	-	42	MHz
Read frequency	FrdDT	-		-	-	10.5	MHz
Data retention time 1	Tret1DT	-	Tj=85°C, after 10,000 program/erase cycles	20	-		years
Data retention time 2	Tret2DT	-	Tj=85°C, after 100,000 program/erase cycles	5	-	-	years
Flash capacitance	-	-		-	16	-	KBytes
Data access size	DaccDT	-	Read	-	Word(32bit) /Half word(16bit) /Byte(8bit)	-	-
Erase block size	DdelDT	-		-	2	-	KBytes
Erase block time	TdelDT	-	One block (2 KBytes)	-	6.8	-	ms
Program block size	DwrDT	-		8	-	128	Bytes
Program block time	TwrDT	-	8 bytes (2 words, 64 bits)	-	2.4	-	ms

Note1: It is necessary to change the Flash read access wait settings according to the bus frequency.

10.9. Program Flash

Table 10.9.1 Electrical Characteristics

(VB=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 150°C unless otherwise noted)

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
Bus frequency (Note1)	FbusCF	-		-	-	42	MHz
Read frequency	TrdCF	-				10.5	MHz
Data retention time 1	Tret1CF	-	Tj=85°C, after 1,000 program/erase cycles	20	-		years
Flash capacitance	-	-		-	192	-	KBytes
Data access size	DaccCF	-	Same as read/program	-	Word (32bit)	-	-
Erase time	Tdel	-	192 KBytes	-	200	-	ms
Program time	Twr	-		-	5	-	s
Erase block size	DdelCF	-		-	8	-	KBytes
Erase block time	TdelCF		One block (8 Kbytes)	-	6.8	-	ms
Program block size	DwrCF	-		-	128	-	Bytes
Program block time	TwrCF	-	32 Word	-	2.4	-	ms

Note1: It is necessary to change the Flash read access wait settings according to the bus frequency.

10.10. LIN

Table 10.10.1 Electrical Characteristics

(VB=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 150°C unless otherwise noted)

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
Supply voltage range	V_{VB}	VB	ECU operating voltage range (Param 9)	8.0	-	18.0	V
Supply voltage range	V_{SUP}	VB	Note：Param 10 of LIN configuration is defined 7.0V(min), IC requires 6.0V(min) on 5V regulator.	6.0	-	18.0	V
Supply voltage MAX Ratings	$V_{SUP\_NON\_OP}$	VB	Voltage range with in which the device is not destroyed. An optional time limit for the maximum value shall be at least 400ms. No guarantee of correct operation. (Param 11)	-0.3	-	40	V
BUS MAX Ratings	$V_{BUS\_MAX\_RATING}$	LIN	Voltage range with in which the device is not destroyed. (Param 82) An optional time limit for the maximum value shall be at least 400ms. No guarantee of correct operation.	-27	-	40	V
Receiver threshold voltage, recessive to dominant edge	V_{th_rec}	LIN	Low Voltage: Recessive Input Threshold (SAE)	0.4	-	0.53	V_{SUP}
Receiver threshold voltage, dominant to recessive edge	V_{th_dom}	LIN	High Voltage: Dominant Input Threshold (SAE)	0.47	-	0.6	V_{SUP}
BUS current limitation	I_{BUS_LIM}	LIN	Current Limitation for Driver dominant state driver on VBUS = VBAT_maxd (Param 12)	40	-	200	mA
Leakage current(dominant)	$I_{BUS\_PAS\_dom}$	LIN	Input leakage current at the receiver incl. slave pull-up resistor as specified in Param 26 driver off VBUS = 0V VBAT = 12V (Param 13)	-1	-	-	mA
Leakage current(recessive)	$I_{BUS\_PAS\_rec}$	LIN	Driver off 8V < VBAT < 18V, 8V < VBUS < 18V, VBUS > VBAT (Param 14)	-	-	20	μA
Leakage current	$I_{BUS\_NO\_GND}$	LIN	Control unit disconnected from ground GNDDevice = VSUP 0 V < VBUS < 18V VBAT = 12V Loss of local ground shall not affect communication in the residual network. (Param 15)	-1	-	1	mA
Leakage current	$I_{BUS\_NO\_BAT}$	LIN	VBAT disconnected VSUP = GND 0 V < VBUS < 18 V Node shall sustain the current that can flow under this condition. Bus shall remain operational under this condition. (Param 16 and SAE)	-	-	23	μA
Voltage of Receiver dominant state	V_{BUS_dom}	LIN	Receiver dominant state Note: Param 17 of LINPHY configuration is not defined minimum voltage. (Param 17)	-27	-	0.4 ×VB	V

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
Voltage of Receiver recessive state	V_{BUS_rec}	LIN	Receiver recessive state (Param 18)	0.6	-	-	V_{SUP}
Receiver center voltage	V_{BUS_CNT}	LIN	VBUS_CNT = (Vth_dom + Vth_rec)/2(Param 19)	0.475	-	0.525	V_{SUP}
Receiver hysteresis	V_{HYS}	LIN	VHYS = Vth_rec–Vth_dom(Param 20 and SAE)	0.07	-	0.175	V_{SUP}
Duty cycle D1 (for worst case at 20 kbps)	D1	LIN	THRec(max) =0,744 × VSUP; THDom(max) =0,581 × VSUP; VSUP = 7,0 V to 18 V; tBIT = 50µs; D1 = tBus_rec(min)/ (2 × tBIT) (Param 27) <PHYFBRM>=0	0.396	-	-	-
Duty cycle D2 (for worst case at 20 kbps)	D2	LIN	THRec(min) =0,422 × VSUP; THDom(min) =0,284 × VSUP; VSUP = 7,6 V to 18 V; tBIT = 50µs; D2 = tBus_rec(max)/ (2 × tBIT) (Param 28) <PHYFBRM>=0	-	-	0.581	-
Duty cycle D3 (for worst case at 10 kbps)	D3	LIN	THRec(max) =0,778 × VSUP; THDom(max) =0,616 × VSUP; VSUP = 7,0 V to 18 V; tBIT = 96µs; D3 = tBus_rec(min)/ (2 × tBIT) (Param 29) <PHYFBRM>=0	0.417	-	-	-
Duty cycle D4 (for worst case at 10 kbps)	D4	LIN	THRec(min) =0,389 × VSUP; THDom(min) =0,251 × VSUP; VSUP = 7,6 V to 18 V; tBIT = 96µs; D4 = tBus_rec(max)/ (2 × tBIT) (Param 30) <PHYFBRM>=0	-	-	0.59	-
Propagation delay	t_{rx_pd}	LIN	Propagation delay of receiver (Param 31) ・bus dominant to RxD LOW ・bus recessive to RxD HIGH <PHYFBRM>=0	-	-	6	µs
Receiver delay symmetry	t_{rx_sym}	LIN	Symmetry of receiver propagation delay rising edge with respect to falling edge (Param 32) <PHYFBRM>=0	-2	-	2	µs
Bus pull-up resistance	R_{SLAVE}	LIN	internal resistance (Param 26)	20	30	60	kΩ
Bus pull-up resistance	R_{MASTER}	LIN	The serial diode is mandatory. Only for valid for transceiver with integrated master pull-up resistor. (Param 25) external resistance	900	-	1100	Ω
LIN input capacity (Guaranteed by design)	C_{SLAVE}	LIN	Capacitance of slave node (Param 37) 250pF -220pF = 30pF max	-	-	30	pF

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
Over temperature detection threshold	T_{OT}	-	(Guaranteed by IC design)	150	-	190	°C
Over temperature detection hysteresis	ΔT_{OT}	-	(Guaranteed by IC design)	-	10	-	°C
Current consumption in Sleep Mode	I_{sleep}	VB	VB=12V, RT=25°C, only working LIN bus Wakeup signal	-	-	3	µA
Dominant time for bus Wakeup	t_{WAKE}	LIN	Wakeup pulse width from LIN bus	30	-	150	µs
Turn off time to sleep state	t_{sleep}	-	Turn off time from Active state to Sleep or Standby state	-	-	1	ms
Wake-up threshold voltage	V_{BUSwk}	LIN	Threshold voltage for Wakeup signal detection	0.4	0.5	0.6	V_{SUP}
ESD Susceptibility HBM pins LIN vs. LINGND	V_{ESDLIN}	LIN	IEC61000-4-2 Conducted HBM	-6	-	6	kV
ESD Susceptibility HBM pins LIN vs. LINGND	$V_{ESDLIN3}$	LIN	AEC-Q100-002	-6	-	6	kV

10.11. 12-V High-Side Driver (HSD_VB)

Table 10.11.1 Electrical Characteristics

(VB=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 150°C unless otherwise noted)

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
On-resistance	RonH0	OUTH0 (12V)	Id = -100mA	1	-	5	Ω
Overcurrent detection threshold	IdetH0	OUTH0 (12V)		-	-	-200	mA
Turn-on delay time	TonH0	OUTH0 (12V)	Time from when HSO0 is turned on via [HSDCR]<HSDGC0> to when its voltage exceeds 10% of VB Load circuit: CL=30 pF, RL=100 Ω	2	-	50	µs
Turn-off delay time	ToffH0	OUTH0 (12V)	Time from when HSO0 is turned off via [HSDCR]<HSDGC0> to when its voltage drops to 90% of VB Load circuit: CL=30 pF, RL=100 Ω	2	-	50	µs
Output leakage current	IILH0	OUTH0 (12V)	OUTH0=OFF, OUTH0=0V	-5	-	5	µA
Overcurrent filtering time	TnfH0	OUTH0 (12V)		-	-	5	µs

10.12. 5-V High-Side Driver (HSD_VCC)

Table 10.12.1 Electrical Characteristics

(VB=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 150°C unless otherwise noted)

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
On-resistance	RonH1	OUTH1 (5V)	Id = -65mA	-	4	7	Ω
Overcurrent detection threshold	IdetH1	OUTH1 (5V)		-250	-	-100	mA
Turn-on delay time	TonH1	OUTH1 (5V)	Time from when HSD1 is turned on via [HSDCR]<HSDGC1> to when its voltage exceeds 10% of VCC Load circuit: CL=30 pF, RL=320 Ω	2	-	50	μs
Turn-off delay time	ToffH1	OUTH1 (5V)	Time from when HSO1 is turned off via [HSDCR]<HSDGC1> to when its voltage drops to 90% of VCC Load circuit: CL=30 pF, RL=320 Ω	2	-	50	μs
Output leakage current	IILH1	OUTH1 (5V)	OUTH1=OFF, OUTH1=0V	-1	-	1	μA

10.13. Low-Side Drivers

Table 10.13.1 Electrical Characteristics

(VB=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 150°C unless otherwise noted)

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
On-resistance	RonLx	OUTLx	Id = 115mA	0.4	-	6	Ω
Turn-on delay time	TonLx	OUTLx	Time from when LSDx is turned on via [LSDCR]<LSDGCx> to when the OUTLx voltage drops to 90% of VB Load circuit: RL=160 Ω, CL=30 pF	1	-	50	μs
Turn-off delay time	ToffLx	OUTLx	Time from when LSDx is turned off via [LSDCR]<LSDGCx> to when the OUTLx voltage exceeds 10% of VB Load circuit: RL=160 Ω, CL=30 pF	1	-	50	μs
Active clamp voltage	VacLx	OUTLx	Id = 115mA at off	-	-	35	V
Output leakage current	IleakLx	OUTLx	OUTLx=0V or OUTLx=VB	-10	-	10	μA
Overcurrent detection threshold	IdetLx	OUTLx		210	-	800	mA
Overcurrent filtering time	TnfLx	OUTLx		1.14	1.2	1.26	μs

10.14. 10-Bit AD

Table 10.14.1 Electrical Characteristics

(VB=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 150°C unless otherwise noted)

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
Conversion time	Tcv	-	Settling time + conversion time GADCCLK=10 MHz	-	16.4	-	μs
DNL error	DNL	-		-1.5	-	1.5	LSB
INL error	INL	-		-2.5	-	2.5	LSB
Total error	Err	-		-3	-	3	LSB
Input voltage division factor 1	Rad1	ADIN0	Ratio of the ADIN0 pin voltage to the buffer input voltage Input range: 0.8V to VAREF	0.429	0.45	0.473	-
Input voltage division factor 2	Rad2	SWIN0to 4	Ratio of the SWINx pin voltage (x=0-4) to the buffer input voltage Input range: 0.5 to 4.0 V	0.762	0.8	0.840	-
Amplifier error (Note1)	Eamp	-	Buffer input-output differential	-10	-	10	mV
Input clamp voltage	Vclp	ADIN0	When <GADCISLx[4:0]>=0x00	3.4	-	-	V

Note1: The amplifier error is an error that is added when an input with ADC_BUF is selected.

10.15. DC characteristics

Table 10.15.1 Electrical Characteristics

(VB=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 150°C unless otherwise noted)

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
Input voltage	VIH	See test conditions.	GPIO_x (0-13), MD0, MD1	0.75 ×VCC	-	-	V
Input voltage	VIL	See test conditions.	GPIO_x (0-13), MD0, MD1	-	-	0.25 ×VCC	V
Pull-up resistor	Rpu	See test conditions.	GPIO_x (0-13)	30	50	100	KΩ
Pull-down resistor	Rpd	See test conditions.	GPIO_x (0-13), MD0, MD1	30	50	100	KΩ
Output voltage	VOH	See test conditions.	GPIO_x (0 to13) Load condition: <GPIOPSx>=00: -1mA <GPIOPSx>=01: -2mA <GPIOPSx>=10: -4mA <GPIOPSx>=11: -6mA	0.8 ×VCC	-	-	V
Output voltage	VOL	See test conditions.	GPIO_x (0 to13) Load condition: <GPIOPSx>=00: 1mA <GPIOPSx>=01: 2mA <GPIOPSx>=10: 4mA <GPIOPSx>=11: 6mA	-	-	0.2 ×VCC	V

10.16. SPI

Table 10.16.1 Electrical Characteristics

(VB=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 150°C unless otherwise noted)

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
SCLK period (controller)	Tm	SCLK		T(Note1) m(Note3) ≥250 ns	-	-	ns
SCLK period (target)	Ts			T (Note1) n(Note2) ≥1 μs	-	-	ns
SCLK Low-level pulse width in Controller mode	tWLM			0.4	-	0.6	Tm
SCLK High-level pulse width in Controller mode	tWHM			0.4	-	0.6	Tm
SCLK Low-level pulse width in Target mode	tWLS			0.4	-	0.6	Ts
SCLK High-level pulse width in Target mode	tWHS			0.4	-	0.6	Ts
SCLK rise/fall to output data valid in Controller mode	tODSM			-	-	50	ns
SCLK rise/fall to SDO hold in Controller mode	tODHM			-20	-	-	ns
SCLK rise/fall to SDO valid in Controller mode	tIDSM			55	-	-	ns
SDI hold time from SCLK rise/fall in Controller mode	tIDHM			100	-	-	ns
CSN valid to SCLK rise/fall in Controller mode	tOFSM	CSN SCLK		T(Note1) m(Note3) - 50	-	-	ns
SCLK rise/fall to SDO valid in Target mode	tODSS	SCLK		-	-	3T + 90	ns
SCLK rise/fall to SDO hold in Target mode	tODHS			2T(Note1)	-	-	ns
SCLK rise/fall to SDI valid in Target mode	tIDSS			10	-	-	ns
SCLK rise/fall to SDI hold in Target mode	tIDHS			3T(Note1) + 20	-	-	ns
CSN valid to SCLK rise/fall in Target mode	tIFSS	CSN SCLK		T(Note1) n(Note2) - 20	-	-	ns
SCLK rise/fall to CSN deasserted in Controller mode	tOFHM			T(Note1) m(Note3) - 50	-	-	ns
SCLK rise/fall to CSN deasserted in Target mode	tIFHS			T(Note1) n(Note2) - 20	-	-	ns

Note1: T represents the SSPCLK period (e.g., 25 ns at 40 MHz).
Note2: n represents a ratio of the SCLK period to the SSPCLK period (n ≥ 12).
Note3: m represents the ratio of the SCLK period to the SSPCLK period (65024 ≥ m ≥ 12).
Note4: The SPI characteristics are guaranteed by design.

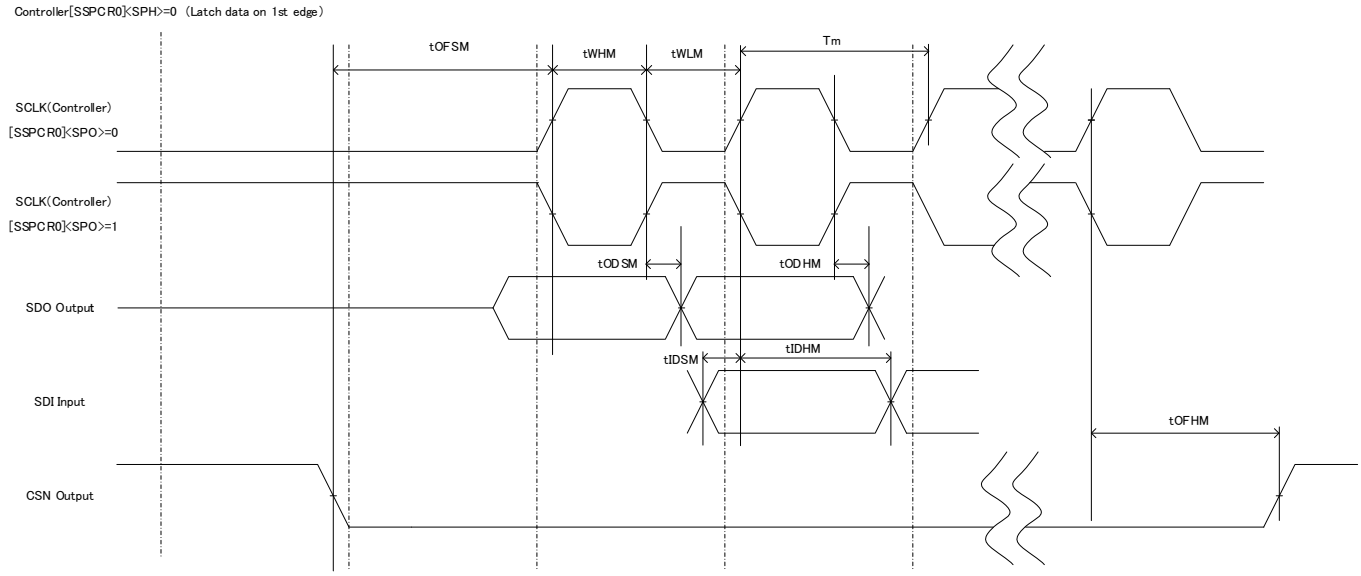


Figure 10.16.1 SPI Communication Waveform 1

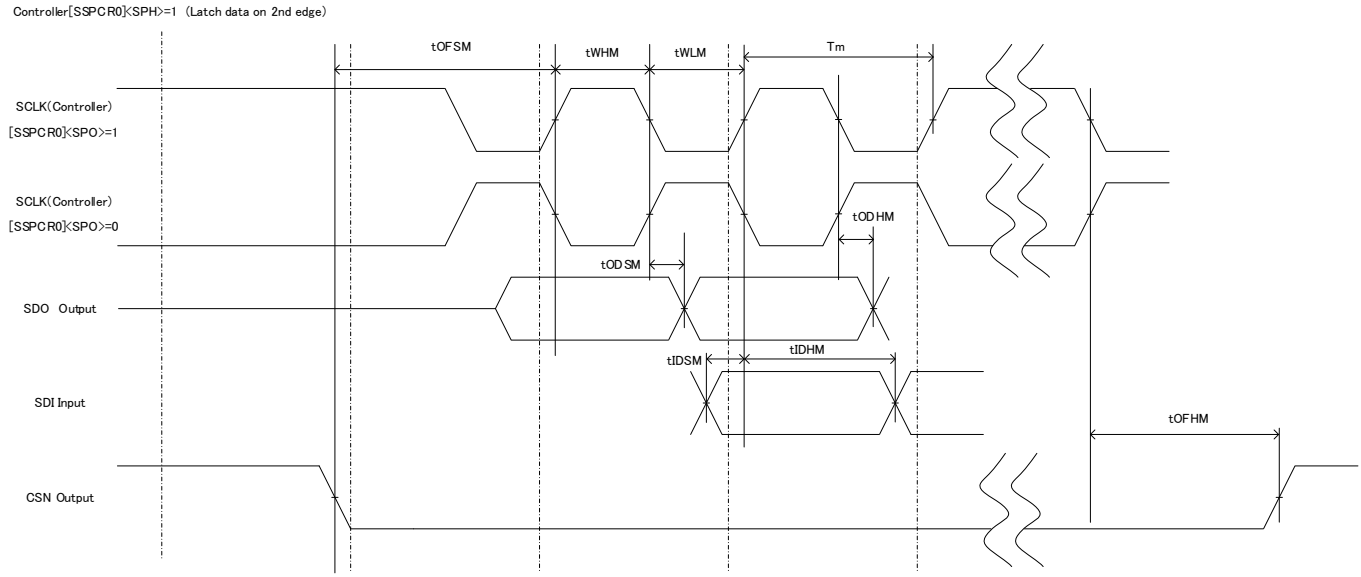


Figure 10.16.2 SPI Communication Waveform 2

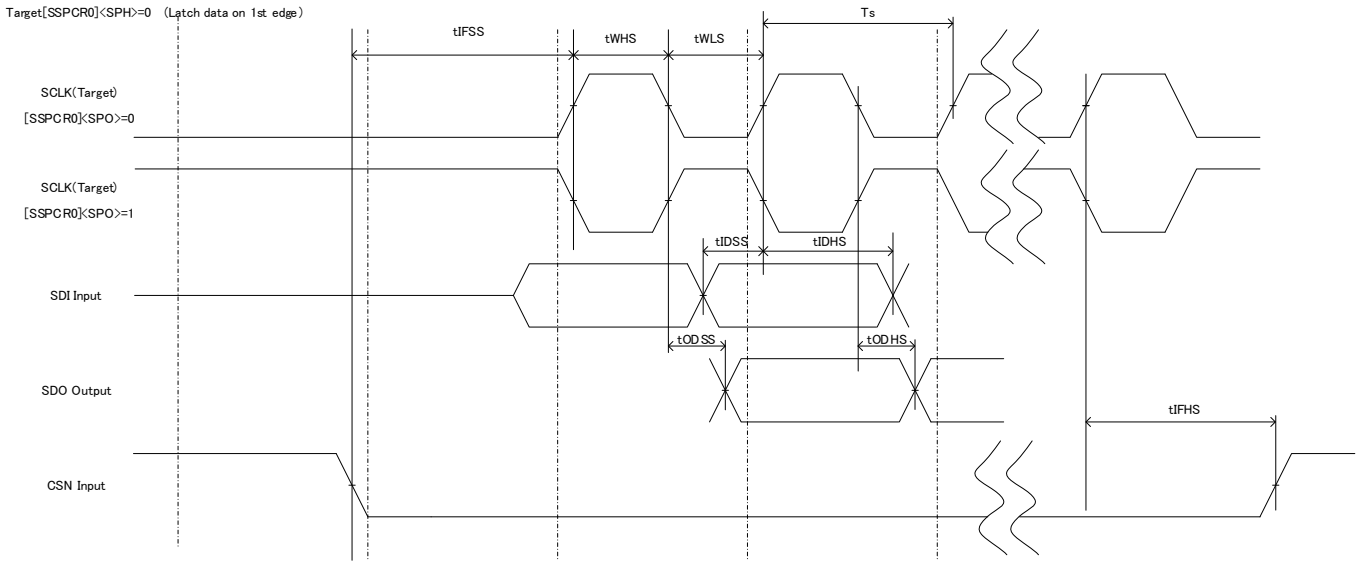


Figure 10.16.3 SPI Communication Waveform 3

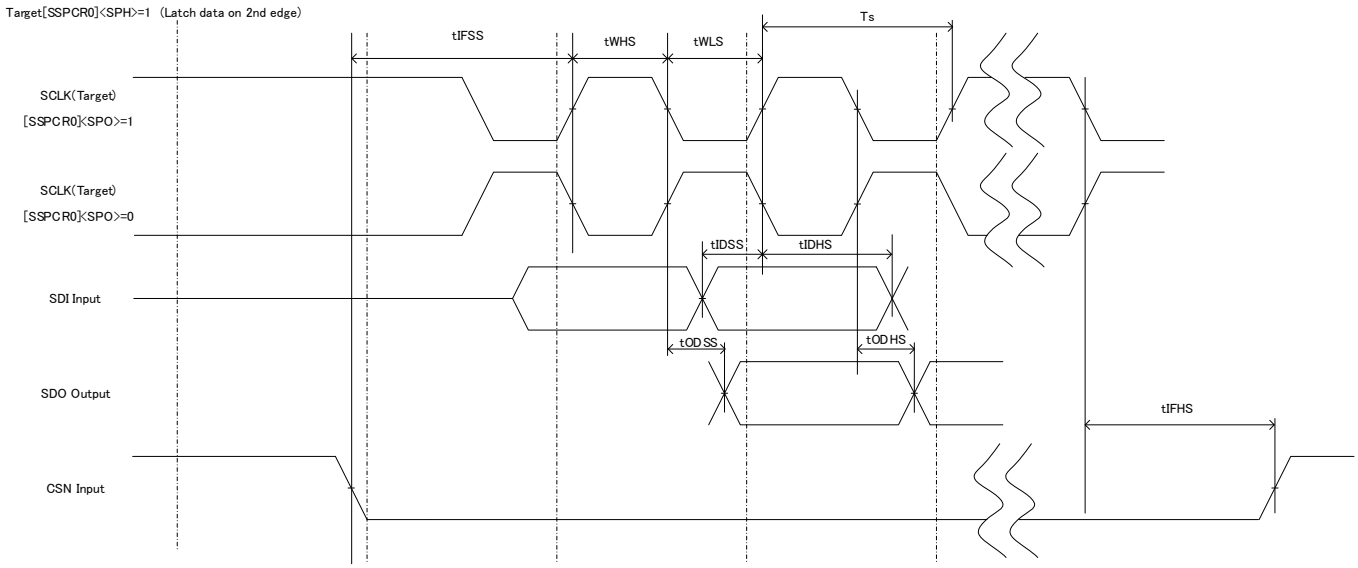


Figure 10.16.4 SPI Communication Waveform 4

10.17. UART

Table 10.17.1 Electrical Characteristics

(VB=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 150°C unless otherwise noted)

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
Transfer rate	-	UART0_TXD, UART0_RXD		-	-	1	Mbps

11. Application Circuit Example

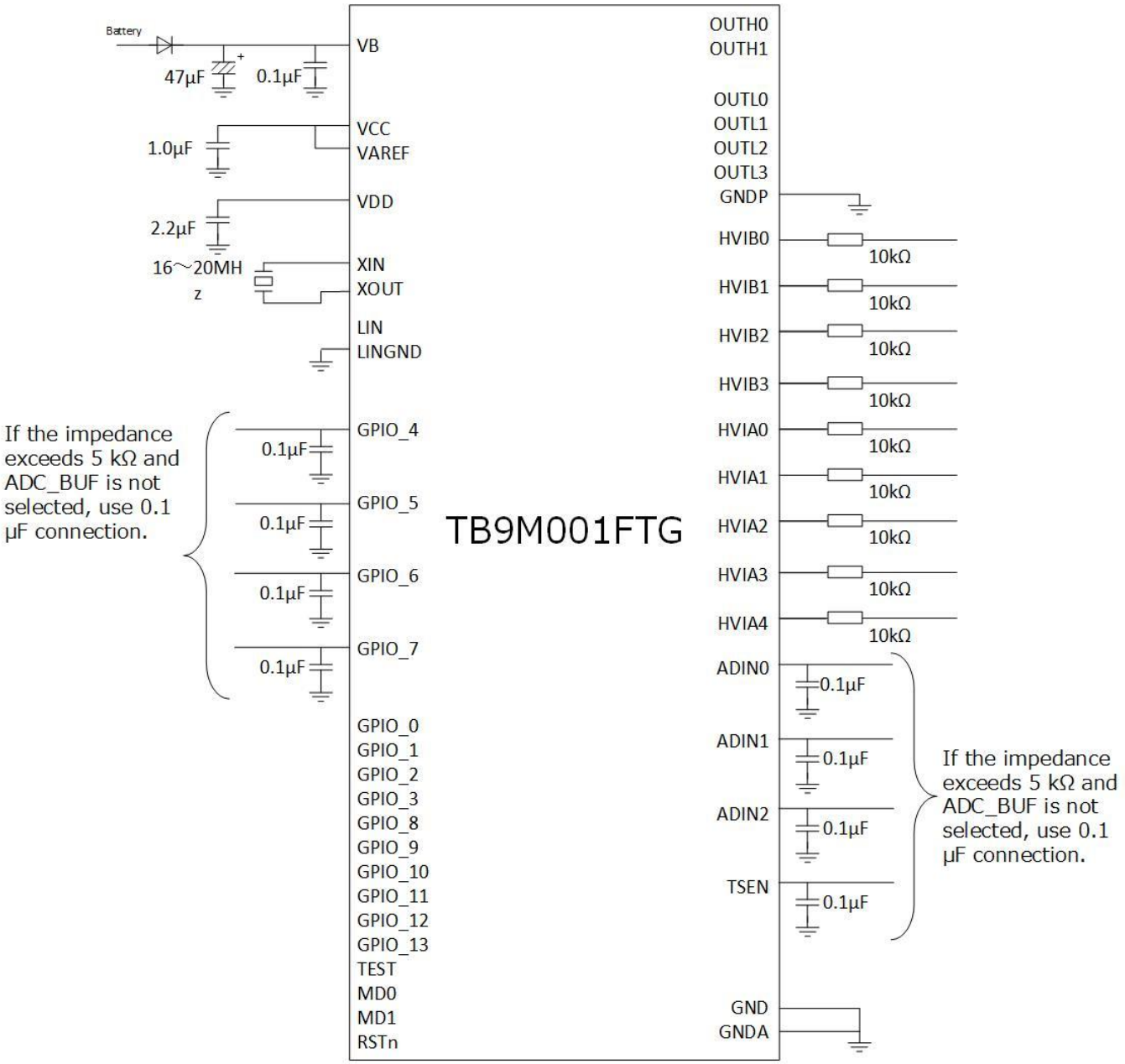
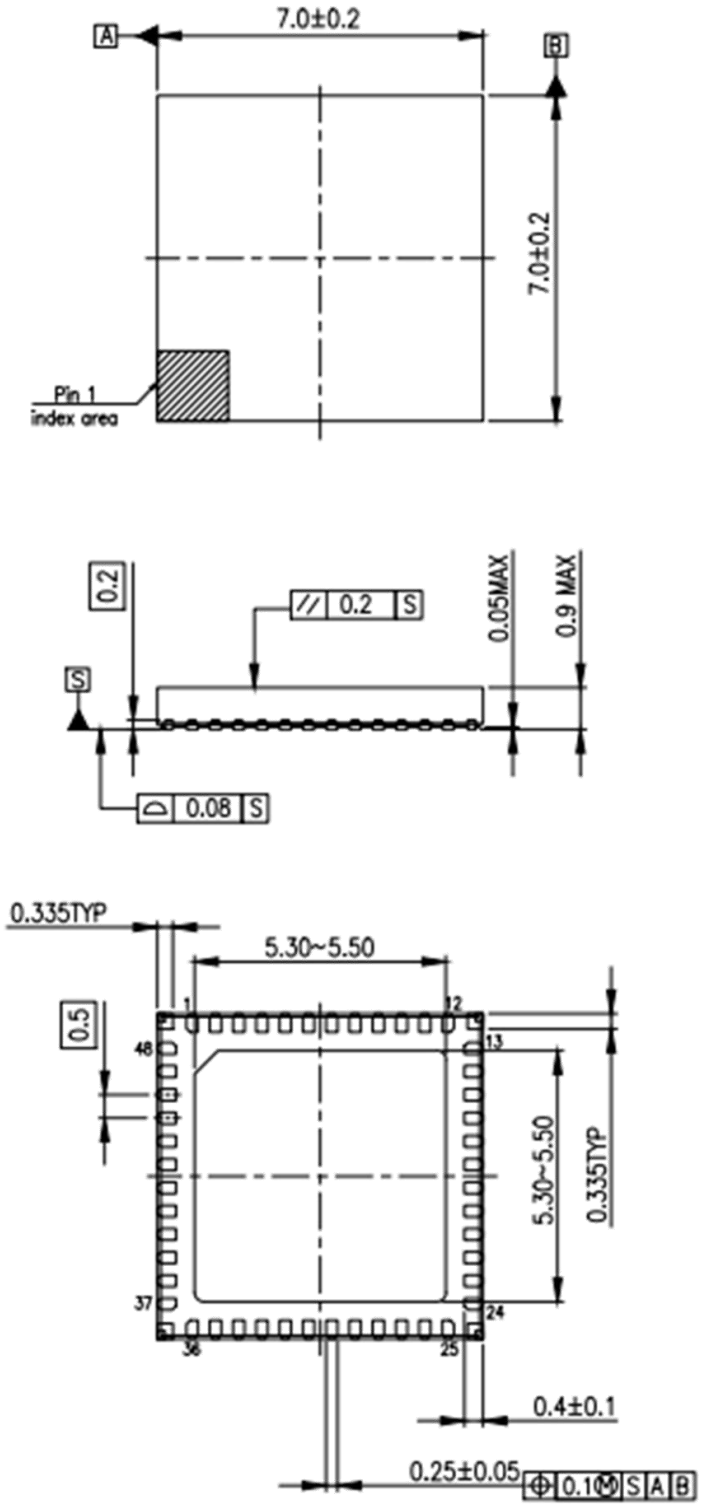


Figure 11.1 Application Circuit Example

12. Package Information

12.1. Package Dimensions

Package dimensions
P-VQFN48-0707-0.50-005
"Unit:mm"



weight: 0.13 g (typ.)

Figure 12.1 Package Dimensions

12.2. Marking

Product name : TB9M001FTG

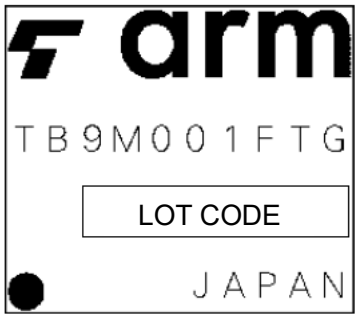
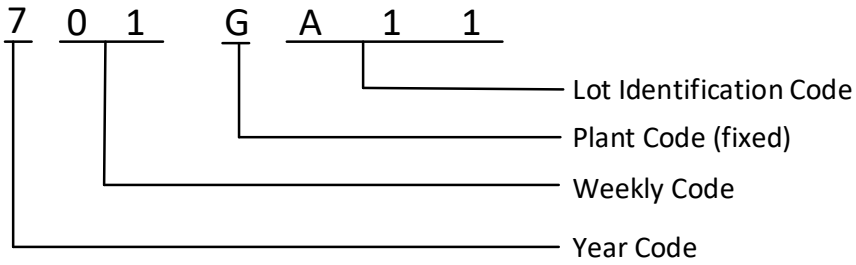


Figure 12.2 Marking

Example: Lot code breakdown



13. IC Usage Considerations

13.1. Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure.

13.2. Points to Remember on Handling of ICs

(1) Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature clears the heat generation status immediately.

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