3-Phase Brushless DC Motor Driver Using TC78B043FNG and TPD4204F

Design Guide

RD259-DGUIDE-01

Toshiba Electronic Devices & Storage Corporation

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1. Introduction

This design guide (hereinafter referred to as "this guide") explains each part of the reference design for 3-Phase Brushless DC Motor Driver Using TC78B043FNG and TPD4204F (hereinafter referred to as "this design").

In recent years, for 3-phase brushless DC motors used in home appliances and industrial equipment such as air conditioners and air purifiers, there is an increasing trend toward adopting Interior Permanent Magnet (IPM) motors (note 1) instead of Surface Permanent Magnet (SPM) motors (note 2) to achieve lower cost, higher output, and higher torque. However, IPM motors tend to generate noise, creating a demand for motor controllers capable of low-noise and highly efficient control.

The motor controller TC78B043FNG enables low-noise motor operation by high-resolution sine-wave drive and sine-wave startup control.
In addition, since it incorporates nonvolatile memory (NVM), various parameters can be adjusted using Serial Peripheral Interface (SPI) (note 3) communication to write settings into the NVM, allowing for high-efficiency motor control through adjustments such as advance-angle control.

Furthermore, since TC78B043FNG contains initial settings suitable for typical motors used in appliances such as air conditioners and air purifiers, the motor can operate without SPI-based parameter writing. The device also provides various control-setting pins (Note 4) (FGC, LATYPE, LAOFS, LA) that allow adjustment of certain parameters, such as advance-angle control, by setting terminal voltages (Note 5).

In this design, an Intelligent Power Device integrating 3-phase inverter switches and gate drivers into a compact package is used for motor drive. TPD4204F MOSFET built-in type, Maximum voltage rating 600 V, maximum output current (DC) rating 2.5 A, SSOP30 package) achieves high-efficiency motor drive in a compact PCB implementation.

Note 1: Surface Permanent Magnet (SPM) Motor:
Motor with a permanent magnet attached to the surface of the rotor.
Note 2: Interior Permanent Magnet (IPM) Motor:
Motor with a permanent magnet embedded inside the rotor.
Note 3: Serial Peripheral Interface:
Synchronous serial communication. A protocol for synchronously sending and receiving data.
Note 4: FGC: Input for setting Rotation pulse / Sine Wave Reset method
LATYPE: Input for setting Lead Angle Control type / with or without Stop Sequence
LAOFS: Input for setting Lead Angle value / SPD value offset
LA: Input for setting Maximum Lead Angle value / Fixed Lead Angle value

Note 5: TC78B043FNG allows more detailed readjustment of motor control parameters through NVM writing via SPI communication than is possible using the various control setting terminals

2. Main Components Used

This chapter describes the main components used in this design.

2.1. TOSHIBA Intelligent Power Device High Voltage 3-phase motor driver IC TPD4024F

The motor-drive section uses TPD4204F, which integrates power MOSFETs rated at 600V.
Its main features are as follows:

- High voltage power side and low voltage signal side terminal are separated.
- Supports three shunt resistance current sensing.
- Bootstrap circuit gives simple high-side supply.
- Bootstrap diodes are built in.
- A dead time can be set as a minimum of 1.4μs, and it is suitable for a Sine-wave drive.
- 3-phase bridge output using MOSFETs.
- Included over-current and under-voltage protection and shutdown, and thermal shutdown.
- The regulator of 7V (Typ.) is built in.
- The package is a surface mount type 30 pin package.

Appearance and Pin Assignment

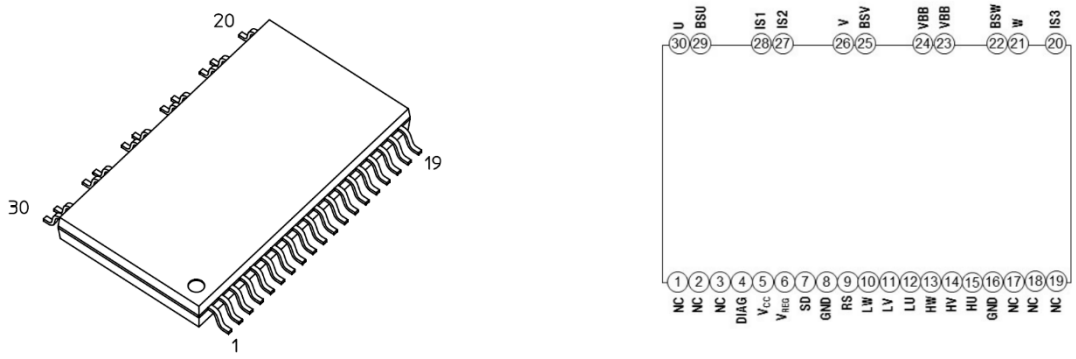

Figure 2.1 Appearance and Pin Assignment of TPD4204F

2.2. Sine Wave PWM Drive Controller for Three-phase Brushless Motor TC78B043FNG

The motor-control section uses the TC78B043FNG, a sine-wave PWM controller for 3-phase brushless motors. Its main features are as follows:

- Sine Wave PWM Drive
- The Operational Supply Voltage Range: VCC = 6V to 23V (Absolute Maximum Rating is 25V)
- Various settings are available owing to NVM and SPI communication
- Automatic Lead Angle Control or Fixed Lead Angle Control is selectable.
- Hall element Input or Hall IC Input is selectable.
- Forward Rotation and Reverse Rotation can be switched.
- Speed Control Input with Analog Voltage, PWM Duty, or SPI is selectable.
- Number of pulses for Rotation Pulse Signal Output is selectable.
- Built-in Regulator Circuit (VREG = 5V (Typ.), 35 mA (max.))
- Thermal Shut Down Function (TSD)
- Power Supply Low Voltage Detection (UVLO)
- Current Limiting Function
- Output Over-current Detection (ISD)
- Lock Protection Function

Appearance and Pin Assignment

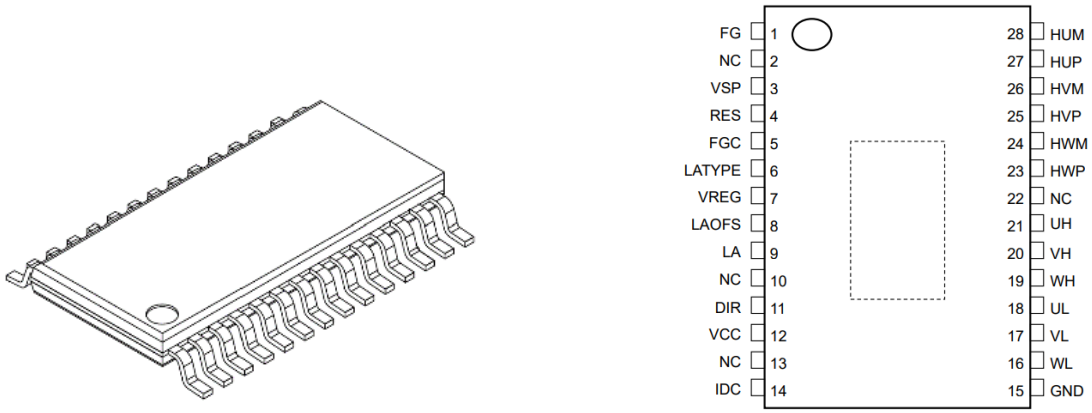

Figure 2.2 Appearance and Pin Assignment of TC78B043FNG

3. Circuit Design

3.1. Design Specifications

This design is intended for a 10-pole IPM motor. To use this design as-is, the motor must be constructed so that the rotor pole count, slot structure, and Hall-sensor placement match the geometry of the board, after which the design board should be integrated into the motor.
To use this design for a motor as it is, it is necessary to construct the motor so that the rotor pole count, slot structure, and Hall sensor placement match the board geometry, and then incorporate the design board into the motor to use it.
Therefore, when using the board, it is recommended that users refer to this design and adjust the TC78B043FNG settings, PCB dimensions, and component placement to meet their specific motor requirements.

A block diagram is shown in the original Figure 3.1, consisting of the motor-drive section using Intelligent Power Device TPD4204F and the motor-control section using TC78B043FNG.

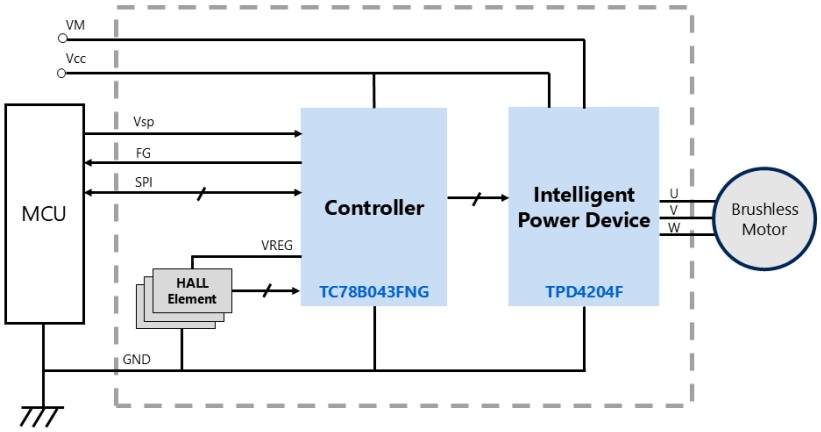

Figure 3.1 Block diagram

3.2. Motor-Drive Section – Intelligent Power Device: TPD4204F

The motor-drive section uses TPD4204F, which integrates power MOSFETs rated at 600V to implement an efficient 3-phase inverter in a compact footprint.
Figure 3.2 shows the peripheral circuit of TPD4204F.

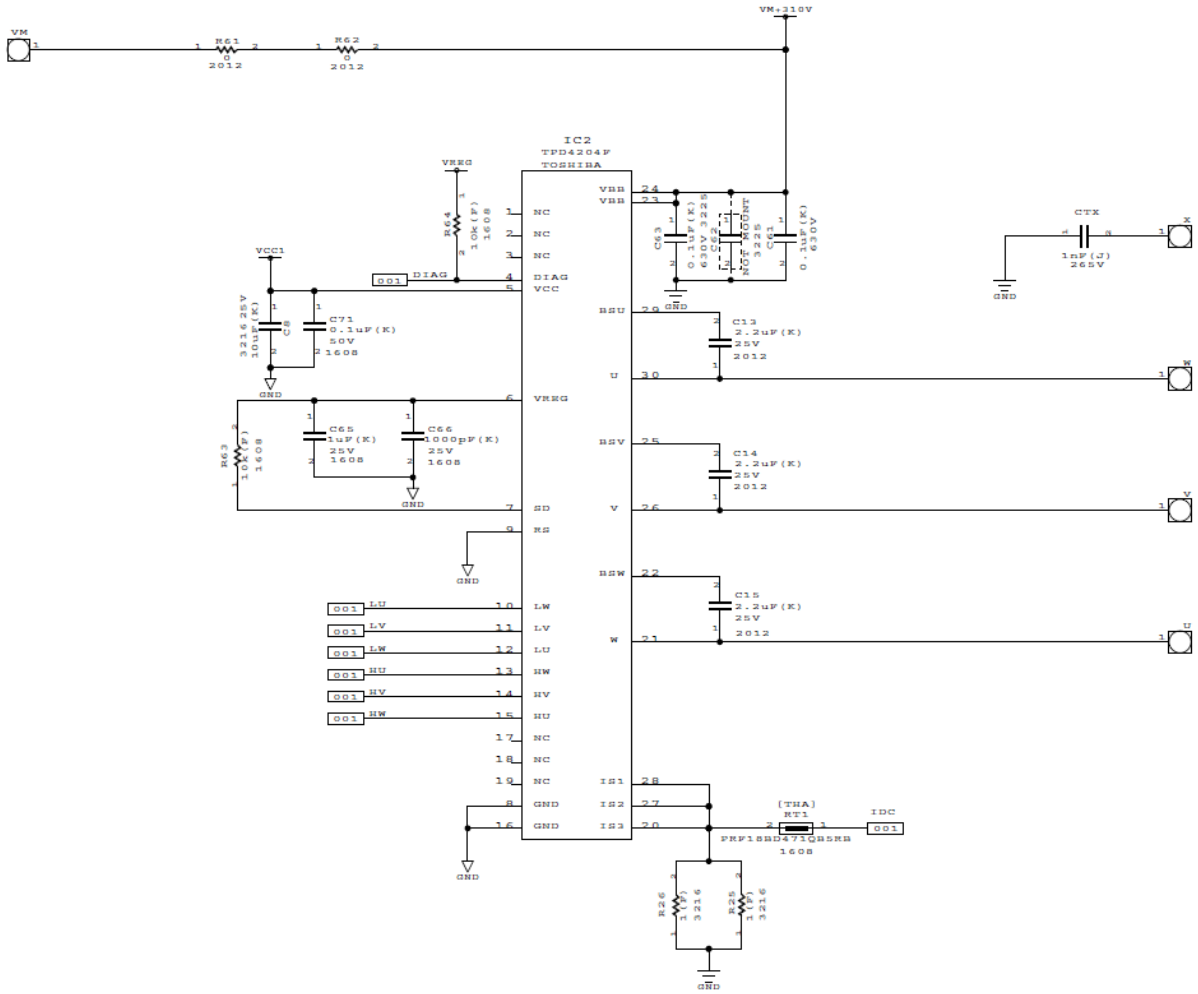

Figure 3.2 peripheral circuit of TPD4204F

3.2.1. Supply Voltage VM (VBB) and GND Pins

The VM and GND pins are used to apply the DC bus supply across the device, and external connection terminals are also provided.
R61 is 0Ω and R62 is 0.22Ω. However, they can be replaced with a proper resistance value for surge protection or with a fuse.
The fuse should be appropriately specified in terms of rated current and fuse time so that excessive current does not continue to flow in the event of an overcurrent condition or IC failure.
The bypass capacitors of the power supply C61, C62, and C63 are chosen to be sufficient for the board in this design, but the required values vary depending on the power-supply type, wiring inductance between the supply and the motor-drive circuit, the allowable supply ripple, and the motor type. In general, it is advisable to select capacitors with some margin; however, larger values increase cost and board area. Select the optimum capacitance for the actual circuit and environment. Place the capacitors as close to the pins as possible and use capacitor types with good high-frequency characteristics.
For VM and GND routing, maximize copper area and trace width to reduce wiring impedance. Avoid forming loops in the power and ground patterns to prevent noise pickup.

3.2.2. DIAG Pin

The DIAG pin is an open-drain diagnostic output. It turns ON when an abnormal condition is detected and turns OFF once the condition returns to normal. The pin is pulled up by resistor R64. Since component R65 is not mounted, the DIAG signal is not used as an abnormal input to the TC78B043FNG in this design.
Faults reported by DIAG include over-current, thermal shutdown, VCC undervoltage, and SD input assertion.

3.2.3. VCC and GND Pins

The VCC and GND pins receive the control-supply voltage. They are common with the TC78B043FNG and have external connection terminals.
Bypass capacitors C8 and C71 are sized to be sufficient for this board, but the optimal values depend on the supply type, wiring inductance, allowable ripple, and motor type. Provide adequate margin while considering size and cost tradeoffs. Place the capacitors close to the pins and use types with good high-frequency characteristics.
Widen the ground copper area to reduce impedance and avoid looped patterns to prevent noise pickup.

3.2.4. VREG Pin

The VREG pin provides a 7V (Typ.) regulator output. The voltage is stabilized with capacitors C65 and C66. Place the capacitors as close to the pin as possible and use types with good high-frequency characteristics.

3.2.5. SD Pin

This is an external protection input pin (L-active, no input hysteresis).
In this design it is pulled up to VREG by R63 so the SD function is not used.

3.2.6. RS Pin

This is a current-sense pin; it is tied to GND in this design, so the function is not used.

3.2.7. LW, LV, LU, HW, HV, HU Pins

These are control input pins connected to the commutation signal outputs of TC78B043FNG.

3.2.8. IS1, IS2, IS3 Pins

These are the source pins of the MOSFETs through which the motor phase currents flow.
In this design, the motor output current is sensed by R25 = 1Ω and R26 = 1Ω connected in parallel (effective 0.5Ω).
The voltage on the shunt resistors is detected by the IDC pin of the TC78B043FNG.
Because large motor currents flow through IS1/2/3 and the shunt resistors, make the routing area as wide and thick as possible to minimize impedance.

3.2.9. U, V, W Pins

These are the output pins connected to the motor.
Because large currents flow through these pins, use wide traces and copper areas to reduce impedance.

3.2.10. X Terminal

The X terminal connects CTX capacitor which is for countermeasure of EMI noise. Connect it to the common point of the coils if required by the application.

3.2.11. BSU, BSV, BSW Pins

These are the bootstrap-capacitor connection pins. Connect bootstrap capacitors C13, C14, and C15 accordingly.

3.3. Motor-Control Section – Controller: TC78B043FNG

The motor control section uses TC78B043FNG, which is a sine wave PWM drive controller for 3-phase brushless motor.

Figure 3.3 shows the peripheral circuit of TC78B043FNG.

The controller has default setting for motor-control settings written in its NVM. If further adjustment is required, the parameters can be set via SPI interface. This guide explains the initial configuration; for additional settings, please refer to the device datasheet.

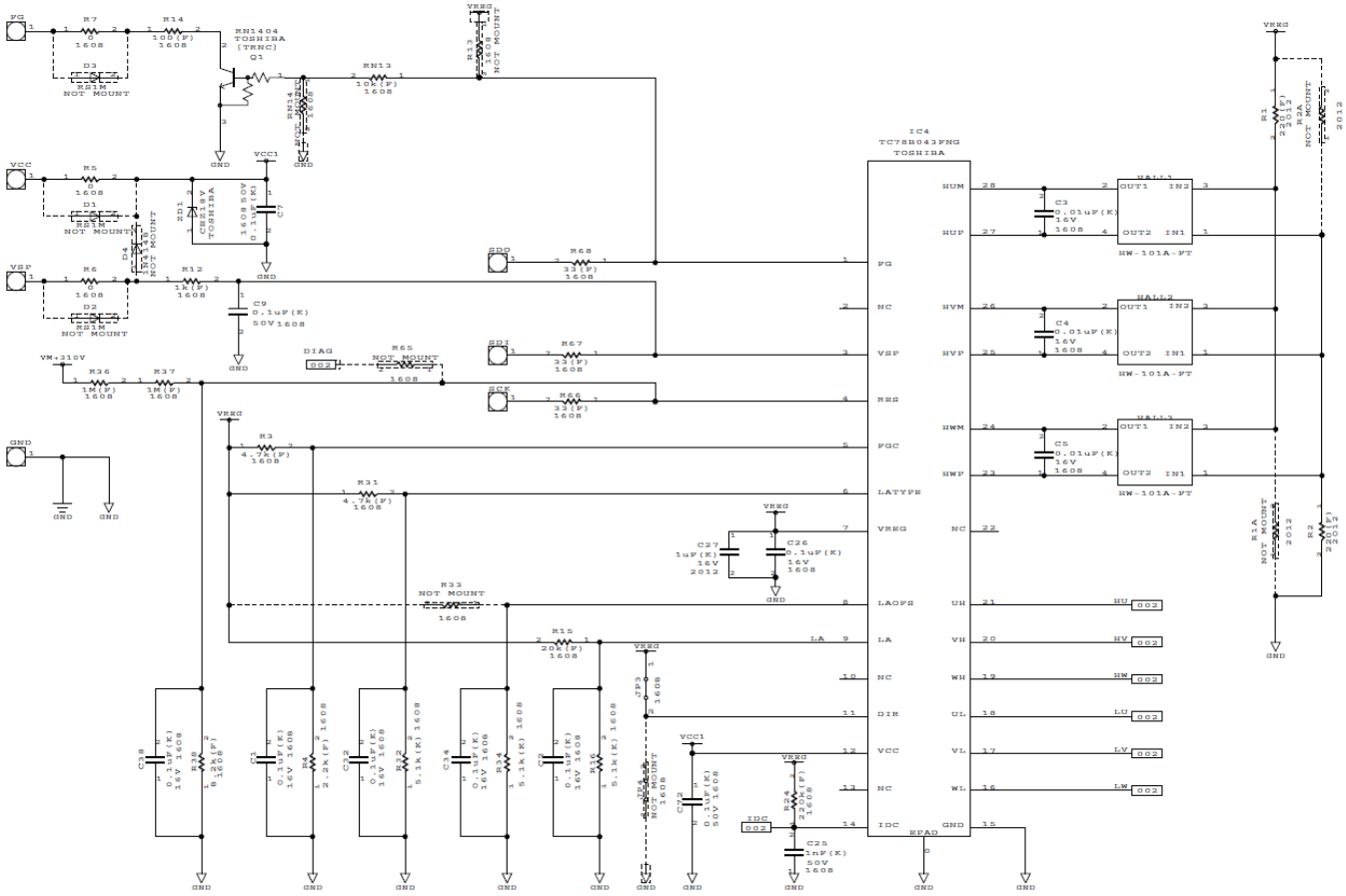

Figure 3.3 peripheral circuit of TC78B043FNG

3.3.1. VCC and GND Pins

The VCC and GND pins supply power to the controller and are common with the TPD4204F. External connection terminals are provided.
To improve ESD and surge robustness, Zener diode ZD1 is included in this design.
R5 is 0Ω and D1 is not mounted on the board. Please remove R5 and choose proper D1 for surge protection if required by application,
D4 is not mounted by default, but it can be added to protect the circuit during hot-plug insertion/removal as required.
Bypass capacitors C7 and C72 are selected to provide sufficient decoupling based on the board design. Optimal capacitance depends on the supply characteristics, wiring inductance, allowable ripple, and motor type. Place the capacitors as close to the pins as possible and use capacitor types with good high frequency characteristics. The ground copper area should be maximized to reduce impendence and avoid looped patterns to prevent noise pickup.

3.3.2. VREG Pin

The VREG pin outputs a 5V (Typ.) regulator voltage. Capacitors C26 and C27 stabilize this node. Place the capacitors as close to the pins as possible and use capacitor types with good high frequency characteristics.

3.3.3. FG (SDO) Pin

The FG pin outputs a rotation pulse signal. External connection terminal is available for monitoring.
In this design, as a measure to protect against ESD, surge, as well as against voltage application exceeding the maximum rated voltage of the FG pin, transistor Q1 is used in the signal path from FG to the external connection terminal.
R7 is 0Ω and D3 is not mounted on the board. Please remove R7 and choose proper D3 for surge protection if required by application,
The pin also serves as the SDO (SPI data-out) pin for SPI communication. An additional external terminal directly connected to SDO is provided for the SPI interface.

3.3.4. VSP (SDI) Pin

The VSP pin is the speed-control input. External terminals are provided so that motor speed can be controlled via analog voltage.
By default, TC78B043FNG is set to Mode A, starts motor when the analog voltage at the VSP pin reaches 2.1 V.
The VSP pin receives the analog voltage through a low-pass filter consisting of R12 and C9, which also allows a PWM input signal to be used.
R6 is 0Ω and D2 is not mounted on the board. Please remove R6 and choose proper D2 for surge protection if required by application,
This pin also serves as SDI (SPI data-in) pin for SPI communication. An additional external terminal connected to SDI is provided for the SPI interface.

3.3.5. RES (SCK) Pin

The RES pin is the anomaly detection input.
If RES pin voltage exceeds 1.9V (Typ.), the controller detects an abnormal condition and stops outputting drive signals.
In this design, it is used to detect over-voltage. VM is divided by R36 + R37 and R38 to generate the RES voltage. For example, VM ≈ 280V results in RES ≈ 1.1V (normal), while VM ≥ 465V results in RES ≈ 1.9V, triggering abnormal protection.
Capacitor C38 provides noise filtering for the pin.
The pin also serves as the SCK (SPI clock) pin for SPI communication. An additional external terminal connected to SCK is provided for the SPI interface.

3.3.6. FGC Pin

The FGC pin is an input pin used to set the FG pulse number, and the sine-wave reset method.
In this design, the FGC pin voltage is approximately 1.6V, generated by dividing VREG, which is 5V (Typ.), with R3 and R4, which corresponds to FG = 2.4 ppr and 60° sine-wave reset method.
Capacitor C1 provides noise filtering for the pin.

3.3.7. LATYPE Pin

The LATYPE pin is an input pin used to set the lead angle control type and to enable or disable the stop sequence is enabled.
In this design, the LATYPE pin voltage is approximately 2.6V, generated by dividing VREG, which is 5V (Typ.), with R31 and R32, which means configuring the controller to fix lead angle control and enable the stop sequence.
Capacitor C32 provides noise filtering for the pin.

3.3.8. LAOFS Pin

The LAOFS pin is an input pin used to set the offset value of lead angle or SPD.
In this design, since lead angle control is set to fixed lead angel type, there is no setting by the LAOFS pin, therefore R33 is not used; R34 pulls the pin down to GND.
Capacitor C34 provides noise filtering for the pin.

3.3.9. LA Pin

The LA pin is an input pin used to set the maximum lead angle value or the fixed lead angle value.
In this design, LA pin voltage is approximately 1V, generated by dividing VREG (5V typ.) with R15 and R16, which resulting in a lead angle of 12°.
Capacitor C2 provides noise filtering for the pin.

3.3.10. DIR Pin

The DIR pin can be used for forward/reverse rotation selection, short-brake input, and fault detection input.
In this design, the DIR pin is tied to VREG using jumper JP4, and jumper JP3 is not used.
The DIR pin is set to rotation selection by default. When the input voltage at the DIR pin is High (VREG), the motor operates in reverse rotation. Please refer to the datasheet for the timing chart of reverse rotation operation.

3.3.11. IDC Pin

The IDC pin is an input pin used as the current-limit input and over-current detection input.
In this design, the motor output current from the IS1, IS2 and IS3 pins of TPD4204F is detected using a 0.5Ω parallel resistor, composed by R25 = 1Ω and R26 = 1Ω. The voltage on the parallel resistor is monitored by IDC pin.
When the IDC voltage exceeds the internal reference voltage of 0.5 V (Typ.), the current-limiting function is activated, and the drive signal goes LOW (motor output OFF). The output is automatically restored in accordance with the PWM frequency to limit the current.
When the IDC pin voltage exceeds the internal reference voltage of 0.8V (Typ.), the over-current protection function is activated, and the drive signal goes Low (motor output OFF). Recovery occurs automatically after 10 ms, or by setting the speed command to 0 or applying refresh operation.
Therefore, in this design,

- When the motor current exceeds 1A, the IDC voltage reaches 0.5V (Typ.) and the current-limiting function operates.
  Motor current = 0.5V / 0.5Ω = 1A
- When the motor current exceeds 1.6A, the IDC voltage reaches 0.8V (Typ.) and the over-current protection function operates.
  Motor current = 0.8V / 0.5Ω = 1.6A

During current limiting, the total power dissipation on the parallel resistors (R25 and R26) is 1 W, with 0.5W applied to each resistor.
During over-current detection, the total power dissipation is 1.28W, and 0.64W is applied to each resistor momentarily.
Please select resistor ratings with sufficient power margin, taking the operating conditions into account.

In addition, C25 (1 nF) and the thermistor RT1 form a low-pass filter for noise reduction. R24 = 220kΩ pulls IDC up to VREG, when the thermistor becomes high-resistance at high temperature, IDC voltage rises accordingly, activating current-limit or over-current protection.

3.3.12. HUM, HUP, HVM, HVP, HWM, HWP Pins

These pins receive Hall-sensor signals. The Hall elements are biased using R1 (to VREG) and R2 (to GND). Capacitors C3, C4, and C5 provide noise filtering for hall signals.
Hall sensors must be properly placed on the PCB board so that they can correctly detect the polarity change of magnetic.

3.3.13. UH, VH, WH, UL, VL, WL Pins

These pins output the commutation drive signals and are connected to the control-input pins of the TPD4204F.

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