32-bit RISC Microcontroller
Reference Manual

Advanced Programmable Motor Control Circuit 2 (A-PMD2-A)

Revision 1.0

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Toshiba Electronic Devices & Storage Corporation

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
ENC	Encoder Input Circuit
PMD	Programmable Motor Control Circuit
PWM	Pulse Width Modulation
T32A	32-bit Timer Event Counter
VE	Vector Engine

1. Outlines

Advanced Programmable Motor Control Circuit 2 (henceforth PMD) controls one motor with one channel.

Function classification	Function	Operation explanation
PWM waveform generation	Basic carrier generation	Use the upper 15 bits of the 24-bit counter counted by fsys as the basic carrier. Generates sawtooth wave with constant amplitude and different period by adjusting the increment value of the counter.
	PWM carrier generation	Generates PWM carrier for U/V/W phases. - Select from 4 types of carrier waveforms for each phase. (triangle wave/sawtooth wave/reverse triangle wave/reverse sawtooth wave) - Individual phase differences can be added to the basic carrier.
	3-phase PWM generation	Generates PWM waveforms from U-/V-/W-phase carriers. - Generates 3-phase identical or 3-phase independent PWM waveforms. - Different duty cycles can be set for the first half/second half of the PWM period. (for triangle wave/reverse triangle wave)
	Conduction control	Generates X-/Y-/Z-phase PWM waveforms from U-/V-/W-phase PWM waveforms. - PWM waveform for each phase is selected from PWM output, reverse PWM output, and "high"/"low" output.
	Dead-time control	Short-circuit prevention period inserted when switching between upper and lower phases (U/X, V/Y, W/Z)
Protection function	EMG protection OVV protection	Control of output by two types of protection control (EMG and OVV) ・EMG factor is input from pin and comparator output. ・OVV factor is input from pin, AD monitoring function, and comparator output.
Inter-channel synchronization	PWM operation protection function	Master and slave channels can be linked. - Start of PWM operation - EMG protection - OVV protection
Linked control	Interrupt	- Can be generated at the carrier center, end or both Generation period can be selected (PWM half period, 1 period, 2 periods, 4 periods). Synchronous trigger generation and buffer update periods can also be aligned. ・EMG protection occurrence ・OVV protection occurrence
	Synchronous trigger generation	Output ADC conversion start trigger - Match of PWM carrier and any comparison value - Carrier center/end of basic carrier or phase-specific carrier
	Encoder control	- Generate encoder sampling timing from PWM waveform - Output information for phase detection
	Debug output	Outputs various operation timings of motor control functions to pin - AD conversion in progress - Synchronous trigger of PMD - Interrupts of ADC, PMD, VE and ENC - VE task transition - Debug output from encoder

2. Configuration

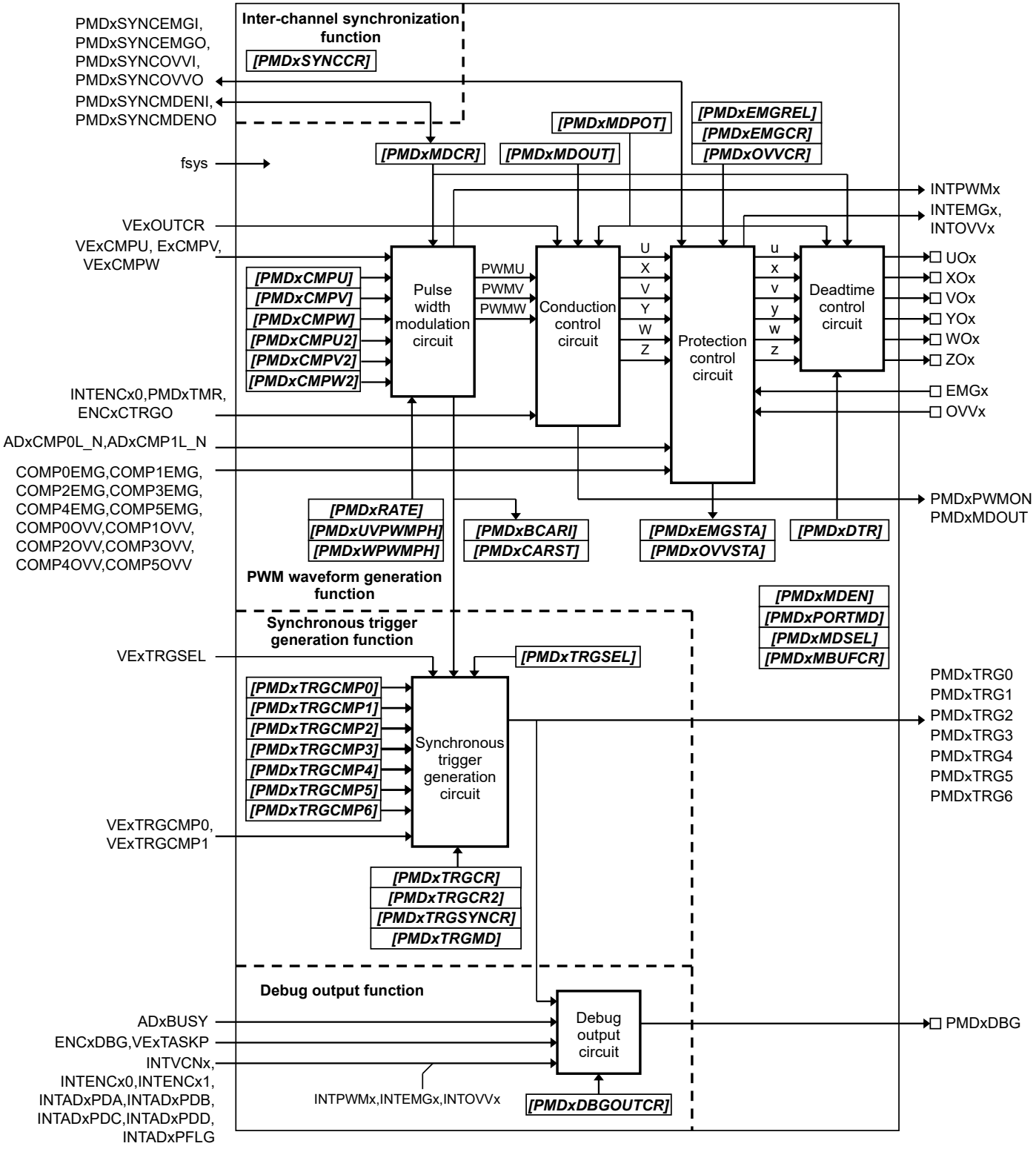

Figure 2.1 Block Diagram of PMD

Table 2.1 List of Signals

No	Signal symbol	Signal name	I/O	Related reference manual
1	fsys	System clock	Input	Clock Control and Operation Mode
2	INTADxPDA	ADC conversion completion interrupt A (Debug output)	Input	Product Information
3	INTADxPDB	ADC conversion completion interrupt B (Debug output)	Input	Product Information
4	INTADxPDC	ADC conversion completion interrupt C (Debug output)	Input	Product Information
5	INTADxPDD	ADC conversion completion interrupt D (Debug output)	Input	Product Information
6	INTADxPFLG	ADC conversion priority interrupt (Debug output)	Input	Product Information
7	ADxCMP0L_N	ADC monitor function 0 (OVV detection)	Input	Product Information
8	ADxCMP1L_N	ADC monitor function 1 (OVV detection)	Input	Product Information
9	ADxBUSY	AD conversion in progress (Debug output)	Input	Product Information
10	INTENCx0	Commutation trigger (ENC position detection synchronization) ENC interrupt 0 (Debug output)	Input	Product Information
11	ENCxCTRGO	Commutation trigger (ENC MCMP synchronization)	Input	Product Information
12	PMDxTMR	Commutation trigger (General purpose timer synchronization)	Input	Product Information
13	VExCMPU	VE U-phase PWM duty (***[VExCMPU]***)	Input	Product Information
14	VExCMPV	VE V-phase PWM duty (***[VExCMPV]***)	Input	Product Information
15	VExCMPW	VE W-phase PWM duty (***[VExCMPW]***)	Input	Product Information
16	VExTRGCMP0	VE trigger compare 0	Input	Product Information
17	VExTRGCMP1	VE trigger compare 1	Input	Product Information
18	VExTRGSEL	VE synchronous trigger output selection	Input	Product Information
19	VExOUTCR	VE conduction control/output control (***[VExOUTCR]***)	Input	Product Information
20	VExTASKP	VE task transition signal (Debug output)	Input	Product Information
21	INTVCNx	VE interrupt (Debug output)	Input	Product Information
22	COMPxEMG	COMP EMG detection	Input	Product Information
23	COMPxOVV	COMP OVV detection	Input	Product Information
24	INTENCx1	ENC interrupt 1 (Debug output)	Input	Product Information
25	ENCxDBG	ENC debug output	Input	Product Information
26	EMGx	EMG detection input	Input	Datasheet
27	OVVx	OVV detection input	Input	Datasheet
28	PMDxSYNCMDENI	Synchronous input for operation start	Input	Product Information
29	PMDxSYNCEMGI	Synchronous input for EMG protection	Input	Product Information
30	PMDxSYNCOVVI	Synchronous input for OVV protection	Input	Product Information
31	UOx	U-phase PWM output	Output	Datasheet
32	XOx	X-phase PWM output	Output	Datasheet
33	VOx	V-phase PWM output	Output	Datasheet
34	YOx	Y-phase PWM output	Output	Datasheet
35	WOx	W-phase PWM output	Output	Datasheet
36	ZOx	Z-phase PWM output	Output	Datasheet
37	PMDxDBG	Debug output	Output	Datasheet
38	INTPWMx	PWM interrupt	Output	Exception, Product Information
39	INTEMGx	EMG interrupt	Output	Exception
40	INTOVVx	OVV interrupt	Output	Exception
41	PMDxTRG0	ADC synchronous trigger output 0	Output	Product Information
42	PMDxTRG1	ADC synchronous trigger output 1	Output	Product Information
43	PMDxTRG2	ADC synchronous trigger output 2	Output	Product Information
44	PMDxTRG3	ADC synchronous trigger output 3	Output	Product Information
45	PMDxTRG4	ADC synchronous trigger output 4	Output	Product Information
46	PMDxTRG5	ADC synchronous trigger output 5	Output	Product Information
47	PMDxTRG6	ADC synchronous trigger output 6	Output	Product Information

No	Signal symbol	Signal name	I/O	Related reference manual
48	PMDxPWMON	PWM signal for ENC	Output	Product Information
49	PMDxMDOUT	PWM output control for ENC	Output	Product Information
50	PMDxSYNCMDENO	Synchronous output for operation start	Output	Product Information
51	PMDxSYNCEMGO	Synchronous output for EMG protection	Output	Product Information
52	PMDxSYNCOVVO	Synchronous output for OVV protection	Output	Product Information

3. Function and Operation

The PMD consists of a PWM waveform generation function, a synchronous trigger generation function, a debug output function, and an inter-channel synchronization function.

The PWM waveform generation function consists of a pulse width modulation circuit, a conduction control circuit, a protection control circuit, and a dead-time control circuit.

- The pulse width modulation circuit generates a PWM carrier and independent 3-phase PWM waveforms.
- The conduction control circuit determines the output patterns for the upper and lower phases of the U, V, and W phases.
- The protection control circuit performs emergency output control based on EMG detection and OVV detection.
- The dead-time control circuit prevents short circuits when switching between upper and lower phases.

The synchronous trigger generation circuit generates 7-channel trigger signals for starting ADC conversion.

The debug output function outputs a monitor signal for the operation timing of peripheral functions used for motor control.

The inter-channel synchronization function can synchronize the operation start and protection of multiple PMDs.

3.1. Clock Supply

When using PMD, the clock supply must be configured. For details, refer to “Clock Supply Setting Function” in the reference manual “Clock Control and Operating Mode”.

3.2. PWM Waveform Generation Function

The configuration of the PWM waveform generation function is shown in Figure 3.1.

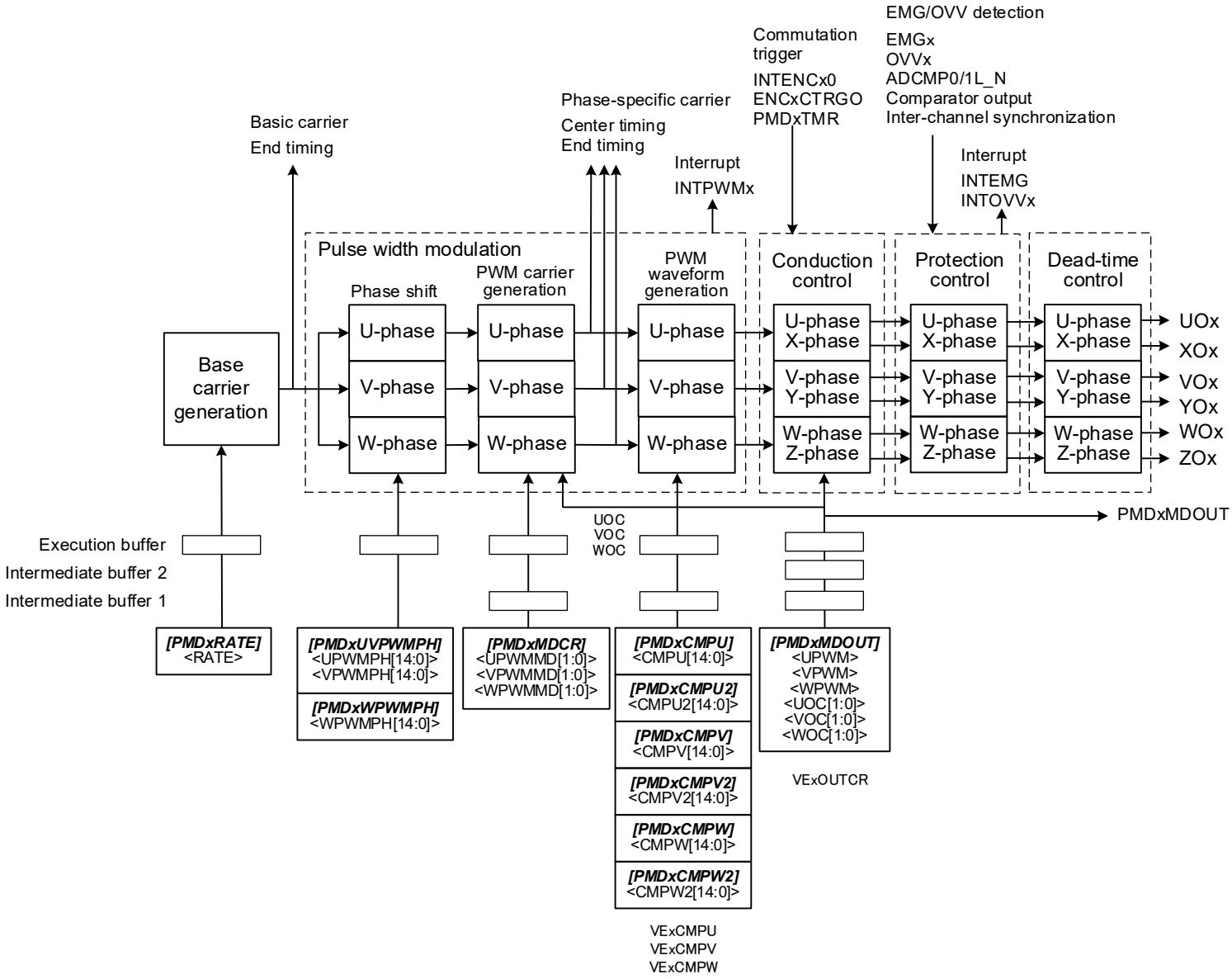

Figure 3.1 Configuration of PWM Waveform Generation Function

3.2.1. Buffers

The basic operation of the buffers is common to PWM waveform generation function and synchronous trigger generation circuit.

The value set in a register is written to a buffer at a specific timing, and the circuit operates by referencing the value in the buffer. Buffers allow the registers to be rewritten without affecting the operation.
The buffers include the execution buffer and the intermediate buffers 1 and 2. It is the value of the execution buffer that is used to control the circuit.

The update timing of the execution buffer and intermediate buffer 2 is explained in the chapters for each function.

The update timing for intermediate buffer 1 is common. Select the basic carrier or U-phase carrier with ***[PMDxMBUFCR]***<BUFCTRSEL> and set the timing with ***[PMDxMBUFCR]***<BUFCTR[2:0]>.
When ***[PMDxMDEN]*** <PWMEN> = 0 or EMG protection status, writing to the register will also update the intermediate buffer 1.

Table 3.1 Update Timing of Intermediate Buffer 1

[PMDxMBUFCR] **<BUFCTR[2:0]>**	**Update timing**
000	Intermediate buffer 1 invalid
001	Carrier end timing
010	Carrier center timing
011	Carrier 3/4 timing
100	Carrier 1/4 timing
101	Carrier center and end timing
110	Carrier 1/4 and 3/4 timing

When a register is read, the last written value can be read. Buffer values cannot be read.

3.2.2. Basic Carrier Generation

The basic carrier is generated by a 24-bit counter that counts up with fsys. 15 of the upper bits of the 24-bit counter are used as the basic carrier.

When counting, the value of ***[PMDxRATE]*** is added. The PWM frequency can be calculated using the following formula.

$$\text{PWM frequency} = \frac{\text{fsys [Hz]}}{2^{24} / \textbf{[PMDxRATE]}\ \text{value}}$$

Note: Denominator values are rounded to the nearest whole number.

By adjusting the added value, a sawtooth wave with constant amplitude and different PWM period is generated as shown in Figure 3.2. Thus, the value of a certain duty cycle will be the same regardless of the period.

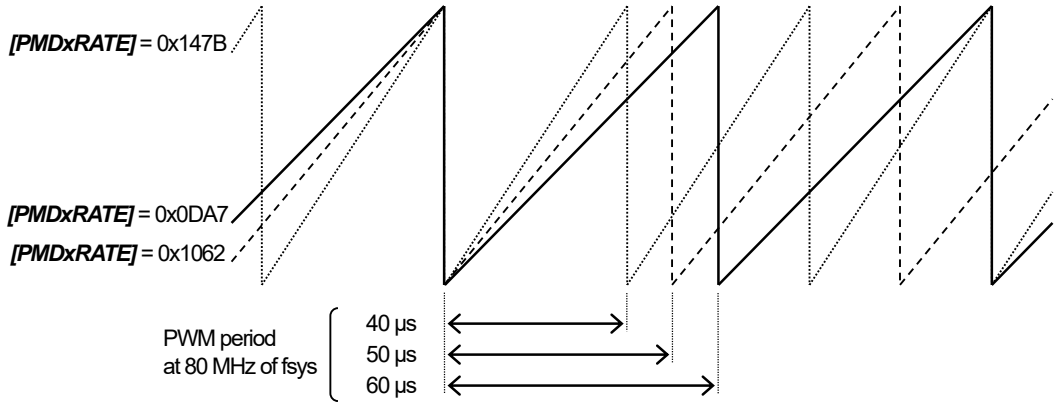

Figure 3.2 Basic Carrier Waveform

[PMDxRATE] has a dual buffer configuration with an execution buffer. The execution buffer is updated at each basic carrier end. If ***[PMDxMDPOT]***<PSYNCS[1:0]> = 00 or ***[PMDxMDEN]***<PWMEN> = 0, writing to ***[PMDxRATE]*** will also update the execution buffer.

3.2.3. Pulse Width Modulation Circuit

The pulse width modulation circuit converts the U-/V-/W-phase carrier, which is phase-shifted from the basic carrier, into PWM carriers and generates PWM waveforms using the PWM carriers.

3.2.3.1. Phase-specific Carrier Generation

The phase-specific carriers are generated by phase shifting the basic carrier.

The phase differences are set by ***[PMDxUVPWMPH]***<UPWMPH[14:0]>, <VPWMPH[14:0]> and ***[PMDxWPWMPH]***<WPWMPH[14:0]>, and the set values are added to the basic carrier.

The set value of the phase difference is the ratio to the PWM period multiplied by 2^{15}.

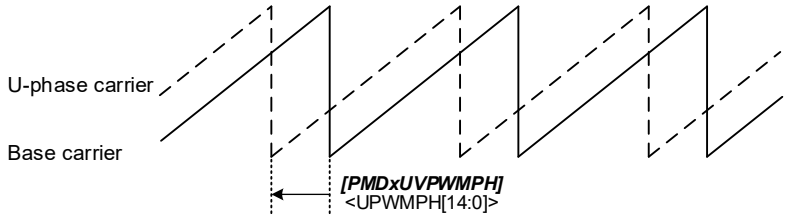

Figure 3.3 Phase Shift Diagram (U-phase)

[PMDxUVPWMPH]<UPWMPH[14:0]>, <VPWMPH[14:0]> and ***[PMDxWPWMPH]***<WPWMPH[14:0]> have a dual buffer configuration with an execution buffer. The execution buffers are updated at each basic carrier end.

3.2.3.2. PWM Carrier Generation

The phase-specific carriers are converted to generate phase-specific PWM carriers.

Sawtooth wave, triangle wave, reverse sawtooth wave, or reverse triangle wave can be selected as PWM carriers. The PWM carrier is selected by ***[PMDxMDCR]***<UPWMMD[1:0]>, <VPWMMD[1:0]>, and <WPWMMD[1:0]>.

The PWM carrier can also be inverted by setting <UOC[1:0]>, <VOC[1:0]>, <WOC[1:0]> of ***[PMDxMDOUT]*** or VExOUTCR (***[VExOUTCR]*** setting from VE) to "00". ***[PMDxMDOUT]*** and VExOUTCR are switched by ***[PMDxMODESEL]***<MDSEL1>.

The waveform of the PWM carrier is shown in Figure 3.4.

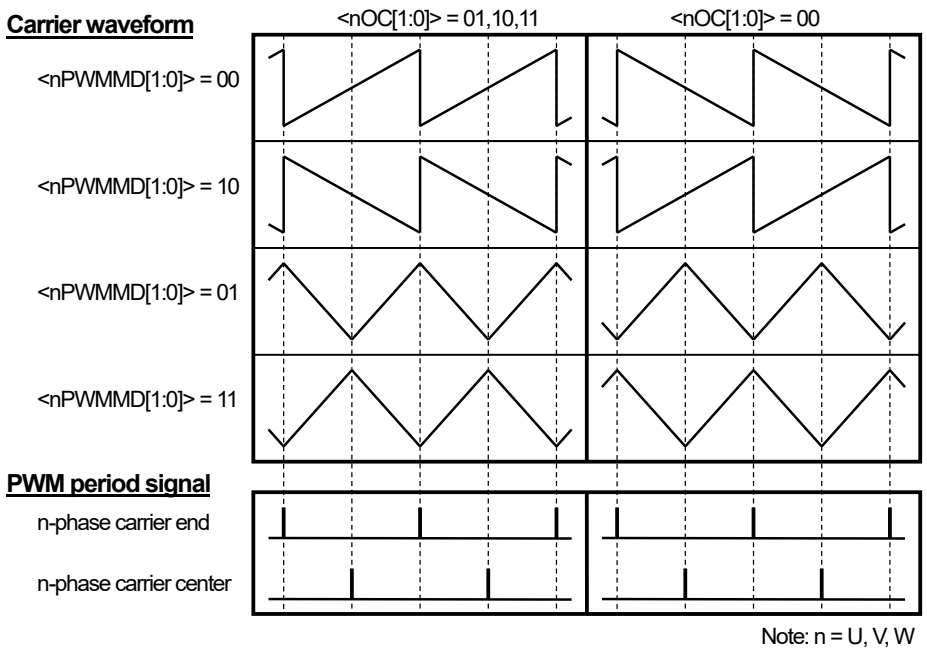

Figure 3.4 PWM Carrier Waveform

For the buffer configuration and the update timing of the execution buffer for ***[PMDxMDOUT]***/VExOUTCR, refer to "3.2.4 Conduction Control Circuit".

[PMDxMDCR]<UPWMMD[1:0]>, <VPWMMD[1:0]>, and <WPWMMD[1:0]> have a configuration with two buffers: execution buffer and intermediate buffer 1.

For sawtooth wave and reverse sawtooth wave, the update timing of the execution buffer is phase-specific carrier end.

The update timing of the execution buffer in the case of triangle wave and reverse triangle wave is shown in Table 3.2.

Table 3.2 Update Timing of Execution Buffers (PWM Carrier Generation: Triangle Wave/Reverse Triangle Wave)

[PMDxMDPOT]		Update timing
<PSYNCSDIS>	<PSYNCS[1:0]>	
1	xx	Basic carrier end
0	00	Writing to the register
	01	Phase-specific carrier center
	10	Phase-specific carrier end
	11	Phase-specific carrier end/center

Note: xx: Don't care

Execution buffer updates can be thinned. Setting ***[PMDxMDCR]***<INTPRD[1:0]> allows execution buffer updates to be thinned along with interrupt thinning. Thinning is enabled by setting ***[PMDxMDCR]***<DCMEN> to "1".

3.2.3.3. PWM Waveform Generation

PWM waveforms of the desired duty cycle are generated from phase-specific PWM carriers and comparison values.

The following two modes are available for PWM waveform generation, which are selected by ***[PMDxMDCR]***<DTYMD>.

- 3-phase independent duty mode
  Generates 3-phase independent PWM waveforms from the respective comparison values of U/V/W phases.
  Used to generate arbitrary drive waveforms such as sine waves.
- 3-phase common duty mode
  The comparison value of U phase is also used for V phase and W phase to generate identical 3-phase PWM waveforms.
  Used for square-wave drive of brushless DC motors.

The PWM waveforms for each PWM carrier are shown.

(1) In case of sawtooth wave

Figure 3.5 shows the PWM waveform when the PWM carrier is a sawtooth wave.

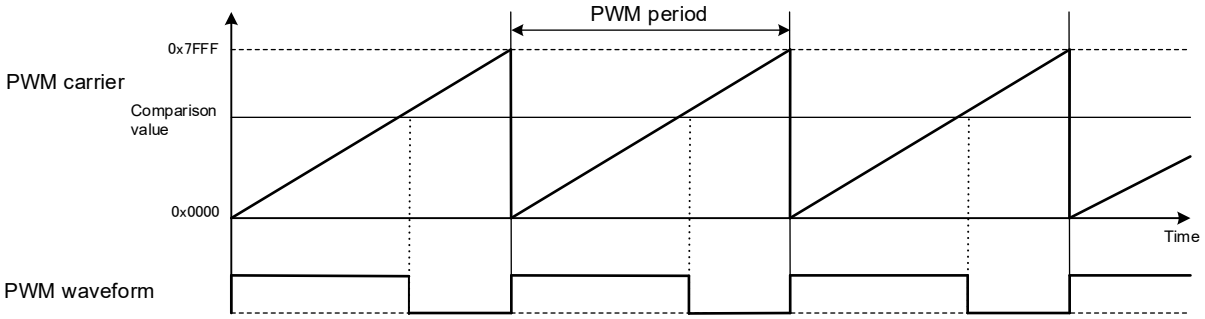

Figure 3.5 PWM Waveform (Sawtooth Wave)

[PMDxCMPU], ***[PMDxCMPV]***, ***[PMDxCMPW]*** or VExCMPU, VExCMPV, VExCMPW from VE can be selected as comparison values.

Table 3.3 Comparison Value Selection (Sawtooth Wave/Reverse Sawtooth Wave)

[PMDxMODESEL] **<MDSEL0>**	***[PMDxMDCR]*** **<CMPSEL>**	**Comparison value**
0	0	***[PMDxCMPn]***
1	0	VExCMPn

n = U, V, W

(2) In case of triangle wave

When the PWM carrier is triangle wave, the following (a) control is possible. When the PWM carrier is reverse triangle wave, either (a) or (b) control is possible.

(a) Use the same comparison value for both the first and second halves of the period (Figure 3.6)
(b) Use different comparison values for the first and second halves of the period (Figure 3.7)

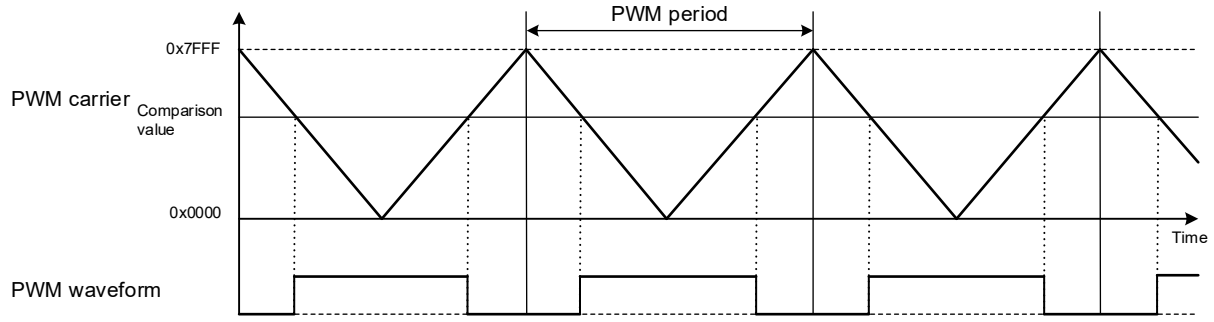

Figure 3.6 PWM Waveform (Triangle Wave (a))

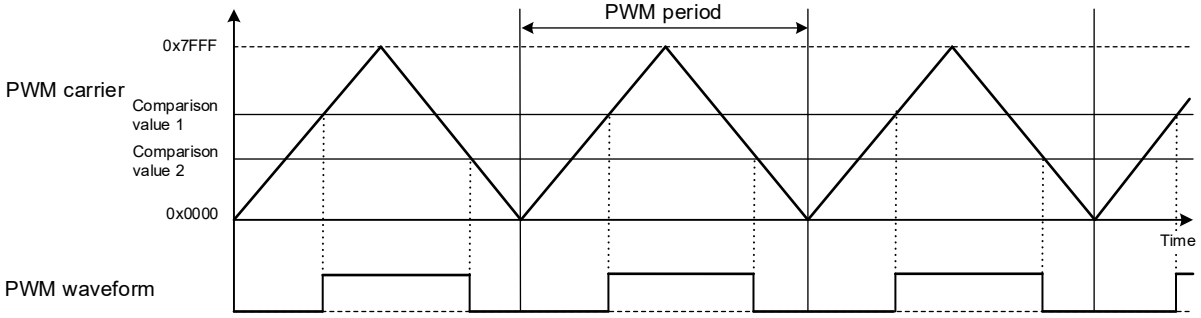

Figure 3.7 PWM Waveform (Triangle Wave (b))

Table 3.4 shows the comparison value selections.

In case (a), the comparison value can be selected from ***[PMDxCMPU]***, ***[PMDxCMPV]***, ***[PMDxCMPW]*** or VExCMPU, VExCMPV, VExCMPW from VE. (No.1, 4)

In case (b), the comparison value for the first half period is ***[PMDxCMPU]***, ***[PMDxCMPV]***, and ***[PMDxCMPW]***. The comparison value for the second half period is ***[PMDxCMPU2]***, ***[PMDxCMPV2]***, and ***[PMDxCMPW2]*** (No.2, 3) or VExCMPU, VExCMPV, and VExCMPW (No.5, 6) from VE can be selected. Use ***[PMDxMDCR]*** <DSYNCS[1:0]> with "11" (updated at phase-specific carrier end and center). Intermediate buffer 1 must be disabled.

Table 3.4 Comparison Value Selection (Triangle Wave/Reverse Triangle Wave)

No.	*[PMDxMODESEL] <MDSEL0>*	*[PMDxMDCR] <CMPSEL>*	*[PMDxMODESEL] <DCMPEN>*	*[PMDxMDCR] <DSYNCS[1:0]>*	*[PMDxMDCR] <nPWMMD[1:0]>*	*[PMDxMDOUT] VExOUTCR <nOC[1:0]>*	Comparison value	
							First half	Second half
1	0	0	-	-	-	-	*[PMDxCMPn]*	
2		1		11	01	00	*[PMDxCMPn]*	*[PMDxCMPn2]*
3					11	01/10/11		
4	1	-	0	-	-	-	VExCMPn	
5			1	11	01	00	*[PMDxCMPn]*	VExCMPn
6					11	01/10/11		

n = U, V, W

The comparison values have a configuration with two buffers: execution buffer and intermediate buffer 1.
For sawtooth wave and reverse sawtooth wave, the update timing of the execution buffer is phase-specific carrier end.

The update timing of the execution buffer in the case of triangle wave and reverse triangle wave is shown in Table 3.5.
If ***[PMDxMDEN]*** <PWMEN> = 0, writing to the register will also update the execution buffer.

Table 3.5 Update Timing of Execution Buffers (PWM Waveform Generation: Triangle Wave/Reverse Triangle Wave)

[PMDxMDCR]			Update timing
<DSYNCSDIS>	<DSYNCS[1:0]>	<INTPRD[1:0]>	
1	xx	xx	Basic carrier end
0	00	01,10,11	Phase-specific carrier end
		00	Phase-specific carrier center/end
	01	xx	Phase-specific carrier center
	10	xx	Phase-specific carrier end
	11	xx	Phase-specific carrier center/end

xx: Don't care

Execution buffer updates can be thinned. Setting ***[PMDxMDCR]***<INTPRD[1:0]> allows execution buffer updates to be thinned along with interrupt thinning. Thinning is enabled by setting ***[PMDxMDCR]***<DCMEN> to "1".

3.2.3.4. Interrupt

Interrupts are generated synchronously with the basic carrier. Interrupts are generated at the carrier end, center, or both.

Depending on the carrier waveform and settings, interrupts are generated at the timings shown in Table 3.6.

Table 3.6 Interrupt Timing

Carrier waveform	*[PMDxMDCR]*		Interrupt timing
	<INTPRD[1:0]>	<PINT>	
Sawtooth wave Reverse sawtooth wave	01/10/11	-	Basic carrier end
Triangle wave Reverse triangle wave	00	-	Basic carrier end and center
	01/10/11	0	Basic carrier center
		1	Basic carrier end

When the interrupt timing is only for the basic carrier end or center, the interrupts can be thinned out by setting ***[PMDxMDCR]*** <INTPRD[1:0]>. Every 1 period, every 2 periods, or every 4 periods can be set.

3.2.4. Conduction Control Circuit

The conduction control circuit generates the lower X-/Y-/Z-phase waveforms from the upper U-/V-/W-phase PWM waveforms. The signals for each phase can also be fixed at a "High" or "Low" level.

Table 3.7 shows the signals generated by ***[PMDxMDCR]***<SYNTMD> setting and ***[PMDxMDOUT]*** setting or VExOUTCR (***[VExOUTCR]*** set value) from VE. "PWM_N" represents the inversion of the PWM waveform.
Table 3.7 shows the case when ***[PMDxMDPOT]***<POLH> and <POLL> are "1" (high active). When "0" (low active), it is inverted by the dead-time control circuit.
Switching between ***[PMDxMDOUT]*** and VExOUTCR is selected by ***[PMDxMODESEL]***<MDSEL1>.

Table 3.7 Signal Control of Conduction Control Circuit

[PMDxMDCR]<SYNTMD> = 0

[PMDxMDOUT]**<nPWM>** ***[VExOUTCR]*****<nPWM>**		**0: H/L output**		**1: PWM output**	
		Upper phase	**Lower phase**	**Upper phase**	**Lower phase**
[PMDxMDOUT]**<nOC[1:0]>** ***[VExMDOUT]*****<nOC[1:0]>**	**00**	Low	Low	PWM	PWM_N
	01	Low	High	Low	PWM
	10	High	Low	PWM	Low
	11	High	High	PWM	PWM_N

[PMDxMDCR]<SYNTMD> = 1

[PMDxMDOUT]**<nPWM>** ***[VExOUTCR]*****<nPWM>**		**0: H/L output**		**1: PWM output**	
		Upper phase	**Lower phase**	**Upper phase**	**Lower phase**
[PMDxMDOUT]**<nOC[1:0]>** ***[VExMDOUT]*****<nOC[1:0]>**	**00**	Low	Low	PWM	PWM_N
	01	Low	High	Low	PWM_N
	10	High	Low	PWM	Low
	11	High	High	PWM	PWM_N

n = U, V, W

[PMDxMDOUT]/VExOUTCR have a configuration with three buffers: execution buffer, intermediate buffer 1, and intermediate buffer2. The value of execution buffer is output as PMDxMDOUT for phase detection in the encoder.

The update timing of the execution buffer is shown in Table 3.8 and Table 3.9.
If ***[PMDxMDEN]*** <PWMEN> =0 or EMG protection status, writing to the register will also update the execution buffer.

Table 3.8 Update Timing of Execution Buffers (Conduction Control: Sawtooth Wave/Reverse Sawtooth Wave)

[PMDxMDPOT] **<PSYNCDIS>**		**0**		**1**
[PMDxMDPOT] **<PSYNCS[1:0]>**		**00**	**00/10/11**	**xx**
[PMDxMDPOT] **<SYNCS[1:0]>**	**00**	Writing to the register	Phase-specific carrier end	Basic carrier end
	01	When INTENCx0 occurs	First phase-specific carrier end per INTENCx0 occurrence	First basic carrier end per INTENCx0 occurrence
	10	When PMDxTMR occurs	First phase-specific carrier end per PMDxTMR occurrence	First basic carrier end per PMDxTMR occurrence
	11	When ENCxCTRGO occurs	First phase-specific carrier end per ENCxCTRGO occurrence	First basic carrier end per ENCxCTRGO occurrence

xx: Don't care

Table 3.9 Update Timing of Execution Buffers (Conduction Control: Triangle Wave/Reverse Triangle Wave)

[PMDxMDPOT] **<PSYNCDIS>**		**0**				**1**
[PMDxMDPOT] **<PSYNCS[1:0]>**		**00**	**01**	**10**	**11**	**xx**
[PMDxMDPOT] **<SYNCS[1:0]>**	**00**	Writing to the register	Phase-specific carrier center	Phase-specific carrier end	Phase-specific carrier end/center	Basic carrier end
	01	When INTENCx0 occurs	First phase-specific carrier center per INTENCx0 occurrence	First phase-specific carrier end per INTENCx0 occurrence	First phase-specific carrier end/center per INTENCx0 occurrence	First basic carrier end per INTENCx0 occurrence
	10	When PMDxTMR occurs	First phase-specific carrier center per PMDxTMR occurrence	First phase-specific carrier end per PMDxTMR occurrence	First phase-specific carrier end/center per PMDxTMR occurrence	First basic carrier end per PMDxTMR occurrence
	11	When ENCxCTRGO occurs	First phase-specific carrier center per ENCxCTRGO occurrence	First phase-specific carrier end per ENCxCTRGO occurrence	First phase-specific carrier end/center per ENCxCTRGO occurrence	First basic carrier end per ENCxCTRGO occurrence

xx: Don't care

Execution buffer updates can be thinned. Setting ***[PMDxMDCR]***<INTPRD[1:0]> allows execution buffer updates to be thinned along with interrupt thinning. Thinning is enabled by setting ***[PMDxMDCR]***<DCMEN> to "1".

Intermediate buffer 2 is updated by the occurrence of ENCxCTRGO (commutation trigger) from ENC.
If ***[PMDxMDEN]*** <PWMEN> =0 or EMG protection status, writing to the register will also update the intermediate buffer 2.

3.2.5. Protection Control Circuit

EMG protection, OVV protection, and protection when using debug tool are available.

3.2.5.1. EMG Protection Control

The EMG protection control circuit controls the pin output of PWM waveforms by detecting EMG factors. The function is enabled by ***[PMDxEMGCR]***<EMGEN> = 1.

Note: After reset, the EMG protection control circuit is enabled.

- EMG factors

The EMG factor has a pin input (EMGx) and inputs from the comparators (CMOPxEMG).
The pin input can be enabled or disabled with ***[PMDxEMGCR]***<EMGISEL>. The active level can also be selected with ***[PMDxEMGCR]***<EMGIPOL>.
The inputs from the comparators can be enabled or disabled with ***[PMDxEMGCR]***<CPAIEN>.

The pin input has a noise filter and the noise rejection time can be selected by ***[PMDxEMGCR]***<EMGCNT[4:0]>. Setting <EMGCNT[4:0]> = 00000 disables the noise filter.

Note: Changing <EMGCNT[4:0]> or <EMGIPOL> while EMG protection control is enabled may cause EMG protection. Perform the "Return from EMG protection" operation after the change.

- EMG protection operation

When an EMG factor is detected, it immediately controls the six PWM output pins.
The pin control is set by ***[PMDxEMGCR]***<EMGMD[1:0]>. Table 3.10 shows the register settings and pin controls.

Table 3.10 Pin Control by EMG

[PMDxEMGCR] **<EMGMD[1:0]>**	**Pin status**	
	Upper phase	**Lower phase**
00	High impedance	High impedance
01	PWM waveform output	High impedance
10	High impedance	PWM waveform output
11	High impedance	High impedance

The protection operation continues until the recovery process is performed. The protection status can be confirmed with ***[PMDxEMGSTA]***<EMGST>. When <EMGST> is "1", it means EMG protection is in operation.

- EMG interrupt

The detection of an EMG factor generates an EMG interrupt (INTEMGx).

- Return from EMG protection state

After setting all the pin outputs to inactive (***[PMDxMDOUT]***<UPWM>, <VPWM>, <WPWM>, <UOC[1:0]>, <VOC[1:0]>, and <WOC[1:0]> set to "0"), write "1" to ***[PMDxEMGCR]***<EMGRS> to return from the EMG protection state. However, while any of the EMG factors is active, it is ignored even if "1" is written. Read ***[PMDxEMGSTA]***<EMGI> and confirm that all the EMG factors are inactive before performing the return process.

- Return from EMG protection state after reset

After reset, the EMG protection control is enabled, so the PMD may enter the protection state due to EMG factor detection. To recover from the EMG protection state, perform the following steps.

(1) The EMG function is selected by the function register (***[PxFRn]***) of the port.
(2) Read ***[PMDxEMGSTA]***<EMGI> and confirm that it is "1".
(3) Set <UPWM>, <VPWM>, <WPWM>, <UOC[1:0]>, <VOC[1:0]>, and <WOC[1:0]> of ***[PMDxMDOUT]*** to "0" to make all pin outputs inactive.
(4) Set ***[PMDxEMGCR]*** <EMGRS> to "1" to return from the EMG protection state.

- Disabling the EMG protection

To disable the EMG protection, set "0x5A" and "0xA5" sequentially in ***[PMDxEMGREL]***, then set ***[PMDxEMGCR]*** to "0". Perform the three steps in sequence.

3.2.5.2. OVV Protection Control

The OVV protection control circuit controls the pin output of PWM waveforms by detecting OVV factors. The function is enabled by ***[PMDxOVVCR]***<OVVEN> = 1.

- OVV factors

The OVV factor has a pin input (OVVx), ADC monitor function signals (ADxCMP0L_N, ADxCMP1L_N), and inputs from the comparators (COMPxOVV). Each can be enabled/disabled with ***[PMDxOVVCR]***<OVVISEL>, <ADIN0EN>, <ADIN1EN>, and <OVVCPAIEN>. The active level of the OVVx pin can be selected with ***[PMDxOVVCR]***<OVVIPOL>.

The pin input has a noise filter and the noise rejection time can be selected by ***[PMDxOVVCR]***<OVVCNT[4:0]>.

Note: Changing <OVVCNT[4:0]> or <OVVIPOL> with OVV enabled may cause OVV protection. Perform the "Return from OVV protection" operation after the change.

- OVV protection operation

When an OVV factor is detected, it immediately controls the six PWM output pins.

The pin control is set by ***[PMDxOVVCR]***<OVVMD[1:0]> and <OVVNOCTL>. Table 3.11 shows the register settings and pin controls. "ON" is the active level set by ***[PMDxMDPOT]***<POLH> and <POLL>, "OFF" is the inactive level.

Table 3.11 Pin Control by OVV

[PMDxEMGCR]		Pin status	
<OVVNOCTL>	**<OVVMD[1:0]>**	**Upper phase**	**Lower phase**
00	00	PWM waveform output	PWM waveform output
01		PWM waveform output	OFF
10		OFF	PWM waveform output
11		PWM waveform output	PWM waveform output
xx	00	Controlled by <OVVNOCTL>	
	01	ON	OFF
	10	OFF	ON
	11	OFF	OFF

The protection status can be confirmed with ***[PMDxOVVSTA]***<OVVST>. When <OVVST> is "1", it means OVV protection is in operation.

If OVV and EMG are detected simultaneously, EMG protection operation takes priority.

- OVV interrupt

The detection of an OVV factor generates an OVV interrupt (INTOVVx).

- Return from OVV protection state

Write "1" to ***[PMDxOVVCR]***<OVVRS> to return from the OVV protection state. However, while any of the OVV factors is active, it is ignored even if "1" is written. Read ***[PMDxOVVSTA]***<OVVI> and confirm that all the OVV factors are inactive before performing the return process.

When ***[PMDxOVVCR]***<OVVRSMD> = 0, the OVV protection state is auto-returned after the OVV factor changes to inactive. The timing of the auto-return is the U-phase carrier end or center if ***[PMDxMDCR]***<INTPRD[1:0]>=00, otherwise the U-phase carrier end.

- Disabling the OVV protection

To disable the OVV protection, set "0x5A" and "0xA5" sequentially in ***[PMDxOVVREL]***, then set ***[PMDxOVVCR]*** to "0". Perform the three steps in sequence.

3.2.5.3. Protection Control when Using Debug Tool

When using debug tool, the PMD output pin can be controlled when the CPU stops due to a debug halt.

The pin control is set by ***[PMDxPORTMD]***<PORTMD[1:0]>. Table 3.12 shows the register settings and pin controls.

If EMG is detected, EMG protection operation takes priority.

Table 3.12 Pin Control by Debug Halt

[PMDxPORTMD] **<PORTMD[1:0]>**	**Pin status**	
	Upper phase	**Lower phase**
00	High impedance	High impedance
01	High impedance	PWM waveform output
10	PWM waveform output	High impedance
11	PWM waveform output	PWM waveform output

3.2.6. Dead-time Control Circuit

The dead-time control circuit inserts dead time and inverts the polarity of the PWM waveform.

- Dead-time insertion and polarity inversion

Dead time is a function that prevents short circuits when the ON/OFF states of the upper and lower phases are reversed. When one of the phases output by the protection control circuit changes from "High" to "Low", the timing for the opposite phase to change from "Low" to "High" is delayed.

Dead time is set to ***[PMDxDTR]***<DTR[9:0]>. Resolution is 4/fsys and can be calculated by the following formula:

Dead time = (<DTR[9:0]> × 4)/fsys (Frequency)

For PWM waveforms with inserted dead time, the polarity is inverted in the case of a low-active setting. The active level is set to ***[PMDxMDPOT]***<POLH> and <POLL>.

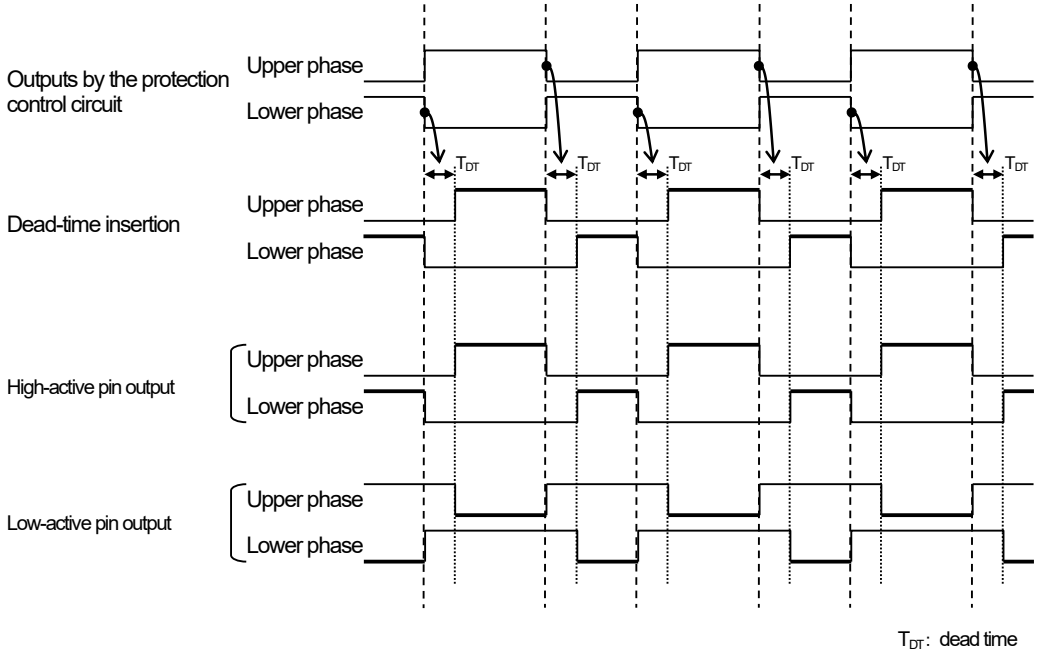

Figure 3.8 Dead-time Control

- Correction for dead time

During the dead-time period, if there is a transition from "High" to "Low" and the "High" period is eliminated, the dead time of the opposite phase can be shortened. Dead-time correction is enabled by setting ***[PMDxMDCR]*** <DTCREN> to "1".
The corrected dead time is calculated by the following formula:

Corrected dead time = Dead time (setting value)
– (Dead time (setting value) – Opposite phase "High" time)
= Opposite phase "High" time

If the upper phase goes "Low" during the dead-time period, the delay time of the lower phase becomes the "High" time of the upper phase; if the lower phase goes "Low" during the dead-time period, the delay time of the upper phase becomes the "High" time of the lower phase.

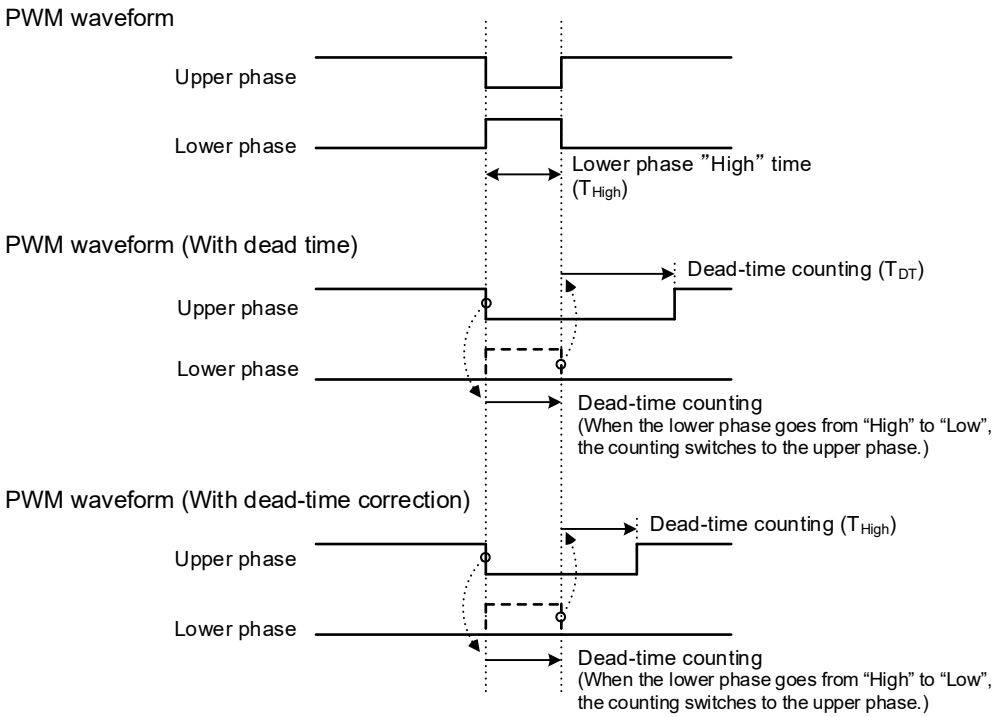

Figure 3.9 Dead-time Correction

Therefore, as shown in Figure 3.10, the dead time is corrected when the "High" time of the upper phase is long (near 100% duty) and when the "High" time of the lower phase is short (near 0% duty).

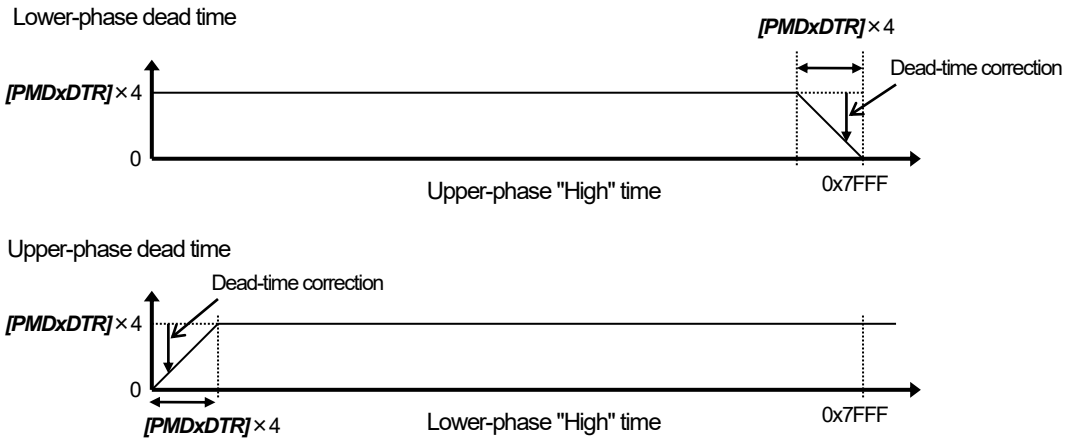

Figure 3.10 PWM Waveform "High" Time and Dead-time Correction

3.3. Synchronous Trigger Generation

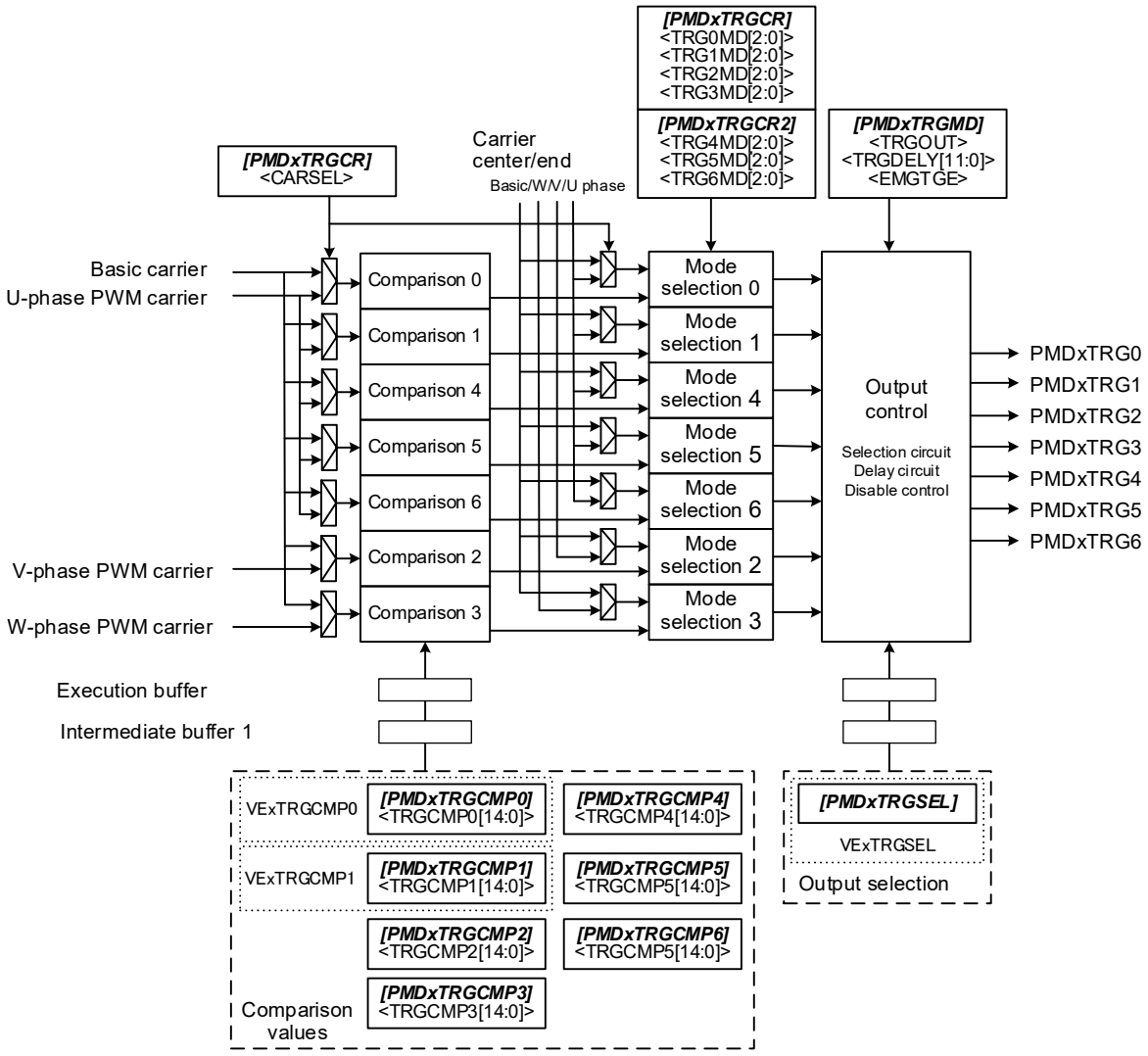

Figure 3.11 Synchronous Trigger Generation Circuit

The synchronous trigger generator circuit generates the trigger signals to start AD conversion.

The basic timing of the synchronous trigger is the match between the PWM carrier and the comparison value, and the center/end of the carrier.

The PWM carrier that generates the synchronous trigger can be selected from either the basic carrier or the U-/V-/W-phase PWM carrier determined by the trigger. The selection is set by ***[PMDxTRGCR]***<CARSEL>.

Table 3.13 Carrier Selection

Synchronous trigger number	*[PMDxTRGCR]*<CARSEL>	
	0	1
0	Basic carrier	U-phase PWM carrier
1		U-phase PWM carrier
2		V-phase PWM carrier
3		W-phase PWM carrier
4		U-phase PWM carrier
5		U-phase PWM carrier
6		U-phase PWM carrier

Output timing is selected by the following registers:

[PMDxTRGCR]<TRG0MD[2:0]>, <TRG1MD[2:0]>, <TRG2MD[2:0]>, <TRG3MD[2:0]>,
[PMDxTRGCR2]<TRG4MD[2:0]>, <TRG5MD[2:0]>, <TRG6MD[2:0]>.

Depending on the PWM carrier type, the synchronous trigger is output at the following timing. However, when ***[PMDxMDCR]***<DCMEM>=1, it is thinned out according to the interrupt period selection setting (***[PMDxMDCR]***<INTPRD[1:0]>).

Table 3.14 Synchronous Trigger Output Timing

[PMDxTRGCR] <TRGnMD[2:0]> *[PMDxTRGCR2]* <TRGmMD[2:0]>	PWM carrier type	
	Triangle wave/reverse triangle wave	Sawtooth wave/reverse saw tooth wave
000	Output disabled	Output disabled
001	Match between first half of PWM carrier and comparison value	Match between PWM carrier and comparison value
010	Match between second half of PWM carrier and comparison value	
011	Match between first/second half of PWM carrier and comparison value	
100	Carrier end	Carrier end
101	Carrier center	
110	Carrier center/end	
111	Output disabled	Output disabled

n = 0,1,2,3

m = 4,5,6

The comparison value to be compared with the carrier is set to ***[PMDxTRGCMP0]*** to ***[PMDxTRGCMP6]*** for each trigger.

Synchronous trigger outputs 0/1 can also use VExTRGCMP0 and VExTRGCMP1 from VE as the comparison value. Set ***[PMDxMODESEL]*** <MDSEL2> which one to use.

Comparison values have a configuration with two buffers: execution buffer and intermediate buffer 1. The update timing of the execution buffer is shown in Table 3.15.

If ***[PMDxMDEN]*** <PWMEN> =0, writing to the register will also update the execution buffer.

Table 3.15 Update Timing of Execution Buffers (Synchronous Trigger Generation Compare Value)

[PMDxTRGCR] <TRGnBE> ***[PMDxTRGCR2]*** <TRGmBE>	***[PMDxTRGSYNCR]*** <TSYNCS[1:0]>	***[PMDxTRGCR]*** <TRGnMD[2:0]> ***[PMDxTRGCR2]*** <TRGmMD[2:0]>	PWM carrier type	
			Triangle wave/ reverse triangle wave	Sawtooth wave/ reverse saw tooth wave
1	xx	xxx	Writing to the register	Writing to the register
0	00	000	Writing to the register	Writing to the register
		001	Carrier end	Carrier end
		010	Carrier center	
		011	Carrier center/end	
		1xx	Writing to the register	Writing to the register
	01	xxx	Carrier end	Carrier end
	10	xxx	Carrier center	
	11	xxx	Carrier center/end	

n = 0,1,2,3

m = 4,5,6

x = Don't care

Execution buffer updates can be thinned. Setting ***[PMDxMDCR]***<INTPRD[1:0]> allows execution buffer updates to be thinned along with interrupt thinning. Thinning is enabled by setting ***[PMDxMDCR]***<DCMEN> to "1".

There are two ways of outputting synchronous triggers: signals output from the mode selection circuit are output to each synchronous trigger, or the signal output from the mode selection 0 circuit is output to one of the synchronous triggers. This is set by ***[PMDxTRGMD]***<TRGOUT>.

When <TRGOUT> is "1", the output selection is determined by ***[PMDxTRGSEL]*** or VExTRGSEL from VE. When ***[PMDxMODESEL]*** <MDSEL3> is set to "0", the output is selected by ***[PMDxTRGSEL]***, and when set to "1", it is selected by VExTRGSEL.

The output selection have a configuration with two buffers: execution buffer and intermediate buffer 1.

For sawtooth wave and reverse sawtooth wave, the update timing of the execution buffer is U-phase carrier end.

The update timing of the execution buffer in the case of triangle wave and reverse triangle wave is shown in Table 3.16.

If ***[PMDxMDEN]*** <PWMEN> =0, writing to the register will also update the execution buffer.

Table 3.16 Update Timing of Execution Buffers
(Synchronous Trigger Generation Output Selection: Triangle wave/Reverse triangle wave)

[PMDxMDCR]			Update timing
<DSYNCSDIS>	<DSYNCS[1:0]>	<INTPRD[1:0]>	
1	xx	xx	Basic carrier end
0	00	01,10,11	U-phase carrier end
		00	U-phase carrier center/end
	01	xx	U-phase carrier center
	10	xx	U-phase carrier end
	11	xx	U-phase carrier center/end

xx: Don't care

Execution buffer updates can be thinned. Setting ***[PMDxMDCR]***<INTPRD[1:0]> allows execution buffer updates to be thinned along with interrupt thinning. Thinning is enabled by setting ***[PMDxMDCR]***<DCMEN> to "1".

Synchronous triggers can be output with a delay. The setting is made at ***[PMDxTRGMD]***<TRGDELY[11:0]>. The delay time can be calculated with the following formula.

Delay time = <TRGDELY[11:0]> × 1/fsys

Synchronous trigger output can be disabled during EMG protection state. The setting is made at ***[PMDxTRGMD]***<EMGTGE>.

3.4. Encoder Sampling Timing Generation

A signal (PWMxPWMON) is output to the encoder to detect the sampling timing. The PWM waveform after dead-time insertion and before polarity control is used for signal generation.

Output signal waveform differs depending on the setting of ***[PMDxMDCR]***<BEMFSAMTIMSEL>.

(1) ***[PMDxMDCR]***<BEMFSAMTIMSEL> = 0

Outputs a OR or AND of PWM waveforms.

For OR, only PWM waveforms for which ***[PMDxMDOUT]***<UPWM>, <VPWM>, and <WPWM> are "1" are valid.

Table 3.17 Encoder Sampling Timing (<BEMFSAMTIMSEL>=0)

[PMDxMDCR]			PMDxPWMON
<PWMONMD>	<DTYMD>	<PWMONORSEL[1:0]>	
1	x	0x	OR of U/V/W/X/Y/Z phases
		10	OR of U/V/W phases
		11	OR of X/Y/Z phases
0	0	0x	OR of U/V/W/X/Y/Z phases
		10	OR of U/V/W phases
		11	OR of X/Y/Z phases
	1	xx	AND of X/Y/Z phases

x: Don't care

(2) ***[PMDxMDCR]***<BEMFSAMTIMSEL> = 1

Do not use the phase shift function for U-/V-/W-phase carriers with this setting.

Pulses are output at the "High" to "Low" change timing of the signal of OR in Table 3.18.

Table 3.18 Encoder Sampling Timing (<BEMFSAMTIMSEL>=1)

[PMDxMDCR] <PWMONORSEL[1:0]>	PMDxPWMON
0x	OR of U/V/W/X/Y/Z phases
10	OR of U/V/W phases
11	OR of X/Y/Z phases

x: Don't care

However, pulses are output at the basic carrier end in periods with the following conditions:

- Duty cycle is less than 50%
- Duty cycle is 100%

Also, it does not output a pulse in a period with 0% duty cycle, but outputs a pulse at the basic carrier end if ***[PMDxMDOUT]***<UPWM>, <VPWM>, or <WPWM> is changed immediately after the start of the period.

3.5. Debug Output Function

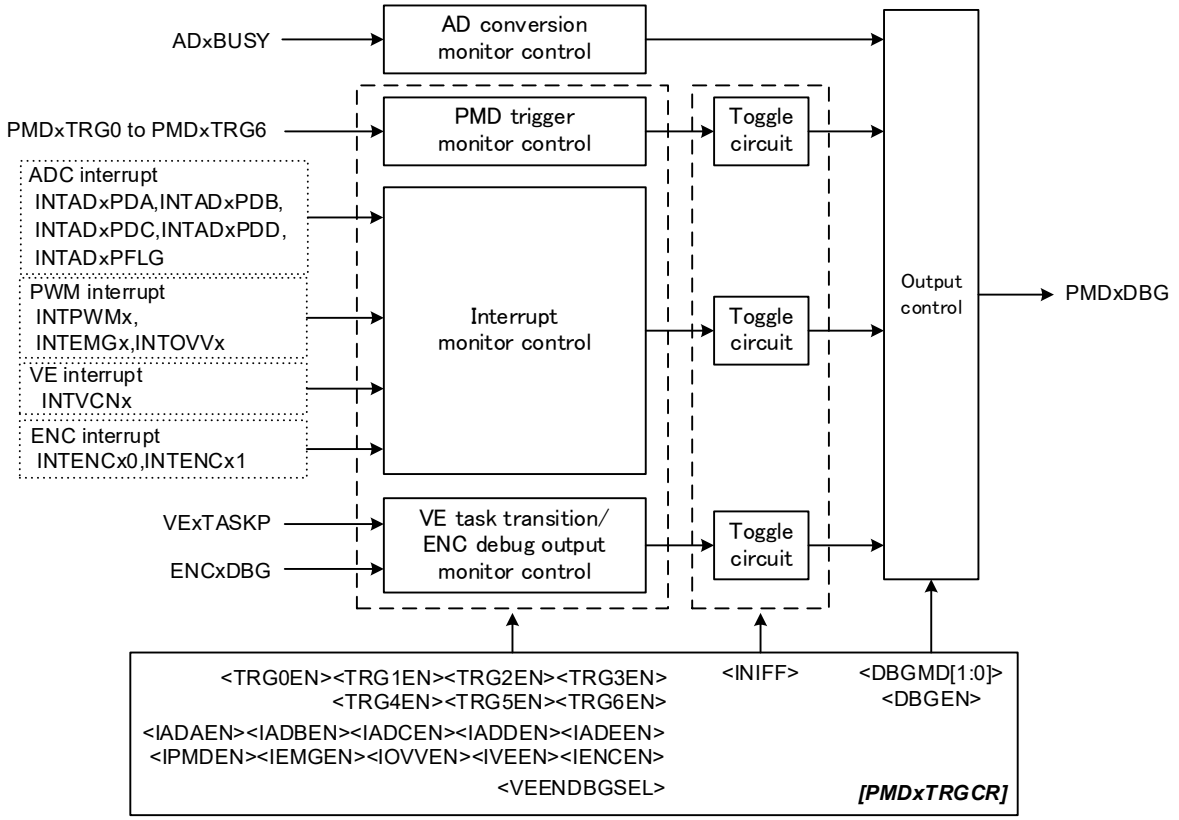

Figure 3.12 Debug Output Function

The debug output function selects and outputs the status of internal signals. This allows the internal signals to be monitored externally. The debug output function is enabled when ***[PMDxDBGOUTCR]***<DBGEN> is set to "1".

The monitor targets four types of signals: AD conversion, PMD trigger, interrupt, and VE task transition/ENC debug. The target signal selected by ***[PMDxDBGOUTCR]***<DEBGMD[1:0]> is output from PMDxDBG.

There are multiple factors to monitor PMD triggers and interrupts, and each factor can be enabled or disabled. For VE task transition and ENC debug output, select one of the factors.

The AD conversion monitor control output is "High" during AD conversion.

The PMD trigger, interrupt, and VE task transition/ENC debug output monitor control outputs have a toggle circuit that invert the output signal each time the valid factors are activated.

The initial state of the toggle circuit output can be selected. Set to ***[PMDxDBGOUTCR]***<INIFF> before enabling the debug output function.

3.6. Inter-channel Synchronization Function

For products with multiple PMD channels, synchronous operation is possible between the master and slave channels for PWM operation start, EMG detection, and OVV detection. For master and slave channels, refer to the reference manual "Product Information".

Synchronous operation is set with ***[PMDxSYNCCR]***. ***[PMDxSYNCCR]*** must be set only for the slave channel.

(1)Start of PWM operation

Setting "1" to ***[PMDxSYNCCR]***<PWMSMD> enables the function.
Setting ***[PMDxMDEN]***<PWMEN> to "1" for the master channel also starts PWM operation for the slave channel.

(2)EMG detection

Enabled by setting ***[PMDxSYNCCR]***<EMGSMD[1:0]>.
When set to "10", the EMG detection of the slave channel is disabled. The EMG protection control circuit of the slave channel is also activated by the EMG detected in the master channel.
When set to "11", the EMG detection of the slave channel is enabled. The EMG protection control circuit of the slave channel operates on EMG detected on both the master and slave channels.
In all cases, interrupts are generated on the channel where the EMG is detected.

(3)OVV detection

Enabled by setting ***[PMDxSYNCCR]***<OVVSMD[1:0]>.
When set to "10", the OVV detection of the slave channel is disabled. The OVV protection control circuit of the slave channel is also activated by the OVV detected in the master channel.
When set to "11", the OVV detection of the slave channel is enabled. The OVV protection control circuit of the slave channel operates on OVV detected on both the master and slave channels.
In all cases, interrupts are generated on the channel where the OVV is detected.

4. Registers

4.1. List of Registers

The control registers and their addresses are shown below.

Peripheral function		Channel/unit	Base address	
			TYPE1	TYPE2
Advanced programmable motor control circuit 2	A-PMD2	ch0	0x40068C00	0x400C8C00
		ch1	0x40068D00	0x400C8D00
		ch2	0x40068E00	0x400C8E00
		ch3	0x40068F00	0x400C8F00

Note: The base address type is different by products. Please refer to "Product Information" of the reference manual for the details.

Register name		Address (Base+)
PMD Enable Register	***[PMDxMDEN]***	0x0000
Port Output Mode Register	***[PMDxPORTMD]***	0x0004
PMD Control Register	***[PMDxMDCR]***	0x0008
PWM Carrier Status Register	***[PMDxCARSTA]***	0x000C
Basic Carrier Register	***[PMDxBCARI]***	0x0010
PWM Frequency Register	***[PMDxRATE]***	0x0014
PWM Duty Comparison U Register	***[PMDxCMPU]***	0x0018
PWM Duty Comparison V Register	***[PMDxCMPV]***	0x001C
PWM Duty Comparison W Register	***[PMDxCMPW]***	0x0020
Mode Selection Register	***[PMDxMODESEL]***	0x0024
PMD Conduction Control Register	***[PMDxMDOUT]***	0x0028
PMD Output Setting Register	***[PMDxMDPOT]***	0x002C
EMG Release Register	***[PMDxEMGREL]***	0x0030
EMG Control Register	***[PMDxEMGCR]***	0x0034
EMG Status Register	***[PMDxEMGSTA]***	0x0038
OVV Control Register	***[PMDxOVVCR]***	0x003C
OVV Status Register	***[PMDxOVVSTA]***	0x0040
Dead Time Register	***[PMDxDTR]***	0x0044
Trigger Comparison 0 Register	***[PMDxTRGCMP0]***	0x0048
Trigger Comparison 1 Register	***[PMDxTRGCMP1]***	0x004C
Trigger Comparison 2 Register	***[PMDxTRGCMP2]***	0x0050
Trigger Comparison 3 Register	***[PMDxTRGCMP3]***	0x0054
Trigger Control Register	***[PMDxTRGCR]***	0x0058
Trigger Output Mode Setting Register	***[PMDxTRGMD]***	0x005C
Trigger Output Selection Register	***[PMDxTRGSEL]***	0x0060
Trigger Update Timing Setting Register	***[PMDxTRGSYNCR]***	0x0064
U-phase/V-phase Phase Difference Register	***[PMDxUVPWMPH]***	0x0068
W-phase Phase Difference Register	***[PMDxWPWMPH]***	0x006C

Register name		Address (Base+)
Intermediate Buffer Control Register	***[PMDxMBUFCR]***	0x0070
Synchronization Control Register	***[PMDxSYNCCR]***	0x0074
Debug Output Control Register	***[PMDxDBGOUTCR]***	0x0078
Trigger Comparison 4 Register	***[PMDxTRGCMP4]***	0x0084
Trigger Comparison 5 Register	***[PMDxTRGCMP5]***	0x0088
Trigger Comparison 6 Register	***[PMDxTRGCMP6]***	0x008C
Trigger Control Register 2	***[PMDxTRGCR2]***	0x0090
PWM Duty Comparison U Register 2	***[PMDxCMPU2]***	0x0094
PWM Duty Comparison V Register 2	***[PMDxCMPV2]***	0x0098
PWM Duty Comparison W Register 2	***[PMDxCMPW2]***	0x009C

4.2. Register Access

Notes regarding register access are summarized below.

- Byte access to the registers of this function is prohibited.
- The registers that can be rewritten during operation (***[PMDxMDEN]***<PWMEN> = 1) are as follows.

Register name	Remarks
[PMDxMDEN]	-
[PMDxMDCR]<UPWMMD[1:0]> <VPWMMD[1:0]> <WPWMMD[1:0]>	With buffer
[PMDxRATE]	With buffer
[PMDxCMPU]	With buffer
[PMDxCMPV]	With buffer
[PMDxCMPW]	With buffer
[PMDxMODESEL]	-
[PMDxMDOUT]	With buffer
[PMDxEMGREL]	-
[PMDxEMGCR] <EMGEN><EMGRS>	-
[PMDxOVVCR] <OVVEN><OVVRS>	-
[PMDxTRGCMP0]	With buffer
[PMDxTRGCMP1]	With buffer
[PMDxTRGCMP2]	With buffer
[PMDxTRGCMP3]	With buffer
[PMDxTRGSEL]	With buffer
[PMDxTRGSYNCR]	-
[PMDxUVPWMPH]	With buffer
[PMDxWPWMPH]	With buffer
[PMDxSYNCCR] <EMGSMD[1:0]> <OVVSMD[1:0]>	When ***[PMDxEMGCR]*** <EMGEN> = 0 When ***[PMDxOVVCR]*** <OVVEN> = 0
Except ***[PMDxDBGOUTCR]*** <DBGEN>	When <DBGEN>=0

Register name	Remarks
[PMDxTRGCMP4]	With buffer
[PMDxTRGCMP5]	With buffer
[PMDxTRGCMP6]	With buffer
[PMDxCMPU2]	With buffer
[PMDxCMPV2]	With buffer
[PMDxCMPW2]	With buffer

4.3. Details of Registers

4.3.1. *[PMDxMDEN]* (PMD Enable Register)

Bit	Bit symbol	After reset	Type	Function
31:1	-	0	R	Read as "0".
0	PWMEN	0	R/W	PMD operation control 0: Stop operation 1: Start operation

Note: When the input/output port is set to the function output (PWM output), the pin outputs are disabled (High impedance) at <PWMEN> = 0.

4.3.2. *[PMDxPORTMD]* (Port Output Mode Register)

Bit	Bit symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1:0	PORTMD[1:0]	00	R/W	Setting of the pin output control at debug halt 00: Upper phase: High impedance Lower phase: High impedance 01: Upper phase: High impedance Lower phase: PMD output 10: Upper phase: PMD output Lower phase: High impedance 11: Upper phase: PMD output Lower phase: PMD output Sets the pin output when debug halt occurs.

4.3.3. *[PMDxMODESEL]* (Mode Selection Register)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0".
7	DCMPEN	0	R/W	Mode selection 4 (Note) Refer to Table 3.4 for details. 0: Comparison values are not switched. 1: Comparison values are switched. This bit selects whether to switch the comparison value of the first half/second half of the PWM carrier when the PWM carrier is a reverse triangle wave and <MDSEL0> = 1.
6:4	-	0	R	Read as "0".
3	MDSEL3	0	R/W	Mode Selection 3 This bit selects which register to use. 0: Use PMD register ***[PMDxTRGSEL]*** 1: Use VE register ***[VExTRGSEL]***
2	MDSEL2	0	R/W	Mode Selection 2 This bit selects which registers to use. 0: Use PMD registers ***[PMDxTRGCMP0]***, ***[PMDxTRGCMP1]*** 1: Use VE registers ***[VExTRGCMP0]***, ***[VExTRGCMP1]***
1	MDSEL1	0	R/W	Mode Selection 1 This bit selects which register to use. 0: Use PMD register ***[PMDxMDOUT]*** 1: Use VE register ***[VExOUTCR]***
0	MDSEL0	0	R/W	Mode Selection 0 This bit selects which registers to use. 0: Use PMD registers ***[PMDxCMPU]***, ***[PMDxCMPV]***, ***[PMDxCMPW]***、 ***[PMDxEMGCR]***<EMGRS> 1: Use VE registers ***[VExCMPU]***, ***[VExCMPV]***, ***[VExCMPW]***

Note: Intermediate buffer 1 must be disabled (***[PMDxMBUFCR]***<BUFCTR[2:0]> = 000) when comparison value switching is enabled.

4.3.4. *[PMDxMDCR]* (PMD Control Register)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as "0".
30:29	PWMONORSEL	00	R/W	PWMxPWMON generation logic (2) 00: OR of U/V/W/X/Y/Z phases 01: OR of U/V/W/X/Y/Z phases 10: OR of U/V/W phases 11: OR of X/Y/Z phases The logical OR of the PWM waveforms of the specified phases is output to PWMxPWMON.
28	BEMFSAMTIMSEL	0	R/W	PWMxPWMON signal pulse output 0: Disabled 1: Enabled When enabled, pulse signals are output when the OR signal selected by <PWMONORSEL> changes from "High" to "Low". Also, the output timing is controlled by the duty cycle. When using this function, the phase shift function of the U-/V-/W-phase carrier cannot be used.
27:26	-	0	R	Read as "0".
25	PWMOCTBUFEN	0	R/W	***[PMDxMDOUT]*** intermediate buffer 2 control 0: Disabled 1: Enabled
24	PWMONMD	0	R/W	PWMxPWMON generation logic (1) 0: Depends on <DTYMD> setting When <DTYMD>=0, it depends on <PWMONORSEL> setting. When <DTYMD>=1, it is the AND of X/Y/Z phases. 1: Depends on <PWMONORSEL> setting
23:20	-	0	R/W	Write as "0".
19:18	-	0	R	Read as "0".
17	CMPSEL	0	R/W	Switching of the comparison value for PWM waveform generation (Note) 0: Disabled 1: Enabled When enabled, the comparison value for PWM waveform generation is switched between the first half and second half. This setting is valid when the PWM carrier is a reverse triangle wave and ***[PMDxMODESEL]***<MDSEL0> = 0. For waveforms other than reverse triangle wave, set it to "0".
16	DSYNCSDIS	0	R/W	Update timing of the execution buffer in PWM duty comparison register 0: <DSYNCS[1:0]> setting is valid 1: Updated at the basic carrier end
15:14	WPWMMD[1:0]	00	R/W	W-phase PWM carrier selection 00: Sawtooth wave 01: Triangle wave 10: Reverse sawtooth wave 11: Reverse triangle wave
13:12	VPWMMD[1:0]	00	R/W	V-phase PWM carrier selection 00: Sawtooth wave 01: Triangle wave 10: Reverse sawtooth wave 11: Reverse triangle wave
11:10	UPWMMD[1:0]	00	R/W	U-phase PWM carrier selection 00: Sawtooth wave 01: Triangle wave 10: Reverse sawtooth wave 11: Reverse triangle wave

Bit	Bit symbol	After reset	Type	Function
9:8	DSYNCS[1:0]	00	R/W	Update timing of the execution buffer in PWM duty comparison register 00: The timing depends on the interrupt period setting <INTPRD[1:0]> When <INTPRD[1:0]> = 00, phase-specific carrier end and center When <INTPRD[1:0]> = other than 00, phase-specific carrier end 01: Update at phase-specific carrier center. 10: Update at phase-specific carrier end. 11: Update at phase-specific carrier end and center. This setting is valid when the PWM carrier is a triangle wave or reverse triangle wave.
7	DTCREN	0	R/W	Dead-time correction control 0: Disabled 1: Enabled
6	DCMEN	0	R/W	Thinning control of the execution buffer update and the synchronous trigger output 0: Disabled 1: Enabled When 2-period interrupt or 4-period interrupt are selected (<INTPRD[1:0]> = 10,11), execution buffer update and ADC synchronous trigger output are thinned. The target execution buffers are as follows: ***[PMDxMDCR]***<UPWMMD[1:0]>, <VPWMMD[1:0]>, <WPWMMD[1:0]>, ***[PMDxCMPU]***, ***[PMDxCMPV]***, ***[PMDxCMPW]***, ***[PMDxCMPU2]***, ***[PMDxCMPV2]***, ***[PMDxCMPW2]***, ***[PMDxMDOUT]***, ***[PMDxTRGCMP0]***, ***[PMDxTRGCMP1]***, ***[PMDxTRGCMP2]***、 ***[PMDxTRGCMP3]***, ***[PMDxTRGCMP4]***, ***[PMDxTRGCMP5]***、 ***[PMDxTRGCMP6]***, ***[PMDxTRGSEL]***
5	SYNTMD	0	R/W	Pin output mode setting Conduction control is performed in conjunction with the setting of ***[PMDxMDOUT]***. Refer to Table 3.7 for details.
4	DTYMD	0	R/W	Duty mode selection 0: 3-phase common ***[PMDxCMPU]*** is used for U/V/W phase, 1: 3-phase independent ***[PMDxCMPU]***, ***[PMDxCMPV]***,and ***[PMDxCMPW]*** are used for each phase.
3	PINT	0	R/W	PWM interrupt timing selection 0: U-phase carrier center 1: U-phase carrier end This setting is valid when the PWM carrier is a triangle wave or reverse triangle wave and other than <INTPRD[1:0]> = 00.
2:1	INTPRD[1:0]	00	R/W	PWM interrupt period selection 00: U-phase carrier every half period (valid for triangle wave or reverse triangle wave) 01: U-phase carrier every 1 period 10: U-phase carrier every 2 periods 11: U-phase carrier every 4 periods This bit selects the frequency of the PWM interrupt request.
0	-	0	R	Read as "0".

Note: Intermediate buffer 1 must be disabled (***[PMDxMBUFCR]***<BUFCTR[2:0]> = 000) when comparison value switching is enabled.

4.3.5. *[PMDxCARSTA]* (PWM Carrier Status Register)

Bit	Bit symbol	After reset	Type	Function
31:3	-	0	R	Read as "0".
2	PWMWST	0	R	W-phase carrier state 0: First half of period 1: Second half of period
1	PWMVST	0	R	V-phase carrier state 0: First half of period 1: Second half of period
0	PWMUST	0	R	U-phase carrier state 0: First half of period 1: Second half of period

4.3.6. *[PMDxBCARI]* (Basic Carrier Register)

Bit	Bit symbol	After reset	Type	Function
31:15	-	0	R	Read as "0".
14:0	BCARI[14:0]	0x0000	R	Basic carrier readout When the PMD function is enabled, the value of the basic carrier can be read. When the PMD function is disabled, the value of ***[PMDxRATE]*** / 2^{10} can be read.

4.3.7. *[PMDxRATE]* (PWM Frequency Register)

Bit	Bit symbol	After reset	Type	Function
31:15	-	0	R	Read as "0".
14:0	RATE[14:0]	0x0000	R/W	PWM frequency setting Set the value of "0x0010" or more. When the value less than "0x0010" is set, it will operate as "0x0010". (When read, the set value can be read.) The set value can be calculated using the following formula: PWM frequency / fsys x 2^{24}

4.3.8. PWM Duty Comparison Register

4.3.8.1. *[PMDxCMPU]* (PWM Duty Comparison U Register)

Bit	Bit symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:0	CMPU[15:0]	0x0000	R/W	U-phase PWM duty cycle setting 0x0000 to 0x8000 These bits set the value to be compared with the U-phase PWM carrier.

4.3.8.2. *[PMDxCMPV]* (PWM Duty Comparison V Register)

Bit	Bit symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:0	CMPV[15:0]	0x0000	R/W	V-phase PWM duty cycle setting 0x0000 to 0x8000 These bits set the value to be compared with the V-phase PWM carrier.

4.3.8.3. *[PMDxCMPW]* (PWM Duty Comparison W Register)

Bit	Bit symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:0	CMPW[15:0]	0x0000	R/W	W-phase PWM duty cycle setting 0x0000 to 0x8000 These bits set the value to be compared with the W-phase PWM carrier.

4.3.8.4. *[PMDxCMPU2]* (PWM Duty Comparison U Register 2)

Bit	Bit symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:0	CMPU2[15:0]	0x0000	R/W	U-phase PWM duty cycle setting 2 0x0000 to 0x8000 These bits set the value to be compared with the second half of the U-phase PWM carrier.

4.3.8.5. *[PMDxCMPV2]* (PWM Duty Comparison V Register 2)

Bit	Bit symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:0	CMPV2[15:0]	0x0000	R/W	V-phase PWM duty cycle setting 2 0x0000 to 0x8000 These bits set the value to be compared with the second half of the V-phase PWM carrier.

4.3.8.6. *[PMDxCMPW2]* (PWM Duty Comparison W Register 2)

Bit	Bit symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:0	CMPW2[15:0]	0x0000	R/W	W-phase PWM duty cycle setting 2 0x0000 to 0x8000 These bits set the value to be compared with the second half of the W-phase PWM carrier.

4.3.9. Carrier Phase Difference Register

4.3.9.1. *[PMDxUVPWMPH]* (U-phase/V-phase Phase Difference Register)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as "0".
30:16	UPWMPH[14:0]	0x0000	R/W	U-phase carrier phase difference setting 0x0000 to 0x7FFF The phase difference from the basic carrier is set.
15	-	0	R	Read as "0".
14:0	VPWMPH[14:0]	0x0000	R/W	V-phase carrier phase difference setting 0x0000 to 0x7FFF The phase difference from the basic carrier is set.

4.3.9.2. *[PMDxWPWMPH]* (W-phase Phase Difference Register)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as "0".
30:16	-	0x0000	R/W	Write as "0".
15	-	0	R	Read as "0".
14:0	WPWMPH[14:0]	0x0000	R/W	W-phase carrier phase difference setting 0x0000 to 0x7FFF The phase difference from the basic carrier is set.

4.3.10. *[PMDxMDPOT]* (PMD Output Setting Register)

Bit	Bit symbol	After reset	Type	Function
31:10	-	0	R	Read as "0".
9:8	SYNCS[1:0]	00	R/W	Execution buffer update timing of conduction control 00: Writing to register 01: INTENCx0: At ENC interrupt generation. 10: PMDxTMR: At general purpose timer interrupt generation. 11: ENCxCTRGO: At ENC MCMP validity generation. This bit selects the execution buffer update timing of the conduction control register in conjunction with <PSYNCS[1:0]>, <PSYNCDIS>.
7:5	-	0	R	Read as "0".
4	PSYNCDIS	0	R/W	Execution buffer update control for PWM carrier generation and conduction control 0: Depends on the setting of <PSYNCS[1:0]> 1: Basic carrier end This bit selects the execution buffer update timing of the conduction control register in conjunction with <PSYNCS[1:0]>, <SYNCS[1:0]>. This bit selects the execution buffer update timing of the PWM carrier generation in conjunction with <PSYNCS[1:0]>.
3	POLH	0	R/W	Selection of the output polarity of the upper-phase outputs (UOx, VOx, and WOx). 0: Low active 1: High active
2	POLL	0	R/W	Selection of the output polarity of the lower-phase outputs (XOx, YOx, and ZOx). 0: Low active 1: High active
1:0	PSYNCS[1:0]	00	R/W	Execution buffer update timing of PWM carrier generation and conduction control 00: Writing to register 01: Phase-specific carrier center 10: Phase-specific carrier end 11: Phase-specific carrier end and center This bit selects the execution buffer update timing of the conduction control in conjunction with <SYNCS[1:0]> and <PSYNCDIS>. This bit selects the execution buffer update timing of the PWM carrier generation in conjunction with <PSYNCDIS>. For sawtooth wave and reverse sawtooth wave, any setting other than "00" updates with the phase-specific carrier end.

4.3.11. *[PMDxMDOUT]* (PMD Conduction Control Register)

Bit	Bit symbol	After reset	Type	Function
31:11	-	0	R	Read as "0".
10	WPWM	0	R/W	W-phase signal control 0: "High"/"Low" output 1: PWM output This bit controls the W-phase signal in conjunction with <WOC[1:0]> and ***[PMDxMDCR]***<SYNTMD>.
9	VPWM	0	R/W	V-phase signal control 0: "High"/"Low" output 1: PWM output This bit controls the W-phase signal in conjunction with <VOC[1:0]> and ***[PMDxMDCR]***<SYNTMD>.
8	UPWM	0	R/W	U-phase signal control 0: "High"/"Low" output 1: PWM output This bit controls the W-phase signal in conjunction with <UOC[1:0]> and ***[PMDxMDCR]***<SYNTMD>.
7:6	-	0	R	Read as "0".
5:4	WOC[1:0]	00	R/W	W-phase signal control This bit controls the W-phase signal in conjunction with <WPWM> and ***[PMDxMDCR]***<SYNTMD>. When <WOC[1:0]> = 00, the W-phase carrier waveform is inverted.
3:2	VOC[1:0]	00	R/W	V-phase signal control This bit controls the W-phase signal in conjunction with <VPWM> and ***[PMDxMDCR]***<SYNTMD>. When <VOC[1:0]> = 00, the V-phase carrier waveform is inverted.
1:0	UOC[1:0]	00	R/W	U-phase signal control This bit controls the W-phase signal in conjunction with <UPWM> and ***[PMDxMDCR]***<SYNTMD>. When <UOC[1:0]> = 00, the U-phase carrier waveform is inverted.

4.3.12. *[PMDxEMGCR]* (EMG Control Register)

Bit	Bit symbol	After reset	Type	Function
31:18	-	0	R	Read as "0".
17:16	-	0	R/W	Write as "0".
15:14	-	0	R	Read as "0".
13	CPAIEN	0	R/W	Comparator EMG detection input control 0: Disabled 1: Enabled
12:8	EMGCNT[4:0]	00000	R/W	EMGx input noise rejection setting "00000" to "11111" These bits set the noise rejection time for the EMGx input. The noise rejection time is calculated using the following formula: <EMGCNT[4:0]> × 16 / fsys When set to "00000", the noise rejection circuit is disabled.
7	EMGIPOL	0	R/W	EMGx pin polarity selection 0: "Low" active 1: "High" active
6	-	0	R	Read as "0".

Bit	Bit symbol	After reset	Type	Function
5	INHEN	1	R/W	Enable or disable of protection control by debug halt 0: Disabled 1: Enabled
4:3	EMGMD[1:0]	11	R/W	EMG protection mode selection 00: Upper phase: high impedance Lower phase: high impedance 01: Upper phase: PWM waveform output Lower phase: high impedance 10: Upper phase: high impedance Lower phase: PWM waveform output 11: Upper phase: high impedance Lower phase: high impedance These bits set the pin control when EMG is detected.
2	EMGISEL	0	R/W	EMGx pin input control 0: Input enabled 1: Input disabled
1	EMGRS	0	W	Return from EMG protection state 0: - 1: Return from protection state Read as "0".
0	EMGEN	1	R/W	EMG protection control enable/disable 0: Disabled 1: Enabled To disable, set ***[PMDxEMGREL]*** to "0x5A" and "0xA5" sequentially, then set <EMGEN> to "0". Perform the three steps in sequence.

4.3.13. *[PMDxEMGSTA]* (EMG Status Register)

Bit	Bit symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1	EMGI	Undefined	R	EMG factor status 0: EMG factor active 1: EMG factor inactive When any of the allowed EMG factors is active, this bit becomes "0".
0	EMGST	0	R	EMG protection state 0: Not protected state 1: Protected state

4.3.14. *[PMDxEMGREL]* (EMG Release Register)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0".
7:0	EMGREL[7:0]	0x00	W	EMG/OVV disable code setting This register is used to disable the EMG and OVV protection functions. After setting "0x5A" and "0xA5" sequentially, set ***[PMDxEMGCR]***<EMGEN> = 0 or ***[PMDxOVVCR]***<OVVEN> = 0.

4.3.15. *[PMDxOVVCR]* (OVV Control Register)

Bit	Bit symbol	After reset	Type	Function
31:23	-	0	R	Read as "0".
22	OVVCPAIEN	0	R/W	Comparator OVV detection input control 0: Disabled 1: Enabled
21:20	OVVNOCTL[1:0]	00	R/W	OVV protection mode selection 00: Upper phase: PWM waveform output Lower phase: PWM waveform output 01: Upper phase: PWM waveform output Lower phase: off 10: Upper phase: off Lower phase: PWM waveform output 11: Upper phase: PWM waveform output Lower phase: PWM waveform output This bit sets the pin control when OVV is detected in <OVVMD[1:0]> = 00. On is the active level, and off is the inactive level. The active level is set by ***[PMDxMDPOT]***<POLL>, <POLH>.
19:17	-	0	R	Read as "0".
16	-	0	R/W	Write as "0".
15	OVVRSMD	0	R/W	OVV return operation selection 0: Return by automatic or by writing "1" to <OVVRS> 1: Return by writing "1" to <OVVRS>
14:13	-	0	R	Read as "0".
12:8	OVVCNT[4:0]	00000	R/W	OVV input detection time 00001 to 11111 These bits set the noise rejection time for the OVVx input. The noise rejection time is calculated using the following formula: <OVVCNT[4:0]> × 16 / fsys When set to "00000", it operates as "00001".
7	OVVIPOL	0	R/W	OVVx pin polarity selection 0: "Low" active 1: "High" active
6	ADIN1EN	0	R/W	ADC monitor function 1 input control 0: Disabled 1: Enabled This bit selects whether to enable or disable the monitor function 1 from ADC.
5	ADIN0EN	0	R/W	ADC monitor function 0 input control 0: Disabled 1: Enabled This bit selects whether to enable or disable the monitor function 0 from ADC.
4:3	OVVMD[1:0]	00	R/W	OVV protection mode selection 00: Depends on the setting of <OVVNOCTL[1:0]> 01: Upper phase on/lower phase off 10: Upper phase off/lower phase on 11: Upper phase/lower phase off These bits set the pin control when OVV is detected. On is the active level, and off is the inactive level. The active level is set by ***[PMDxMDPOT]***<POLL>, <POLH>.
2	OVVISEL	0	R/W	OVVx pin input control 0: Input enabled 1: Input disabled

Bit	Bit symbol	After reset	Type	Function
1	OVVRS	0	W	Return from OVV protection state 0: - 1: Return from protection state Read as "0".
0	OVVEN	0	R/W	Enable/disable of OVV protection control 0: Disabled 1: Enabled To disable, set ***[PMDxEMGREL]*** to "0x5A" and "0xA5" sequentially, then set <OVVEN> to "0". Perform the three steps in sequence.

4.3.16. *[PMDxOVVSTA]* (OVV Status Register)

Bit	Bit symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1	OVVI	Undefined	R	OVV factor status 0: OVV factor active 1: OVV factor inactive When any of the enabled OVV factors is active, this bit becomes "0".
0	OVVST	0	R	OVV protection state 0: Not protected state 1: Protected state

4.3.17. *[PMDxDTR]* (Dead Time Register)

Bit	Bit symbol	After reset	Type	Function
31:10	-	0	R	Read as "0".
9:0	DTR[9:0]	0x000	R/W	Dead-time setting 0x000 to 0x3FF Dead time is calculated using the following formula: <DTR[9:0]> setting value × 4 / fsys

4.3.18. Trigger Comparison Register

4.3.18.1. *[PMDxTRGCMP0]* (Trigger Comparison 0 Register)

Bit	Bit symbol	After reset	Type	Function
31:15	-	0	R	Read as "0".
14:0	TRGCMP0[14:0]	0x0000	R/W	Synchronous trigger output 0 comparison register 0x0000 to 0x7FFF These bits set the comparison value with the basic carrier or U-phase PWM carrier.

4.3.18.2. *[PMDxTRGCMP1]* (Trigger Comparison 1 Register)

Bit	Bit symbol	After reset	Type	Function
31:15	-	0	R	Read as "0".
14:0	TRGCMP1[14:0]	0x0000	R/W	Synchronous trigger output 1 comparison register 0x0000 to 0x7FFF These bits set the comparison value with the basic carrier or U-phase PWM carrier.

4.3.18.3. *[PMDxTRGCMP2]* (Trigger Comparison 2 Register)

Bit	Bit symbol	After reset	Type	Function
31:15	-	0	R	Read as "0".
14:0	TRGCMP2[14:0]	0x0000	R/W	Synchronous trigger output 2 comparison register 0x0000 to 0x7FFF These bits set the comparison value with the basic carrier or V-phase PWM carrier.

4.3.18.4. *[PMDxTRGCMP3]* (Trigger Comparison 3 Register)

Bit	Bit symbol	After reset	Type	Function
31:15	-	0	R	Read as "0".
14:0	TRGCMP3[14:0]	0x0000	R/W	Synchronous trigger output 3 comparison register 0x0000 to 0x7FFF These bits set the comparison value with the basic carrier or W-phase PWM carrier.

4.3.18.5. *[PMDxTRGCMP4]* (Trigger Comparison 4 Register)

Bit	Bit symbol	After reset	Type	Function
31:15	-	0	R	Read as "0".
14:0	TRGCMP4[14:0]	0x0000	R/W	Synchronous trigger output 4 comparison register 0x0000 to 0x7FFF These bits set the comparison value with the basic carrier or U-phase PWM carrier.

4.3.18.6. *[PMDxTRGCMP5]* (Trigger Comparison 5 Register)

Bit	Bit symbol	After reset	Type	Function
31:15	-	0	R	Read as "0".
14:0	TRGCMP5[14:0]	0x0000	R/W	Synchronous trigger output 5 comparison register 0x0000 to 0x7FFF These bits set the comparison value with the basic carrier or U-phase PWM carrier.

4.3.18.7. *[PMDxTRGCMP6]* (Trigger Comparison 6 Register)

Bit	Bit symbol	After reset	Type	Function
31:15	-	0	R	Read as "0".
14:0	TRGCMP6[14:0]	0x0000	R/W	Synchronous trigger output 6 comparison register 0x0000 to 0x7FFF These bits set the comparison value with the basic carrier or U-phase PWM carrier.

4.3.19. *[PMDxTRGCR]* (Trigger Control Register)

Bit	Bit symbol	After reset	Type	Function
31:17	-	0	R	Read as "0".
16	CARSEL	0	R/W	Carrier selection 0: Basic carrier 1: Phase-specific PWM carrier
15	TRG3BE	0	R/W	***[PMDxTRGCMP3]*** execution buffer update 0: Synchronous update (refer to Table 3.15) 1: Writing to register
14:12	TRG3MD[2:0]	000	R/W	Synchronous trigger output 3 mode selection These bits select the synchronous trigger output timing and execution buffer update timing. Refer to Table 3.14 for synchronous trigger output timing. Refer to Table 3.15 for execution buffer update timing.
11	TRG2BE	0	R/W	***[PMDxTRGCMP2]*** execution buffer update 0: Synchronous update (refer to Table 3.15) 1: Writing to register
10:8	TRG2MD[2:0]	000	R/W	Synchronous trigger output 2 mode selection These bits select the synchronous trigger output timing and execution buffer update timing. Refer to Table 3.14 for synchronous trigger output timing. Refer to Table 3.15 for execution buffer update timing.
7	TRG1BE	0	R/W	***[PMDxTRGCMP1]***/VExTRGCMP1 execution buffer update 0: Synchronous update (refer to Table 3.15) 1: Writing to register
6:4	TRG1MD[2:0]	000	R/W	Synchronous trigger output 1 mode selection These bits select the synchronous trigger output timing and execution buffer update timing. Refer to Table 3.14 for synchronous trigger output timing. Refer to Table 3.15 for execution buffer update timing.
3	TRG0BE	0	R/W	***[PMDxTRGCMP0]***/VExTRGCMP0 execution buffer update 0: Synchronous update (refer to Table 3.15) 1: Writing to register
2:0	TRG0MD[2:0]	000	R/W	Synchronous trigger output 0 mode selection These bits select the synchronous trigger output timing and execution buffer update timing. Refer to Table 3.14 for synchronous trigger output timing. Refer to Table 3.15 for execution buffer update timing.

4.3.20. *[PMDxTRGCR2]* (Trigger Control Register 2)

Bit	Bit symbol	After reset	Type	Function
31:12	-	0	R	Read as "0".
11	TRG6BE	0	R/W	***[PMDxTRGCMP6]*** execution buffer update 0: Synchronous update (refer to Table 3.15) 1: Writing to register
10:8	TRG6MD[2:0]	000	R/W	Synchronous trigger output 6 mode selection These bits select the synchronous trigger output timing and execution buffer update timing. Refer to Table 3.14 for synchronous trigger output timing. Refer to Table 3.15 for execution buffer update timing.
7	TRG5BE	0	R/W	***[PMDxTRGCMP5]*** execution buffer update 0: Synchronous update (refer to Table 3.15) 1: Writing to register

Bit	Bit symbol	After reset	Type	Function
6:4	TRG5MD[2:0]	000	R/W	Synchronous trigger output 5 mode selection These bits select the synchronous trigger output timing and execution buffer update timing. Refer to Table 3.14 for synchronous trigger output timing. Refer to Table 3.15 for execution buffer update timing.
3	TRG4BE	0	R/W	***[PMDxTRGCMP4]*** execution buffer update 0: Synchronous update (refer to Table 3.15) 1: Writing to register
2:0	TRG4MD[2:0]	000	R/W	Synchronous trigger output 4 mode selection These bits select the synchronous trigger output timing and execution buffer update timing. Refer to Table 3.14 for synchronous trigger output timing. Refer to Table 3.15 for execution buffer update timing.

4.3.21. *[PMDxTRGSYNCR]* (Trigger Update Timing Setting Register)

Bit	Bit symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1:0	TSYNCS[1:0]	00	R/W	Execution buffer update timing setting of trigger comparison register 00: Depending on the following register settings ***[PMDxTRGCR]***<TRGnMD[2:0]> (n = 0 to 3) ***[PMDxTRGCR2]***<TRGmMD[2:0]> (m = 4 to 6) 01: Update at phase-specific PWM center 10: Update at phase-specific PWM end 11: Update at phase-specific PWM end and center

4.3.22. *[PMDxTRGMD]* (Trigger Output Mode Setting Register)

Bit	Bit symbol	After reset	Type	Function
31:28	-	0	R	Read as "0".
27:16	TRGDELY[11:0]	0x000	R/W	Trigger output delay 0x000: No delay 0x001 to 0xFFF: Delay value The delay time is calculated using the following formula: <TRGDELY[11:0]> setting value × 1 / fsys
15:2	-	0	R	Read as "0".
1	TRGOUT	0	R/W	Trigger output mode 0: Trigger fixed output 1: Trigger selection output The trigger fixed output outputs a trigger signal according to the settings of each trigger output. The trigger selection output outputs synchronous trigger 0 to one of PMDxTRG0 to PMDxTRG6 selected by ***[PMDxTRGSEL]***.
0	EMGTGE	0	R/W	Output during EMG protection 0: Trigger output disabled 1: Trigger output enabled

4.3.23. *[PMDxTRGSEL]* (Trigger Output Selection Register)

Bit	Bit symbol	After reset	Type	Function
31:3	-	0	R	Read as "0".
2:0	TRGSEL[2:0]	000	R/W	Trigger output port selection 000: Output from PMDxTRG0 001: Output from PMDxTRG1 010: Output from PMDxTRG2 011: Output from PMDxTRG3 100: Output from PMDxTRG4 101: Output from PMDxTRG5 110: Output from PMDxTRG6 111: No output These bits are valid when trigger selection output (***[PMDxTRGMD]***<TRGOUT> = 1).

4.3.24. *[PMDxMBUFCR]* (Intermediate Buffer Control Register)

Bit	Bit symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
3	BUFCTRSEL	0	R/W	Intermediate buffer 1 update carrier selection 0: U-phase carrier 1: Basic carrier
2:0	BUFCTR[2:0]	000	R/W	Intermediate buffer 1 update control 000: Intermediate buffer 1 disabled 001: Carrier end 010: Carrier center 011: Carrier 3/4 timing 100: Carrier 1/4 timing 101: Carrier end and center 110: Carrier 1/4 and 3/4 timing 111: Reserved

4.3.25. *[PMDxSYNCCR]* (Synchronization Control Register)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0".
7:6	OVVSMD[1:0]	00	R/W	OVV synchronous operation setting 00: Synchronous operation disabled 01: Synchronous operation disabled 10: Synchronous operation enabled (OVV detection disabled for own channel) 11: Synchronous operation enabled (OVV detection enabled for own channel) These bits are valid when ***[PMDxOVVCR]***<OVVEN> = 1.
5:4	EMGSMD[1:0]	00	R/W	Synchronization setting of EMG protection operation 00: Synchronous operation disabled 01: Synchronous operation disabled 10: Synchronous operation enabled (EMG detection disabled for own channel) 11: Synchronous operation is enabled (EMG detection enabled for own channel) These bits are valid when ***[PMDxEMGCR]***<EMGEN> = 1.
3:1	-	0	R	Read as "0".
0	PWMSMD	0	R/W	Synchronous setting of PMD operation start 0: Synchronous operation disabled 1: Synchronous operation enabled When enabled, the ***[PMDxMDEN]***<PWMEN> setting is disabled.

4.3.26. *[PMDxDBGOUTCR]* (Debug Output Control Register)

Bit	Bit symbol	After reset	Type	Function
31	INIFF	0	R/W	PMDxDBG output initial state setting 0: "Low" output 1: "High" output When <DBGEN> =0, PMDxDBG output is updated to the set value. The initial value cannot be set using the ADC conversion timing monitor (<DBGMD[1:0]> = 00).
30:25	-	0	R	Read as "0".
24	VEENDBGSEL	0	R/W	VE task transition/ENC debug output monitor selection 0: Select VE task transition 1: Select ENC debug output
23	-	0	R	Read as "0".
22	TRG6EN	0	R/W	PMD trigger 6 monitor setting 0: PMDxTRG6 disabled 1: PMDxTRG6 enabled
21	TRG5EN	0	R/W	PMD trigger 5 monitor setting 0: PMDxTRG5 disabled 1: PMDxTRG5 enabled
20	TRG4EN	0	R/W	PMD trigger 4 monitor setting 0: PMDxTRG4 disabled 1: PMDxTRG4 enabled
19	TRG3EN	0	R/W	PMD trigger 3 monitor setting 0: PMDxTRG3 disabled 1: PMDxTRG3 enabled

Bit	Bit symbol	After reset	Type	Function
18	TRG2EN	0	R/W	PMD trigger 2 monitor setting 0: PMDxTRG2 disabled 1: PMDxTRG2 enabled
17	TRG1EN	0	R/W	PMD trigger 1 monitor setting 0: PMDxTRG1 disabled 1: PMDxTRG1 enabled
16	TRG0EN	0	R/W	PMD trigger 0 monitor setting 0: PMDxTRG0 disabled 1: PMDxTRG0 enabled
15:13	-	0	R	Read as "0".
12	IENCEN	0	R/W	ENC interrupt monitor setting 0: INTENCx0/INTENx1 disabled 1: INTENCx0/INTENx1 enabled
11	IVEEN	0	R/W	VE interrupt monitor setting 0: INTVCNx disabled 1: INTVCNx enabled
10	IOVVEN	0	R/W	PMD interrupt monitor setting 0: INTOVVx disabled 1: INTOVVx enabled
9	IEMGEN	0	R/W	PMD interrupt monitor setting 0: INTEMGx disabled 1: INTEMGx enabled
8	IPMDEN	0	R/W	PMD interrupt monitor setting 0: INTPWMx disabled 1: INTPWMx enabled
7	IADEEN	0	R/W	ADC interrupt monitor setting 0: INTADxPFLG disabled 1: INTADxPFLG enabled
6	IADDEN	0	R/W	ADC interrupt monitor setting 0: INTADxPDD disabled 1: INTADxPDD enabled
5	IADCEN	0	R/W	ADC interrupt monitor setting 0: INTADxPDC disabled 1: INTADxPDC enabled
4	IADBEN	0	R/W	ADC interrupt monitor setting 0: INTADxPDB disabled 1: INTADxPDB enabled
3	IADAEN	0	R/W	ADC interrupt monitor setting 0: INTADxPDA disabled 1: INTADxPDA enabled
2:1	DBGMD[1:0]	0	R/W	Debug mode selection 00: ADC conversion monitor 01: PMD trigger monitor 10: Interrupt monitor 11: VE task transition/ENC debug output monitor
0	DBGEN	0	R/W	Debug output setting 0: Debug output disabled 1: Debug output enabled

5. Revision History

Table 5.1 Revision History

Revision	Date	Description
1.0	2026-01-30	- First release

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