

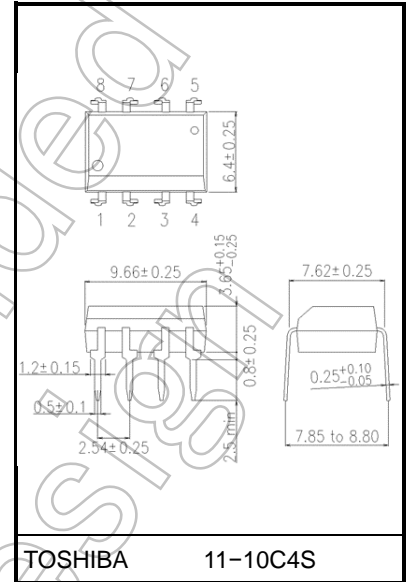
# 6N135, 6N136

Digital Logic Isolation  
 Line Receiver  
 Power Supply Control  
 Switching Power Supply  
 Transistor Inverter

The TOSHIBA 6N135 and 6N136 consists of an infrared emitting diode and a one chip photo diode-transistor.  
 Each unit is 8-lead DIP package.

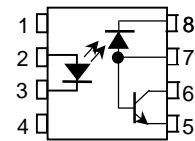
- Isolation voltage: 2500 V<sub>rms</sub> (min)
- High speed: t<sub>pHL</sub>, t<sub>pLH</sub> = 0.5 μs (typ.) (R<sub>L</sub> = 1.9kΩ)
- TTL compatible
- If base pin is open, output signal will be noisy by environmental condition. For this base, TLP550 is suitable
- UL-recognized: UL 1577, File No.E67349
- CQC-approved(6N136): GB4943.1,GB8898 Japan and Factory

Unit: mm

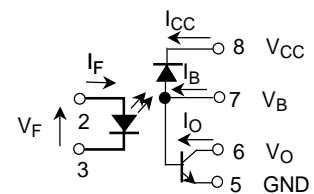


Weight: 0.54 g (typ.)

### Pin Configurations



- 1 : N.C.
- 2 : ANODE
- 3 : CATHODE
- 4 : N.C.
- 5 : EMITTER
- 6 : COLLECTOR
- 7 : BASE, ANODE
- 8 : CATHODE



Start of commercial production  
 1982-10

### Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
LED	Forward current (Note 1)	I <sub>F</sub>	25	mA
	Pulse forward current (Note 2)	I <sub>FP</sub>	50	mA
	Total pulse forward current (Note 3)	I <sub>FPT</sub>	1	A
	Reverse voltage	V <sub>R</sub>	5	V
	Diode power dissipation (Note 4)	P <sub>D</sub>	45	mW
Detector	Output current	I <sub>O</sub>	8	mA
	Peak output current	I <sub>OP</sub>	16	mA
	Emitter-base reverse voltage (pin 5-7)	V <sub>EB</sub>	5	V
	Supply voltage	V <sub>CC</sub>	-0.5 to 15	V
	Output voltage	V <sub>O</sub>	-0.5 to 15	V
	Base current (pin 7)	I <sub>B</sub>	5	mA
	Output power dissipation (Note 5)	P <sub>O</sub>	100	mW
Operating temperature range		T <sub>opr</sub>	-55 to 100	°C
Storage temperature range		T <sub>stg</sub>	-55 to 125	°C
Lead solder temperature (10s) (Note 6)		T <sub>sol</sub>	260	°C
Isolation voltage (Note 7)		BVS	2500	V <sub>rms</sub>

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

(Note 1) Derate 0.8 mA above 70°C.

(Note 2) 50 % duty cycle, 1 ms pulse width.  
Derate 1.6 mA / °C above 70 °C.

(Note 3) Pulse width 1μs, 300pps.

(Note 4) Derate 0.9 mW / °C above 70 °C.

(Note 5) Derate 2 mW / °C above 70 °C.

(Note 6) Soldering portion of lead: Up to 2 mm from the body of the device.

(Note 7) R.H. ≤ 60%, AC, 60 s

### Electrical Characteristics

Over Recommended Temperature ( $T_a = 0^\circ\text{C}\sim 70^\circ\text{C}$  unless otherwise noted)

Characteristics		Symbol	Test Condition	Min	(**)Typ.	Max	Unit
Current transfer ratio	6N135	CTR	$I_F = 16\text{ mA}, V_O = 0.4\text{ V}$ $V_{CC} = 4.5\text{ V}, T_a = 25^\circ\text{C}$ (Note 8)	7	18	—	%
	6N136			19	24	—	%
	6N135	CTR	$I_F = 16\text{ mA}, V_O = 0.5\text{ V}$ $V_{CC} = 4.5\text{ V}$ (Note 1)	5	13	—	%
	6N136			15	21	—	%
Logic low output voltage	6N135	VOL	$I_F = 16\text{ mA}, I_O = 1.1\text{ mA}$ $V_{CC} = 4.5\text{ V}$	—	0.1	0.4	V
	6N136		$I_F = 16\text{ mA}, I_O = 2.4\text{ mA}$ $V_{CC} = 4.5\text{ V}$	—	0.1	0.4	V
Logic high output current		IOH	$I_F = 0\text{ mA}, V_O = V_{CC} = 5.5\text{ V}$ $T_a = 25^\circ\text{C}$	—	3	500	nA
			$I_F = 0\text{ mA}, V_O = V_{CC} = 15\text{ V}$ $T_a = 25^\circ\text{C}$	—	0.1	1	$\mu\text{A}$
		IOH	$I_F = 0\text{ mA}, V_O = V_{CC} = 15\text{ V}$	—	—	50	$\mu\text{A}$
Logic low supply current		ICCL	$I_F = 16\text{ mA}, V_O = \text{open}$ $V_{CC} = 15\text{ V}$	—	40	—	$\mu\text{A}$
Logic high supply current		ICCH	$I_F = 0\text{ mA}, V_O = \text{open}$ $V_{CC} = 15\text{ V}, T_a = 25^\circ\text{C}$	—	0.01	1	$\mu\text{A}$
		ICCH	$I_F = 0\text{ mA}, V_O = \text{open}$ $V_{CC} = 15\text{ V}$	—	—	2	$\mu\text{A}$
Input forward voltage		VF	$I_F = 16\text{ mA}, T_a = 25^\circ\text{C}$	—	1.65	1.7	V
Temperature coefficient of forward voltage		$\Delta V_F / \Delta T_a$	$I_F = 16\text{ mA}$	—	-1.9	—	$\text{mV} / ^\circ\text{C}$
Input reverse breakdown voltage		BVR	$I_R = 10\text{ }\mu\text{A}, T_a = 25^\circ\text{C}$	5	—	—	V
Input capacitance		CIN	$f = 1\text{ MHz}, V_F = 0\text{ V}$	—	60	—	pF
Resistance (input-output)		RI-O	$V_{I-O} = 500\text{ V}$ R.H. $\leq 60\%$ (Note 9)	—	$10^{12}$	—	$\Omega$
Capacitance (input-output)		CI-O	$f = 1\text{ MHz}, V = 0\text{ V}$ (Note 9)	—	0.6	—	pF
Transistor DC current gain		hFE	$V_O = 5\text{ V}, I_O = 3\text{ mA}$	—	80	—	—

(\*\*) All typical values are at  $T_a = 25^\circ\text{C}$

Not for New

### Switching Specifications

(unless otherwise specified.  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ ,  $I_F = 16\text{mA}$ )

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	
Propagation delay time to logic low at output	6N135	t <sub>pHL</sub>	1	R <sub>L</sub> = 4.1 k $\Omega$	—	0.2	1.5	$\mu\text{s}$
	6N136			R <sub>L</sub> = 1.9 k $\Omega$	—	0.2	0.8	$\mu\text{s}$
Propagation delay time to logic high at output	6N135	t <sub>pLH</sub>	1	R <sub>L</sub> = 4.1 k $\Omega$	—	1.0	1.5	$\mu\text{s}$
	6N136			R <sub>L</sub> = 1.9 k $\Omega$	—	0.5	0.8	$\mu\text{s}$
Common mode transient immunity at logic high level output (Note 10)	6N135	CM <sub>H</sub>	2	I <sub>F</sub> = 0 mA V <sub>CM</sub> = 10 V <sub>p-p</sub> R <sub>L</sub> = 4.1 k $\Omega$	—	1000	—	V / $\mu\text{s}$
	6N136			I <sub>F</sub> = 0 mA V <sub>CM</sub> = 10 V <sub>p-p</sub> R <sub>L</sub> = 1.9 k $\Omega$	—	1000	—	V / $\mu\text{s}$
Common mode transient immunity at logic low level output (Note 10)	6N135	CM <sub>L</sub>	2	V <sub>CM</sub> = 10 V <sub>p-p</sub> R <sub>L</sub> = 4.1 k $\Omega$ I <sub>F</sub> = 16 mA	—	-1000	—	V / $\mu\text{s}$
	6N136			V <sub>CM</sub> = 10 V <sub>p-p</sub> R <sub>L</sub> = 1.9 k $\Omega$ I <sub>F</sub> = 16 mA	—	-1000	—	V / $\mu\text{s}$
Bandwidth (Note 11)	BW	—	R <sub>L</sub> = 100 $\Omega$	—	2	—	MHz	

(Note 8) DC current transfer ratio is defined as the ratio of output collector current, I<sub>O</sub>, to the forward LED input current, I<sub>F</sub>, times 100 %.

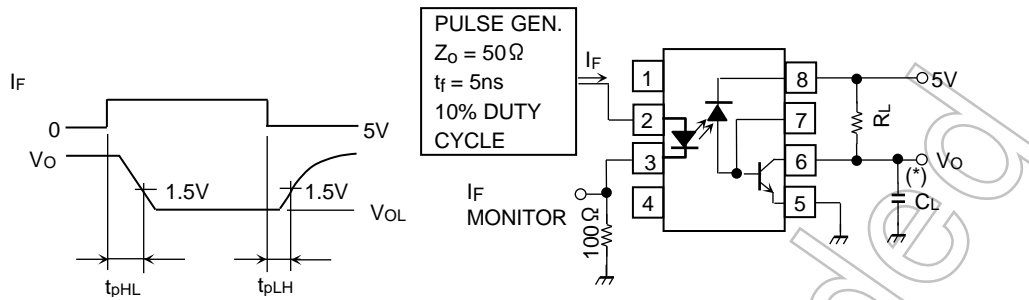
(Note 9) Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

(Note 10) Common mode transient immunity in logic high level is the maximum tolerable (positive) dV<sub>CM</sub> / dt on the leading edge of the common mode pulse, V<sub>CM</sub>, to assure that the output will remain in a logic high state (i.e., V<sub>O</sub> > 2.0 V).

Common mode transient immunity in logic low level is the maximum tolerable (negative) dV<sub>CM</sub> / dt on the trailing edge of the common mode pulse signal, V<sub>CM</sub>, to assure that the output will remain in a logic low state (i.e., V<sub>O</sub> < 0.8 V).

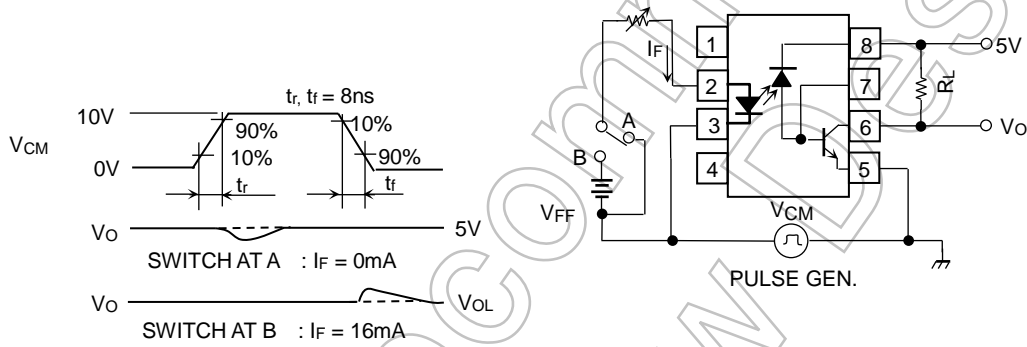
(Note 11) The frequency at which the AC output voltage is 3dB below the low frequency asymptote.

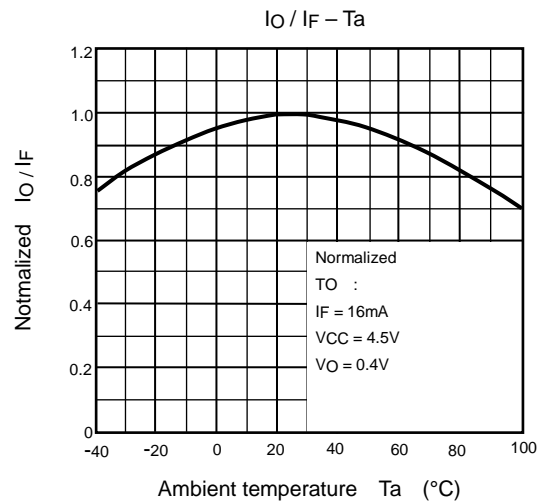
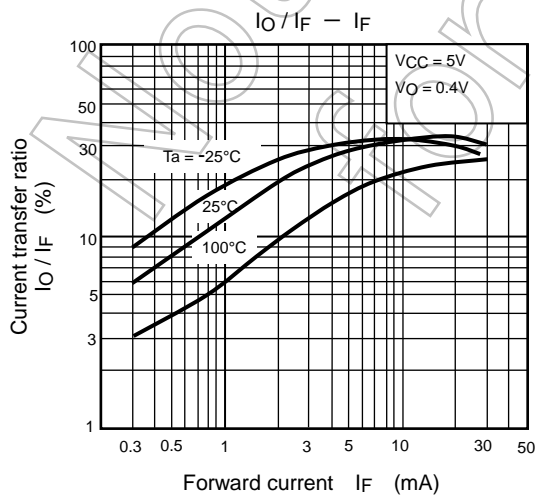
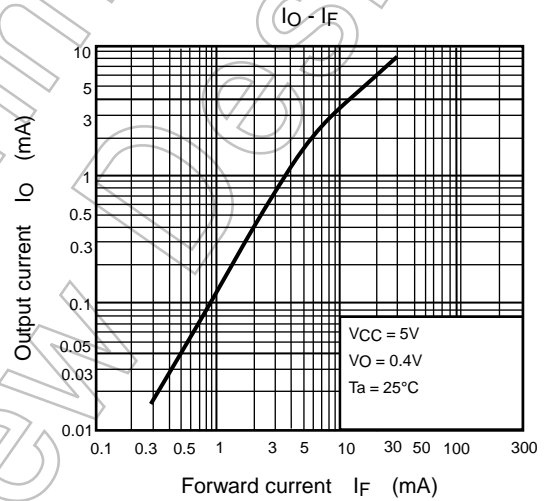
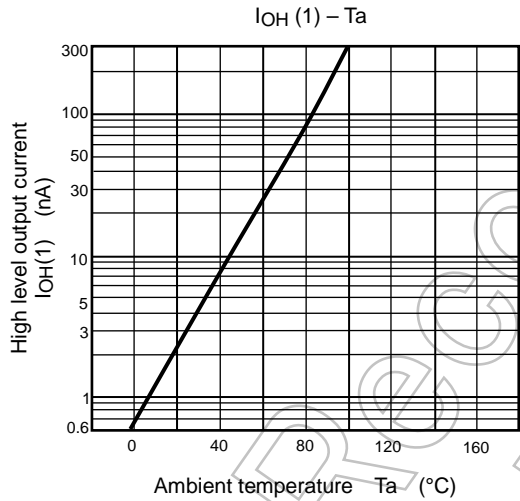
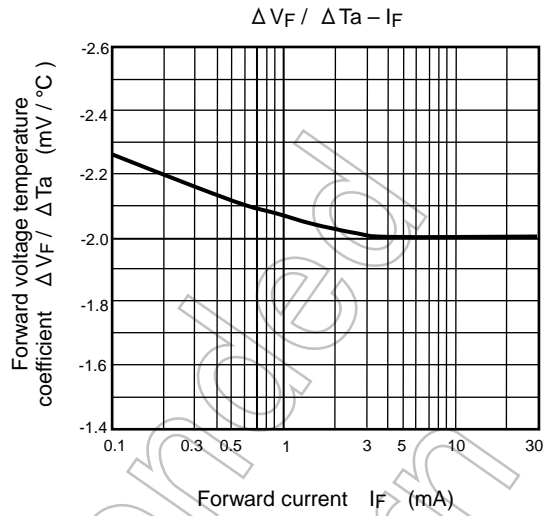
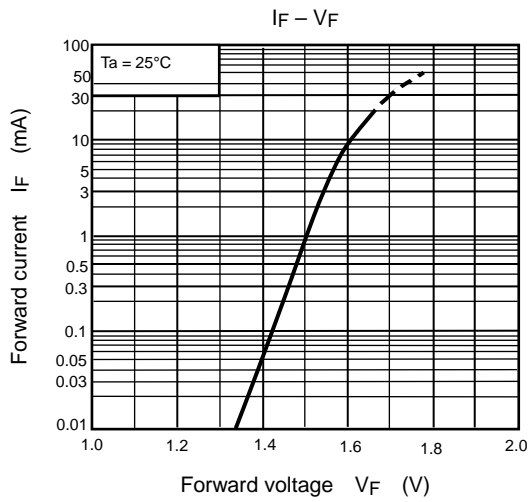
### Test Circuit 1.



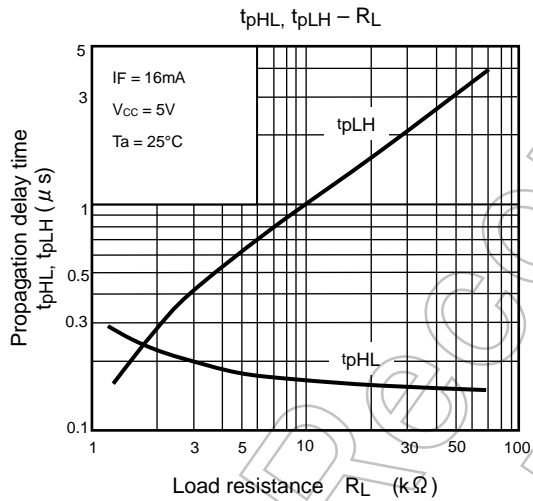
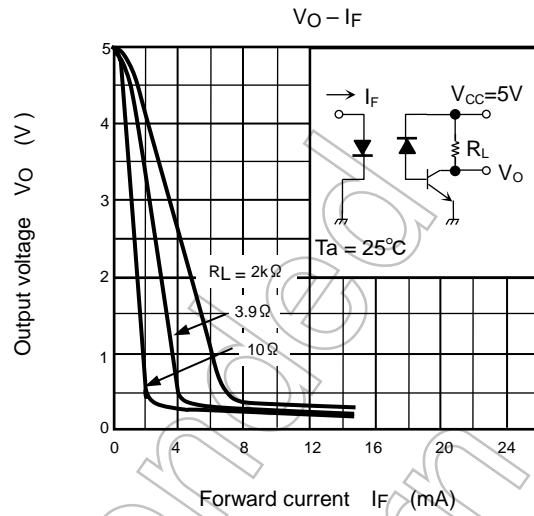
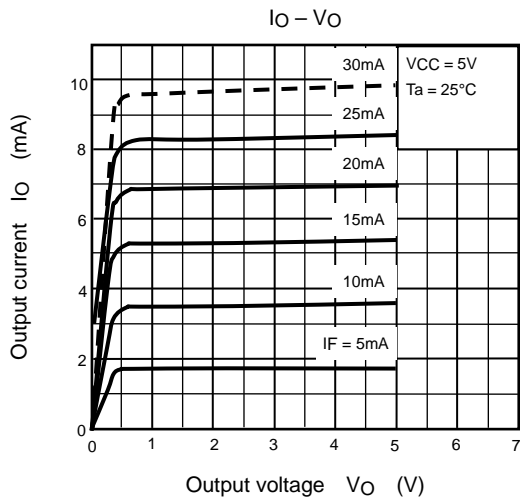
(\*) CL is approximately 15PF which includes probe and stray wiring capacitance.

### Test Circuit 2.





NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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