32-bit RISC Microcontroller
Reference Manual

Serial Memory Interface (SMIF-D)

Revision 1.0

2026-01

Toshiba Electronic Devices & Storage Corporation

Contents

List of Figures

List of Tables

Preface

Related Document

Document name
Data Sheet
Clock Control and Operation Mode
Exception
Input/Output Ports

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

Terms and Abbreviation

Some of abbreviations used in this document are as follows:

DPI	Dual Peripheral Interface
OPI	Octal Peripheral Interface
SI	Serial Input
SMIF	Serial Memory Interface
SO	Serial Output
SPI	Serial Peripheral Interface
STR	Single Transfer Rate
QPI	Quad Peripheral Interface

1. Outlines

The serial memory interface (SMIF) connects to the external device (serial memory and others) which has serial I/O or multi I/O communication interface. It outputs a transfer clock and chip selects.

This reference manual mainly describes the serial memory which receives them.

The list of the SMIF functions is shown in the following table.
Communication modes can be used depending on the pin specification. Regarding the pin specification, refer to datasheet for each product.

Function category	Function	Function
Connection to serial memory	Connection	- Up to 2 serial memories can be connected.
	Memory capacity	- 64 KB to 128 MB
	Communication mode	- Communication Mode STR-SPI(standard SPI compatible) STR-Dual (direct access only) STR-DPI (direct access only) STR-Quad STR-QPI STR-Octal STR-OPI - MSB first - SPI Mode 0 support - Number of address bytes in command with address can be specified among 2, 3, or 4. Note: Communication using data strobe and data mask signal is not supported.
	Memory mapping	- Mapping address: "0xA0000000" to "0xA7FFFFFF"
	Access mode	- Direct access - Indirect access
	Command transfer count	- Up to 288 bytes can be transferred by registers.
	Chip select	- Selection from Serial memory 0 and Serial memory 1. - Deassertion times of SMIxCS0_N and SMIxCS1_N can be set.
	Other functions	- A function to automatically polling the "WIP" of the status register in the SPI Flash before direct access and wait until the "Idle" state. - The dummy byte count be selected from 0 to 31 bytes.

2. Configuration

The block diagram and the list of the signals of SMIF are shown as follows:

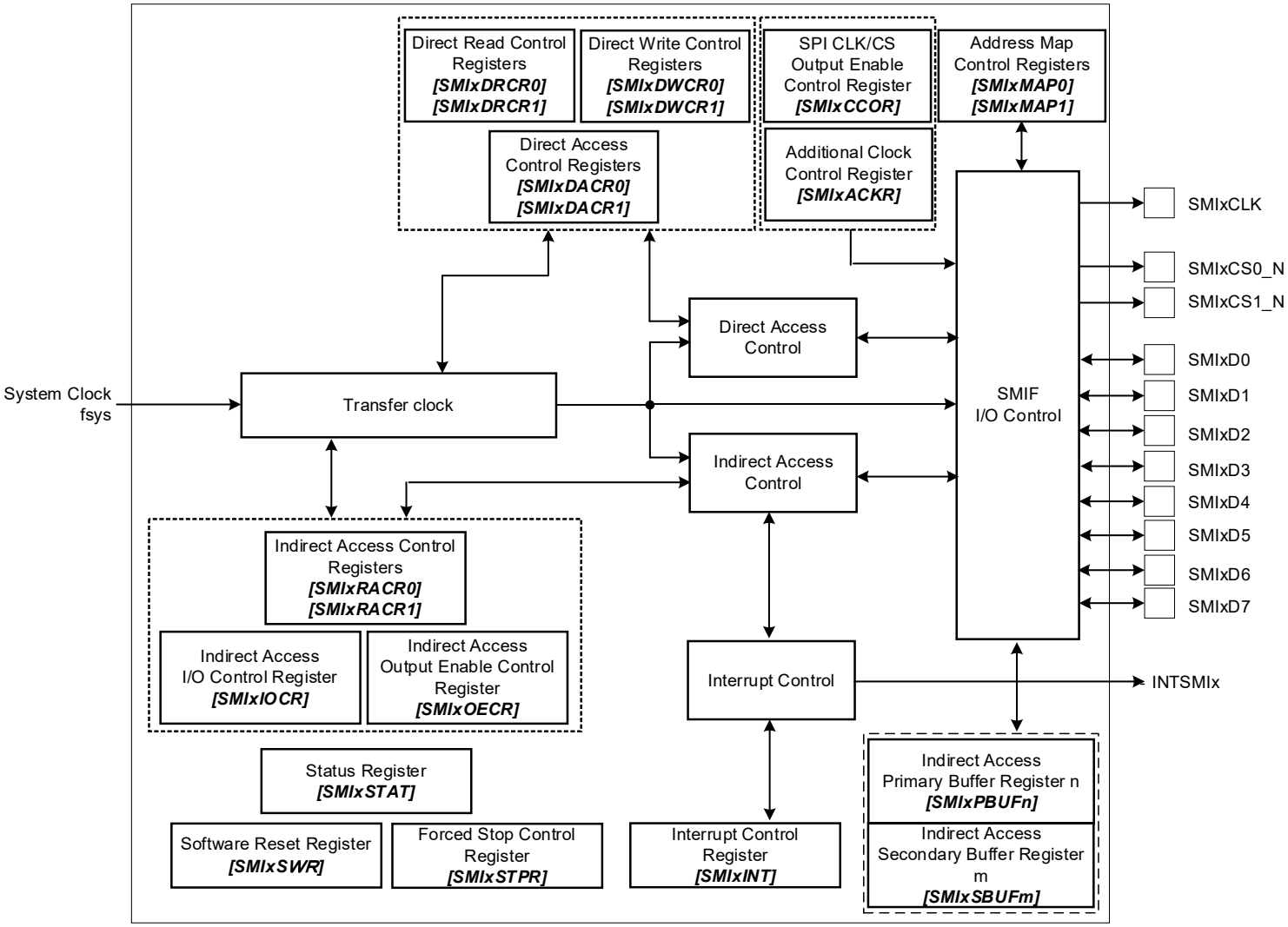

Figure 2.1 Block Diagram of SMIF

Table 2.1 List of Signals

No	symbol	Signal name	I/O	Reference manual
1	fsys	System clock	Input	Clock Control and Operation Mode
2	SMIxCLK	Access clock	Output	Data sheet
3	SMIxCS0_N	Chip select 0	Output	Data sheet
4	SMIxCS1_N	Chip select 1	Output	Data sheet
5	SMIxD0	Data input and output 0	I/O	Data sheet
6	SMIxD1	Data input and output1	I/O	Data sheet
7	SMIxD2	Data input and output 2	I/O	Data sheet
8	SMIxD3	Data input and output3	I/O	Data sheet
9	SMIxD4	Data input and output4	I/O	Data sheet
10	SMIxD5	Data input and output 5	I/O	Data sheet
11	SMIxD6	Data input and output 6	I/O	Data sheet
12	SMIxD7	Data input and output 7	I/O	Data sheet
13	INTSMIx	Interrupt	Output	Exception

3. Function and Operation

SMIF can connect to up to 2 serial memories. Each memory capacity of 64 KB to 128MB is available.

The memory can be accessed by "Direct access" to read/write data by address specification and "Indirect access" which issues a command using program registers.

3.1. Clock Supply

When SMIF is used, the corresponding clock enable bits should be set to "1" (Clock supply) in fsys supply stop register A (***[CGFSYSENA]***, ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]***, ***[CGFSYSMENB]***), and fsys supply stop register C (***[CGFSYSMENC]***), and fc supply stop register (***[CGFCEN]***). The corresponding registers and the bit location depend on the product. Some products do not have all registers. For the details, refer to reference manual "Clock Control and Operation Mode".

When the clock supply is stopped or the operation mode is transited to STOP1/STOP2 mode, it should be checked that SMIF stops.

3.2. Communication Mode

The communication format between SMIF and a serial memory is STR-SPI(Standard SPI compatible), STR-Dual (direct mode only), STR-DPI (direct mode only), STR-Quad, STR-QPI, STR-Octal, STR-OPI Read/Write.

The serial memory should satisfy the following conditions.

- Memory capacity: 64 KB to 128 MB.
- SPI Mode 0 is supported.
- The unused upper bits of address are "Don't care".
- The bit 0 of the status register is the bit of "Write In Progress (WIP)" when a SPI Flash is used as a serial memory.
- MSB first

3.3. Memory Mapping

The address to access a serial memory can be mapped to any region in "0xA0000000" to "0xA7FFFFFF" (128 MB). If the area which is not mapped is read, an unknown value returns. After releasing reset, the serial memory 0 is mapped, but the serial memory 1 is not mapped.

When using serial memory 1, it is necessary to set the memory mapping. If the serial memory whose capacity is smaller than the mapped area is mapped, a mirror area is read when the mapped area is accessed.

Figure 3.1 shows an example that the mapping area of the serial memory 0 is "0xA0000000" to "0xA0BFFFFF" (12 MB) and the mapping area of the serial memory 1 is "0xA0C00000" to "0xA0FFFFFF" (4 MB), and a 4-MB serial memory is connected to each area, respectively.

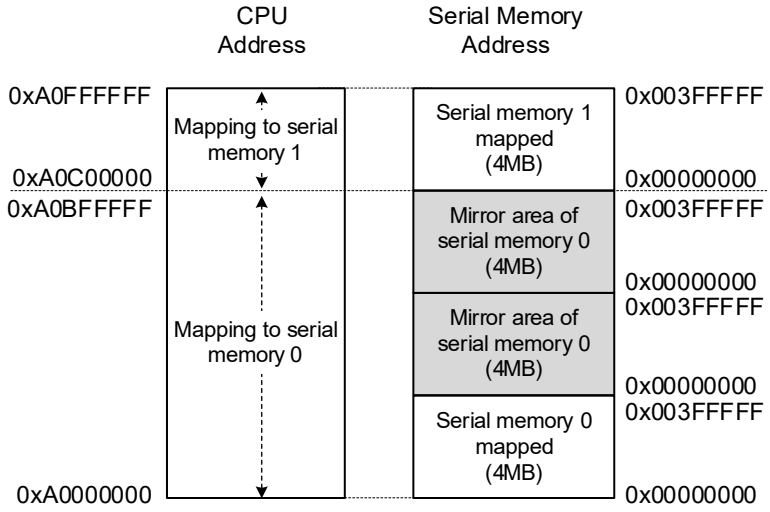

Figure 3.1 Example of Memory Mapping

3.4. Access Mode

There are two access modes to access a serial memory, "Direct access" which reads/writes the data by specifying addresses and "Indirect access" which issues a command by registers.

3.4.1. Direct Access

The serial memory can be directly read from or write to by accessing addresses "0xA0000000" to "0xA7FFFFFF". This is "Direct access". When a read to an address in the range of "0xA0000000" to "0xA7FFFFFF" is detected, a read/write command is issued to serial memory.

3.4.1.1. SPI Flash Command

The initial command which is issued in the direct access mode is FAST READ (op-code = 0x0B). The command can be replaced to one of the following multi I/O commands. But the supported commands depend on the connected serial memory.

The following shows main communication modes and their timing charts.

(1) STR-SPI

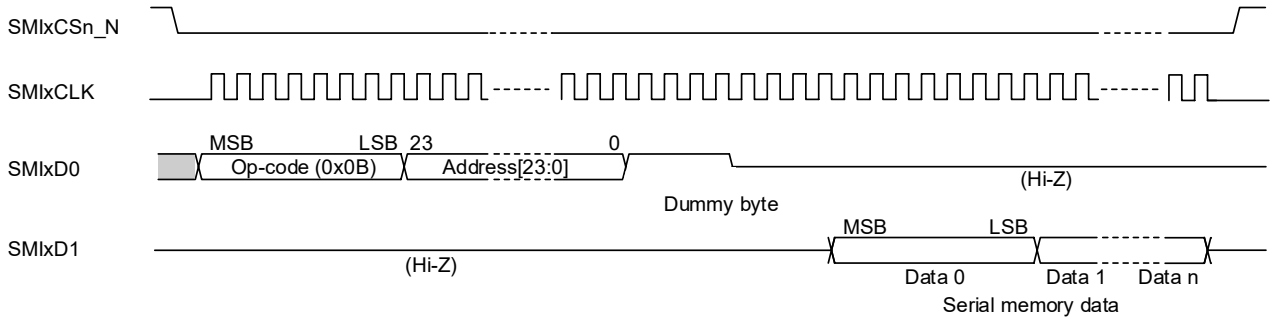

Figure 3.2 STR-SPI: FAST READ

(2) STR-Dual (only direct access)

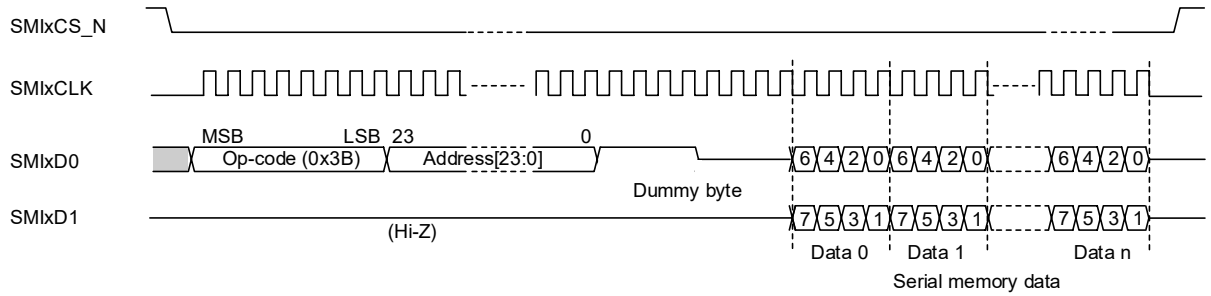

Figure 3.3 STR-Dual: FAST READ Quad Output

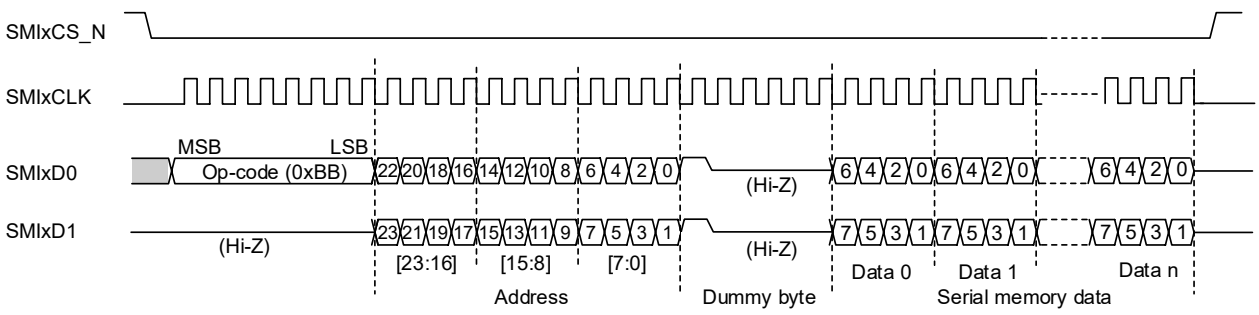

Figure 3.4 STR-Dual: FAST READ Dual I/O

(3) STR-DPI (direct access only)

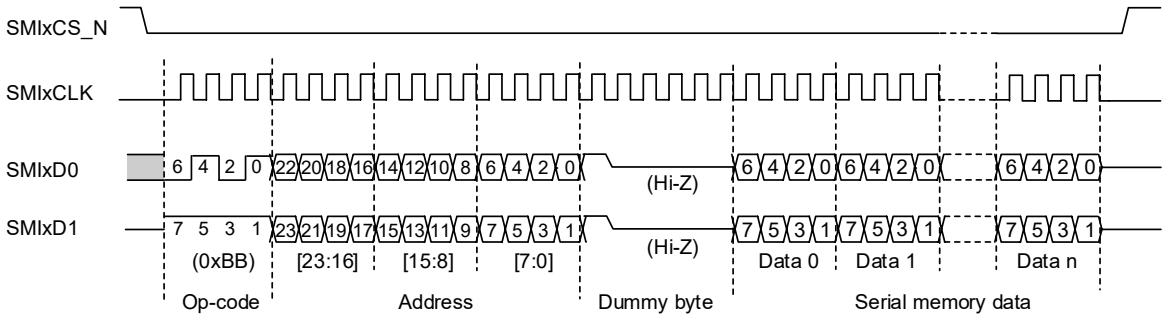

Figure 3.5 STR-DPI: FAST READ

(4) STR-Quad

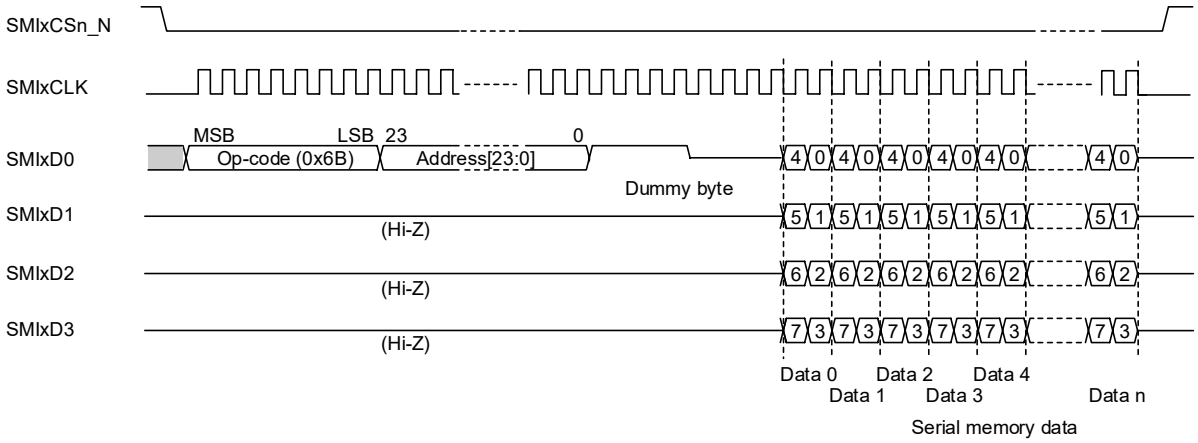

Figure 3.6 STR-Quad: FAST READ Quad Output

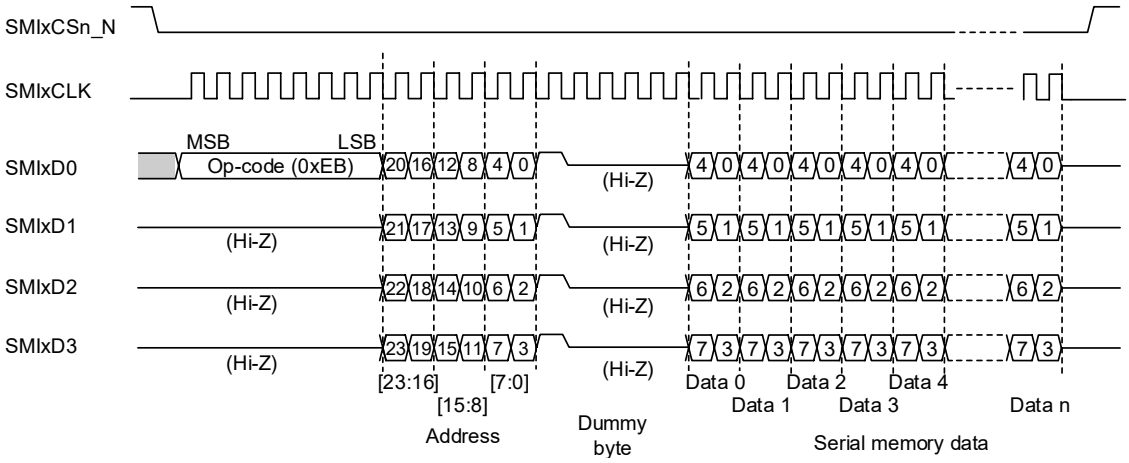

Figure 3.7 STR-Quad: FAST READ Quad I/O

(5) STR-QPI

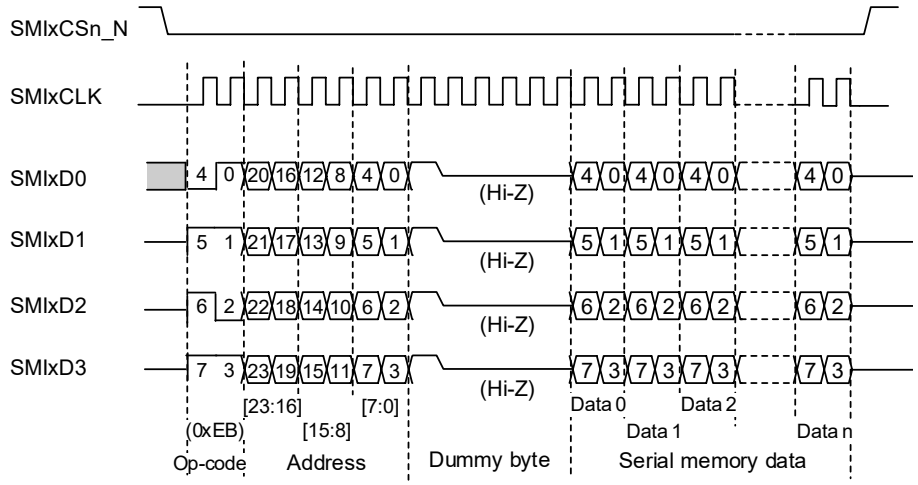

Figure 3.8 STR-QPI: FAST READ

(6) STR-Qctal

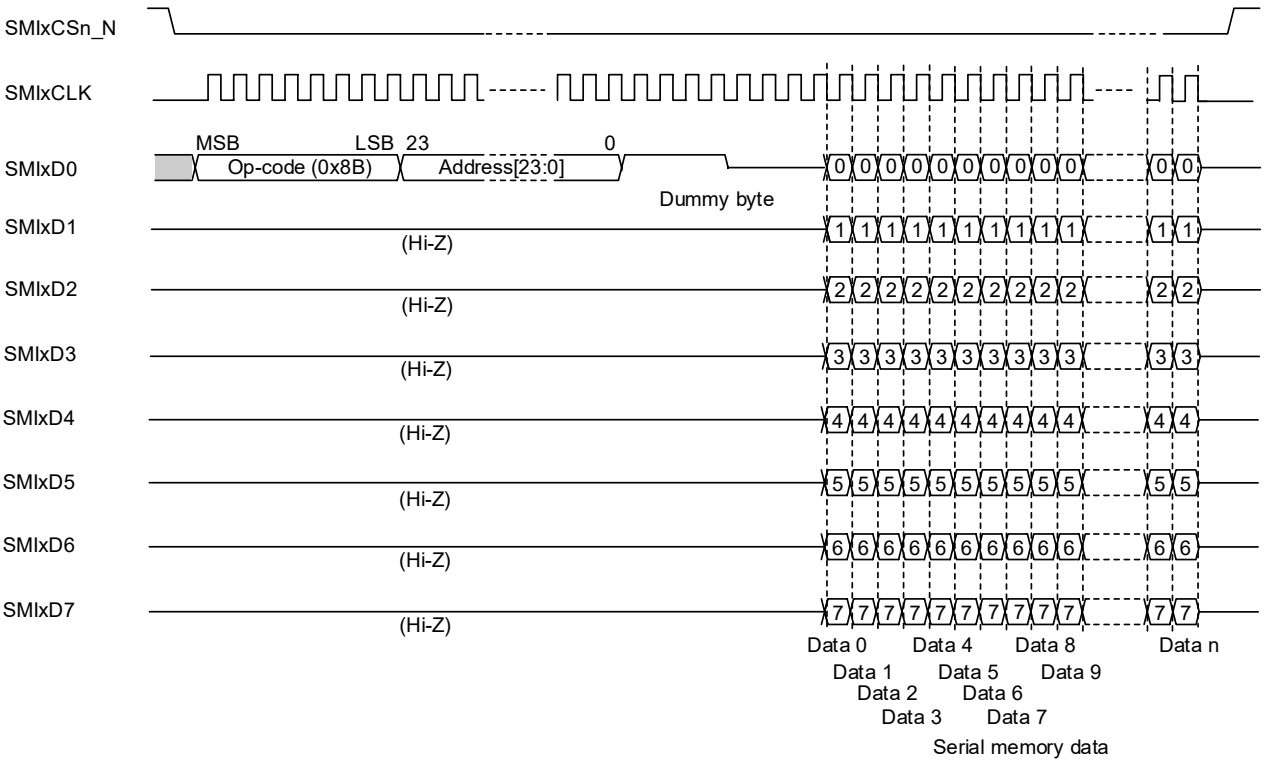

Figure 3.9 STR-Octal: FAST READ Octal Output

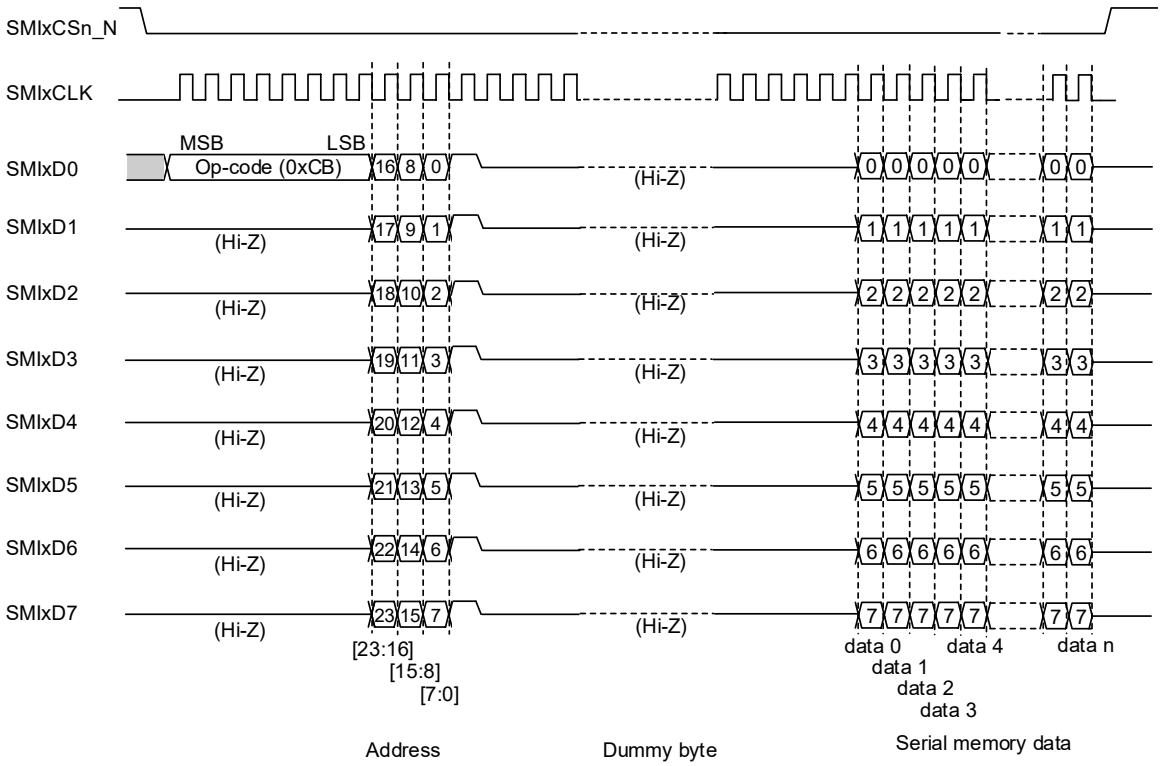

Figure 3.10 STR-Octal: FAST READ Octal I/O

(7) STR-OPI

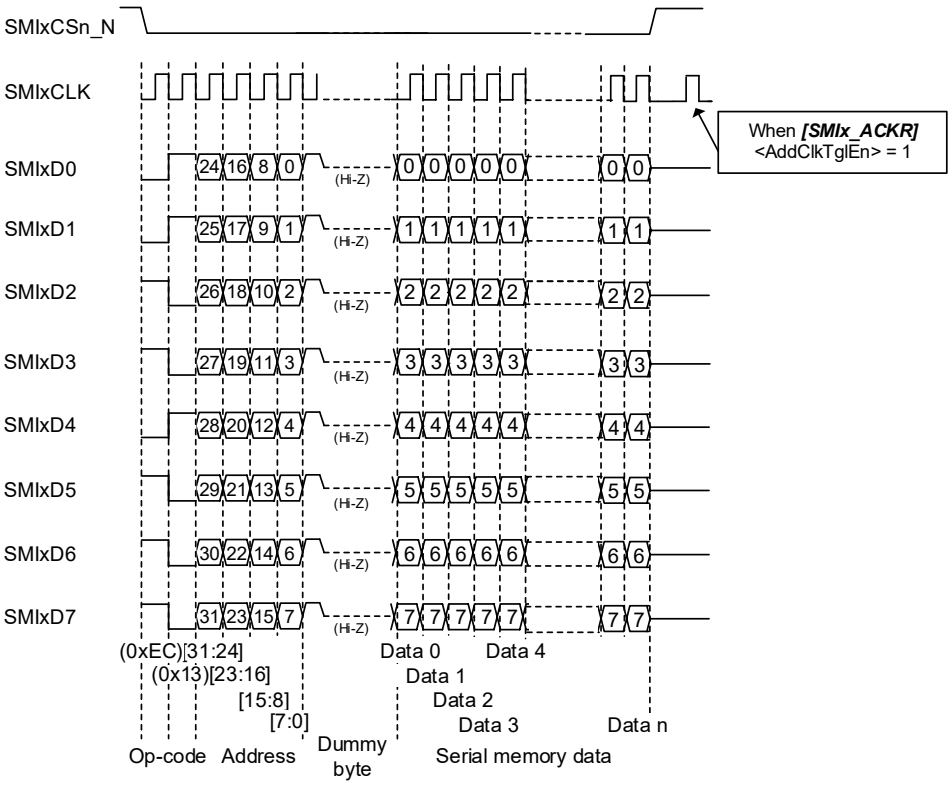

Figure 3.11 STR-OPI: Fast Read

3.4.1.2. Polling of WIP Bit

This function is mainly used for debugging.

Generally, SPI Flash cannot receive Read command during Write or Erase operation. So, when SMIF issues Read command to SPI Flash, the memory does not respond during Write or Erase operation. As a result, invalid data returns. Software should control this access not to be done.

This function enables to receive a correct data even when SPI Flash is read during Write or Erase operation. If a read is detected while this function is enabled, SMIF polls WIP bit in Status register in SPI Flash until it becomes "0". Then, the Read command is issued. This makes the correct data received. ***[SMIxDACRn]***<PollWIP> should be set to "1" to enable this function.

When the operation starts after the reset deassertion, WIP bit in Status register of SPI Flash should be polled to confirm that the state is neither Write nor Erase one. This function is controlled by the value in ***[SMIxDACRn]***<PollWIP>.

When this function is enabled, the overhead of a read becomes bigger because of the polling WIP bit per read.

Do not enable this function if no SPI Flash is connected or if a serial memory such as SPI RAM that does not have a WIP bit is connected.

3.4.1.3. Setting Procedure of Direct Access

(1) The base address and the capacity are set in ***[SMIxMAP0]***and ***[SMIxMAP1]*** according to the mapped serial memory.
(2) The transfer clock, CS deassertion time, and WIP polling function are set in ***[SMIxDACR0]***and ***[SMIxDACR1]***.
(3) The command op-code, the dummy byte count, and the input/output control are set in ***[SMIxDRCR0]***, ***[SMIxDRCR1]***, ***[SMIxDWCR0]***, and ***[SMIxDWCR1]***.
(4) Address in the mapping area in the serial memory is read/write.

Note: Immediately after the reset deassertion, the serial memory 0 is mapped to addresses "0xA0000000" to "0xA0FFFFFF" (16 MB).

3.4.2. Indirect Access

Indirect access issues commands such as PAGE PROGRAM, ERASE, CHIP ERASE, STATUS READ, and READ to SPI Flash through registers. Up to 288 bytes commands can be issued to SPI Flash using 32 bytes primary buffer and 256 bytes secondary buffer. The setting of indirect access is set in ***[SMIxRACR0]*** and ***[SMIxRACR1]*** for the serial memory 0 and the serial memory 1, respectively.

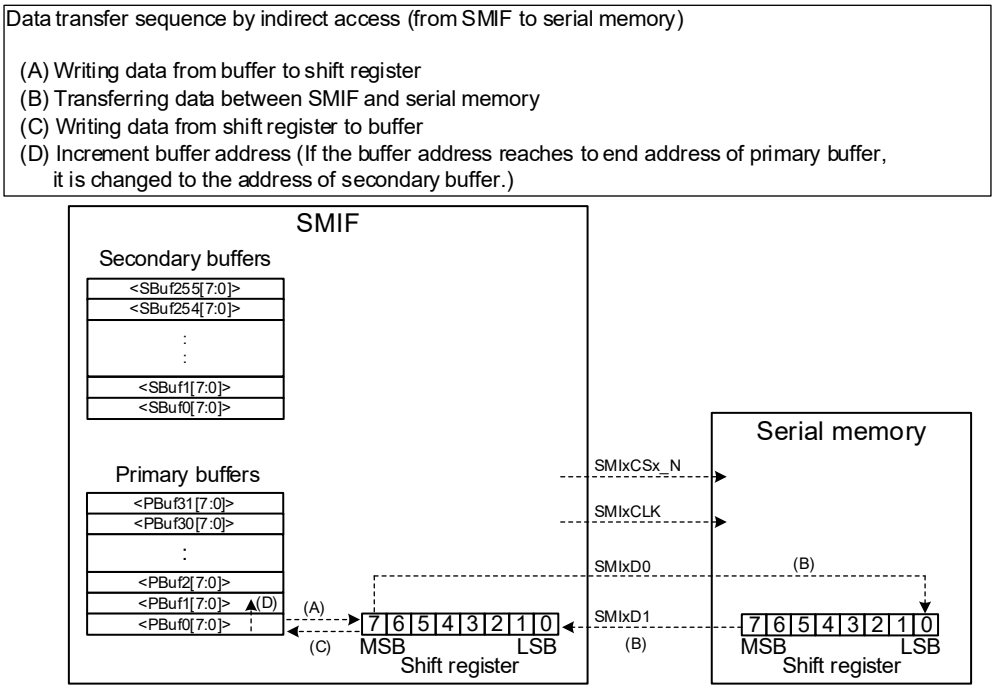

Figure 3.12 Indirect Access

3.4.3. Setting Procedure of Indirect Access

(1) No execution of the indirect access should be checked by reading ***[SMIxSTAT]***<CycProg>.

(2) The serial memory which should be accessed, the transfer byte count, and others should be set in ***[SMIxRACR0]***, ***[SMIxRACR1]***, and ***[SMIxINT]***.

(3) The command data should be set in the buffers ***[SMIxPBUFn]*** and ***[SMIxSBUFm]***.
(n = 0 to 7, m = 0 to 63)

(4) When ***[SMIxRACR1]***<CycGo> is set to "1", the commands are issued successively.

3.5. Transfer Clock

The frequency of the transfer clock (SMIxCLK) depends on a dividing value specified by ***[SMIxDACR0]***<SPR[4:0]>, ***[SMIxDACR1]***<SPR[4:0]>. ***[SMIxRACR0]***<SPR[4:0]>.

Frequency of SMIxCLK = fsys frequency / dividing value

The frequency of the transfer clock decided by a dividing value is shown in the following table.

Table 3.1 Transfer Clock

<SPR[4:0]>	0	1	2	3	4	5	6	7	8	9	10	11	12	・・・	28	29	30	31
Dividing / fsys [MHz]	2	2	3	4	5	6	7	8	9	10	11	12	13	・・・	29	30	31	32
200	100	100	66.6	50	40	33.3	28.5	25	22.2	20	18.1	16.6	15.3		6.89	6.66	6.45	6.25
160	80	80	53.3	40.0	32.0	26.7	22.9	20.0	17.8	16.0	14.5	13.3	12.3		5.52	5.33	5.16	5.00
140	70	70	46.7	35.0	28.0	23.3	20.0	17.5	15.6	14.0	12.7	11.7	10.8		4.83	4.67	4.52	4.38
120	60	60	40.0	30.0	24.0	20.0	17.1	15.0	13.3	12.0	10.9	10.0	9.2		4.14	4.00	3.87	3.75
100	50	50	33.3	25.0	20.0	16.7	14.3	12.5	11.1	10.0	9.1	8.3	7.7	・・・	3.45	3.33	3.23	3.13
80	40	40	26.7	20.0	16.0	13.3	11.4	10.0	8.9	8.0	7.3	6.7	6.2		2.76	2.67	2.58	2.50
60	30	30	20.0	15.0	12.0	10.0	8.6	7.5	6.7	6.0	5.5	5.0	4.6		2.07	2.00	1.94	1.88
40	20	20	13.3	10.0	8.0	6.7	5.7	5.0	4.4	4.0	3.6	3.3	3.1		1.38	1.33	1.29	1.25
20	10	10	6.7	5.0	4.0	3.3	2.9	2.5	2.2	2.0	1.8	1.7	1.5		0.69	0.67	0.65	0.63

Note1: When the dividing value is an odd number, the duty of the transfer clock is not 50 %.
Low width = (Dividing value)/2 + 0.5, High width = (Dividing value)/2 - 0.5.

Note2: Regarding of the available frequency of transfer clock, refer to "Electrical Characteristics" in datasheet.

3.6. Data Input and Output Timing

The data input or output is synchronous with the falling edge of SMIxCLK.

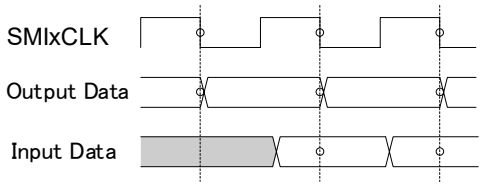

Figure 3.13 Data Input and Output Timing

3.7. Interrupt

When the SPI cycle controlled by the indirect access completes, ***[SMIxSTAT]***<CycDone> is set to "1". At the same time, the interrupt (INTSMIx) can be generated. The setting of ***[SMIxINT]***<SCDIntEn>=1 enables the interrupt generation.

In order to clear the generated interrupt, ***[SMIxSTAT]***<CycDone> should be set to "0".

When the SPI cycle controlled by the forced stop processing completes, ***[SMIxSTAT]***<StpProgDone> is set to "1". At the same time, the interrupt (INTSMIx) can be generated. The setting of ***[SMIxINT]***<SDIntEn>=1 enables the interrupt generation.

In order to clear the generated interrupt, ***[SMIxSTAT]***<StpProgDone> should be set to "0".

4. Registers

4.1. Register List

The control registers and their addresses are shown in the following tables.

Peripheral function		Channel/Unit	Base address	
			TYPE1	TYPE2
Serial memory interface	SMIF	ch 0	0x4000C000	0x4003C000

Note: The base address is different by products. Please refer to reference manual "Product Information" for details.

Register name		Address (Base+)
Address Map Control Register 0	***[SMIxMAP0]***	0x0000
Address Map Control Register 1	***[SMIxMAP1]***	0x0004
Direct Access Control Register 0	***[SMIxDACR0]***	0x0008
Direct Access Control Register 1	***[SMIxDACR1]***	0x000C
Direct Read Control Register 0	***[SMIxDRCR0]***	0x0010
Direct Read Control Register 1	***[SMIxDRCR1]***	0x0014
Direct Write Control Register 0	***[SMIxDRCR0]***	0x0018
Direct Write Control Register 1	***[SMIxDRCR1]***	0x001C
Indirect Access Control Register 0	***[SMIxRACR0]***	0x0400
Indirect Access Control Register 1	***[SMIxRACR1]***	0x0404
Indirect Access I/O Control Register	***[SMIxIOCR]***	0x0408
Indirect Access Output Enable Control Register	***[SMIxOECR]***	0x040C
Interrupt Control Register	***[SMIxINT]***	0x0440
Status Register	***[SMIxSTAT]***	0x0444
Software reset Register	***[SMIxSWR]***	0x0480
Additional Clock Control Register	***[SMIxACKR]***	0x0484
Transfer Clock/CS Pin Output Control Register	***[SMIxCCOR]***	0x0488
Forced Stop Control Register	***[SMIxSTPR]***	0x048C
Indirect Access Primary Buffer Register n	***[SMIxPBUFn]*** (n = 0 to 7)	0x0500 to 0x051C
Indirect Access Secondary Buffer Register m	***[SMIxSBUFm]*** (m = 0 to 63)	0x0600 to 0x06FC

4.2. Details of Registers

4.2.1. *[SMIxMAP0]* (Address Map Control Register 0)

Bit	Bit symbol	After reset	Type	Function
31:28	-	0	R	Read as "0".
27:16	FBA[11:0]	0x000	R/W	Mapping base address of Serial memory 0. (Note1) (Note2) "0x000" to "0x7FF": Base address <FBA[11:0]> upper base address of Serial memory 0.The lower address is set to "0x0000". ("0xA0000000" to "0xA7FF0000")
15:6	-	0	R	Read as "0".
5:2	FDEN[3:0]	1000	R/W	Capacity of serial memory 0 (Note2) 0000: 64KB 0110: 4MB 0001: 128KB 0111: 8MB 0010: 256KB 1000: 16MB 0011: 512KB 1001: 32MB 0100: 1MB 1010: 64MB 0101: 2MB 1011:128MB Others: : Reserved
1	WE	0	R/W	Write Enable 0: Disabled 1: Enabled
0	RE	1	R/W	Read Control 0: Disabled 1: Enabled

Note1: The value of <FBA[11:0]> should be aligned with the value set by <FDEN[3:0]>.

Note2: The address areas of serial memory 0 and serial memory 1 cannot overlap.

4.2.2. *[SMIxMAP1]* (Address Map Control Register 1)

Bit	Bit symbol	After reset	Type	Function
31:28	-	0	R	Read as "0".
27:16	FBA[11:0]	0x000	R/W	Mapping base address of Serial memory 1. (Note1) (Note2) "0x000" to "0x7FF": Base address <FBA[11:0]> upper base address of Serial memory 1.The lower address is set to "0x0000". ("0xA0000000" to "0xA7FF0000")
15:6	-	0	R	Read as "0".
5:2	FDEN[3:0]	1000	R/W	Capacity of Serial memory 1 (Note2) 0000: 64KB 0110: 4MB 0001: 128KB 0111: 8MB 0010: 256KB 1000: 16MB 0011: 512KB 1001: 32MB 0100: 1MB 1010: 64MB 0101: 2MB 1011:128MB Others: : Reserved
1	WE-	0	R/W	Write Enable 0: Disabled 1: Enabled
0	RE	1	R/W	Read Control 0: Disabled 1: Enabled

Note1: The value of <FBA[15:0]> should be aligned with the value set by <FDEN[3:0]>.

Note2: The address areas of serial memory 0 and serial memory 1 cannot overlap.

4.2.3. *[SMIxDACRn]* (Direct Access Control Register n) (n = 0, 1)

Bit	Bit symbol	After reset	Type	Function
31:21	-	0	R	Read as "0".
20:16	SPR[4:0]	11111	R/W	Dividing value for transfer clock of serial memory n 00000: 2 00001: 2 : 11110: 31 11111: 32
15:8	SCSD[7:0]	0x00	R/W	Deassertion time for SMIxCSn_N of serial memory n "0x00" to "0xFF": Deassertion time Deassertion time = fsys cycle time × <SCSD[7:0]>
7	-	0	R	Read as "0".
6	PollWIP	0	R/W	WIP in status register in SPI Flash is polled until it becomes "0" just before READ command is issued to SPI Flash. 0: Disabled 1: Enabled For the details, refer to Section "3.4.1.2 Polling of WIP Bit".
5:4	SDCE[1:0]	00	R/W	Write as "01". (Note 2)
3	-	0	R	Read as "0".
2	-	0	R/W	Write as "0".
1:0	-	0	R	Read as "0".

Note: The <SDCE[1:0]> becomes "00" after the reset. It should be written to "01" in the initialization setting.

4.2.4. *[SMIxDRCRn]* (Direct Read Control Register n) (n = 0, 1)

Bit	Bit symbol	After reset	Type	Function
31:24	CmdOp1[7:0]	0x00	R/W	Op-code 1 of SPI command of serial memory n Op-code of SPI command should be set.
23:16	CmdOp0[7:0]	0x0B	R/W	Op-code 0 of SPI command of serial memory n Op-code of SPI command should be set.
15:11	DmyBc[4:0]	00001	R/W	SPI dummy byte count of serial memory n "0" to "31"
10:9	AddrBc[1:0]	00	R/W	SPI address byte count 00: 3 bytes 01: 2 bytes 10: 4 bytes 11: Reserved
8	CmdBc	0	R/WR	SPI command byte count 0: 1 byte 1: 2 bytes
7:6	DatIO[1:0]	00	R/W	SPI data input and output control of serial memory n 00: Single 10: Quad 01: Dual 11: Octal
5:4	DmyIO[1:0]	00	R/W	SPI dummy input and output control of serial memory n 00: Single 10: Quad 01: Dual 11: Octal
3:2	AdrIO[1:0]	00	R/W	SPI address input and output control of serial memory n 00: Single 10: Quad 01: Dual 11: Octal
1:0	CmdIO[1:0]	00	R/W	SPI command input and output control of serial memory n 00: Single 10: Quad 01: Dual 11: Octal

4.2.5. *[SMIxDWCRn]* (Direct Write Control Register n) (n=0, 1)

Bit	Bit symbol	After reset	Type	Function
31:24	CmdOp1[7:0]	0x00	R/W	Op-code1 of SPI command of serial memory n Op-code of SPI command should be set.
23:16	CmdOp0[7:0]	0x02	R/W	Op-code 0 of SPI command of serial memory n Op-code of SPI command should be set.
15:11	DmyBc[4:0]	00000	R/W	SPI dummy byte count of serial memory n Set <DmyBc[4:0]> to "00000".
10:9	AddrBc[1:0]	00	R/W	SPI address byte count 00: 3 bytes 01: 2 bytes 10: 4 bytes 11: Reserved
8	CmdBc	0	R/WR	SPI command byte count 0: 1 byte 1: 2 bytes
7:6	DatIO[1:0]	00	R/W	SPI data input and output control of serial memory n 00: Single 10: Quad 01: Dual 11: Octal
5:4	DmyIO[1:0]	00	R/W	SPI dummy input and output control of serial memory n 00: Single 10: Quad 01: Dual 11: Octal
3:2	AdrIO[1:0]	00	R/W	SPI address input and output control of serial memory n 00: Single 10: Quad 01: Dual 11: Octal
1:0	CmdIO[1:0]	00	R/W	SPI command input and output control of serial memory n 00: Single 10: Quad 01: Dual 11: Octal

4.2.6. *[SMIxRACR0]* (Indirect Access Control Register 0)

Bit	Bit symbol	After reset	Type	Function
31:21	-	0	R	Read as "0".
20:16	SPR[4:0]	11111	R/W	Dividing value for transfer clock of serial memory n 00000: 2 00001: 2 : 11110: 31 11111: 32
15:8	SCSD[7:0]	0xFF	R/W	Deassertion time for SMIxCSn_N of serial memory n "0x00" to "0xFF": Deassertion time Deassertion time = fsys cycle time × <SCSD[7:0]>
7:6	-	0	R	Read as "0".
5:4	SDCE[1:0]	00	R/W	Write as "01". (Note2)
3	-	0	R	Read as "0".
2	-	0	R/W	Write as "0".
1:0	-	0	R	Read as "0".

Note: The <SDCE[1:0]> becomes "00" after the reset. It should be written to "01" in the initialization setting.

4.2.7. *[SMIxRACR1]* (Indirect Access Control Register 1)

Bit	Bit symbol	After reset	Type	Function
31:24	SBufBc[7:0]	0x00	R/W	Transfer bytes count of the secondary buffer "0" to "255" The data, whose number is ***[SMIxRACR1]***<SBufBc[7:0]> +1, in the secondary buffer are transferred.
23:22	-	0	R	Read as "0".
21	-	0	R/W	Write as "0".
20:16	PBufBc[4:0]	00000	R/W	Transfer bytes count of the primary buffer (Note2) "0" to "31" The data, whose number is ***[SMIxRACR1]***<SBufBc[7:0]> +1, in the primary buffer are transferred.
15:6	-	0	R	Read as "0".
5	SBufEn	0	R/W	Secondary buffers enable control (Note3) 0: Secondary buffers are not used. 1: Secondary buffer is used.
4	PBufEn	0	R/W	Primary buffers enable control 0: Primary buffer is not used. 1: Primary buffer is used.
3:2	-	0	R	Read as "0".
1	CSNum	0	R/W	Asserted CS 0: SMIxCS0_N 1: SMIxCS1_N
0	CycGo	0	R/W	Indirect access control 0: Do not care 1: Start by indirect access (Note1) After starting, this bit is cleared. Read as "0".

Note1: <CycGo> should not be set to "1" while ***[SMIxSTAT]***<CycProg> is "1" (during SPI cycle).

Note2: When transferring with Quad or Octal by using the secondary buffer, use the following settings.
For Quad: <PBufBc[4:0]> ≥ 1
For Octal: <PBufBc[4:0]> ≥ 2

Note3: It is not possible to use only secondary buffer. Use in conjunction with primary buffer.

4.2.8. *[SMIxIOCR]* (Indirect Access I/O Control Register)

Bit	Bit symbol	After reset	Type	Function
31:21	-	0	R	Read as "0".
20:16	PBufIOCtrl[4:0]	00000	R/W	Width control for primary buffer output "0" to "6" For example, specify "00000" for QPI and OPI where all of the configured commands are multi I/O communication
15:4	-	0	R	Read as "0".
3:2	SBufIOCtrlEn[1:0]	00	R/W	Secondary Buffer I/O Control Register (Note) 00: Single 01: Reserved 10: Quad 11: Octal
1:0	PBufIOCtrlEn[1:0]	00	R/W	Primary Buffer I/O control Register 00: Single 01: Reserved 10: Quad 11: Octal

Note: When not using the secondary buffer, set <SBufIOCtrlEn[1:0]> to the same setting as <PBufIOCtrlEn[1:0]>.

4.2.9. *[SMIxOECR]* (Indirect Access Output Enable Control Register)

Bit	Bit symbol	After reset	Type	Function
31:21	-	0	R	Read as "0".
20:16	PBufOEnC[4:0]	00000	R/W	Primary Buffer Output Enable Control (Note1) "0" to "6" When <PBufOCEn> = 1, the primary buffer data transmission/reception direction is switched from the specified byte transfer position. For example, specify "4" for FAST READ, which has one command op-code byte count and 3 address byte count. By doing so, the I/O direction is switched to the input direction during the dummy communication period, and a turnaround is realized.
15:1	-	0	R	Read as "0".
0	PBufOCEn	0	R/W	Primary Buffer Output Control (Note2) 0: Disabled 1: Enabled

Note 1: Set <PBufOEnC[4:0]> to the value equal or greater than ***[SMIxIOCR]***<PBufIOCtrl[4:0]>.

Note 2: Set <PBufOCEn> to "0" when using single for SPI command input/output.

4.2.10. *[SMIxINT]* (Interrupt Control Register)

Bit	Bit symbol	After reset	Type	Function
31:5	-	0	R	Read as "0".
4	SDIntEn	0	R/W	Forced stop processing completion interrupt control 0: Disabled 1: Enabled Control the completion interrupt output for forced stop processing.
3:1	-	0	R	Read as "0".
0	SCDIntEn	0	R/W	Indirect access completion interrupt control 0: Disabled 1: Enabled Control the completion interrupt output of indirect access.

4.2.11. *[SMIxSTAT]* (Status Register)

Bit	Bit symbol	After reset	Type	Function
31:7	-	0	R	Read as "0".
6	DiAccInProg	0	R	Status of direct access in progress 0: No direct access has occurred. 1: Direct access has occurred. Indicate whether direct access has occurred.
5		0	R	Read as "0".
4	StpProgDone	0	R	Status of forced stop process done 0: Forced stop processing is not completed or has not occurred. 1: Forced stop processing has been completed. Indicate the completion status of the forced stop processing. The hardware sets this bit to "1". It remains "1" until cleared by software. When this bit is set and ***[SMIxINT]***<SDIntEn> is "1", an interrupt is asserted.
			W	Forced stop interrupt clear 0: Clear 1: Don't care
3:2	-	0	R	Read as "0".
1	CycProg	0	R	Status of SPI cycle in progress 0: Indirect access has not occurred. 1: Indirect access has occurred. This bit is set to "1" after <CycGo> is set. It is reset to "0" when the SPI cycle is completed.
0	CycDone	0	R	Status SPI cycle done 0: Indirect access is not completed or has not occurred. 1: Indirect access has been completed. After completing the SPI cycle, the hardware sets this bit to "1". It remains "1" until cleared by software. If this bit is set and ***[SMIxINT]***<SCDIntEn> is "1", an interrupt will be asserted.
			W	SPI cycle completion interrupt clear 0: Clear 1: Don't care

4.2.12. *[SMIxSWR]* (Software Reset Register)

Bit	Bit symbol	After Reset	Type	Function
31:1	-	0	R	Read as "0".
0	RstEn	0	R/W	Reset enable Control software reset to SMIF. When "1" is written to this field, SMIF immediately executes reset processing. After this, when the reset is completed, this field is cleared to "0" (Note). 0: Software reset completed or not issued 1: Software reset in progress

Note: After executing reset processing, <RstEn> should be polling until it becomes "0".

4.2.13. *[SMIxACKR]* (Additional Clock Control Register)

Bit	Bit symbol	After Reset	Type	Function
31:9	-	0	R	Read as "0".
8	AddClkTglEn	0	R/W	Additional clock toggle enable 0: Additional clock not output 1: Additional clock output When SMIxCSn_N becomes "High" after SPI transfer is completed, it controls whether to output one additional transfer clock pulse. The setting of <FrcClkOutEn> has priority.
7:1	-	0	R	Read as "0".
0	FrcClkOutEn	0	R/W	SMIxCLK output enable 0: SMIxCLK is output only when SPI communication occurs 1: SMIxCLK is output without SPI transfer If ***[SMIxCCOR]***<ClkOE> = 1, output SMIxCLK.

4.2.14. *[SMIxCCOR]* (Transfer Clock/CS Output Enable Control Register)

Bit	Bit symbol	After Reset	Type	Function
31:6	-	0	R	Read as "0".
5	Cs1OE	0	R/W	Chip select 1 output enable 0: Disabled (Hi-Z) 1: Enabled Control the output f SMIxCS1_N.
4	Cs0OE	0	R/W	Chip select 0 output enable 0: Disabled (Hi-z) 1: Enabled Control the output of SMIxCS0_N.
3:1	-	0	R	Read as "0".
0	ClkOE	0	R/W	Clock Output Enable 0: Disabled (Hi-z) 1: Enabled Control the output of SMIxCLK.

Note: The port should be also set. Refer to reference manual "Input/Output PORT" for details.

4.2.15. *[SMIxSTPR]* (Forced Stop Control Register)

Bit	Bit symbol	After Reset	Type	Function
31:1	-	0	R	Read as "0".
0	StopEn	0	R/W	Stop Enable 0: Request not issued 1: Request issued Issue a request to force SMIF to stop the operation. If "1" is written to this field ("0" write is ignored), SMIF immediately executes stopping processing. The software reset is required to initialize SMIF.

Note: When communication with the serial memory is occurring, SMIF sets the chip select signal to "High" and interrupts the communication. If a forced stop is performed, the validity of the data is not guaranteed.

4.2.16. *[SMIxPBUFn]* (Indirect Access Primary Buffer Register n) (n = 0 to 7)

Bit	Bit symbol	After reset	Type	Function
31:24	PBuf(4n+3)[7:0]	Undefined	R/W	Primary buffer
23:16	PBuf(4n+2)[7:0]	Undefined	R/W	Primary buffer
15:8	PBuf(4n+1)[7:0]	Undefined	R/W	Primary buffer
7:0	PBuf(4n+0)[7:0]	Undefined	R/W	Primary buffer

Note: The capacity of the primary buffer differs depending on the product. For details, refer to the reference manual "Product Information".

4.2.17. *[SMIxSBUFm]* (Indirect Access Secondary Buffer Register m) (m = 0 to 63)

Bit	Bit symbol	After reset	Type	Function
31:24	SBuf(4m+3)[7:0]	Undefined	R/W	Secondary buffer
23:16	SBuf(4m+2)[7:0]	Undefined	R/W	Secondary buffer
15:8	SBuf(4m+1)[7:0]	Undefined	R/W	Secondary buffer
7:0	SBuf(4m+0)[7:0]	Undefined	R/W	Secondary buffer

Note: The capacity of the secondary buffer differs depending on the product. For details, refer to the reference manual "Product Information".

5. Example of Usage

5.1. Initial Setting

Software must initialize the SMIF after the it is released from reset. This section describes the following:

In order to use SMIF, a clock must be supplied to SMIF. Refer to the reference manual "Clock Control and Operation Mode" for the procedure. And it is necessary to assign I/O pin functions so that SMIF can use the I/O pins of the product. For the procedure, refer to the reference manual "Input/Output PORT".

After the above settings are completed, perform initial settings using the registers of SMIF. The outline of the initial setting is as follows.

- Common settings for direct access and indirect access
- Direct access serial memory 0 setting
- Direct access serial memory 1 setting
- Indirect access settings

5.1.1. Common Settings for Direct Access and Indirect Access

The following registers are related to both direct access and indirect access.

- ***[SMIxINT]***
  - Controls interrupt output of both forced stop and indirect access complete.
  - The interrupts of SMIF are a level output of polarity "High". When using interrupt, its clearing must be done in software.

- ***[SMIxACKR]***
  - <AddClkTglEn>
    This bit is set to "1" if the serial memory requires SMIxCLK output after deassertion of chip select to decide the completion of each SPI communication. Normally this bit should be set to "0", but some special devices need to be set to "1". Set this bit according to the specifications of the serial memory.
  - <FrcClkOutEn>
    This bit is used when SMIxCLK output is required to confirm the reset release of serial memory. Set this bit to "1" according to the reset release sequence of the serial memory, and then set it to "0" again after the wait period. The wait period depends on the serial memory specifications. Do not perform SPI communication with this bit set to "1".

- ***[SMIxCCOR]***
  - Control the I/O direction of SMIxCLK, SMIxCS0_N, SMIxCS1_N. Set the pins to be used to output enable. It is different from the control of the port part. Note that both controls are required.

5.1.2. Direct Access Serial Memory 0 Setting

Shows the initial state for direct access serial memory 0.

- Memory map: Refer to the reference manual "Clock Control and Operation Mode". The SMIF has a 128MB area.
- Read command issuing function: Enabled
- Write command issuing function: Disabled
- Read command: Op-code byte count: 1, op-code: 0x0B, address byte count: 3, dummy byte count: 1
- Write command: Op-code byte count: 1, op-code: 0x02, address byte count: 3, dummy byte count: 0
- Chip select deassertion time: 0 ns
- Transfer clock: Divide fsys by 32

Set SMIF according to the serial memory connected to the chip select pin (SMIxCS0_N). Perform the following procedure.

(1) Set memory map according to the serial memory specification. Set it by ***[SMIxMAP0]***<FBA[11:0]>, <FDEN[3:0]>.
(2) Set the transfer clock, chip select deassertion time according to the serial memory AC timing. Set it by ***[SMIxDACR0]***<SPR[4:0]>, <SCSD[7:0]>.
(3) If necessary, change the command configuration issued to the serial memory (for example, when using multi I/O as 4 × I/O or 8 × I/O). Set it by ***[SMIxDRCR0].***
(4) If a write command is issued to a flash memory, set the command configuration to issue with ***[SMIxDWCR0]***. Then, set ***[SMIxMAP0]***<WE> to "1".

5.1.3. Direct Access Serial Memory 1 Setting

The function of direct access serial memory 1 is disabled after reset. Set ***[SMIxMAP1]***<FBA[11:0]>, <FDEN[3:0]>, ***[SMIxDACR1]***<SPR[4:0]>, <SCSD[7:0]>, <SDCE[1:0]>, ***[SMIxDRCR1]***, and ***[SMIxDWCR1]*** according to the serial memory specification. After these settings are completed, set ***[SMIxMAP1]***<RE> and <WE> to "1" to enable SMIF to issue read and write commands.

5.1.4. Indirect Access Setting

The indirect access setting includes the selection of the chip select that issues the command. In indirect access, different settings can be made each time a transfer is performed.

The transfer clock and chip select deassert time must be set according to the serial memory.
Set them by ***[SMIxRACR0]***<SPR[4:0]>, <SCSD[7:0]>, <SDCE[1:0]> respectively. Use ***[SMIxINT]***<SCDIntEn> to set whether to generate the interrupt when the indirect access is completed.

5.1.5. Transfer Clock

The frequency of the transfer clock (SMIxCLK) is decided by the dividing value of ***[SMIxDACR0]***<SPR[4:0]>, ***[SMIxDACR1]***<SPR[4:0]>, and ***[SMIxRACR0]***<SPR[4:0]>.

Frequency of transfer clock = fsys frequency / dividing value

Note1: When the dividing value is an odd number, the duty of the transfer clock is not 50 %.
Low width = (Dividing value)/2 + 0.5, High width = (Dividing value)/2 - 0.5.

Note2: Regarding of the available frequency of transfer clock, refer to "Electrical Characteristics" in datasheet.

5.2. Programming Method for Direct Access

The software does not need to change the direct access settings as long as it continues to communicate with the serial memory.

When SMIF detects a read or write access to the direct access area, it issues a command to the serial memory based on the following register settings. For details on the settings, refer to 5.1.2 and 5.1.3.

- ***[SMIxMAP0]***
- ***[SMIxMAP1]***
- ***[SMIxDACR0]***
- ***[SMIxDACR1]***
- ***[SMIxDRCR0]***
- ***[SMIxDRCR1]***
- ***[SMIxDWCR0]***
- ***[SMIxDWCR1]***

To change ***[SMIxDACR0]***<SPR[4:0]> and ***[SMIxDACR1]***<SPR[4:0]>, perform a dummy read (read without using the return value of read) for the corresponding direct access area after changing the setting. This dummy read is not required during the initial setting.

Note: When the software changes the direct access setting, instructions cannot be executed in the target direct access area.

5.3. Programming Method for Indirect Access

5.3.1. Basic Procedure

Follow the procedure below to program indirect access.

(1) To wait for the completion of indirect access by interrupt, write "1" to ***[SMIxINT]***<SCDIntEn>.

(2) Check ***[SMIxSTAT]***<CycPrgrs> for no indirect access in progress.

(3) If necessary, set the transfer clock and chip select deassertion time by ***[SMIxRACR0]***<SPR[4:0]>, <SCSD[7:0]> respectively.

(4) Change the command configuration issued to the serial memory.

(5) Set ***[SMIxRACR1]***<CycGo> to "1" to start indirect access (Note 1).

(6) Wait for the indirect access to complete. (Wait for the indirect access completion interrupt or wait until ***[SMIxSTAT]***<CycDone> is set to "1" (Note 2).)

(7) Write "0" to ***[SMIxSTAT]***<CycDone>.

Note 1: Writing "1" to ***[SMIxRACR1]***<CycGo> and setting values of other bits may be changed at the same time.

Note 2: Writing to the following registers is prohibited until ***[SMIxSTAT]***<CycDone> is set to "1" after writing "1" to ***[SMIxRACR1]***<CycGo>.

- ***[SMIxRACR0]***
- ***[SMIxRACR1]***
- ***[SMIxIOCR]***
- ***[SMIxOECR]***
- ***[SMIxPBUFn]***
- ***[SMIxSBUFm]***

Set the command configuration for the supported device as follows.

The data width and transfer direction of I/O used for communication with serial memory are set as follows using ***[SMIxIOCR]*** and ***[SMIxOECR]***.

(1) ***[SMIxIOCR]***

(a) <PBufIOCtrlEn[1:0]>
Set these bits to "00" for SPI communication, "10" (4×I/O) or "11" (8×I/O) for multi I/O communication.

(b) <PBufIOCtrl[4:0]>
When <PBufIOCtrlEn[1:0]> is set for SPI communication, these bits setting is invalid. When it is set for multi I/O communication, specify the byte number at which the I/O width switches. For example, for QPI and OPI communication where the entire command is multi I/O communication, set these bits to "00000".

(2) ***[SMIxOECR]***

(a) <PBufOCEn>
Set this bit to "0" for transmission, "0" for SPI communication and reception, "1" for multi I/O communication and reception.

(b) <PBufOEnC[4:0]>
When transmission or <PBufOCEn> is set for SPI communication, these bits setting is invalid. When it is set for multi I/O communication and reception, specify the byte number at which the I/O direction switches from OUT to IN. For example, if the command op-code byte count is "1" and the address byte count is "3" for FAST READ, set these bits to "00100".

- Set the command op-code and address to be used for transfer in ***[SMIxPBUFn]***.
- The transfer direction is transmission, set the transmission data in ***[SMIxSBUFm]***.
- ***[SMIxRACR1]***<SBufBc[7:0]>, <PBufBc[4:0]>, <SBufEn>, <PBufEn> are set the number of bytes in the primary and secondary buffers used for transfer (Note 1)).
- Set the chip select number to which the communication destination device is connected to ***[SMIxRACR1]***<CSNum> (Note).

Note: Writing "1" to ***[SMIxRACR1]***<CycGo> and setting values of other bits may be changed at the same time.

5.3.2. Programming Example: PAGE PROGRAM, WRITE

The procedure for transmitting 256-byte data (Data[2047:0]) to the 3-byte physical address (Addr[23:0]) of the SPI Flash is shown below.

Note: The SPI Flash enters the BUSY state after executing this command. A device in the BUSY state can normally communicate only with some commands such as status register read. If the instruction are stored in the SPI Flash, do not fetch the instruction from the SPI Flash until the BUSY state is released. If a memory read access to the SPI Flash is executed during BUSY state, a correct data cannot be read from the SPI Flash.

The command configuration is as follows: command op-code byte count: 1, address byte count: 3, dummy byte count: 0, payload data byte count: 256. The I/O width of the command is all SPI. The command op-code is "0x02".

(1) Set the following values in the primary buffer.

- <PBuf0[7:0]> = Op-code (0x02)
- <PBuf1[7:0]> = Address[23:16] (Addr[23:16])
- <PBuf2[7:0]> = Address[15:8] (Addr[15:8])
- <PBuf3[7:0]> = Address[7:0] (Addr[7:0])

(2) Set the following values in the secondary buffer.

- <SBuf0[7:0]> = Data 0 (Data[7:0], data written to Addr[23:0] + 0x00)
- <SBuf1[7:0]> = Data 1 (Data[15:8], data written to Addr[23:0] + 0x01)
  :
- <SBuf254[7:0]> = Data 254 (Data[2039:2032], data written to Addr[23:0] + 0xFE)
- <SBuf255[7:0]> = Data 255 (Data[2047:2040], data written to Addr[23:0] + 0xFF)

(3) ***[SMIxRACR1]*** settings

- <PBufEn> = 1, <PBufBc[4:0]> = 00011
- <SBufEn> = 1, <SBufBc[7:0]> = 0xFF
- <CSNum> = Chip select number connected to SPI Flash

(4) ***[SMIxIOCR]*** settings

- <PBufIOCtrlEn[1:0]> = 00 (SPI communication)
- <SBufIOCtrlEn[1:0]> = 00 (SPI communication)
- <PBufIOCtrl[4:0]> = Don't care

(5) ***[SMIxOECR]*** settings

- <PBufOCEn> = 0 (transmit)
- <PBufOEnC[4:0]> = Don't care

(6) Set ***[SMIxRACR1]***<CycGo> to "1" to start indirect access.

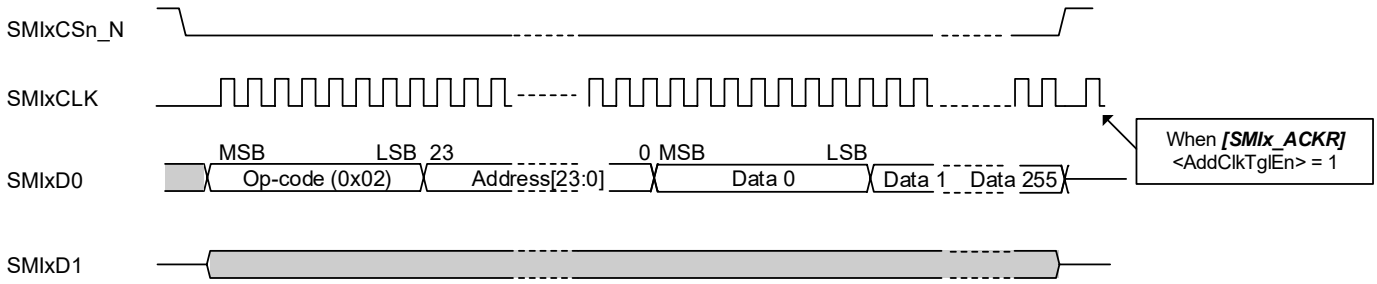

Figure 5.1 PAGE PROGRAM, WRITE

5.3.3. Programming Example: Quad I/O PAGE PROGRAM, Quad I/O WRITE

The procedure for transmitting 256-byte data (Data[2047:0]) to the 3-byte physical address (Addr[23:0]) of the SPI Flash by 4 × I/O is shown below.

Note: The SPI Flash enters the BUSY state after executing this command. A device in the BUSY state can normally communicate only with some commands such as status register read. If the instruction are stored in the SPI Flash, do not fetch the instruction from the SPI Flash until the BUSY state is released. If a memory read access to the SPI Flash is executed during BUSY state, a correct data cannot be read from the SPI Flash.

The command configuration is as follows: command op-code byte count: 1, address byte count: 3, dummy byte count: 0, payload data byte count: 256. The I/O width of the command is SPI for command op-code, 4 × I/O following address. The command of op-code is "0x38".

(1) Set the following values in the primary buffer.

- <PBuf0[7:0]> = Op-code (0x38)
- <PBuf1[7:0]> = Address[23:16] (Addr[23:16])
- <PBuf2[7:0]> = Address[15:8] (Addr[15:8])
- <PBuf3[7:0]> = Address[7:0] (Addr[7:0])

(2) Set the following values in the secondary buffer.

- <SBuf0[7:0]> = Data 0 (Data[7:0], data written to Addr[23:0] + 0x00)
- <SBuf1[7:0]> = Data 1 (Data[15:8], data written to Addr[23:0] + 0x01)
  :
- <SBuf254[7:0]> = Data 254 (Data[2039:2032], data written to Addr[23:0] + 0xFE)
- <SBuf255[7:0]> = Data 255 (Data[2047:2040], data written to Addr[23:0] + 0xFF)

(3) ***[SMIxRACR1]*** settings

- <PBufEn> = 1, <PBufBc[4:0]> = 00011
- <SBufEn> = 1, <SBufBc[7:0]> = 0xFF
- <CSNum> = Chip select number connected to SPI Flash

(4) ***[SMIxIOCR]*** settings

- <PBufIOCtrlEn[1:0]> = 10 (4 × I/O communication)
- <SBufIOCtrlEn[1:0]> = 10 (4 × I/O communication)
- <PBufIOCtrl[4:0]> = 00001 (single communication for command op-code, multi I/O communication following address)

(5) ***[SMIxOECR]*** settings

- <PBufOCEn> = 0 (transmit)
- <PBufOEnC[4:0]> = Don't care

(6) Set ***[SMIxRACR1]***<CycGo> to "1" to start indirect access.

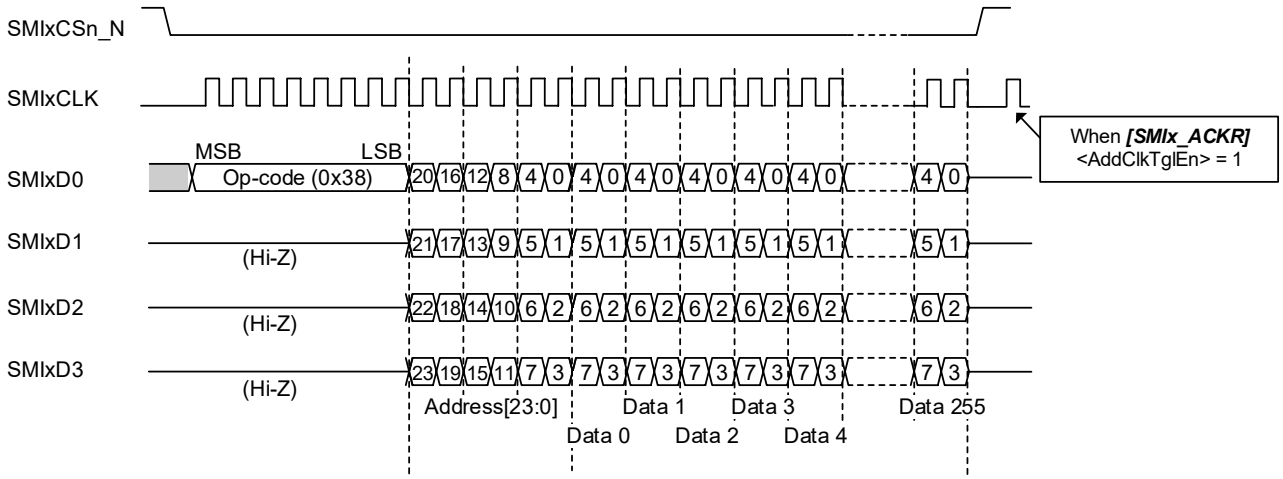

Figure 5.2 Quad I/O PAGE PROGRAM, Quad I/O WRITE

5.3.4. Programming Example: QPI PAGE PROGRAM, QPI WRITE

The procedure for transmitting 256-byte data (Data[2047:0]) to the 3-byte physical address (Addr[23:0]) of the SPI Flash by QPI is shown below.

Note: The SPI Flash enters the BUSY state after executing this command. A device in the BUSY state can normally communicate only with some commands such as status register read. If the instruction are stored in the SPI Flash, do not fetch the instruction from the SPI Flash until the BUSY state is released. If a memory read access to the SPI Flash is executed during BUSY state, a correct data cannot be read from the SPI Flash.

The command configuration is as follows: command op-code byte count: 1, address byte count: 3, dummy byte count: 0, payload data byte count: 256. The I/O width of the command is all 4 × I/O. The command op-code is "0x02".

(1) Set the following values in the primary buffer.

- <PBuf0[7:0]> = Op-code (0x02)
- <PBuf1[7:0]> = Address[23:16] (Addr[23:16])
- <PBuf2[7:0]> = Address[15:8] (Addr[15:8])
- <PBuf3[7:0]> = Address[7:0] (Addr[7:0])

(2) Set the following values in the secondary buffer.

- <SBuf0[7:0]> = Data 0 (Data[7:0], data written to Addr[23:0] + 0x00)
- <SBuf1[7:0]> = Data 1 (Data[15:8], data written to Addr[23:0] + 0x01)
  :
- <SBuf254[7:0]> = Data 254 (Data[2039:2032], data written to Addr[23:0] + 0xFE)
- <SBuf255[7:0]> = Data 255 (Data[2047:2040], data written to Addr[23:0] + 0xFF)

(3) ***[SMIxRACR1]*** settings

- <PBufEn> = 1, <PBufBc[4:0]> = 00011
- <SBufEn> = 1, <SBufBc[7:0]> = 0xFF
- <CSNum> = Chip select number connected to SPI Flash

(4) ***[SMIxIOCR]*** settings

- <PBufIOCtrlEn[1:0]> = 10 (4 × I/O communication)
- <SBufIOCtrlEn[1:0]> = 10 (4 × I/O communication)
- <PBufIOCtrl[4:0]> = 00000 (multi I/O communication)

(5) ***[SMIxOECR]*** settings

- <PBufOCEn> = 0 (transmit)
- <PBufOEnC[4:0]> = Don't care

(6) Set ***[SMIxRACR1]***<CycGo> to "1" to start indirect access.

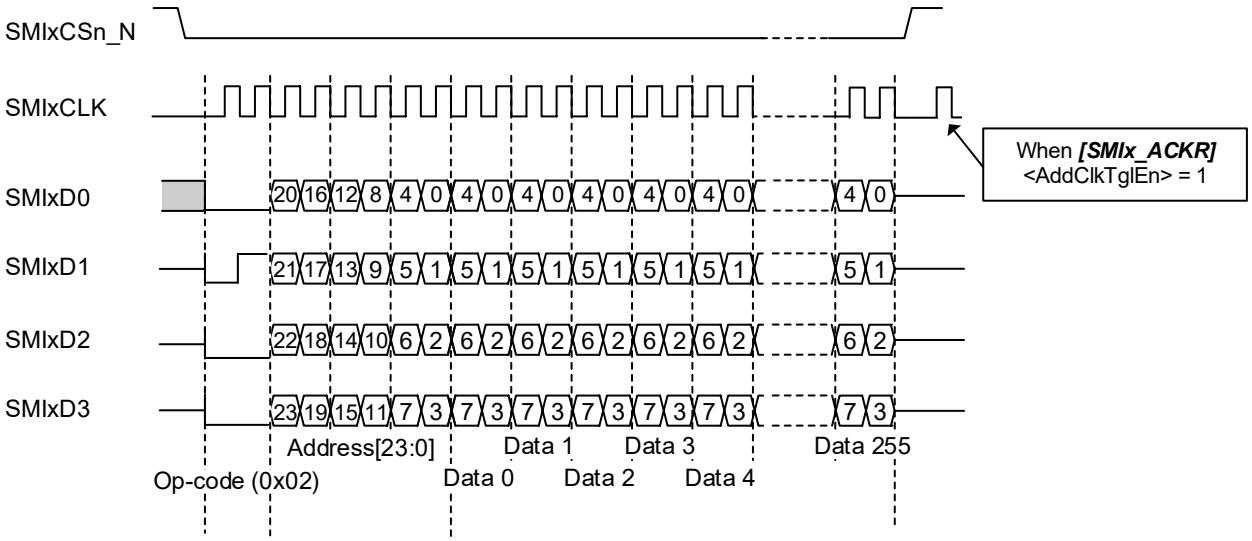

Figure 5.3 QPI PAGE PROGRAM, QPI WRITE

5.3.5. Programming Example: Octal I/O PAGE PROGRAM, Octal I/O WRITE

The procedure for transmitting 256-byte data (Data[2047:0]) to the 3-byte physical address (Addr[23:0]) of the SPI Flash by 8 × I/O is shown below.

Note: The SPI Flash enters the BUSY state after executing this command. A device in the BUSY state can normally communicate only with some commands such as status register read. If the instruction are stored in the SPI Flash, do not fetch the instruction from the SPI Flash until the BUSY state is released. If a memory read access to the SPI Flash is executed during BUSY state, a correct data cannot be read from the SPI Flash.

The command configuration is as follows: command op-code byte count: 1, address byte count: 3, dummy byte count: 0, payload data byte count: 256. The I/O width of the command is SPI for command op-code, 8 × I/O following address. The command op-code is "0xC2".

(1) Set the following values in the primary buffer.

- <PBuf0[7:0]> = Op-code (0xC2)
- <PBuf1[7:0]> = Address[23:16] (Addr[23:16])
- <PBuf2[7:0]> = Address[15:8] (Addr[15:8])
- <PBuf3[7:0]> = Address[7:0] (Addr[7:0])

(2) Set the following values in the secondary buffer.

- <SBuf0[7:0]> = Data 0 (Data[7:0], data written to Addr[23:0] + 0x00)
- <SBuf1[7:0]> = Data 1 (Data[15:8], data written to Addr[23:0] + 0x01)
  :
- <SBuf254[7:0]> = Data 254 (Data[2039:2032], data written to Addr[23:0] + 0xFE)
- <SBuf255[7:0]> = Data 255 (Data[2047:2040], data written to Addr[23:0] + 0xFF)

(3) ***[SMIxRACR1]*** settings

- <PBufEn> = 1, <PBufBc[4:0]> = 00011
- <SBufEn> = 1, <SBufBc[7:0]> = 0xFF
- <CSNum> = Chip select number connected to SPI Flash

(4) ***[SMIxIOCR]*** settings

- <PBufIOCtrlEn[1:0]> = 11 (8 × I/O communication)
- <SBufIOCtrlEn[1:0]> = 11 (8 × I/O communication)
- <PBufIOCtrl[4:0]> = 00001 (single communication for command op-code, multi I/O communication following address)

(5) ***[SMIxOECR]*** settings

- <PBufOCEn> = 0 (transmit)
- <PBufOEnC[4:0]> = Don't care

(6) Set ***[SMIxRACR1]***<CycGo> to "1" to start indirect access.

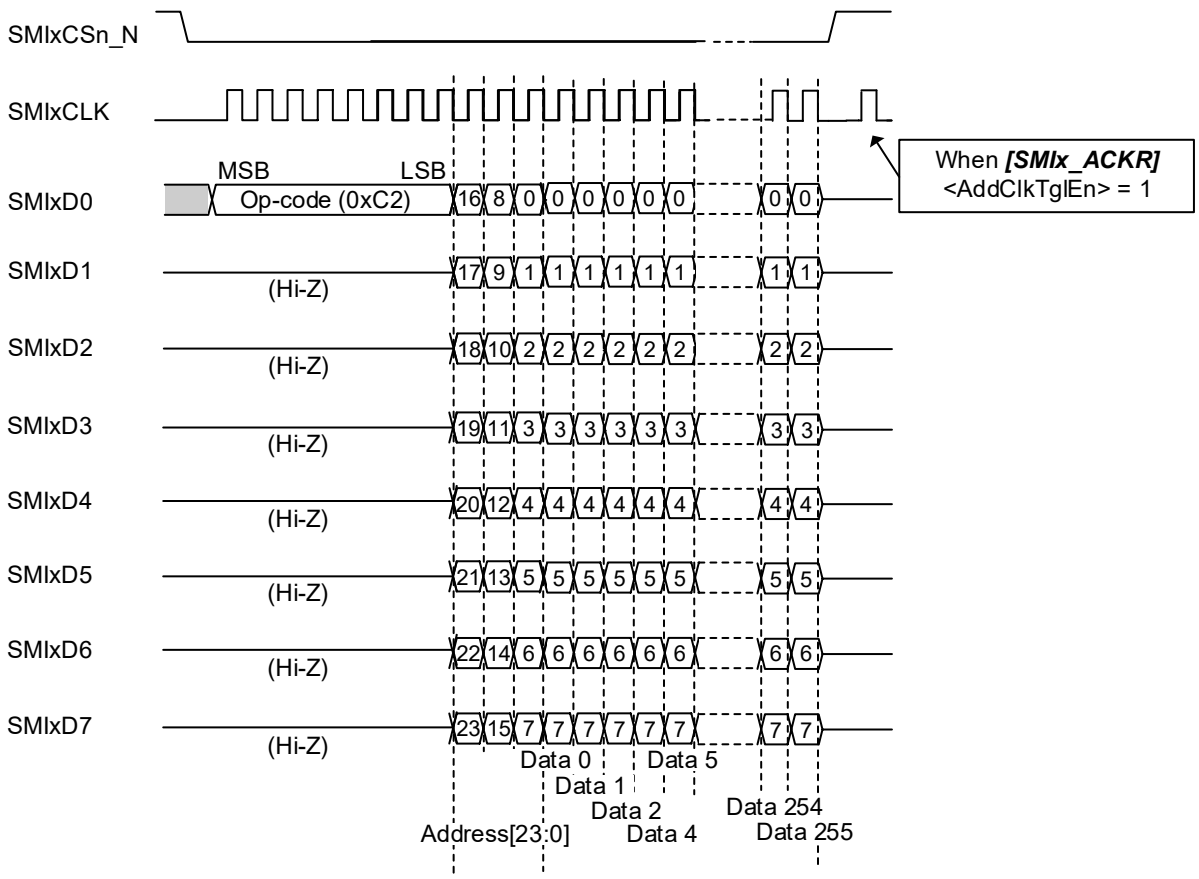

Figure 5.4 Octal I/O PAGE PROGRAM, Octal I/O WRITE

5.3.6. Programming Example: OPI PAGE PROGRAM, OPI WRITE

The procedure for transmitting 256-byte data (Data[2047:0]) to the 4-byte physical address (Addr[31:0]) of the SPI Flash by OPI is shown below.

Note: The SPI Flash enters the BUSY state after executing this command. A device in the BUSY state can normally communicate only with some commands such as status register read. If the instruction are stored in the SPI Flash, do not fetch the instruction from the SPI Flash until the BUSY state is released. If a memory read access to the SPI Flash is executed during BUSY state, a correct data cannot be read from the SPI Flash.

The command configuration is as follows: command op-code byte count: 2, address byte count: 4, dummy byte count: 0, payload data byte count: 256. The I/O width of the command is all 8 × I/O. The command op-code is "0x12ED".

(1) Set the following values in the primary buffer.

- <PBuf0[7:0]> = Op-code (0x12)
- <PBuf1[7:0]> = Op-code (0xED)
- <PBuf2[7:0]> = Address[31:24] (Addr[31:24])
- <PBuf3[7:0]> = Address[23:16] (Addr[23:16])
- <PBuf4[7:0]> = Address[15:8] (Addr[15:8])
- <PBuf5[7:0]> = Address[7:0] (Addr[7:0])

(2) Set the following values in the secondary buffer.

- <SBuf0[7:0]> = Data 0 (Data[7:0], data written to Addr[23:0] + 0x00)
- <SBuf1[7:0]> = Data 1 (Data[15:8], data written to Addr[23:0] + 0x01)
  :
- <SBuf254[7:0]> = Data 254 (Data[2039:2032], data written to Addr[23:0] + 0xFE)
- <SBuf255[7:0]> = Data 255 (Data[2047:2040], data written to Addr[23:0] + 0xFF)

(3) ***[SMIxRACR1]*** settings

- <PBufEn> = 1, <PBufBc[4:0]> = 00101
- <SBufEn> = 1, <SBufBc[7:0]> = 0xFF
- <CSNum> = Chip select number connected to SPI Flash

(4) ***[SMIxIOCR]*** settings

- <PBufIOCtrlEn[1:0]> = 11 (8 × I/O communication)
- <SBufIOCtrlEn[1:0]> = 11 (8 × I/O communication)
- <PBufIOCtrl[4:0]> = 00000 (multi I/O communication)

(5) ***[SMIxOECR]*** settings

- <PBufOCEn> = 0 (transmit)
- <PBufOEnC[4:0]> = Don't care

(6) Set ***[SMIxRACR1]***<CycGo> to "1" to start indirect access.

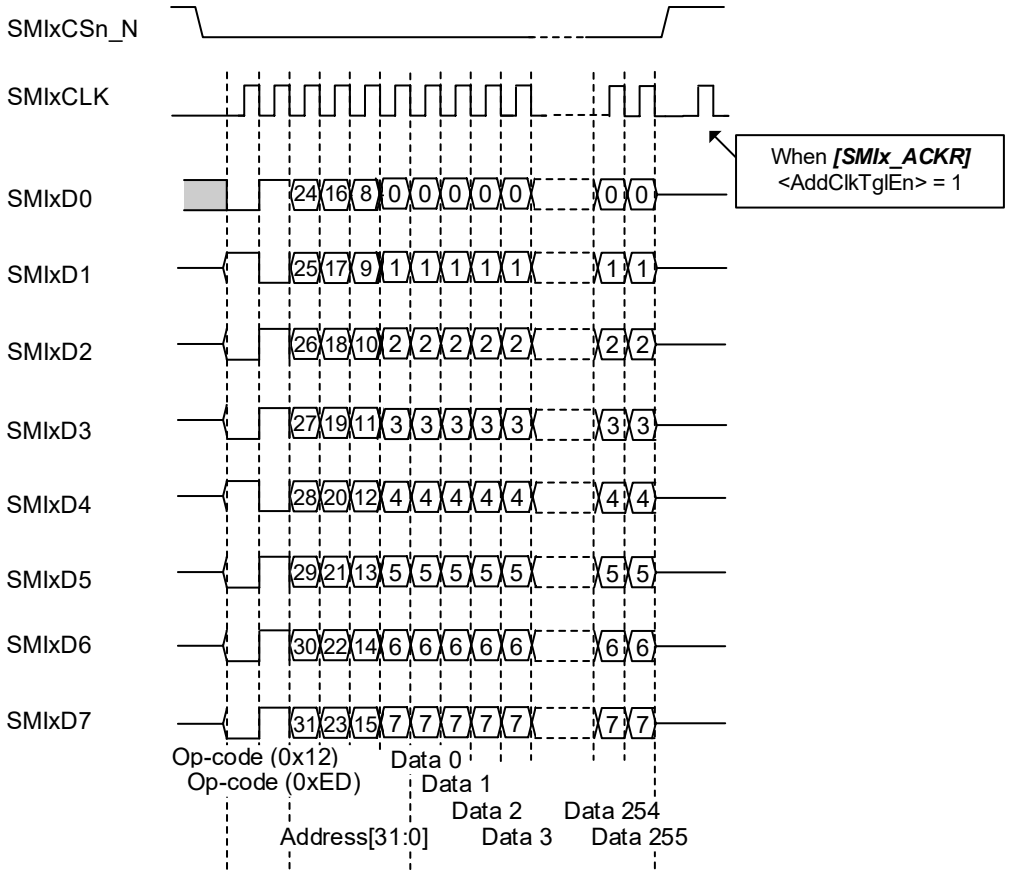

Figure 5.5 OPI PAGE PROGRAM, OPI WRITE

5.3.7. Programming Example: SECTOR ERASE

The procedure for issuing SECROR ERASE (op-code: 0x20) to the 3-byte physical address (Addr[23:0]) of the SPI Flash is shown below.

Note: The SPI Flash enters the BUSY state after executing this command. A device in the BUSY state can normally communicate only with some commands such as status register read. If the instruction are stored in the SPI Flash, do not fetch the instruction from the SPI Flash until the BUSY state is released. If a memory read access to the SPI Flash is executed during BUSY state, a correct data cannot be read from the SPI Flash.

(1) Set the following values in the primary buffer.

- <PBuf0[7:0]> = Op-code (0x20)
- <PBuf1[7:0]> = Address[23:16] (Addr[23:16])
- <PBuf2[7:0]> = Address[15:8] (Addr[15:8])
- <PBuf3[7:0]> = Address[7:0] (Addr[7:0])

(2) Set the following values in the secondary buffer.

No secondary buffer is used.

(3) ***[SMIxRACR1]*** settings

- <PBufEn> = 1, <PBufBc[4:0]> = 00011
- <SBufEn> = 0, <SBufBc[7:0]> = Don't care
- <CSNum> = Chip select number connected to SPI Flash

(4) ***[SMIxIOCR]*** settings

- <PBufIOCtrlEn[1:0]> = 00 (SPI communication)
- <SBufIOCtrlEn[1:0]> = 00 (SPI communication)
- <PBufIOCtrl[4:0]> = Don't care

(5) ***[SMIxOECR]*** settings

- <PBufOCEn> = 0 (transmit)
- <PBufOEnC[4:0]> = Don't care

(6) Set ***[SMIxRACR1]***<CycGo> to "1" to start indirect access.

5.3.8. Programming Example: CHIP ERASE

The procedure for issuing SECROR ERASE (op-code: 0xC7) to the SPI Flash is shown below.

Note: The SPI Flash enters the BUSY state after executing this command. A device in the BUSY state can normally communicate only with some commands such as status register read. If the instruction are stored in the SPI Flash, do not fetch the instruction from the SPI Flash until the BUSY state is released. If a memory read access to the SPI Flash is executed during BUSY state, a correct data cannot be read from the SPI Flash.

(1) Set the following values in the primary buffer.

- <PBuf0[7:0]> = Op-code (0xC7)

(2) Set the following values in the secondary buffer.

No secondary buffer is used.

(3) ***[SMIxRACR1]*** settings

- <PBufEn> = 1, <PBufBc[4:0]> = 00000
- <SBufEn> = 0, <SBufBc[7:0]> = Don't care
- <CSNum> = Chip select number connected to SPI Flash

(4) ***[SMIxIOCR]*** settings

- <PBufIOCtrlEn[1:0]> = 00 (SPI communication)
- <SBufIOCtrlEn[1:0]> = 00 (SPI communication)
- <PBufIOCtrl[4:0]> = Don't care

(5) ***[SMIxOECR]*** settings

- <PBufOCEn> = 0 (transmit)
- <PBufOEnC[4:0]> = Don't care

(6) Set ***[SMIxRACR1]***<CycGo> to "1" to start indirect access.

5.3.9. Programming Example: READ STATUS REGISTER

The procedure for issuing READ STATUS REGISTER (op-code: 0x05) to the serial memory and one byte data is read is shown below.

(1) Set the following values in the primary buffer.

- <PBuf0[7:0]> = Op-code (0x05)

(2) The status data returned from the serial memory is stored to the secondary buffer after an indirect access is completed.

- <SBuf0[7:0]> = Data[7:0] (status register bit[7:0] of the serial memory stored)

(3) ***[SMIxRACR1]*** settings

- <PBufEn> = 1, <PBufBc[4:0]> = 00000
- <SBufEn> = 1, <SBufBc[7:0]> = 0x00
- <CSNum> = Chip select number connected to serial memory

(4) ***[SMIxIOCR]*** settings

- <PBufIOCtrlEn[1:0]> = 00 (SPI communication)
- <SBufIOCtrlEn[1:0]> = 00 (SPI communication)
- <PBufIOCtrl[4:0]> = Don't care

(5) ***[SMIxOECR]*** settings

- <PBufOCEn> = 0 (receive)
- <PBufOEnC[4:0]> = Don't care

(6) Set ***[SMIxRACR1]***<CycGo> to "1" to start indirect access.

The value of status register returned from the serial memory is stored to the <SBuf0[7:0]> after an indirect access is completed.

5.3.10. Programming Example: FAST READ

The procedure for receiving 256-byte data (Data[2047:0]) from the 3-byte physical address (Addr[23:0]) of the serial memory is shown below.

The command configuration is as follows: command op-code byte count: 1, address byte count: 3, dummy byte count: 1, payload data byte count: 256. The I/O width of the command is all SPI. The command op-code is "0x0B".

(1) Set the following values in the primary buffer.

- <PBuf0[7:0]> = Op-code (0x0B)
- <PBuf1[7:0]> = Address[23:16] (Addr[23:16])
- <PBuf2[7:0]> = Address[15:8] (Addr[15:8])
- <PBuf3[7:0]> = Address[7:0] (Addr[7:0])

(2) The data returned from the serial memory is stored to the secondary buffer after an indirect access is completed.

- <SBuf0[7:0]> = Data 0 (Data[7:0], data read from Addr[23:0] + 0x00)
- <SBuf1[7:0]> = Data 1 (Data[15:8], data read from Addr[23:0] + 0x01)
  :
- <SBuf254[7:0]> = Data 254 (Data[2039:2032], data read from Addr[23:0] + 0xFE)
- <SBuf255[7:0]> = Data 255 (Data[2047:2040], data read from Addr[23:0] + 0xFF)

(3) ***[SMIxRACR1]*** settings

- <PBufEn> = 1, <PBufBc[4:0]> = 00100
- <SBufEn> = 1, <SBufBc[7:0]> = 0xFF
- <CSNum> = Chip select number connected to serial memory

(4) ***[SMIxIOCR]*** settings

- <PBufIOCtrlEn[1:0]> = 00 (SPI communication)
- <SBufIOCtrlEn[1:0]> = 00 (SPI communication)
- <PBufIOCtrl[4:0]> = Don't care

(5) ***[SMIxOECR]*** settings

- <PBufOCEn> = 0 (receive)
- <PBufOEnC[4:0]> = Don't care

(6) Set ***[SMIxRACR1]***<CycGo> to "1" to start indirect access.

The data returned from the serial memory is stored to the <SBuf0[7:0]> to <SBuf255[7:0]> after an indirect access is completed.

Note: Setting dummy byte count depend on setting to the configuration register such as a part number of serial memory.

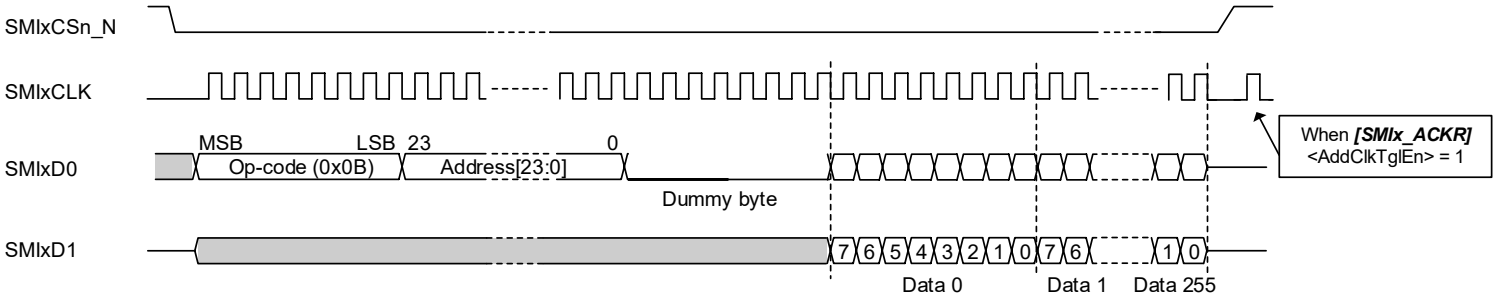

Figure 5.6 FAST READ

5.3.11. Programming Example: Quad I/O FAST READ

The procedure for receiving 256-byte data (Data[2047:0]) from the 3-byte physical address (Addr[23:0]) of the serial memory by 4 × I/O is shown below.

The command configuration is as follows: command op-code byte count: 1, address byte count: 3, dummy byte count: 3, payload data byte count: 256. The I/O width of the command is SPI for command op-code, 4 × I/O following address. The command op-code is "0xEB".

(7) Set the following values in the primary buffer.

- <PBuf0[7:0]> = Op-code (0xEB)
- <PBuf1[7:0]> = Address[23:16] (Addr[23:16])
- <PBuf2[7:0]> = Address[15:8] (Addr[15:8])
- <PBuf3[7:0]> = Address[7:0] (Addr[7:0])

(8) The data returned from the serial memory is stored to the secondary buffer after an indirect access is completed.

- <SBuf0[7:0]> = Data 0 (Data[7:0], data read from Addr[23:0] + 0x00)
- <SBuf1[7:0]> = Data 1 (Data[15:8], data read from Addr[23:0] + 0x01)
  :
- <SBuf254[7:0]> = Data 254 (Data[2039:2032], data read from Addr[23:0] + 0xFE)
- <SBuf255[7:0]> = Data 255 (Data[2047:2040], data read from Addr[23:0] + 0xFF)

(9) ***[SMIxRACR1]*** settings

- <PBufEn> = 1, <PBufBc[4:0]> = 00110
- <SBufEn> = 1, <SBufBc[7:0]> = 0xFF
- <CSNum> = Chip select number connected to serial memory

(10) ***[SMIxIOCR]*** settings

- <PBufIOCtrlEn[1:0]> = 10 (4 × I/O communication)
- <SBufIOCtrlEn[1:0]> = 10 (4 × I/O communication)
- <PBufIOCtrl[4:0]> = 00001 (single communication for command op-code, multi I/O communication following address)

(11) ***[SMIxOECR]*** settings

- <PBufOCEn> = 1
- <PBufOEnC[4:0]> = 00100 (direction of SMIxDn changes to IN from dummy byte cycle.)

(12) Set ***[SMIxRACR1]***<CycGo> to "1" to start indirect access.

The data returned from the serial memory is stored to the <SBuf0[7:0]> to <SBuf255[7:0]> after an indirect access is completed.

Note: Setting dummy byte count depend on setting to the configuration register such as a part number of serial memory.

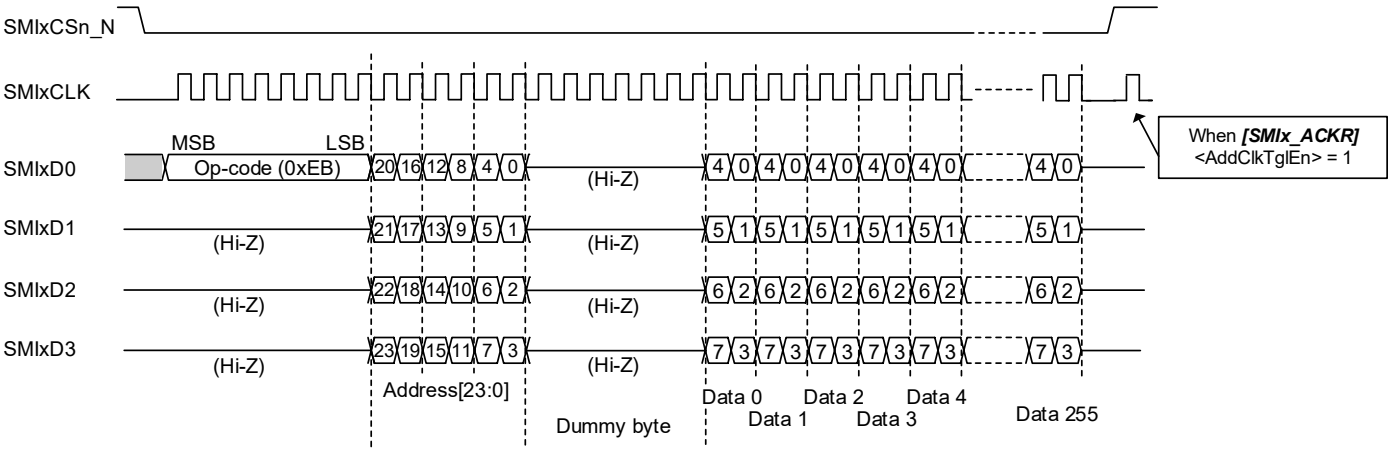

Figure 5.7 Quad I/O FAST READ

5.3.12. Programming Example: QPI FAST READ

The procedure for receiving 256-byte data (Data[2047:0]) from the 3-byte physical address (Addr[23:0]) of the serial memory by 4 × I/O is shown below.

The command configuration is as follows: command op-code byte count: 1, address byte count: 3, dummy byte count: 3, payload data byte count: 256. The I/O width of the command is all 4 × I/O. The command op-code is "0xEB".

(1) Set the following values in the primary buffer.

- <PBuf0[7:0]> = Op-code (0xEB)
- <PBuf1[7:0]> = Address[23:16] (Addr[23:16])
- <PBuf2[7:0]> = Address[15:8] (Addr[15:8])
- <PBuf3[7:0]> = Address[7:0] (Addr[7:0])

(2) The data returned from the serial memory is stored to the secondary buffer after an indirect access is completed.

- <SBuf0[7:0]> = Data 0 (Data[7:0], data read from Addr[23:0] + 0x00)
- <SBuf1[7:0]> = Data 1 (Data[15:8], data read from Addr[23:0] + 0x01)
  :
- <SBuf254[7:0]> = Data 254 (Data[2039:2032], data read from Addr[23:0] + 0xFE)
- <SBuf255[7:0]> = Data 255 (Data[2047:2040], data read from Addr[23:0] + 0xFF)

(3) ***[SMIxRACR1]*** settings

- <PBufEn> = 1, <PBufBc[4:0]> = 00110
- <SBufEn> = 1, <SBufBc[7:0]> = 0xFF
- <CSNum> = Chip select number connected to serial memory

(4) ***[SMIxIOCR]*** settings

- <PBufIOCtrlEn[1:0]> = 10 (4 × I/O communication)
- <SBufIOCtrlEn[1:0]> = 10 (4 × I/O communication)
- <PBufIOCtrl[4:0]> = 00000 (multi I/O communication)

(5) ***[SMIxOECR]*** settings

- <PBufOCEn> = 1
- <PBufOEnC[4:0]> = 00100 (direction of SMIxDn changes to IN from dummy byte cycle.)

(6) Set ***[SMIxRACR1]***<CycGo> to "1" to start indirect access.

The data returned from the serial memory is stored to the <SBuf0[7:0]> to <SBuf255[7:0]> after an indirect access is completed.

Note: Setting dummy byte count depend on setting to the configuration register such as a part number of serial memory.

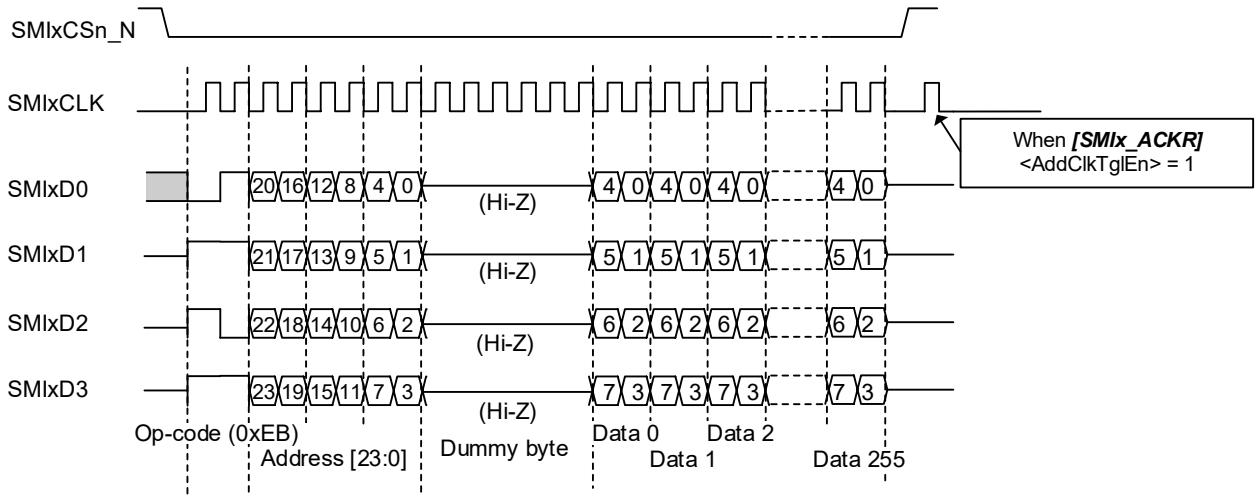

Figure 5.8 QPI FAST READ

5.3.13. Programming Example: Qctal I/O FAST READ

The procedure for receiving 256-byte data (Data[2047:0]) from the 3-byte physical address (Addr[23:0]) of the serial memory by 8 × I/O is shown below.

The command configuration is as follows: command op-code byte count: 1, address byte count: 3, dummy byte count: 16, payload data byte count: 256. The I/O width of the command is SPI for command op-code, 8 × I/O following address. The command op-code is "0xCB".

(1) Set the following values in the primary buffer.

- <PBuf0[7:0]> = Op-code (0xCB)
- <PBuf1[7:0]> = Address[23:16] (Addr[23:16])
- <PBuf2[7:0]> = Address[15:8] (Addr[15:8])
- <PBuf3[7:0]> = Address[7:0] (Addr[7:0])

(2) The data returned from the serial memory is stored to the secondary buffer after an indirect access is completed.

- <SBuf0[7:0]> = Data 0 (Data[7:0], data read from Addr[23:0] + 0x00)
- <SBuf1[7:0]> = Data 1 (Data[15:8], data read from Addr[23:0] + 0x01)
  :
- <SBuf254[7:0]> = Data 254 (Data[2039:2032], data read from Addr[23:0] + 0xFE)
- <SBuf255[7:0]> = Data 255 (Data[2047:2040], data read from Addr[23:0] + 0xFF)

(3) ***[SMIxRACR1]*** settings

- <PBufEn> = 1, <PBufBc[4:0]> = 10011
- <SBufEn> = 1, <SBufBc[7:0]> = 0xFF
- <CSNum> = Chip select number connected to serial memory

(4) ***[SMIxIOCR]*** settings

- <PBufIOCtrlEn[1:0]> = 11 (8 × I/O communication)
- <SBufIOCtrlEn[1:0]> = 11 (8 × I/O communication)
- <PBufIOCtrl[4:0]> = 00001 (single communication for command op-code, multi I/O communication following address)

(5) ***[SMIxOECR]*** settings

- <PBufOCEn> = 1
- <PBufOEnC[4:0]> = 00100 (direction of SMIxDn changes to IN from dummy byte cycle.)

(6) Set ***[SMIxRACR1]***<CycGo> to "1" to start indirect access.

The data returned from the serial memory is stored to the <SBuf0[7:0]> to <SBuf255[7:0]> after an indirect access is completed.

Note: Setting dummy byte count depend on setting to the configuration register such as a part number of serial memory.

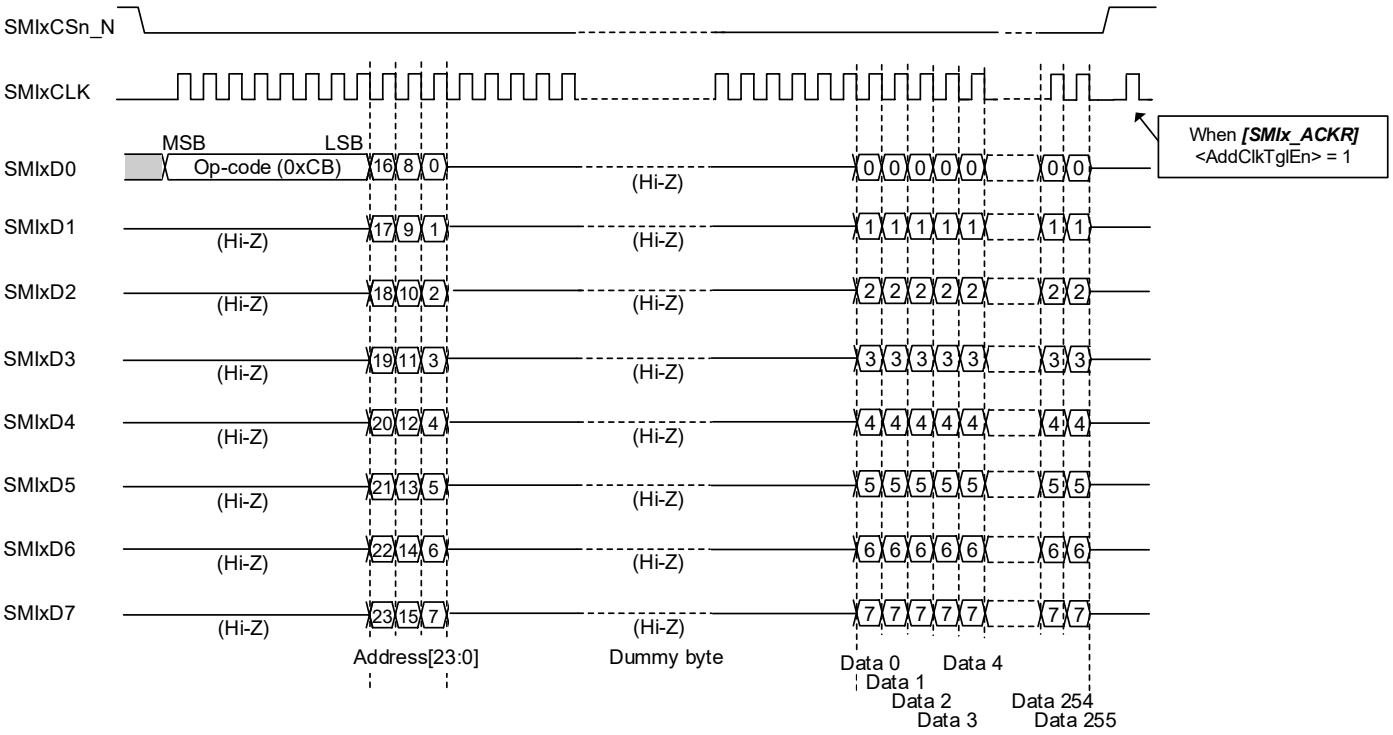

Figure 5.9 Octal FAST READ

5.3.14. Programming Example: OPI FAST READ

The procedure for receiving 256-byte data (Data[2047:0]) from the 4-byte physical address (Addr[31:0]) of the serial memory by 8 × I/O is shown below.

The command configuration is as follows: command op-code byte count: 2, address byte count: 4, dummy byte count: 20, payload data byte count: 256. The I/O width of the command is all 8 × I/O. The command op-code is "0xEC13".

(1) Set the following values in the primary buffer.

- <PBuf0[7:0]> = Op-code (0xEC)
- <PBuf1[7:0]> = Op-code (0x13)
- <PBuf2[7:0]> = Address[31:24] (Addr[31:24])
- <PBuf3[7:0]> = Address[23:16] (Addr[23:16])
- <PBuf4[7:0]> = Address[15:8] (Addr[15:8])
- <PBuf5[7:0]> = Address[7:0] (Addr[7:0])

(2) The data returned from the serial memory is stored to the secondary buffer after an indirect access is completed.

- <SBuf0[7:0]> = Data 0 (Data[7:0], data read from Addr[23:0] + 0x00)
- <SBuf1[7:0]> = Data 1 (Data[15:8], data read from Addr[23:0] + 0x01)
  :
- <SBuf254[7:0]> = Data 254 (Data[2039:2032], data read from Addr[23:0] + 0xFE)
- <SBuf255[7:0]> = Data 255 (Data[2047:2040], data read from Addr[23:0] + 0xFF)

(3) ***[SMIxRACR1]*** settings

- <PBufEn> = 1, <PBufBc[4:0]> = 11001
- <SBufEn> = 1, <SBufBc[7:0]> = 0xFF
- <CSNum> = Chip select number connected to serial memory

(4) ***[SMIxIOCR]*** settings

- <PBufIOCtrlEn[1:0]> = 11 (8 × I/O communication)
- <SBufIOCtrlEn[1:0]> = 11 (8 × I/O communication)
- <PBufIOCtrl[4:0]> = 00000 (multi I/O communication)

(5) ***[SMIxOECR]*** settings

- <PBufOCEn> = 1
- <PBufOEnC[4:0]> = 00110 (direction of SMIxDn changes to IN from dummy byte cycle.)

(6) Set ***[SMIxRACR1]***<CycGo> to "1" to start indirect access.

The data returned from the serial memory is stored to the <SBuf0[7:0]> to <SBuf255[7:0]> after an indirect access is completed.

Note: Setting dummy byte count depend on setting to the configuration register such as a part number of serial memory.

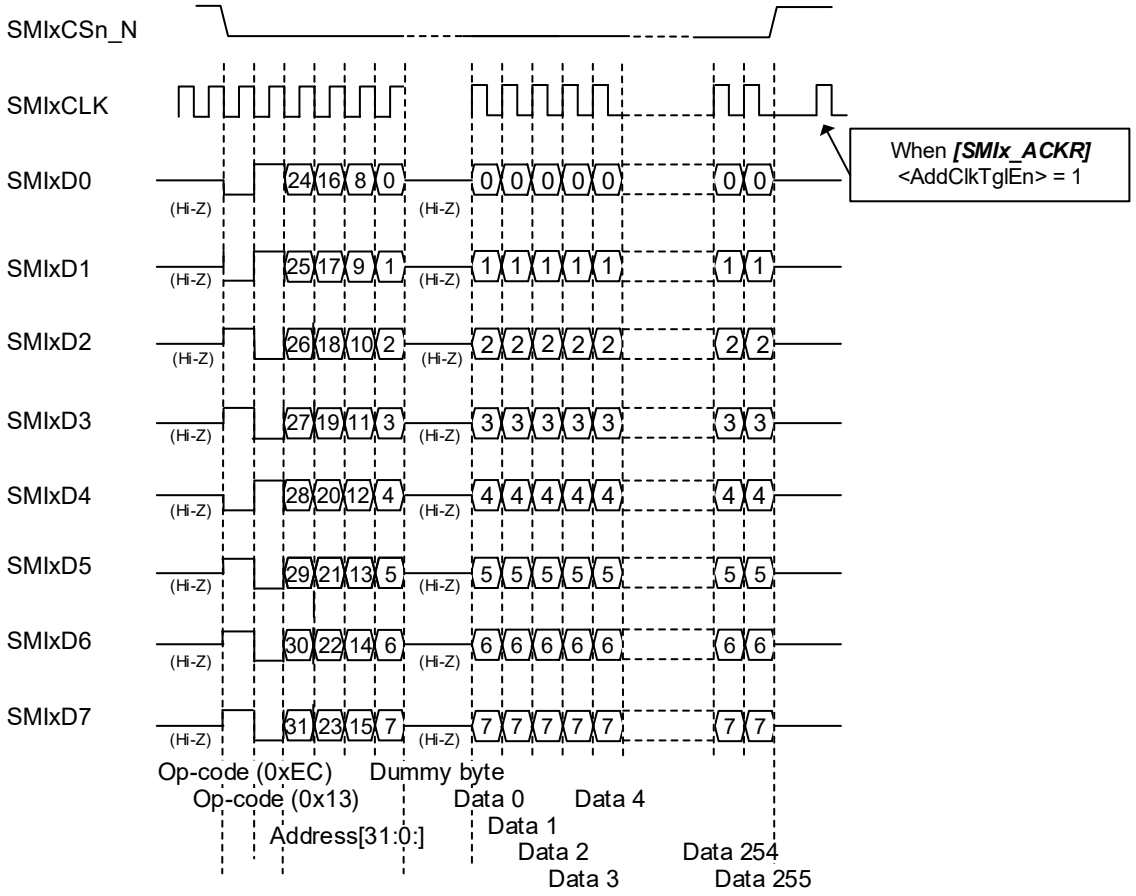

Figure 5.10 OPI FAST READ

5.4. Others

5.4.1. Forced Stop

A forced stop is a process for urgently stopping the operation of SMIF. When the communication with the serial memory is in progress, the communication is aborted, and the chip select signal is set to "High". At this time, communication data is not guaranteed.

Even after a forced stop, the internal registers of SMIF can be accessed. However, SMIF can't communicate to serial memory. To re-communicate, it is necessary to perform software reset and configure communication settings again.

The procedure for performing a forced stop is shown below.

(1) If using interrupt, write "1" to ***[SMIxINT]***<SDIntEn>.
(2) Write "1" to ***[SMIxSTPR]***<StopEn>.
(3) Wait for an interrupt or until ***[SMIxSTAT]***<StpProgDone> is set to "1".
(4) Write "0" to ***[SMIxSTAT]***<StpProgDone>
(5) Perform a software reset according to the procedure in 5.4.2.

5.4.2. Software Reset

The procedure for performing a software reset is shown below.

(1) Check that both ***[SMIxSTAT]***<DirAccInPrgrs> and <CycPrgrs> are "0".
(2) Write "1" to ***[SMIxSWR]***<RstEn>.
(3) Wait until "0" is read from ***[SMIxSWR]***<RstEn>.

Note1: When a forced stop is done, step 1 can be omitted.
Note2: During this procedure, a new direct access or indirect access request must not be issued to SMIF.

5.5. Connection Example with Serial Memory

The following shows an example of a connection with serial memories.
Each pin is assumed to be processed externally as shown below. Decide the processing of each pin according to the actual connected serial memory and external circuit.

- SMIxCS0_N, SMIxCS1_N: Pull-up
- SMIxCLK: Pull-down
- SMIxD0 to 7: Pull-up (Note)

Note: When SMIxDn not used for connection to serial memory, they can be used as input/output ports.

5.5.1. Connection Example with Standard SPI

(1) Serial memory 0

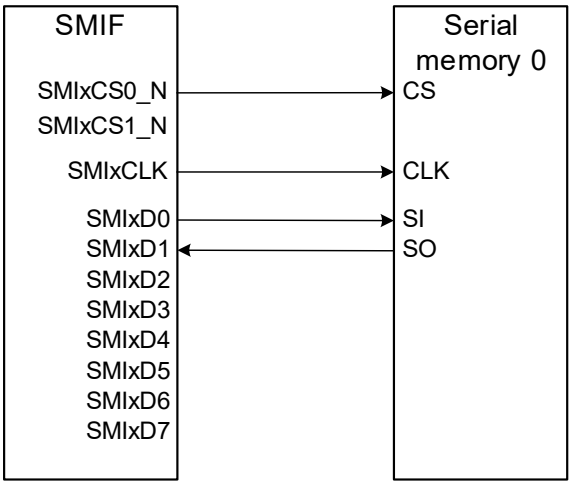

Figure 5.11 Connection Example with Standard SPI (Serial Memory 0)

(2) Serial memory 0 and 1

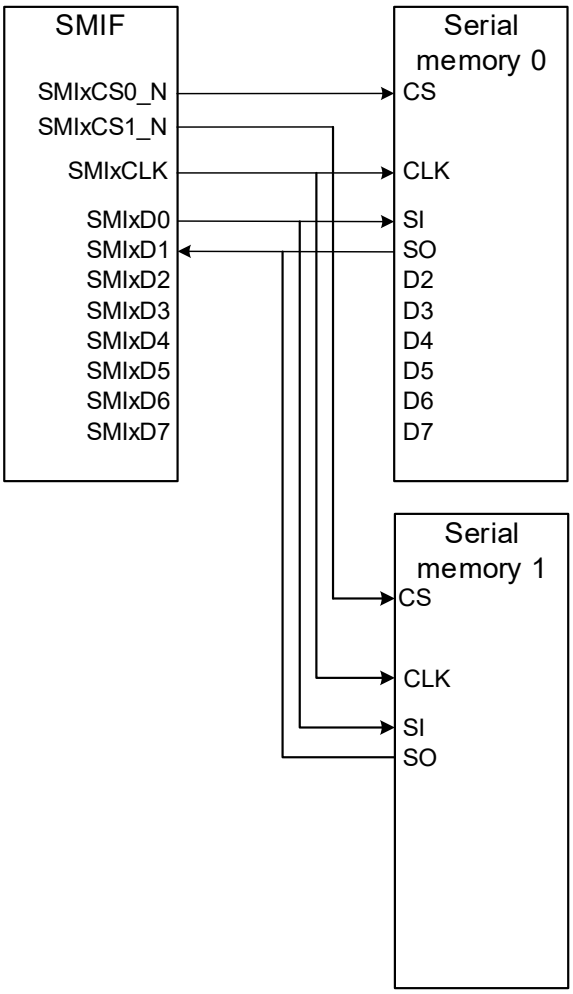

Figure 5.12 Connection Example with Standard SPI (Serial Memory 0 and 1)

5.5.2. Connection Example with Dual and DPI

(1) Serial memory 0

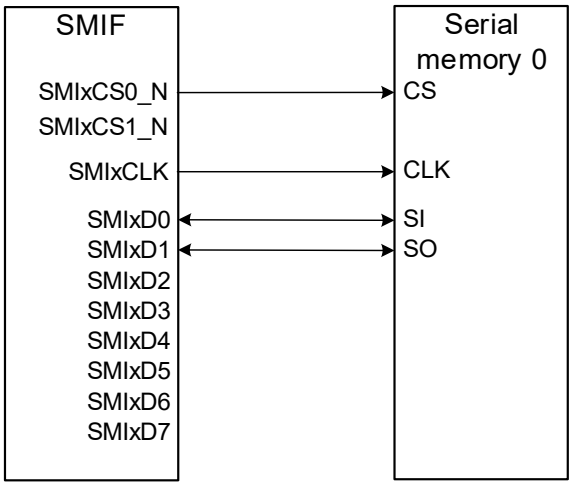

Figure 5.13 Connection Example with Dual and QPI (Serial Memory 0)

(2) Serial memory 0 and 1

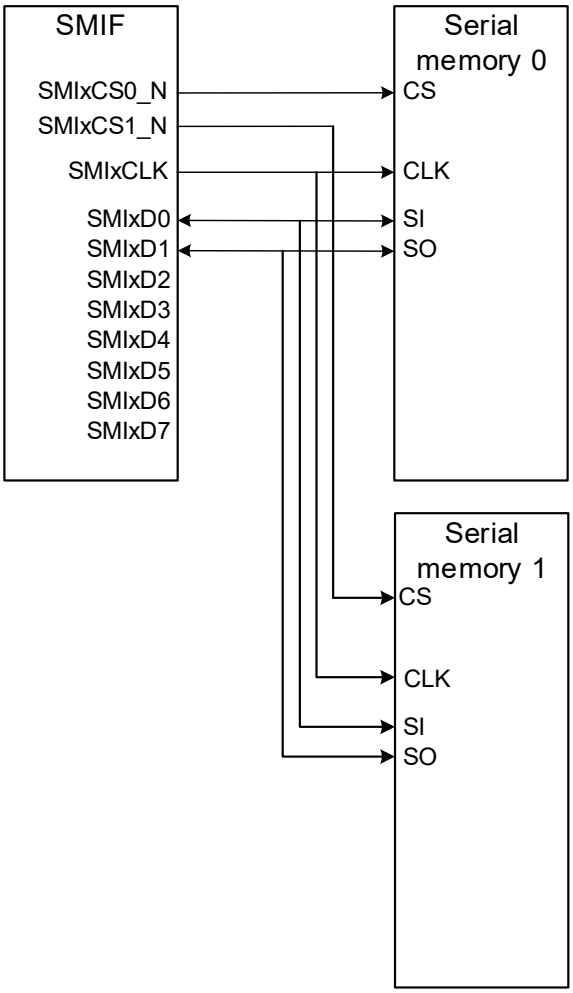

Figure 5.14 Connection Example with Dual and DPI (Serial Memory 0 and 1)

5.5.3. Connection Example with Quad/QPI

(1) Serial memory 0

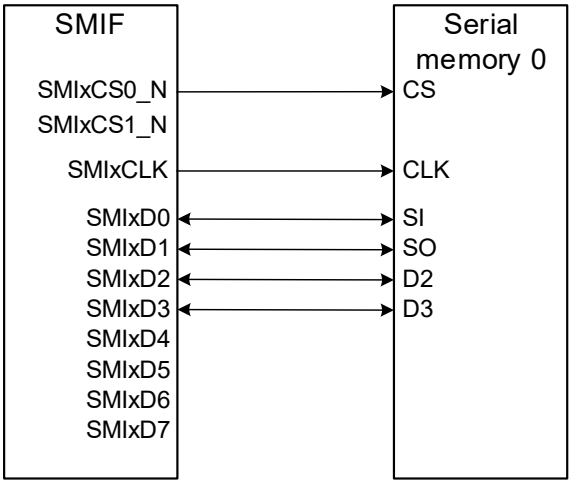

Figure 5.15 Connection Example with Quad and QPI (Serial Memory 0)

(2) Serial memory 0 and 1

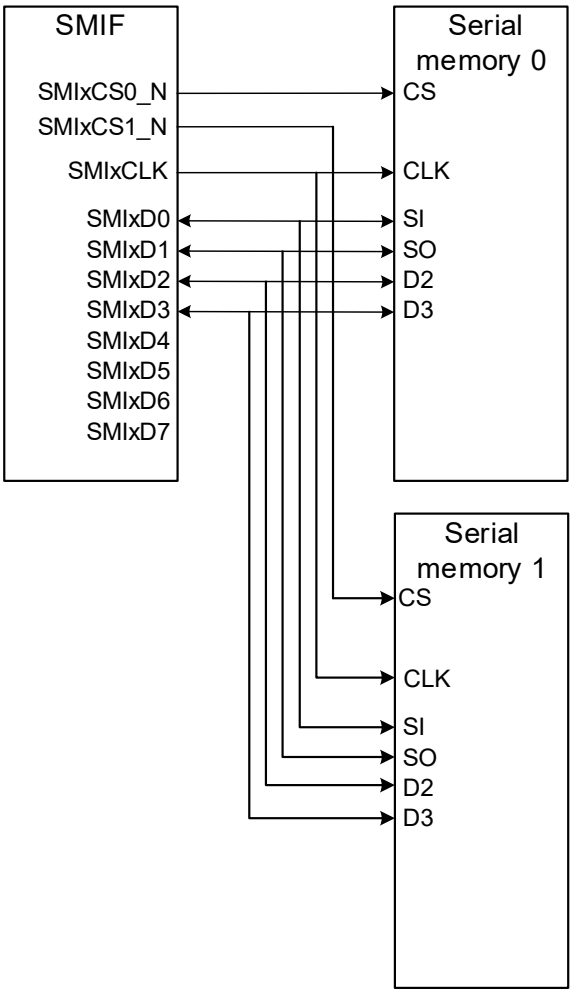

Figure 5.16 Connection Example with Quad/QPI (Serial Memory 0 and 1)

5.5.4. Connection Example with Octal/OPI

(1) Serial memory 0

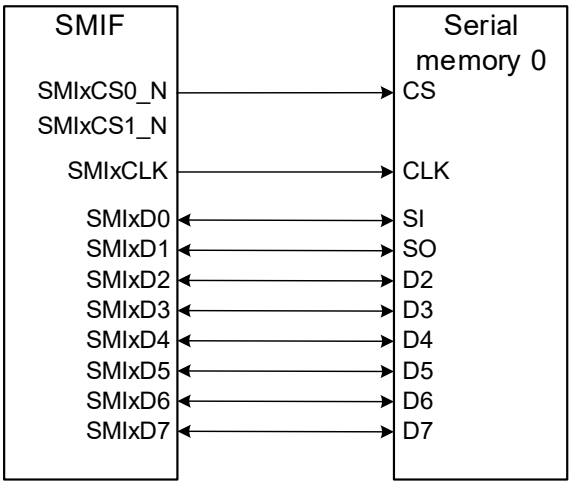

Figure 5.17 Connection Example with Octal/OPI (Serial Memory 0)

(2) Serial memory 0 and 1

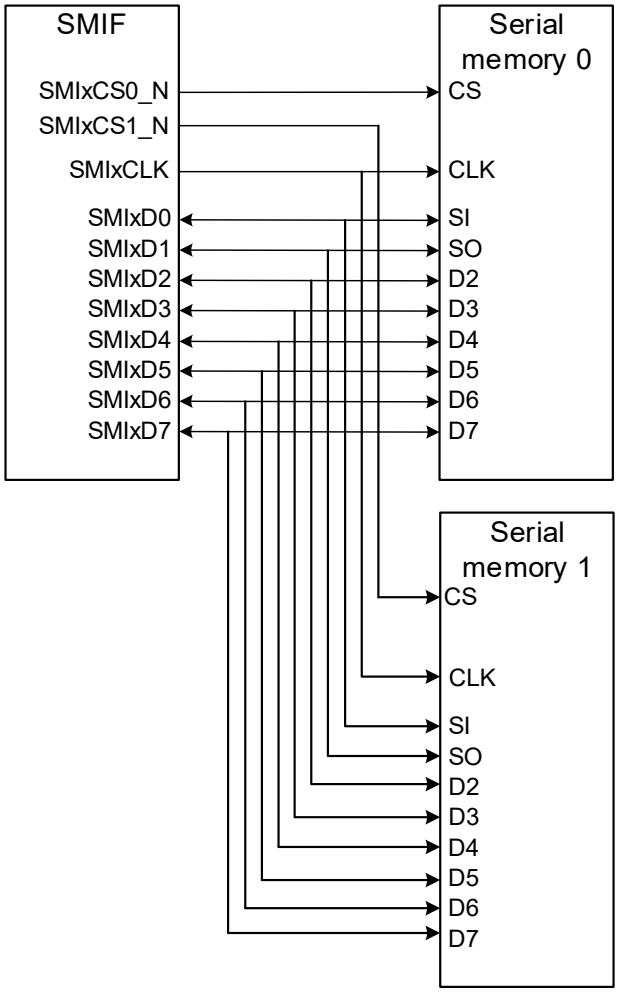

Figure 5.18 Connection Example with Octal/OPI (Serial Memory 0 and 1)

6. Precaution for Usage

Do not access addresses to which no registers have been assigned.

7. Revision History

Table 7.1 Revision History

Revision	Date	Function
1.0	2026-01-30	- First release

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as "TOSHIBA".
Hardware, software and systems described in this document are collectively referred to as "Product".

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the datasheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**