32-bit RISC Microcontroller

TXZ+ Family
TMPM4L Group(1)

Reference Manual
Input/Output Ports
(PORT-M4L(1))

Revision 1.0

2026-01

Toshiba Electronic Devices & Storage Corporation

Contents

List of Figures

List of Tables

Preface

Related Document

Document name
Product Information
Clock Control and Operation Mode
Exception
Flash Memory
I^2C Interface Version A
Serial Peripheral Interface
Serial Memory Interface
12-bit Analog to Digital Convertor
32-bit Timer Event Counter
Asynchronous Serial Communication Circuit
Advanced Programmable Motor Control Circuit 2
Advanced Encoder Input Circuit 2
Debug Interface

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

EI2C	I^2C Interface Version A
JTAG	Joint Test Action Group
SW	Serial Wire

1. Outlines

It is described about the register and setting of port. A list of the functions is indicated below.

Function classification	Function	Description
Ports	-	Programmable pull-up and Programmable pull-down can be selected. Open-drain output can be selected. Drive capability can be selected for some ports
Peripheral function pins	Clock output	System clock output is possible.
	External interrupt	Interrupt input pins
	32-bit timer event counter	Input capture input pins, timer output pins
	Serial peripheral interface	Chip select input pin, chip select output pins, data input pin, data output pin, clock input/output pin
	Asynchronous serial communication circuit	Data input pin, data output pin, handshake function pins
	I^2C interface version A	Data input/output pin, clock input/output pin
	Serial memory interface	Chip select output pins, data input/output pins, clock output pin
	Analog digital convertor	Analog input pins
	Advanced programmable motor control circuit 2	X/Y/Z-phase output pins, U/V/W-phase output pins, EMG detection input pin, overvoltage detection input pin.
	Advanced encoder input circuit 2	Encoder input pins
	Trigger selector	External trigger input pins
Debug pins	JTAG	Test mode select input pin, serial clock input pin, serial data output pin, serial data input pin, test reset input pin
	SW	Serial wire data input/output pin, serial wire clock input pin, serial wire viewer output pin
	Trace	Trace clock output pin, trace data output pins
Control pins	High-speed oscillation circuit	High-speed oscillator connection pin/external clock input pin
	BOOT mode control	BOOT mode control pin

2. Description of Operation

2.1. Clock Supply

When port is used, set an applicable clock enable bit to "1" (clock supply) in fsys supply stop registers A or B (***[CGFSYSENA]***, ***[CGFSYSENB]***), fc supply stop register (***[CGFCEN]***). The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to Reference Manual “Clock Control and Operation Mode”.

3. Signal Connection List

Port assignments and terminal numbers for each product as seen from the functional terminals.

The "-" part in the table indicates "no terminal" or "no function assigned".

Table 3.1 Signal Connection List (1/6)

Function	Function pin name	Port name	M4L4 (LQFP64)	M4L2 (LQFP48/VQFN48)	M4L1 (LQFP44)
UART ch 0	UT0RXD	PD2	22	15	14
		PD3	21	14	13
	UT0TXDA	PD2	22	15	14
		PD3	21	14	13
UART ch 1	UT1RXD	PA3	29	22	21
		PA4	30	23	22
		PA5	31	24	23
		PA6	32	25	-
	UT1TXDA	PA3	29	22	21
		PA4	30	23	22
		PA5	31	24	23
		PA6	32	25	-
UART ch 2	UT2RXD	PC2	15	12	11
		PC3	16	13	12
		PA1	27	20	19
		PA2	28	21	20
	UT2TXDA	PC2	15	12	11
		PC3	16	13	12
		PA1	27	20	19
		PA2	28	21	20
	UT2CTS_N	PA0	26	19	18
	UT2RTS_N	PA0	26	19	18
UART ch 3	UT3RXD	PC0	13	10	9
		PC1	14	11	10
		PD5	19	-	-
		PD4	20	-	-
	UT3TXDA	PC0	13	10	9
		PC1	14	11	10
		PD5	19	-	-
		PD4	20	-	-
	UT3CTS_N	PC4	17	-	-
		PC5	18	-	-
	UT3RTS_N	PC4	17	-	-
		PC5	18	-	-
UART ch 4	UT4RXD	PA7	33	-	-
		PJ2	34	-	-
	UT4TXDA	PA7	33	-	-
		PJ2	34	-	-
	UT4CTS_N	PJ1	35	-	-
	UT4RTS_N	PJ1	35	-	-

Table 3.2 Signal Connection List (2/6)

Function	Function pin name	Port name	M4L4 (LQFP64)	M4L2 (LQFP48/VQFN48)	M4L1 (LQFP44)
UART ch 5	UT5RXD	PG1	64	48	-
	UT5TXDA	PG0	62	46	-
	UT5CTS_N	PG2	1	-	-
	UT5RTS_N	PG2	1	-	-
EI2C ch 0	EI2C0SCL	PA3	29	22	21
	EI2C0SDA	PA4	30	23	22
EI2C ch 1	EI2C1SCL	PA5	31	24	-
	EI2C1SDA	PA6	32	25	-
TSPI ch 0	TSPI0RXD	PG1	64	-	-
	TSPI0TXD	PG0	62	-	-
	TSPI0SCK	PG2	1	-	-
	TSPI0CSIN	PG3	2	-	-
	TSPI0CS0	PG3	2	-	-
TSPI ch 1	TSPI1RXD	PC3	16	13	12
	TSPI1TXD	PC2	15	12	11
	TSPI1SCK	PC1	14	11	10
	TSPI1CSIN	PC0	13	10	9
	TSPI1CS0	PC0	13	10	9
	TSPI1CS1	PD3	21	14	13
		PB7	10	7	-
TSPI ch 2	TSPI2RXD	PA2	28	21	20
	TSPI2TXD	PA1	27	20	19
	TSPI2SCK	PA0	26	19	18
	TSPI2CSIN	PD0	25	18	17
	TSPI2CS0	PD0	25	18	17
	TSPI2CS1	PD1	24	17	16
		PJ0	36	-	-
SMIF ch 0	SMI0CS0_N	PC0	13	10	9
	SMI0CS1_N	PB7	10	7	-
	SMI0CLK	PC1	14	11	10
	SMI0D0	PC2	15	12	11
	SMI0D1	PC3	16	13	12
	SMI0D2	PC4	17	-	-
		PD3	21	14	13
	SMI0D3	PC5	18	-	-
		PD2	22	15	14

Table 3.3 Signal Connection List (3/6)

Function	Function pin name	Port name	M4L4 (LQFP64)	M4L2 (LQFP48/VQFN48)	M4L1 (LQFP44)
T32A ch 0	T32A00INA0	PG3	2	-	-
		PC0	13	10	9
	T32A00INA1	PC1	14	11	10
		PJ1	35	-	-
	T32A00OUTA	PC1	14	11	10
		PJ1	35	-	-
	T32A00INB0	PC1	14	11	10
		PJ1	35	-	-
	T32A00INB1	PG3	2	-	-
		PC0	13	10	9
	T32A00OUTB	PG3	2	-	-
		PB7	10	7	-
	T32A00INC0	PG3	2	-	-
	T32A00OUTC	PJ1	35	-	-
T32A ch 1	T32A01INA0	PC2	15	12	11
		PD5	19	-	-
	T32A01INA1	PC3	16	13	12
		PD4	20	-	-
	T32A01OUTA	PC3	16	13	12
		PD4	20	-	-
	T32A01INB0	PC3	16	13	12
		PD4	20	-	-
	T32A01INB1	PC2	15	12	11
		PD5	19	-	-
	T32A01OUTB	PC2	15	12	11
		PD5	19	-	-
	T32A01INC0	PC2	15	12	11
		PD5	19	-	-
	T32A01OUTC	PC3	16	13	12
		PD4	20	-	-
T32A ch 2	T32A02INA0	PA3	29	22	21
		PA7	33	-	-
	T32A02INA1	PJ2	34	-	-
	T32A02OUTA	PA4	30	23	22
		PJ2	34	-	-
	T32A02INB0	PA4	30	23	22
		PJ2	34	-	-
	T32A02INB1	PA7	33	-	-
	T32A02OUTB	PA3	29	22	21
		PA7	33	-	-
	T32A02INC0	PA7	33	-	-
	T32A02OUTC	PJ2	34	-	-

Table 3.4 Signal Connection List (4/6)

Function	Function pin name	Port name	M4L4 (LQFP64)	M4L2 (LQFP48/VQFN48)	M4L1 (LQFP44)
T32A ch 3	T32A03INA0	PD3	21	14	13
	T32A03INA1	PD2	22	15	14
		PG1	64	48	-
	T32A03OUTA	PD2	22	15	14
		PG1	64	48	-
	T32A03INB0	PD2	22	15	14
		PG1	64	48	-
	T32A03INB1	PD3	21	14	13
	T32A03OUTB	PD3	21	14	13
	T32A03INC0	PD3	21	14	13
	T32A03OUTC	PD2	22	15	14
		PG1	64	48	-
T32A ch 4	T32A04INA0	PA1	27	20	19
		PJ0	36	-	-
	T32A04INA1	PA2	28	21	20
	T32A04OUTA	PA2	28	21	20
	T32A04INB0	PA2	28	21	20
	T32A04INB1	PA1	27	20	19
		PJ0	36	-	-
	T32A04OUTB	PA1	27	20	19
		PJ0	36	-	-
	T32A04INC0	PA1	27	20	19
		PJ0	36	-	-
	T32A04OUTC	PA2	28	21	20
12-bit ADC unit A unit B	AINA13/ AINB13	PF5	44	33	-
	AINA12/ AINB12	PF4	45	34	31
	AINA11/ AINB11	PF3	46	35	32
	AINA10/ AINB10	PF2	47	36	33
	AINA09/ AINB09	PF1	48	37	34
	AINA08/ AINB08	PF0	49	-	-
	AINA07/ AINB07	PE7	50	-	-
	AINA06/ AINB06	PE6	51	-	-
	AINA05/ AINB05	PE5	52	-	-
	AINA04/ AINB04	PE4	53	-	-
	AINA03/ AINB03	PE3	54	38	35
	AINA02/ AINB02	PE2	55	39	36
	AINA01/ AINB01	PE1	56	40	37
	AINA00/ AINB00	PE0	57	41	38

Table 3.5 Signal Connection List (5/6)

Function	Function pin name	Port name	M4L4 (LQFP64)	M4L2 (LQFP48/VQFN48)	M4L1 (LQFP44)
INT	INT00	PD3	21	14	13
	INT01	PD2	22	15	14
	INT02	PD0	25	18	17
	INT03	PA0	26	19	18
	INT04	PA4	30	23	22
	INT05	PH0	37	26	24
	INT06	PH1	38	27	25
	INT07	PF4	45	34	31
	INT08	PF3	46	35	32
	INT09	PB7	10	7	-
	INT10	PA6	32	25	-
	INT11	PF5	44	33	-
	INT12	PG1	64	48	-
	INT13	PG3	2	-	-
	INT14	PC4	17	-	-
	INT15	PC5	18	-	-
	INT16	PA7	33	-	-
	INT17	PJ2	34	-	-
	INT18	PJ1	35	-	-
	INT19	PJ0	36	-	-
	INT20	PG2	1	-	-
A-PMD2 ch 0	EMG0	PB6	9	-	-
		PB7	10	7	-
		PH1	38	27	25
	OVV0	PB6	9	-	-
		PB7	10	7	-
		PH1	38	27	25
	UO0	PB0	3	1	1
	VO0	PB1	4	2	2
		PB2	5	3	3
	WO0	PB2	5	3	3
		PB4	7	5	5
	XO0	PB1	4	2	2
		PB3	6	4	4
	YO0	PB3	6	4	4
		PB4	7	5	5
	ZO0	PB5	8	6	6
	PMD0DBG	PC4	17	-	-
		PD2	22	15	14
		PA0	26	19	18
A-ENC2 ch 0	ENC0A	PA0	26	19	18
	ENC0B	PA1	27	20	19
	ENC0Z	PA2	28	21	20

Table 3.6 Signal Connection List (6/6)

Function	Function pin name	Port name	M4L4 (LQFP64)	M4L2 (LQFP48/VQFN48)	M4L1 (LQFP44)
TRGSEL	TRGIN0	PC0	13	10	9
	TRGIN1	PA5	31	24	23
	TRGIN2	PG1	64	48	-
JTAG/SW	TMS	PD0	25	18	17
	TCK	PD1	24	17	16
	TDO	PH0	37	26	24
	TDI	PA4	30	23	22
	TRST_N	PA3	29	22	21
	SWDIO	PD0	25	18	17
	SWCLK	PD1	24	17	16
	SWV	PH0	37	26	24
TRACE	TRACECLK	PC5	18	-	-
	TRACEDATA0	PG3	2	-	-
	TRACEDATA1	PG2	1	-	-
Control pin	X1	PH0	37	26	24
	EHCLKIN	PH0	37	26	24
	X2	PH1	38	27	25
	SCOUT	PA0	26	19	18
	BOOT_N	PG0	62	46	43

4. Registers

Input/output port has function register and drive-capability control register.

4.1. Function Registers

The following registers must be set when using the port. Each register is 32 bits. The configuration of the register depends on the port count and its function assignment.

"x" and "n" in the following table show a port name and a function number, respectively.

Register name		Type	Setting value	Description
[PxDATA]	Data register	R/W	0 or 1	Read from a port or an output data. And write to an output data.
[PxCR]	Output control register	R/W	0: Output disabled 1: Output enabled	Output control
[PxFRn]	Function register n	R/W	0: PORT 1: Function	Function setting When “1” is set, the assigned function is enabled. Each function assigned to a port has its own function register. If multiple functions are assigned to one bit of port, only one function should be enabled.
[PxOD]	Open-drain control register	R/W	0: CMOS 1: Open drain	Programmable open-drain control The programmable open drain is a pseudo-open drain. An output buffer is disabled by setting ***[PxOD]*** to “1” when the output data is “1”.
[PxPUP]	Pull-up control register	R/W	0: Pull up disabled 1: Pull up enabled	Programmable pull-up resistor control
[PxPDN]	Pull-down control register	R/W	0: Pull down disabled 1: Pull down enabled	Programmable pull-down resistor control
[PxIE]	Input control register	R/W	0: Input disabled 1: Input enabled	Input control Up to 100ns is required that a state of port is reflected to ***[PxDATA]*** after ***[PxIE]*** is set to “1”.

4.1.1. Setting of Using Alternated Pin

To use the alternated pins as peripheral function output pins, set the function register (***[PxFRn]***<bit m>=1) to use as the peripheral function and then set output control register to enable output (***[PxCR]***<bit m>=1). If output is enabled before setting the function register, the data register value of the port is output until the function register is set.

To use the alternated pins as input pins of the peripheral function, set the input control register to enable input (***[PxIE]***<bit m>=1) and set the function register (***[PxFRn]***<bit m>=1) to use as the peripheral function, then set the peripheral functions.

To use the alternated pins as input/output pin of the peripheral functions such as I^2C, set the input control register to enable input (***[PxIE]***<bit m>=1), set the function register (***[PxFRn]***<bit m>=1) to use as the peripheral function and set the output control register to enable output (***[PxCR]***<bit m>=1), then set the peripheral function.

- When some functions are assigned to the same pin, use only one function exclusively.
- When the same function is assigned to some ports, use only one pin exclusively.

4.1.2. Function Registers List

When the bit which is not assigned is read, "0" is read. The write to it is ignored.

Table 4.1 Base Address of Port Registers

Peripheral function		Channel/unit	Base address
Input/output ports	PA	-	0x40080000
	PB	-	0x40080100
	PC	-	0x40080200
	PD	-	0x40080300
	PE	-	0x40080400
	PF	-	0x40080500
	PG	-	0x40080600
	PH	-	0x40080700
	PJ	-	0x40080800

Table 4.2 List of Registers

Register name	Address (Base+)	Port A	Port B	Port C	Port D	Port E	Port F
Data register	0x0000	***[PADATA]***	***[PBDATA]***	***[PCDATA]***	***[PDDATA]***	***[PEDATA]***	***[PFDATA]***
Output control register	0x0004	***[PACR]***	***[PBCR]***	***[PCCR]***	***[PDCR]***	***[PECR]***	***[PFCR]***
Function register 1	0x0008	***[PAFR1]***	-	***[PCFR1]***	***[PDFR1]***	-	-
Function register 2	0x000C	***[PAFR2]***	-	***[PCFR2]***	***[PDFR2]***	-	-
Function register 3	0x0010	***[PAFR3]***	***[PBFR3]***	***[PCFR3]***	***[PDFR3]***	-	-
Function register 4	0x0014	***[PAFR4]***	***[PBFR4]***	***[PCFR4]***	***[PDFR4]***	-	-
Function register 5	0x0018	***[PAFR5]***	-	***[PCFR5]***	***[PDFR5]***	-	-
Function register 6	0x001C	***[PAFR6]***	***[PBFR6]***	***[PCFR6]***	***[PDFR6]***	-	-
Function register 7	0x0020	***[PAFR7]***	***[PBFR7]***	***[PCFR7]***	***[PDFR7]***	-	-
Function register 8	0x0024	***[PAFR8]***	***[PBFR8]***	***[PCFR8]***	***[PDFR8]***	-	-
Open-drain control register	0x0028	***[PAOD]***	***[PBOD]***	***[PCOD]***	***[PDOD]***	***[PEOD]***	***[PFOD]***
Pull-up control register	0x002C	***[PAPUP]***	***[PBPUP]***	***[PCPUP]***	***[PDPUP]***	***[PEPUP]***	***[PFPUP]***
Pull-down control register	0x0030	***[PAPDN]***	***[PBPDN]***	***[PCPDN]***	***[PDPDN]***	***[PEPDN]***	***[PFPDN]***
Input control register	0x0038	***[PAIE]***	***[PBIE]***	***[PCIE]***	***[PDIE]***	***[PEIE]***	***[PFIE]***

Register name	Address (Base+)	Port G	Port H	Port J
Data register	0x0000	***[PGDATA]***	***[PHDATA]***	***[PJDATA]***
Output control register	0x0004	***[PGCR]***	***[PHCR]***	***[PJCR]***
Function register 1	0x0008	***[PGFR1]***	-	***[PJFR1]***
Function register 2	0x000C	***[PGFR2]***	-	***[PJFR2]***
Function register 3	0x0010	***[PGFR3]***	-	-
Function register 4	0x0014	***[PGFR4]***	-	-
Function register 5	0x0018	***[PGFR5]***	-	***[PJFR5]***
Function register 6	0x001C	***[PGFR6]***	[PHFR6]	***[PJFR6]***
Function register 7	0x0020	***[PGFR7]***	***[PHFR7]***	***[PJFR7]***
Function register 8	0x0024	***[PGFR8]***	***[PHFR8]***	***[PJFR8]***
Open-drain control register	0x0028	***[PGOD]***	***[PHOD]***	***[PJOD]***
Pull-up control register	0x002C	***[PGPUP]***	-	***[PJPUP]***
Pull-down control register	0x0030	***[PGPDN]***	***[PHPDN]***	***[PJPDN]***
Input control register	0x0038	***[PGIE]***	***[PHIE]***	***[PJIE]***

Note: Do not access the addresses described as "-".

4.1.3. List of Port Function Register Settings

It is explained about viewpoint of a list of the port function register settings tables.

The column of ***[PxFRn]*** shows the function register which should be set. When this register is set to "1", the corresponding function is enabled. (x is a port name and n is a function number.)

The bit of the "N/A" in the tables returns "0" when it is read. The write to the bit is ignored.

"0" or "1" in the tables shows the setting value. "0/1" means either value can be set.

PORT	Reset status / Function	Input/output	Port type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PA0	After reset			0	0	0	0	0	0	0
	Input port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output port	Output		0/1	1	0	0/1	0/1	0/1	0
	INTx	Input	FTU4	0/1	0	0	0/1	0/1	0/1	1
	Function output A	Output	FTU1	0/1	1	*[PAFR1]*	0/1	0/1	0/1	0
	Function input B	Input	FTU1	0/1	0	*[PAFR2]*	0/1	0/1	0/1	1
	Function output C	Output	FTU1	0/1	1	*[PAFR3]*	0/1	0/1	0/1	0
	Function input D	Input	FTU1	0/1	0	*[PAFR4]*	0/1	0/1	0/1	1

[PxFRn]	Pin				
	Function output A	Function input B	Function output C	Function input D	Input port / Output port
[PAFR1]<bit0>	1	0	0	0	0
[PAFR2]<bit0>	0	1	0	0	0
[PAFR3]<bit0>	0	0	1	0	0
[PAFR4]<bit0>	0	0	0	1	0

4.1.4. PORT A

Table 4.3 Port A Register Settings

PORT	Reset status / Function	Input/output	Port type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PA0	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT03	Input	FTU4	0/1	0	0	0/1	0/1	0/1	1
	UT2CTS_N	Input	FTU1	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	UT2RTS_N	Output	FTU1	0/1	1	***[PAFR2]***	0/1	0/1	0/1	0
	TSPI2SCK	Input	FTU1	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
		Output			1					0
	ENC0A	Input	FTU1	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	PMD0DBG	Output	FTU1	0/1	1	***[PAFR7]***	0/1	0/1	0/1	0
	SCOUT	Output	FTU1	0/1	1	***[PAFR8]***	0/1	0/1	0/1	0
PA1	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT2TXDA	Output	FTU1	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	UT2RXD	Input	FTU1	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	TSPI2TXD	Output	FTU2	0/1	1	***[PAFR3]***	0/1	0/1	0/1	0
	ENC0B	Input	FTU1	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	T32A04INA0	Input	FTU1	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
	T32A04INB1	Input	FTU1	0/1	0	***[PAFR6]***	0/1	0/1	0/1	1
	T32A04OUTB	Output	FTU1	0/1	1	***[PAFR7]***	0/1	0/1	0/1	0
	T32A04INC0	Input	FTU1	0/1	0	***[PAFR8]***	0/1	0/1	0/1	1
PA2	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT2RXD	Input	FTU1	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	UT2TXDA	Output	FTU1	0/1	1	***[PAFR2]***	0/1	0/1	0/1	0
	TSPI2RXD	Input	FTU1	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
	ENC0Z	Input	FTU1	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	T32A04INB0	Input	FTU1	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
	T32A04INA1	Input	FTU1	0/1	0	***[PAFR6]***	0/1	0/1	0/1	1
	T32A04OUTA	Output	FTU1	0/1	1	***[PAFR7]***	0/1	0/1	0/1	0
	T32A04OUTC	Output	FTU1	0/1	1	***[PAFR8]***	0/1	0/1	0/1	0
PA3	After reset (TRST_N)	Input	FTU3	0	0	***[PAFR8]***	0	1	0	1
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT1TXDA	Output	FTU1	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	UT1RXD	Input	FTU1	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	EI2C0SCL	I/O	FTU1	0/1	1	***[PBFR5]***	1	0/1	0/1	1
	T32A02INA0	Input	FTU1	0/1	0	***[PAFR6]***	0/1	0/1	0/1	1
	T32A02OUTB	Output	FTU1	0/1	1	***[PAFR7]***	0/1	0/1	0/1	0

PORT	Reset status / Function	Input/output	Port type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PA4	After reset (TDI)	Input	FTU2	0	0	***[PAFR8]***	0	1	0	1
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT04	Input	FTU4	0/1	0	0	0/1	0/1	0/1	1
	UT1RXD	Input	FTU1	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	UT1TXDA	Output	FTU1	0/1	1	***[PAFR2]***	0/1	0/1	0/1	0
	EI2C0SDA	I/O	FTU1	0/1	1	***[PAFR5]***	1	0/1	0/1	1
	T32A02INB0	Input	FTU1	0/1	0	***[PAFR6]***	0/1	0/1	0/1	1
	T32A02OUTA	Output	FTU1	0/1	1	***[PAFR7]***	0/1	0/1	0/1	0
PA5	After reset	Input	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT1TXDA	Output	FTU1	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	UT1RXD	Input	FTU1	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	TRGIN1	Input	FTU1	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	EI2C1SCL	I/O	FTU1	0/1	1	***[PAFR5]***	1	0/1	0/1	1
PA6	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT10	Input	FTU4	0/1	0	0	0/1	0/1	0/1	1
	UT1RXD	Input	FTU1	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	UT1TXDA	Output	FTU1	0/1	1	***[PAFR2]***	0/1	0/1	0/1	0
	EI2C1SDA	I/O	FTU1	0/1	1	***[PAFR5]***	1	0/1	0/1	1
PA7	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT16	Input	FTU4	0/1	0	0	0/1	0/1	0/1	1
	UT4TXDA	Output	FTU1	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	UT4RXD	Input	FTU1	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	T32A02INA0	Input	FTU1	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
	T32A02INB1	Input	FTU1	0/1	0	***[PAFR6]***	0/1	0/1	0/1	1
	T32A02OUTB	Output	FTU1	0/1	1	***[PAFR7]***	0/1	0/1	0/1	0
	T32A02INC0	Input	FTU1	0/1	0	***[PAFR8]***	0/1	0/1	0/1	1

4.1.5. PORT B

Table 4.4 Port B Register Settings

PORT	Reset status / Function	Input/output	Port type	Control register						
				[PBDATA]	*[PBCR]*	*[PBFRn]*	*[PBOD]*	*[PBPUP]*	*[PBPDN]*	*[PBIE]*
PB0	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UO0	Output	FTU2	0/1	1	***[PBFR6]*** / ***[PBFR7]***	0/1	0/1	0/1	0
PB1	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	XO0	Output	FTU2	0/1	1	***[PBFR6]***	0/1	0/1	0/1	0
	VO0	Output	FTU2	0/1	1	***[PBFR7]***	0/1	0/1	0/1	0
PB2	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	VO0	Output	FTU2	0/1	1	***[PBFR6]***	0/1	0/1	0/1	0
	WO0	Output	FTU2	0/1	1	***[PBFR7]***	0/1	0/1	0/1	0
PB3	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	YO0	Output	FTU2	0/1	1	***[PBFR6]***	0/1	0/1	0/1	0
	XO0	Output	FTU2	0/1	1	***[PBFR7]***	0/1	0/1	0/1	0
PB4	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	WO0	Output	FTU2	0/1	1	***[PBFR6]***	0/1	0/1	0/1	0
	YO0	Output	FTU2	0/1	1	***[PBFR7]***	0/1	0/1	0/1	0
PB5	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	ZO0	Output	FTU2	0/1	1	***[PBFR6]*** / ***[PBFR7]***	0/1	0/1	0/1	0
PB6	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	EMG0	Input	FTU1	0/1	0	***[PBFR6]***	0/1	0/1	0/1	1
	OVV0	Input	FTU1	0/1	0	***[PBFR7]***	0/1	0/1	0/1	1

PORT	Reset status / Function	Input/output	Port type	Control register						
				[PBDATA]	*[PBCR]*	*[PBFRn]*	*[PBOD]*	*[PBPUP]*	*[PBPDN]*	*[PBIE]*
PB7	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT09	Input	FTU4	0/1	0	0	0/1	0/1	0/1	1
	TSPI1CS1	Output	FTU1	0/1	1	***[PBFR3]***	0/1	0/1	0/1	0
	SMI0CS1_N	Output	FTU1	0/1	1	***[PBFR4]***	0/1	0/1	0/1	0
	OVV0	Input	FTU1	0/1	0	***[PBFR6]***	0/1	0/1	0/1	1
	EMG0	Input	FTU1	0/1	0	***[PBFR7]***	0/1	0/1	0/1	1
	T32A00OUTB	Output	FTU1	0/1	1	***[PBFR8]***	0/1	0/1	0/1	0

4.1.6. PORT C

Table 4.5 Port C Register Settings

PORT	Reset status / Function	Input/output	Port type	Control register						
				[PCDATA]	*[PCCR]*	*[PCFRn]*	*[PCOD]*	*[PCPUP]*	*[PCPDN]*	*[PCIE]*
PC0	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT3TXDA	Output	FTU1	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
	UT3RXD	Input	FTU1	0/1	0	***[PCFR2]***	0/1	0/1	0/1	1
	TSPI1CS0	Output	FTU1	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0
	SMI0CS0_N	Output	FTU1	0/1	1	***[PCFR4]***	0/1	0/1	0/1	0
	TSPI1CSIN	Input	FTU1	0/1	0	***[PCFR5]***	0/1	0/1	0/1	1
	TRGIN0	Input	FTU1	0/1	0	***[PCFR6]***	0/1	0/1	0/1	1
	T32A00INA0	Input	FTU1	0/1	0	***[PCFR7]***	0/1	0/1	0/1	1
	T32A00INB1	Input	FTU1	0/1	0	***[PCFR8]***	0/1	0/1	0/1	1
PC1	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT3RXD	Input	FTU1	0/1	0	***[PCFR1]***	0/1	0/1	0/1	1
	UT3TXDA	Output	FTU1	0/1	1	***[PCFR2]***	0/1	0/1	0/1	0
	TSPI1SCK	Input	FTU1	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
		Output			1					0
	SMI0CLK	Output	FTU1	0/1	1	***[PCFR4]***	0/1	0/1	0/1	0
	T32A00INB0	Input	FTU1	0/1	0	***[PCFR6]***	0/1	0/1	0/1	1
	T32A00INA1	Input	FTU1	0/1	0	***[PCFR7]***	0/1	0/1	0/1	1
	T32A00OUTA	Output	FTU1	0/1	1	***[PCFR8]***	0/1	0/1	0/1	0
PC2	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT2TXDA	Output	FTU1	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
	UT2RXD	Input	FTU1	0/1	0	***[PCFR2]***	0/1	0/1	0/1	1
	TSPI1TXD	Output	FTU2	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0
	SMI0D0	Input	FTU1	0/1	0	***[PCFR4]***	0/1	0/1	0/1	1
		Output			1					0
	T32A01INA0	Input	FTU1	0/1	0	***[PCFR5]***	0/1	0/1	0/1	1
	T32A01INB1	Input	FTU1	0/1	0	***[PCFR6]***	0/1	0/1	0/1	1
	T32A01OUTB	Output	FTU1	0/1	1	***[PCFR7]***	0/1	0/1	0/1	0
	T32A01INC0	Input	FTU1	0/1	0	***[PCFR8]***	0/1	0/1	0/1	1

PORT	Reset status / Function	Input/output	Port type	Control register						
				[PCDATA]	*[PCCR]*	*[PCFRn]*	*[PCOD]*	*[PCPUP]*	*[PCPDN]*	*[PCIE]*
PC3	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT2RXD	Input	FTU1	0/1	0	***[PCFR1]***	0/1	0/1	0/1	1
	UT2TXDA	Output	FTU1	0/1	1	***[PCFR2]***	0/1	0/1	0/1	0
	TSPI1RXD	Input	FTU1	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
	SMI0D1	Input	FTU1	0/1	0	***[PCFR4]***	0/1	0/1	0/1	1
		Output			1					0
	T32A01INB0	Input	FTU1	0/1	0	***[PCFR5]***	0/1	0/1	0/1	1
	T32A01INA1	Input	FTU1	0/1	0	***[PCFR6]***	0/1	0/1	0/1	1
	T32A01OUTA	Output	FTU1	0/1	1	***[PCFR7]***	0/1	0/1	0/1	0
	T32A01OUTC	Output	FTU1	0/1	1	***[PCFR8]***	0/1	0/1	0/1	0
PC4	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT14	Input	FTU4	0/1	0	0	0/1	0/1	0/1	1
	UT3RTS_N	Output	FTU1	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
	UT3CTS_N	Input	FTU1	0/1	0	***[PCFR2]***	0/1	0/1	0/1	1
	SMI0D2	Input	FTU1	0/1	0	***[PCFR4]***	0/1	0/1	0/1	1
		Output			1					0
	PMD0DBG	Output	FTU1	0/1	1	***[PCFR8]***	0/1	0/1	0/1	0
PC5	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT15	Input	FTU4	0/1	0	0	0/1	0/1	0/1	1
	UT3CTS_N	Input	FTU1	0/1	0	***[PCFR1]***	0/1	0/1	0/1	1
	UT3RTS_N	Output	FTU1	0/1	1	***[PCFR2]***	0/1	0/1	0/1	0
	SMI0D3	Input	FTU1	0/1	0	***[PCFR4]***	0/1	0/1	0/1	1
		Output			1					0
	TRACECLK	Output	FTU1	0/1	1	***[PCFR8]***	0/1	0/1	0/1	0

4.1.7. PORT D

Table 4.6 Port D Register Settings

PORT	Reset status / Function	Input/output	Port type	Control register						
				[PDDATA]	*[PDCR]*	*[PDFRn]*	*[PDOD]*	*[PDPUP]*	*[PDPDN]*	*[PDIE]*
PD0	After reset (TMS/SWDIO)	Input/output	FTU2	0	1 (Note)	***[PDFR8]***	0	1	0	1
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT02	Input	FTU4	0/1	0	0	0/1	0/1	0/1	1
	TSPI2CS0	Output	FTU1	0/1	1	***[PDFR3]***	0/1	0/1	0/1	0
	TSPI2CSIN	Input	FTU1	0/1	0	***[PDFR4]***	0/1	0/1	0/1	1
PD1	After reset (TCK/SWCLK)	Input	FTU2	0	0	***[PDFR8]***	0	0	1	1
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	TSPI2CS1	Output	FTU1	0/1	1	***[PDFR2]***	0/1	0/1	0/1	0
PD2	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT01	Input	FTU4	0/1	0	0	0/1	0/1	0/1	1
	UT0RXD	Input	FTU1	0/1	0	***[PDFR1]***	0/1	0/1	0/1	1
	UT0TXDA	Output	FTU1	0/1	1	***[PDFR2]***	0/1	0/1	0/1	0
	PMD0DBG	Output	FTU1	0/1	1	***[PDFR3]***	0/1	0/1	0/1	0
	SMI0D3	Input	FTU1	0/1	0	***[PDFR4]***	0/1	0/1	0/1	1
		Output			1					0
	T32A03INB0	Input	FTU1	0/1	0	***[PDFR5]***	0/1	0/1	0/1	1
	T32A03INA1	Input	FTU1	0/1	0	***[PDFR6]***	0/1	0/1	0/1	1
	T32A03OUTA	Output	FTU1	0/1	1	***[PDFR7]***	0/1	0/1	0/1	0
	T32A03OUTC	Output	FTU1	0/1	1	***[PDFR8]***	0/1	0/1	0/1	0
PD3	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT00	Input	FTU4	0/1	0	0	0/1	0/1	0/1	1
	UT0TXDA	Output	FTU1	0/1	1	***[PDFR1]***	0/1	0/1	0/1	0
	UT0RXD	Input	FTU1	0/1	0	***[PDFR2]***	0/1	0/1	0/1	1
	TSPI1CS1	Output	FTU1	0/1	1	***[PDFR3]***	0/1	0/1	0/1	0
	SMI0D2	Input	FTU1	0/1	0	***[PDFR4]***	0/1	0/1	0/1	1
		Output			1					0
	T32A03INA0	Input	FTU1	0/1	0	***[PDFR5]***	0/1	0/1	0/1	1
	T32A03INB1	Input	FTU1	0/1	0	***[PDFR6]***	0/1	0/1	0/1	1
	T32A03OUTB	Output	FTU1	0/1	1	***[PDFR7]***	0/1	0/1	0/1	0
	T32A03INC0	Input	FTU1	0/1	0	***[PDFR8]***	0/1	0/1	0/1	1

PORT	Reset status / Function	Input/output	Port type	Control register						
				[PDDATA]	*[PDCR]*	*[PDFRn]*	*[PDOD]*	*[PDPUP]*	*[PDPDN]*	*[PDIE]*
PD4	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT3RXD	Input	FTU1	0/1	0	***[PDFR1]***	0/1	0/1	0/1	1
	UT3TXDA	Output	FTU1	0/1	1	***[PDFR2]***	0/1	0/1	0/1	0
	T32A01INB0	Input	FTU1	0/1	0	***[PDFR4]***	0/1	0/1	0/1	1
	T32A01INA1	Input	FTU1	0/1	0	***[PDFR5]***	0/1	0/1	0/1	1
	T32A01OUTA	Output	FTU1	0/1	1	***[PDFR6]***	0/1	0/1	0/1	0
	T32A01OUTC	Output	FTU1	0/1	1	***[PDFR7]***	0/1	0/1	0/1	0
PD5	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UT3TXDA	Output	FTU1	0/1	1	***[PDFR1]***	0/1	0/1	0/1	0
	UT3RXD	Input	FTU1	0/1	0	***[PDFR2]***	0/1	0/1	0/1	1
	T32A01INA0	Input	FTU1	0/1	0	***[PDFR4]***	0/1	0/1	0/1	1
	T32A01INB1	Input	FTU1	0/1	0	***[PDFR5]***	0/1	0/1	0/1	1
	T32A01OUTB	Output	FTU1	0/1	1	***[PDFR6]***	0/1	0/1	0/1	0
	T32A01INC0	Input	FTU1	0/1	0	***[PDFR7]***	0/1	0/1	0/1	1

Note: This pin is enabled to output after receiving the command from a debug tool.

4.1.8. PORT E

Table 4.7 Port E Register Settings

PORT	Reset status / Function	Input/output	Port type	Control register						
				[PEDATA]	*[PECR]*	*[PEFRn]*	*[PEOD]*	*[PEPUP]*	*[PEPDN]*	*[PEIE]*
PE0	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA00/ AINB00 (Note)	Input	FTU5	0/1	0	N/A	0/1	0	0	0
PE1	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA01/ AINB01 (Note)	Input	FTU5	0/1	0	N/A	0/1	0	0	0
PE2	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA02/ AINB02 (Note)	Input	FTU5	0/1	0	N/A	0/1	0	0	0
PE3	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA03/ AINB03 (Note)	Input	FTU5	0/1	0	N/A	0/1	0	0	0
PE4	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA04/ AINB04 (Note)	Input	FTU5	0/1	0	N/A	0/1	0	0	0
PE5	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA05/ AINB05 (Note)	Input	FTU5	0/1	0	N/A	0/1	0	0	0
PE6	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA06/ AINB06 (Note)	Input	FTU5	0/1	0	N/A	0/1	0	0	0
PE7	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA07/ AINB07 (Note)	Input	FTU5	0/1	0	N/A	0/1	0	0	0

Note: When using as analog input pins (AINAx/AINBx), ***[PEIE]*** should be set to disable input "0", ***[PECR]*** should be set to disable output "0", ***[PEPUP]*** should be set to disable pull-up "0", and ***[PEPDN]*** should be set to disable pull-down "0".

4.1.9. PORT F

Table 4.8 Port F Register Settings

PORT	Reset status / Function	Input/output	Port type	Control register						
				[PFDATA]	*[PFCR]*	*[PFFRn]*	*[PFOD]*	*[PFPUP]*	*[PFPDN]*	*[PFIE]*
PF0	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA08/ AINB08 (Note)	Input	FTU5	0/1	0	N/A	0/1	0	0	0
PF1	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA09/ AINB09 (Note)	Input	FTU5	0/1	0	N/A	0/1	0	0	0
PF2	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA10/ AINB10 (Note)	Input	FTU5	0/1	0	N/A	0/1	0	0	0
PF3	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	INT08	Input	FTU4	0/1	0	N/A	0/1	0/1	0/1	1
	AINA11/ AINB11 (Note)	Input	FTU5	0/1	0	N/A	0/1	0	0	0
PF4	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	INT07	Input	FTU4	0/1	0	N/A	0/1	0/1	0/1	1
	AINA12/ AINB12 (Note)	Input	FTU5	0/1	0	N/A	0/1	0	0	0
PF5	After reset	-	-	0	0	N/A	0	0	0	0
	Input port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	INT11	Input	FTU4	0/1	0	N/A	0/1	0/1	0/1	1
	AINA13/ AINB13 (Note)	Input	FTU5	0/1	0	N/A	0/1	0	0	0

Note: When using as analog input pins (AINAx/AINBx), ***[PFIE]*** should be set to disable input "0", ***[PFCR]*** should be set to disable output "0", ***[PFPUP]*** should be set to disable pull-up "0", and ***[PFPDN]*** should be set to disable pull-down "0".

4.1.10. PORT G

Table 4.9 Port G Register Settings

PORT	Reset status / Function	Input/output	Port type	Control register						
				[PGDATA]	*[PGCR]*	*[PGFRn]*	*[PGOD]*	*[PGPUP]*	*[PGPDN]*	*[PGIE]*
PG0	During reset (BOOT_N)	Input (Note)	FTU6a	0	0	0	0	0 (Note)	0	N/A
	After reset	-	-	0	0	0	0	0	0	N/A
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	N/A
	UT5TXDA	Output	FTU1	0/1	1	***[PGFR1]***	0/1	0/1	0/1	N/A
	TSPI0TXD	Output	FTU2	0/1	1	***[PGFR3]***	0/1	0/1	0/1	N/A
PG1	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT12	Input	FTU4	0/1	0	0	0/1	0/1	0/1	1
	UT5RXD	Input	FTU1	0/1	0	***[PGFR1]***	0/1	0/1	0/1	1
	TSPI0RXD	Input	FTU1	0/1	0	***[PGFR3]***	0/1	0/1	0/1	1
	TRGIN2	Input	FTU1	0/1	0	***[PGFR4]***	0/1	0/1	0/1	1
	T32A03INB0	Input	FTU1	0/1	0	***[PGFR5]***	0/1	0/1	0/1	1
	T32A03INA1	Input	FTU1	0/1	0	***[PGFR6]***	0/1	0/1	0/1	1
	T32A03OUTA	Output	FTU1	0/1	1	***[PGFR7]***	0/1	0/1	0/1	0
	T32A03OUTC	Output	FTU1	0/1	1	***[PGFR8]***	0/1	0/1	0/1	0
PG2	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT20	Input	FTU4	0/1	0	0	0/1	0/1	0/1	1
	UT5CTS_N	Input	FTU1	0/1	0	***[PGFR1]***	0/1	0/1	0/1	1
	UT5RTS_N	Output	FTU1	0/1	1	***[PGFR2]***	0/1	0/1	0/1	0
	TSPI0SCK	Input	FTU1	0/1	0	***[PGFR3]***	0/1	0/1	0/1	1
		Output			1					0
	TRACEDATA1	Output	FTU1	0/1	1	***[PGFR8]***	0/1	0/1	0/1	0
PG3	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT13	Input	FTU4	0/1	0	0	0/1	0/1	0/1	1
	TSPI0CSIN	Input	FTU1	0/1	0	***[PGFR2]***	0/1	0/1	0/1	1
	TSPI0CS0	Output	FTU1	0/1	1	***[PGFR3]***	0/1	0/1	0/1	0
	T32A00INA0	Input	FTU1	0/1	0	***[PGFR4]***	0/1	0/1	0/1	1
	T32A00INB1	Input	FTU1	0/1	0	***[PGFR5]***	0/1	0/1	0/1	1
	T32A00OUTB	Output	FTU1	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0
	T32A00INC0	Input	FTU1	0/1	0	***[PGFR7]***	0/1	0/1	0/1	1
	TRACEDATA0	Output	FTU1	0/1	1	***[PGFR8]***	0/1	0/1	0/1	0

Note: During the reset period by the reset pin (RESET_N), the state of the BOOT_N pin can be input to PG0 with pull-up enabled and input enabled.

4.1.11. PORT H

Table 4.10 Port H Register Settings

PORT	Reset status / Function	Input/output	PORT Type	Control register						
				[PHDATA]	*[PHCR]*	*[PHFRn]*	*[PHOD]*	*[PHPUP]*	*[PHPDN]*	*[PHIE]*
PH0	After reset (TDO/SWV)	Output	FTU2	0	1 (Note)	***[PHFR8]***	0	N/A	0	0
	Input port	Input	-	0/1	0	0	0/1	N/A	0/1	1
	Output port	Output	-	0/1	1	0	0/1	N/A	0/1	0
	INT5	Input	FTU4	0/1	0	0	0/1	N/A	0/1	1
	X1	Input	FTU11b	0/1	0	0	0/1	N/A	0	0
	EHCLKIN	Input	FTU11b	0/1	0	0	0/1	N/A	0	0/1
PH1	After reset	-	-	0	0	0	0	N/A	0	0
	Input port	Input	-	0/1	0	0	0/1	N/A	0/1	1
	Output port	Output	-	0/1	1	0	0/1	N/A	0/1	0
	INT6	Input	FTU4	0/1	0	0	0/1	N/A	0/1	1
	X2	Output	FTU11b	0/1	0	0	0/1	N/A	0	0
	EMG0	Input	FTU1	0/1	0	***[PHFR6]***	0/1	N/A	0/1	1
	OVV0	Input	FTU1	0/1	0	***[PHFR7]***	0/1	N/A	0/1	1

Note: This pin is enabled to output after receiving the command from a debug tool.

4.1.12. PORT J

Table 4.11 Port J Register Settings

PORT	Reset status / Function	Input/output	PORT Type	Control register						
				[PJDATA]	*[PJCR]*	*[PJFRn]*	*[PJOD]*	*[PJPUP]*	*[PJPDN]*	*[PJIE]*
PJ0	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT19	Input	FTU4	0/1	0	0	0/1	0/1	0/1	1
	TSPI2CS1	Output	FTU1	0/1	1	***[PJFR2]***	0/1	0/1	0/1	0
	T32A04INA0	Input	FTU1	0/1	0	***[PJFR5]***	0/1	0/1	0/1	1
	T32A04INB1	Input	FTU1	0/1	0	***[PJFR6]***	0/1	0/1	0/1	1
	T32A04OUTB	Output	FTU1	0/1	1	***[PJFR7]***	0/1	0/1	0/1	0
	T32A04INC0	Input	FTU1	0/1	0	***[PJFR8]***	0/1	0/1	0/1	1
PJ1	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT18	Input	FTU4	0/1	0	0	0/1	0/1	0/1	1
	UT4CTS_N	Input	FTU1	0/1	0	***[PJFR1]***	0/1	0/1	0/1	1
	UT4RTS_N	Output	FTU1	0/1	1	***[PJFR2]***	0/1	0/1	0/1	0
	T32A00INB0	Input	FTU1	0/1	0	***[PJFR5]***	0/1	0/1	0/1	1
	T32A00INA1	Input	FTU1	0/1	0	***[PJFR6]***	0/1	0/1	0/1	1
	T32A00OUTA	Output	FTU1	0/1	1	***[PJFR7]***	0/1	0/1	0/1	0
	T32A00OUTC	Output	FTU1	0/1	1	***[PJFR8]***	0/1	0/1	0/1	0
PJ2	After reset	-	-	0	0	0	0	0	0	0
	Input port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT17	Input	FTU4	0/1	0	0	0/1	0/1	0/1	1
	UT4RXD	Input	FTU1	0/1	0	***[PJFR1]***	0/1	0/1	0/1	1
	UT4TXDA	Output	FTU1	0/1	1	***[PJFR2]***	0/1	0/1	0/1	0
	T32A02INB0	Input	FTU1	0/1	0	***[PJFR5]***	0/1	0/1	0/1	1
	T32A02INA1	Input	FTU1	0/1	0	***[PJFR6]***	0/1	0/1	0/1	1
	T32A02OUTA	Output	FTU1	0/1	1	***[PJFR7]***	0/1	0/1	0/1	0
	T32A02OUTC	Output	FTU1	0/1	1	***[PJFR8]***	0/1	0/1	0/1	0

4.2. Drive-capability Control Register

Output drive capability can be selected for the following pins from 1 to 4 mA.

- PA0 to 2
- PB7
- PC0 to 5
- PD0 to 3
- PG0 to 3
- PJ0

When changing the drive capability, make sure that ***[PxCR]*** of the target port is "0" (output prohibited).
Output drive capability is 1mA in the STOP2 mode.

4.2.1. Drive-capability Control Register List

Peripheral function		Channel/unit	Base address
Drive-capability Control	DRV	-	0x40090000

Register name		Address (Base+)
Drive-capability Control Register 0	***[DRVCR0]***	0x0000
Drive-capability Control Register 1	***[DRVCR1]***	0x0100

4.2.2. *[DRVCR0]* (Drive-capability Control Register 0)

Bit	Bit symbol	After reset	Type	Function
31:30	DRV15[1:0]	11	R/W	PG1 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA
29:28	DRV14[1:0]	11	R/W	PG0 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA
27:26	DRV13[1:0]	11	R/W	PD3 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA
25:24	DRV12[1:0]	11	R/W	PD2 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA
23:22	DRV11[1:0]	11	R/W	PD1 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA
21:20	DRV10[1:0]	11	R/W	PD0 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA
19:18	DRV9[1:0]	11	R/W	PC5 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA
17:16	DRV8[1:0]	11	R/W	PC4 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA
15:14	DRV7[1:0]	11	R/W	PC3 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA
13:12	DRV6[1:0]	11	R/W	PC2 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA

Bit	Bit symbol	After reset	Type	Function
11:10	DRV5[1:0]	11	R/W	PC1 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA
9:8	DRV4[1:0]	11	R/W	PC0 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA
7:6	DRV3[1:0]	11	R/W	PB7 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA
5:4	DRV2[1:0]	11	R/W	PA2 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA
3:2	DRV1[1:0]	11	R/W	PA1 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA
1:0	DRV0[1:0]	11	R/W	PA0 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA

4.2.3. *[DRVCR1]* (Drive-capability Control Register 1)

Bit	Bit symbol	After reset	Type	Function
31:6	-	0	R	Read as "0".
5:4	DRV18[1:0]	11	R/W	PJ0 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA
3:2	DRV17[1:0]	11	R/W	PG3 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA
1:0	DRV16[1:0]	11	R/W	PG2 drive-capability control 00: 1 mA 01: 2 mA 10: 3 mA 11: 4 mA

5. Port Circuit Diagram

The port has 7 types of circuits, FTU1 to FTU6a and FTU11b. Each circuit diagram is shown in the following page and after. For information on the presence or absence of the drive-capability control register, refer to "4.2. Drive-capability Control Register".

The dot line block shows "Equivalent Circuit" which is described in "Datasheet".

The "I/O Reset" shown in the circuit diagram is described the power-on reset (POR).

5.1. Type FTU1

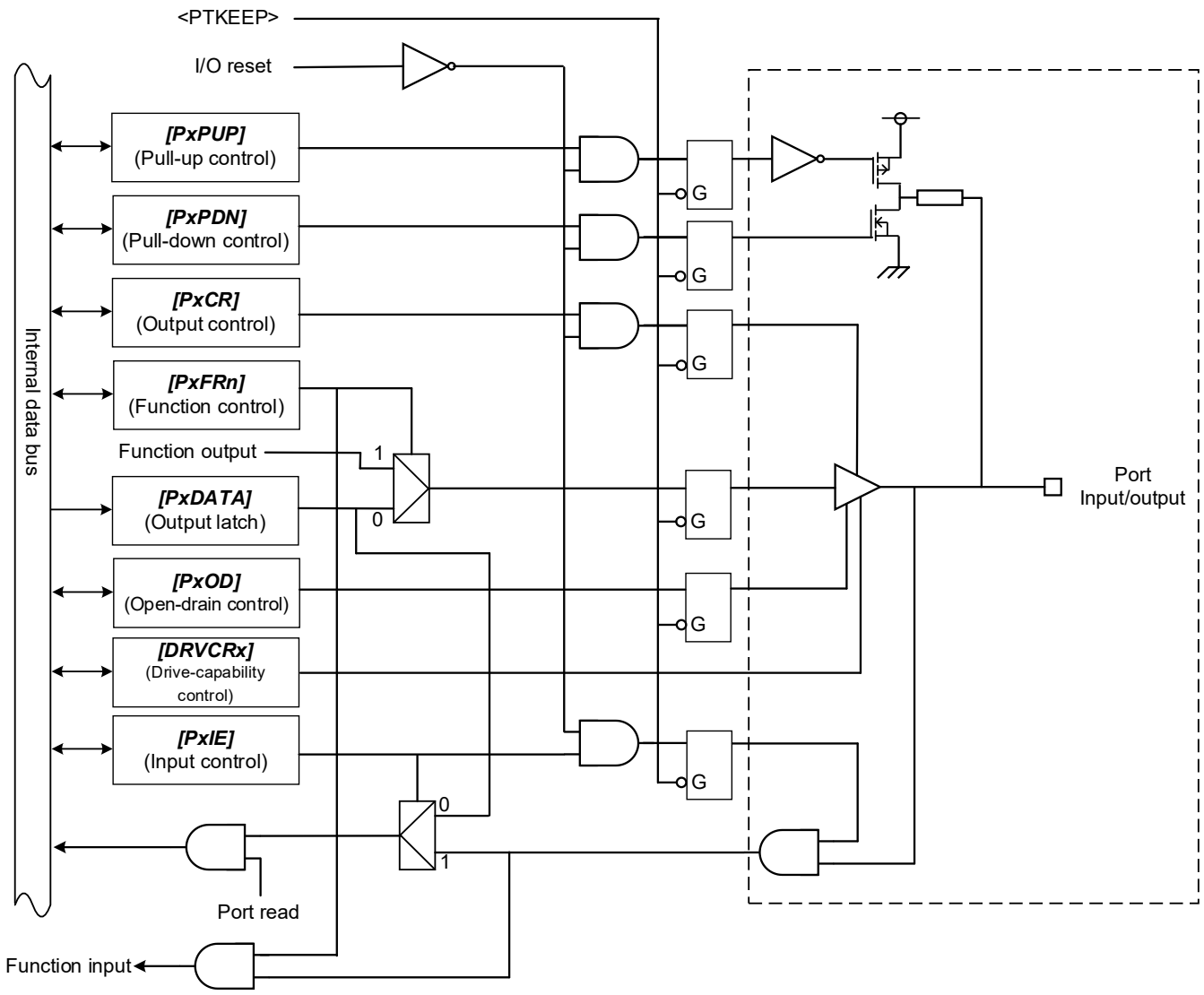

Figure 5.1 Port Type FTU1

5.2. Type FTU2

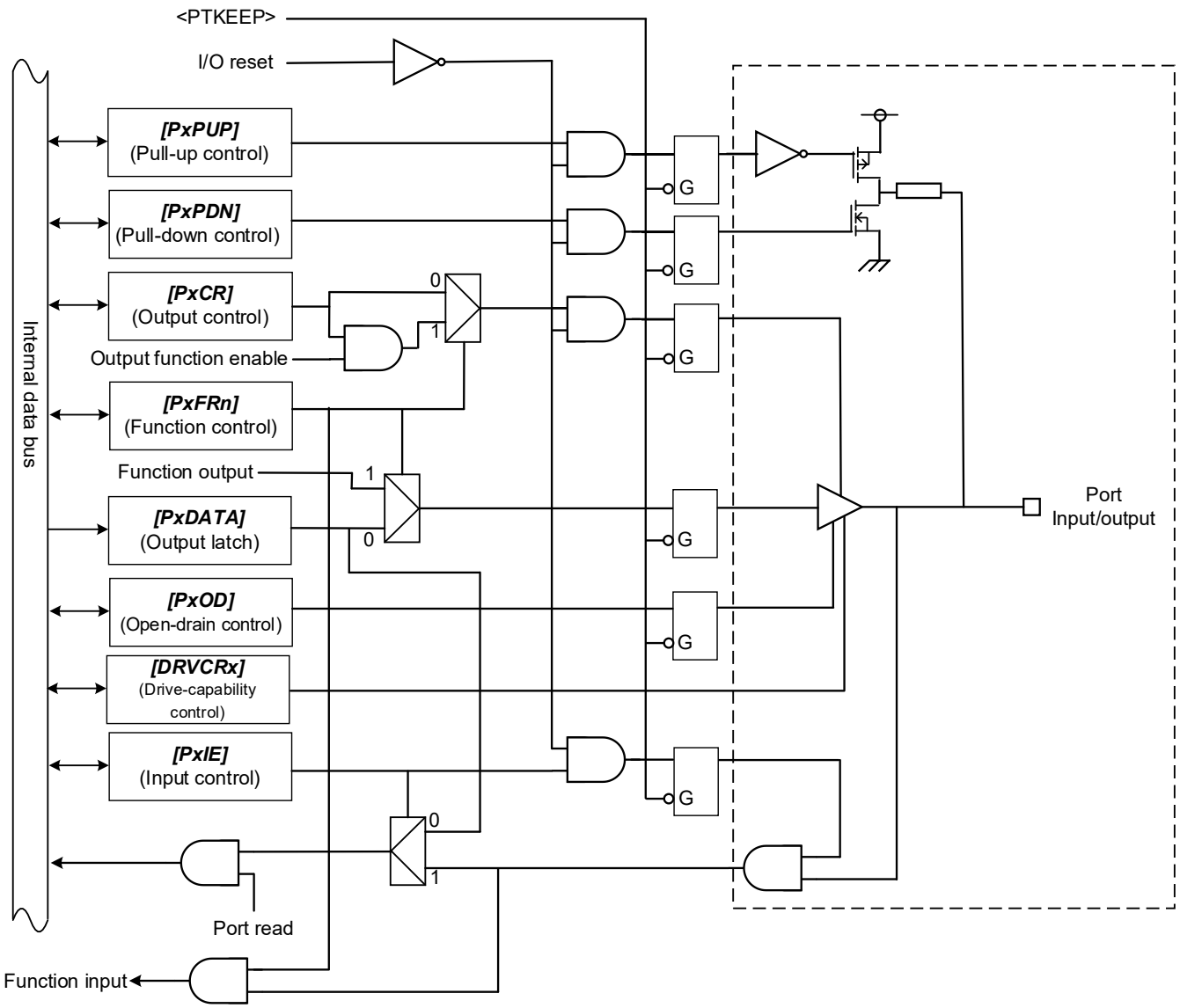

Figure 5.2 Port Type FTU2

5.3. Type FTU3

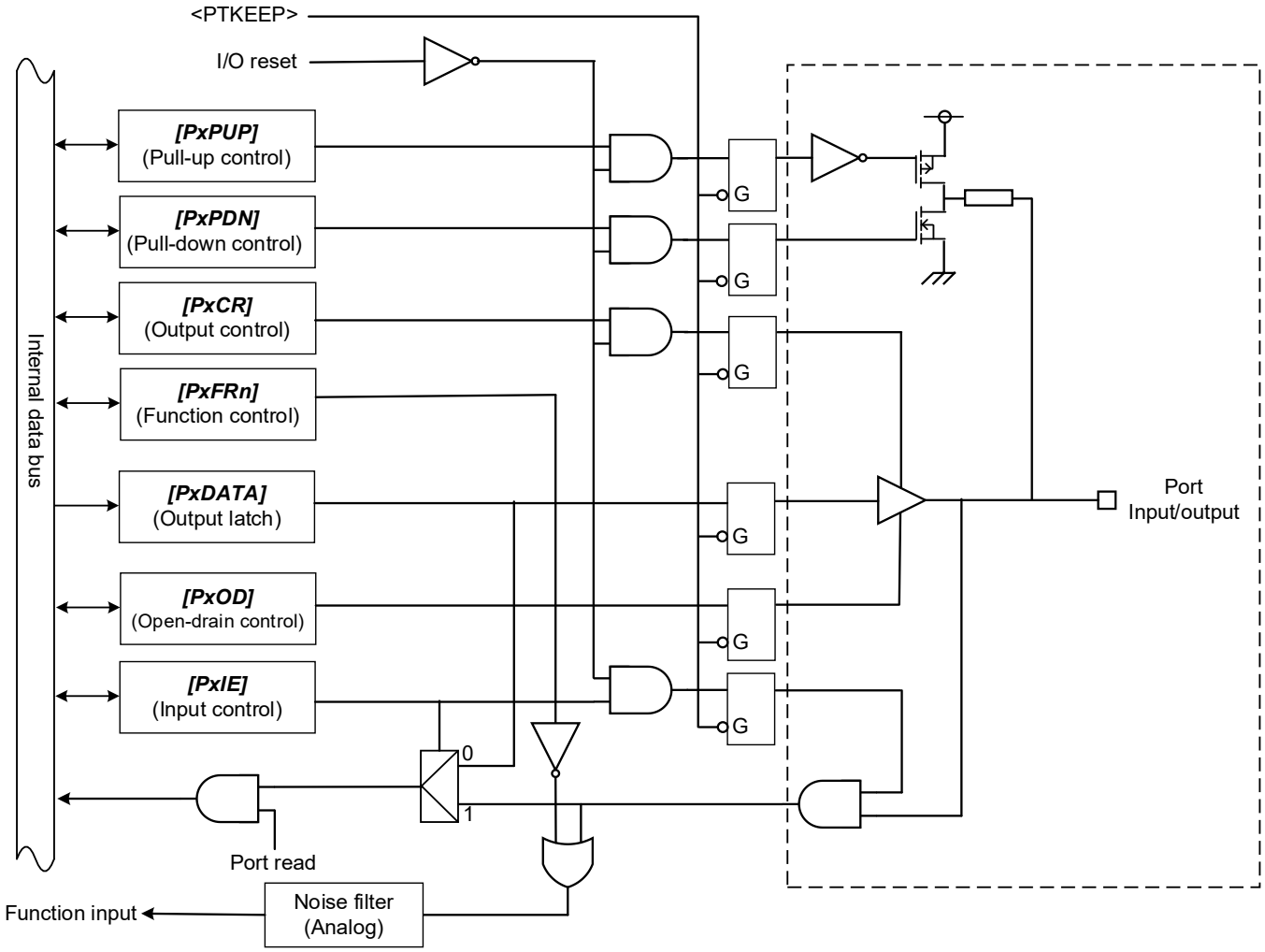

Figure 5.3 Port Type FTU3

5.4. Type FTU4

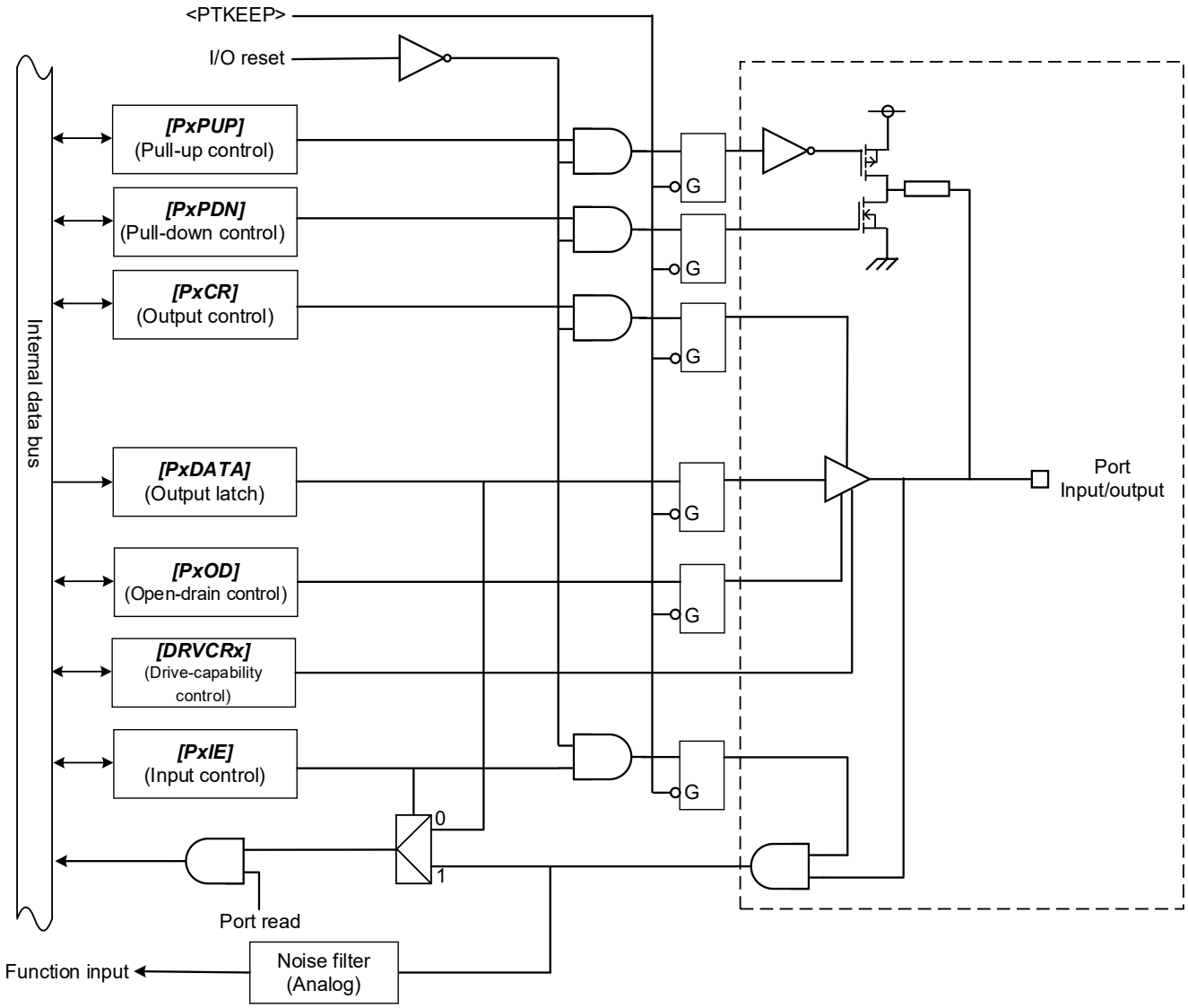

Figure 5.4 Port Type FTU4

5.5. Type FTU5

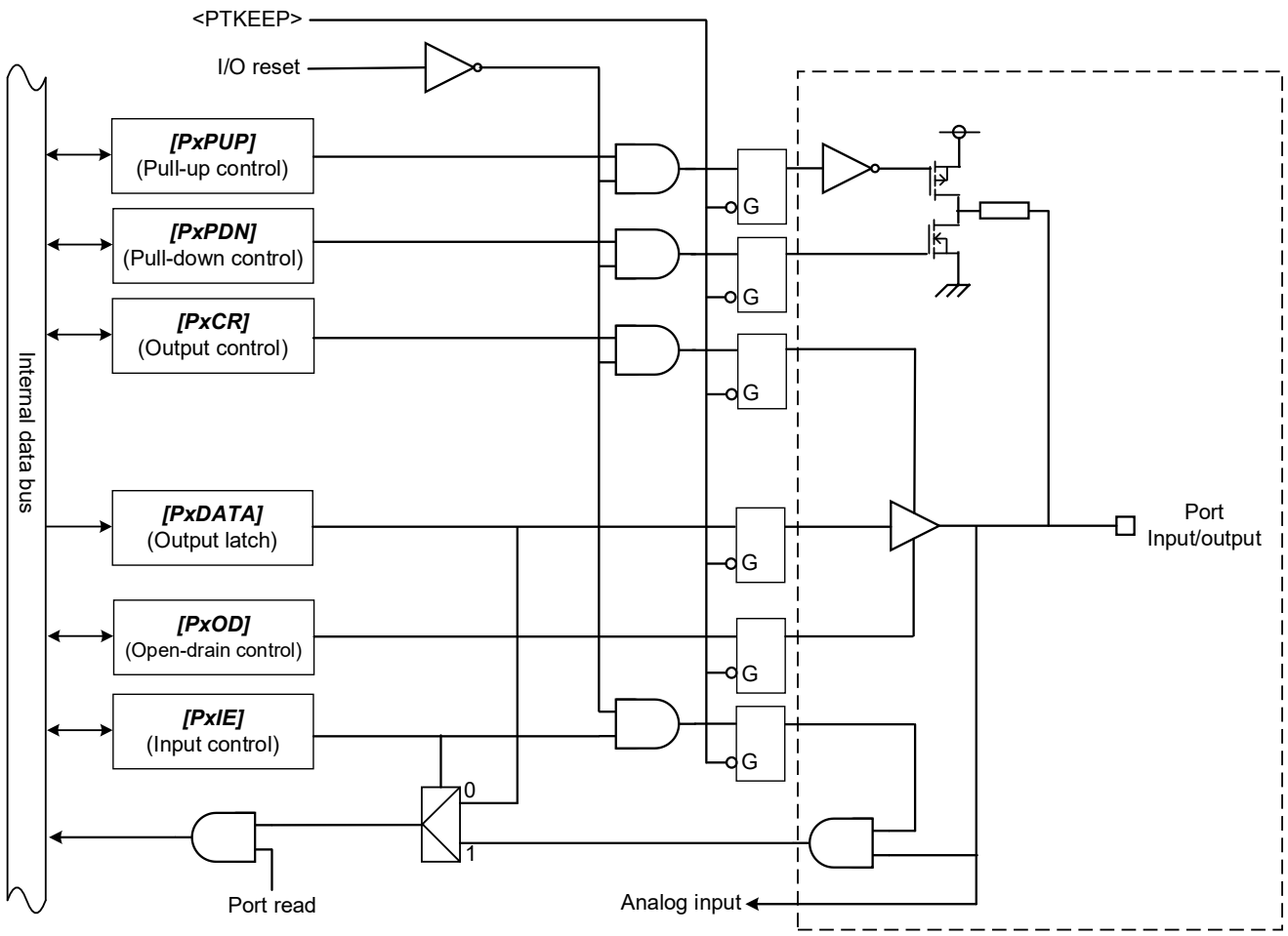

Figure 5.5 Port Type FTU5

5.6. Type FTU6a

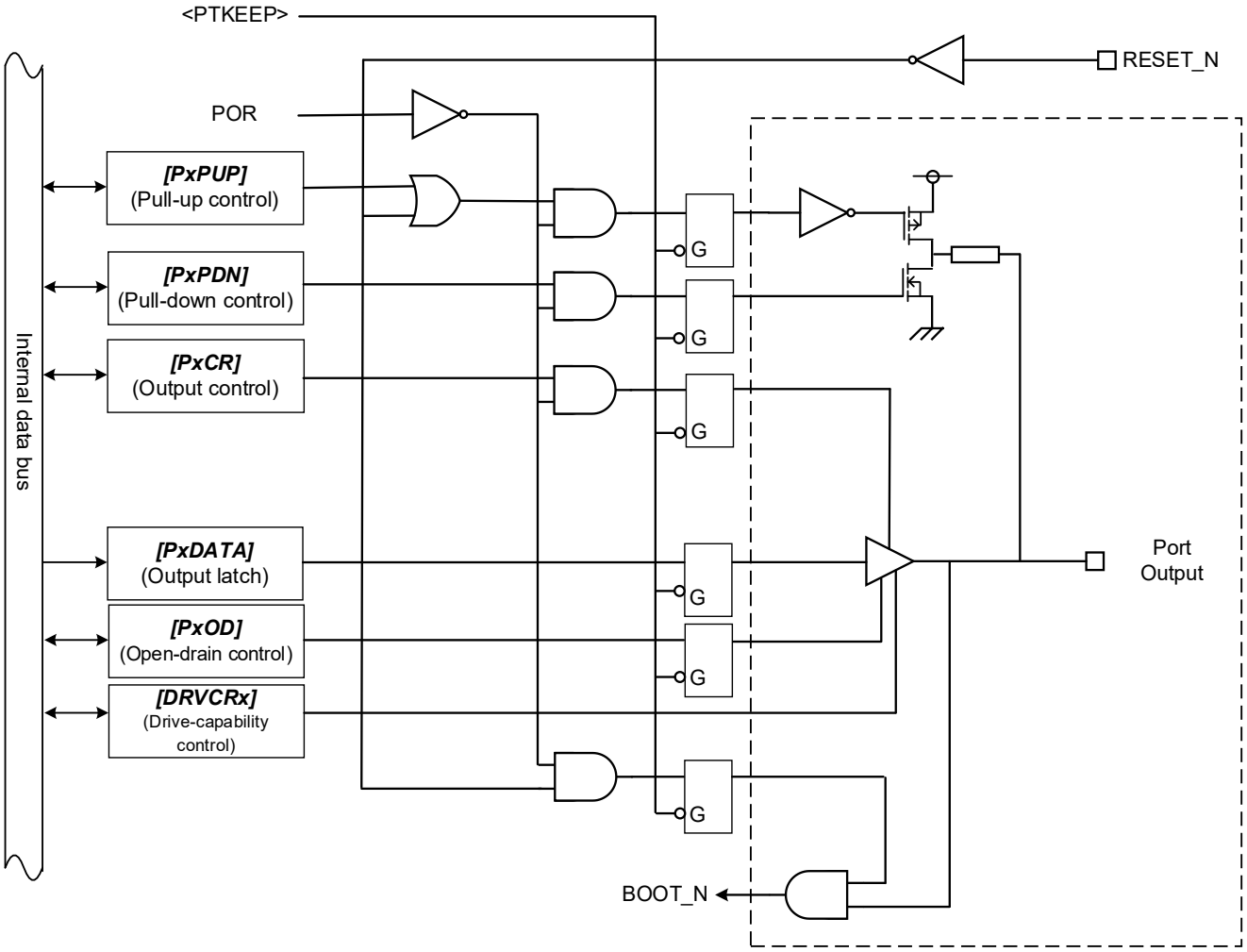

Figure 5.6 Port Type FTU6a

5.7. Type FTU11b

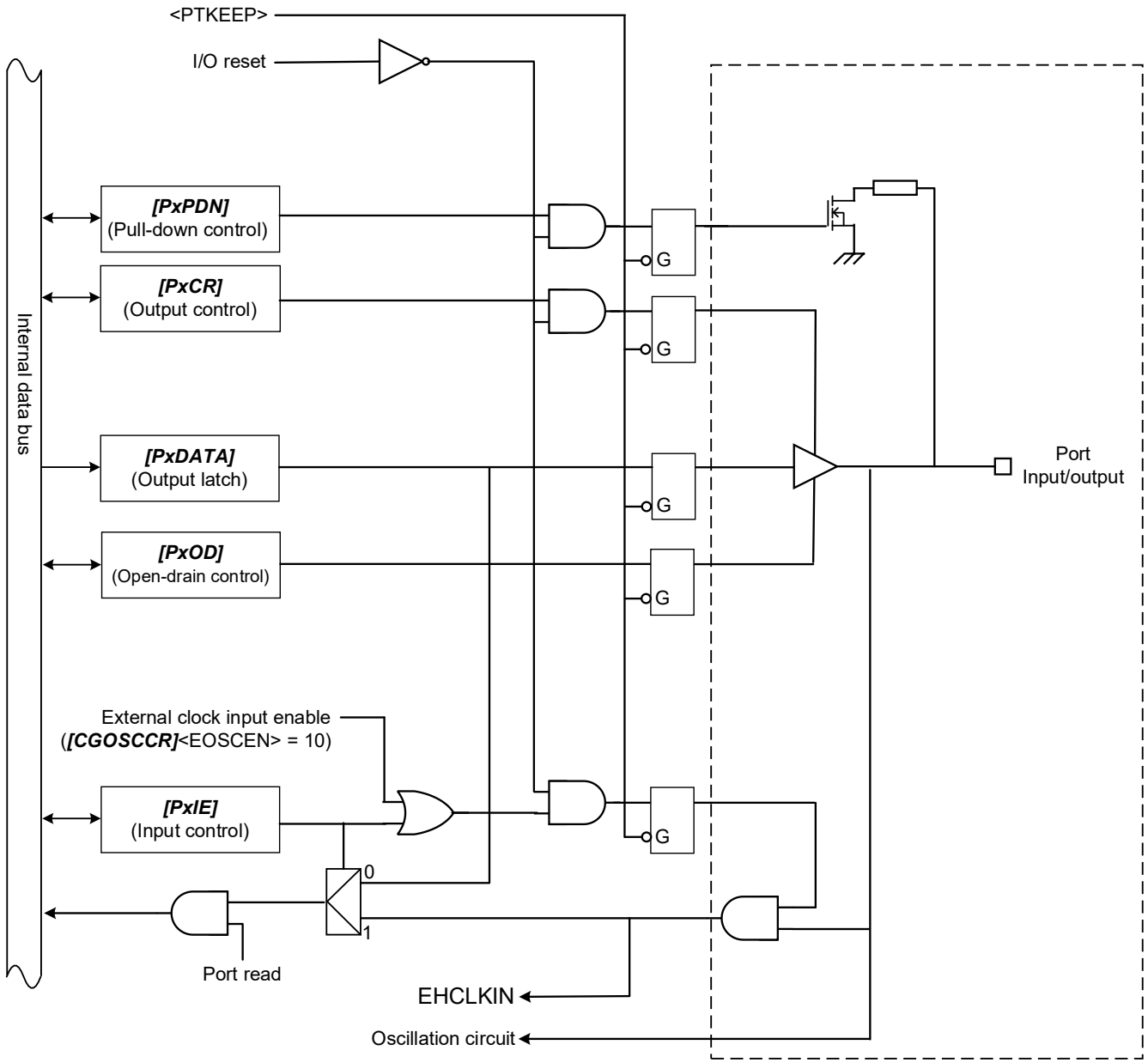

Figure 5.7 Port Type FTU11b

6. Precaution

6.1. Pin Status during Reset Period

During the reset period, the pin status is high impedance except for below pins. And, the pull-up/pull-down is disabled.

- The debug interface alternate pins (PD0, PD1, PA3, PA4, PH0) are used as debug pins.
- PG0 (BOOT_N) is enabled to input and pulled-up during reset period by RESET_N pin.
  At the rising edge of the RESET_N pin, if PG0 is "High" level, MCU enters single chip mode and boots from the on-chip flash memory.
  If PG0 is "Low" level, MCU enters single BOOT mode and boots from the internal BOOT ROM.

6.2. Unused Pins

We recommend that each unused pin should be connected to the power supply pin or GND pin via resistor.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.

6.3. Important Points of Using Debug Interface Pins Used as General-purpose Ports

After releasing reset, if the debug interface pins are used as the general I/O ports by the user program, the debug tool cannot be connected with MCU and control the MCU.

When the debug tool cannot debug the MCU, it can be connected with the MCU again by setting the MCU to the single BOOT mode and erasing the internal flash memory via the UART.

For details, refer to the reference manual "Flash memory".

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
1.0	2026-01-30	- First release

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**