32-Bit RISC Microcontroller

TXZ+ Family
TMPM4L Group (1)

Reference Manual
Clock Control and Operation Mode
(CG-M4L(1))

Revision 1.0

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC2	Advanced Encoder input Circuit 2
A-PMD2	Advanced Programmable Motor Control Circuit 2
A-VE2	Advanced Vector Engine 2
COMP	Comparator
DAC	Digital to Analog Converter
CG	Clock Control and Operation Mode
CRC	Cyclic Redundancy Check
D-Bus	DCode memory interface
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
EHOSC	External High-speed Oscillator
EI2C	I^2C Interface Version A
fsys	frequency of SYSTEM Clock
IA (INTIF)	Interrupt control register A
IB (INTIF)	Interrupt control register B
I-Bus	ICode memory interface
IHOSC	Internal High-speed Oscillator
IMN	Interrupt Monitor
INT	Interrupt
LVD	Voltage Detection Circuit
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
POR	Power-on Reset Circuit
PORF	Power-on Reset Circuit for FLASH and Debug
RAMP	RAM Parity
RLM	Power Supply Control/Reset
S-Bus	System interface
SAM	Secure Access Memory
SCOUT	Source Clock Output
SIWDT	Clock Selective Watchdog Timer
SMIF	Serial Memory Interface
TRGSEL	Trigger Selection Circuit
TRM	Trimming Circuit
TSPI	Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Asynchronous Serial Communication Circuit

1. Clock Control and Operation Mode

1.1. Outlines

The clock/mode control block can select a clock gear and prescaler clock and set the warming up of oscillator and so on.

Furthermore, this product has NORMAL mode and a low-power consumption mode as the operation mode in order to reduce power consumption by operation mode transition depending on the situation.

Functions related to a clock are as follows.

- System clock control
- Prescaler clock control

1.2. Clock Control

1.2.1. Clock Types

A list of clocks is shown below.

EHCLKIN:	The high-speed clock input from the external
fosc:	A clock generated in the internal oscillation circuit or input from the X1 and X2 pins after being selected by ***[CGOSCCR]***<OSCSEL>
f_{PLLREF}:	A clock selected by ***[CGSYSCR]***<PLLREFSEL[2:0]>
f_{PLL}:	A clock multiplied with PLL0
fc:	A clock selected by ***[CGPLL0SEL]***<PLL0SEL> (High-speed clock)
fsys:	A system clock selected by ***[CGSYSCR]***<GEAR[2:0]>
ΦT0:	A clock selected by ***[CGSYSCR]***<PRCK[3:0]> (Prescaler clock)
f_{IHOSC1}:	A clock generated with the internal high-speed oscillator 1
f_{IHOSC2}:	A clock generated with the internal high-speed oscillator 2
ADCLK:	A conversion clock for the ADC
TRCLKIN:	A clock for tracing facilities of a debugging circuit (Trace or SWV)

1.2.2. Initial State of Clock Setting by Reset

Each clock setting is initialized to the following states by reset.

External high-speed oscillator:	Stop
Internal high-speed oscillator 1:	Oscillation
Internal high-speed oscillator 2:	Stop
PLL (multiplying circuit):	Stop
Gear clock:	fc (no frequency dividing)

1.2.3. Clock System Diagram

The figure below shows a clock system diagram.

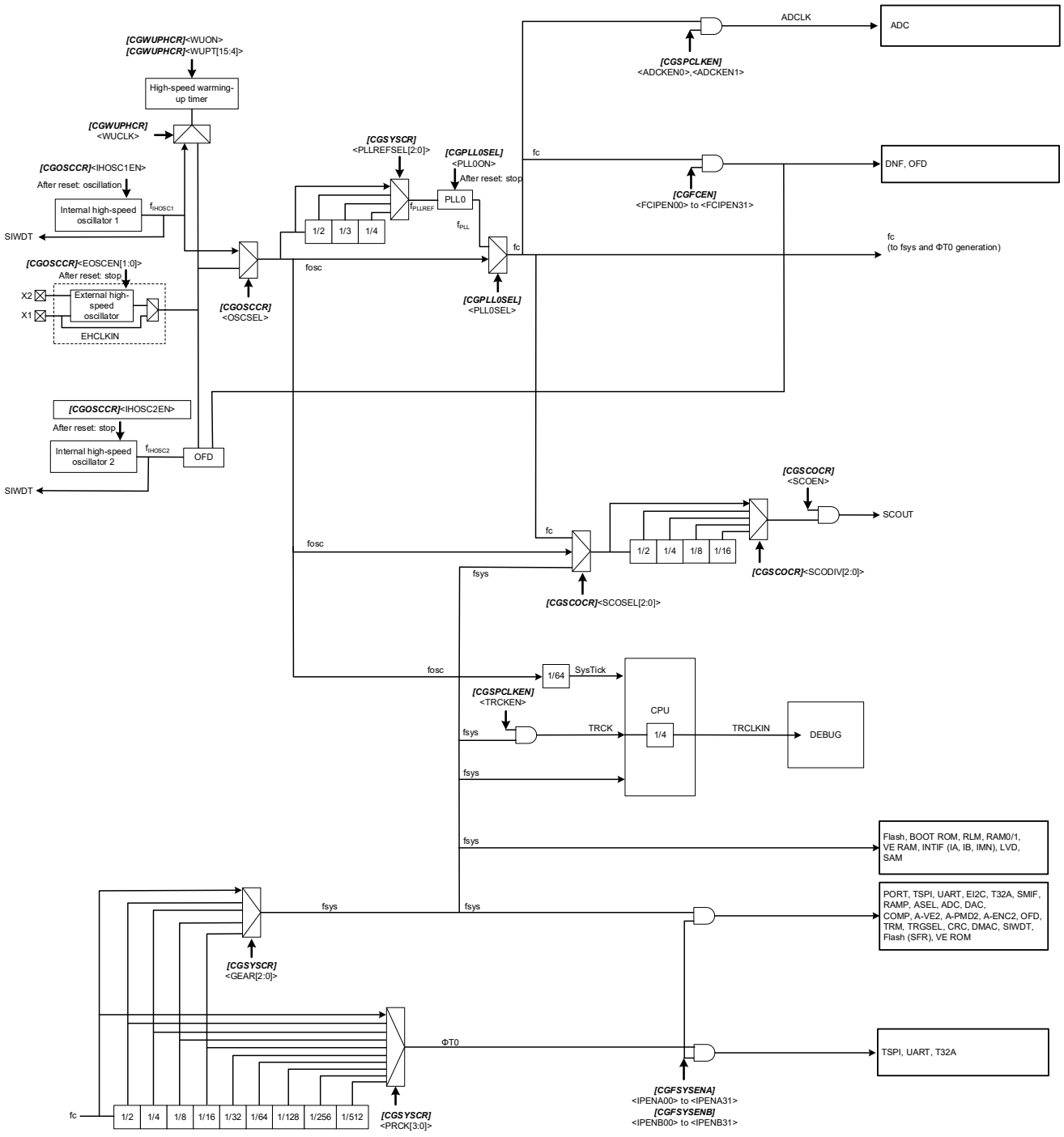

Figure 1.1 Clock System Diagram

1.2.4. Warming-up Function

The Warming-up function is to stabilize the oscillation of the oscillator.

1.2.4.1. Warming-up Timer for High-speed Oscillation

The warming-up timer has a built-in 16-bit warming-up timer. It is used when waiting for the stable oscillation of internal high-speed oscillator 1 and external high-speed oscillator.

It is used for waiting for the stable oscillation of internal oscillator 1 when an operation mode transits from STOP1 mode to NORMAL mode among mode transitions. Regarding of a detail description for releasing STOP1 mode, refer to "".

1.2.4.2. Setting Value of Warming-up Timer

The setting value of warming-up timer is as follows.

- For external high-speed oscillation
  The time for stable oscillation of an external high-speed oscillator is calculated using the following formula. The lower 4 bits of calculated value is rounded down and the upper 12 bits are set to ***[CGWUPHCR]***<WUPT[15:4]>.

  Setting value of warming timer (16 bits)
  = (warming-up time (s) / clock period (s)) - 16

  (Example) When 5 ms of warming-up time is set up with 10 MHz oscillator (clock period is 100 (ns))
  Warming-up timer setting value (16 bits) = (5ms / 100ns) - 16
  = 50000 - 16
  = 49984
  = 0xC340
  Since upper 12 bits are set, the below value is set.
  [CGWUPHCR]<WUPT[15:4]> = 0xC34

- For internal high-speed oscillator 1
  The time for stable oscillation of an internal high-speed oscillator 1 is a constant value. "0x000" is set to ***[CGWUPHCR]***<WUPT[15:4]>. The time for stable oscillation of internal oscillator 1 (about 160 (μs)) is set when the warming-up timer operates by this setting.

1.2.4.3. Directions for Use of Warming-up Timer

The directions for use of a warming-up timer are explained.

(1) Selection of clock
The clock counted by the warming-up timer is selected among a clock of internal oscillator 1 and one of external oscillator by ***[CGWUPHCR]***<WUCLK>.

The warming-up timer is used for a high-speed oscillation, the clock classification (internal oscillation or external oscillation) counted with a warming-up timer is selected by ***[CGWUPHCR]***<WUCLK>.

(2) Calculation of warming-up timer setting value
Regarding of calculating way of setting value to the warming-up time, refer to "1.2.4.2. Setting Value of Warming-up Timer". The calculated value is set to ***[CGWUPHCR]***<WUPT[15:4]>.

(3) Start warming-up timer and confirm completion of warming up
When software (Instruction) performs the start of warming-up timer and confirms completion of warming up, the followings are performed.
1. Set "1" to ***[CGWUPHCR]***<WUON> to start warming-up timer. Setting "0" to it doesn't perform the forced stop of warming timer. It is ignored.
2. Check ***[CGWUPHCR]***<WUEF> changing "1" → "0". When ***[CGWUPHCR]***<WUEF> is "1", the warming-up timer is under counting up. When it is "0", the warming up is completed. After completion, the warming-up timer is reset and initialized.

Note: Since a warming-up timer is operating with the oscillating clock, a warming-up time includes an error, when oscillation frequency has fluctuation. Therefore, it serves an approximate time.

1.2.5. Clock Multiplying Circuit (PLL)

The clock multiplying circuit outputs the f_{PLL} clock (up to 80MHz) multiplied by the optimum condition for the frequency of the PLL reference clock f_{PLLREF} (6MHz ≤ f_{PLLREF} < 12MHz) divided the output clock fosc of the high-speed oscillator.

It is possible to make the frequency of an oscillator low and to make the frequency of an internal clock high by this circuit.

1.2.5.1. PLL Setting after Reset Release

The PLL is disabled after reset release.

In order to use the PLL, select the PLL reference clock by ***[CGSYSCR]***<PLLREFSEL[2:0]> and set ***[CGPLL0SEL]***<PLL0SET[23:0]> to a multiplication value while ***[CGPLL0SEL]***<PLL0ON> is "0". Then wait until approximately 100 µs as a PLL initialization time. And set <PLL0ON> to "1" to start PLL operation. Then, the f_{PLL} clock which is multiplied fosc can be used by setting ***[CGPLL0SEL]*** <PLL0SEL> to "1" after waiting for approximately 100 µs as a lock up time.

Regarding of PLL reference clock selection, refer to "Table 1.1 Selection of PLL Reference Clock (f_{PLLREF})".

Table 1.1 Selection of PLL Reference Clock (f_{PLLREF})

fosc frequency (MHz)	Dividing ratio	f_{PLLREF} frequency (MHz)
6 ≤ fosc < 12	1 / 1	6 ≤ f_{PLLREF} < 12
12 ≤ fosc < 18	1 / 2	6 ≤ f_{PLLREF} < 9
18 ≤ fosc < 24	1 / 3	6 ≤ f_{PLLREF} < 8
24 = fosc	1 / 4	6 = f_{PLLREF}

1.2.5.2. Formula and Example of Setting Value for PLL Multiplication

The details of the items of ***[CGPLL0SEL]***<PLL0SET[23:0]> which set up a PLL multiplication are shown below.

Table 1.2 Details of Setting Value to *[CGPLL0SEL]*<PLL0SET[23:0]>

Items of PLL0SET	Function		
[23:17]	Correction value setting	The quotient of f_{PLLREF} / 340000 (integer part). Refer to Table 1.3.	
[16:14]	f_{PLLREF} setting	000: $6 \leq f_{PLLREF} \leq 7$ 001: $7 < f_{PLLREF} \leq 8$ 010: $8 < f_{PLLREF} \leq 10$ 011: $10 < f_{PLLREF} < 12$ Others: Reserved (Unit: MHz)	
[13:12]	Dividing setting	00: Reserved 01: 1 / 2 (Divided by 2) 10: 1 / 4 (Divided by 4) 11: 1 / 8 (Divided by 8)	
[11:8]	Fraction part of multiplication value	0000: 0.0000 0001: 0.0625 0010: 0.1250 0011: 0.1875 0100: 0.2500 0101: 0.3125 0110: 0.3750 0111: 0.4375	1000: 0.5000 1001: 0.5625 1010: 0.6250 1011: 0.6875 1100: 0.7500 1101: 0.8125 1110: 0.8750 1111: 0.9375
[7:0]	Integer part of multiplication value	0x00: 0 0x01: 1 0x02: 2 : 0xFD: 253 0xFE: 254 0xFF: 255	

Note: A multiplication value is the total of <PLL0SET[7:0]> (integer part) and <PLL0SET[11:8]> (fraction part).

f_{PLL} is calculated by the following formula.

$f_{PLL} = f_{PLLREF} \times$ (***[CGPLL0SEL]***<PLL0SET[7:0]> + ***[CGPLL0SEL]***<PLL0SET[11:8]>) ×
[CGPLL0SEL]<PLL0SET[13:12]>

Note1: The absolute value of frequency accuracy is not guaranteed.
Note2: There is no linearity in the frequency by the fraction part of multiplication value.
Note3: $f_{PLL} \leq$ Maximum operating frequency

Table 1.3 PLL Correction Value (Example)

f_{PLLREF} (MHz)	<PLL0SET[23:17]> (decimal, integral value)
6.00	18
8.00	24
10.00	30

The PLL correction value can be calculated by following formula.

When f_{PLLREF} is 6.0 MHz, the correction value is 6 / 0.34 = 17.64 → 18; A fraction part is rounded up.

The major examples of a setting value to ***[CGPLL0SEL]***<PLL0SET[23:0]> are shown below.

The target clock frequency (f_{PLL}) is generated from input frequency (f_{PLLREF}). The f_{PLLREF} is multiplied and divided by PLL.

A dividing ratio is chosen from 1 / 2, 1 / 4, and 1 / 8.
Moreover, the multiplied frequency must be within the following ranges.

100 MHz ≤ fPLLREF × Multiplication value ≤ 200 MHz

Table 1.4 Example of PLL0SET Setting Value

f_{PLLREF} (MHz)	Multiplication value	Dividing ratio	f_{PLL} (MHz)	<PLL0SET[23:0]>
6.00	26.625	1 / 2	79.88	0x241A1A
8.00	20.0000	1 / 2	80.00	0x305014
10.00	16.0000	1 / 2	80.00	0x3C9010

1.2.5.3. Change of PLL Multiplication Value under Operating

It changes to a setup which sets "0" to ***[CGPLL0SEL]***<PLL0SEL> first and does not use a PLL multiplication clock operation when changing a multiplication value while the PLL multiplication clock is using. And ***[CGPLL0SEL]***<PLL0ST> = 0 is read, after checking having changed to a setup which does not use a multiplication clock, ***[CGPLL0SEL]***<PLL0ON> is set to "0", and PLL is stopped.

Then, the multiplication value of ***[CGPLL0SEL]***<PLL0SET> is changed, ***[CGPLL0SEL]***<PLL0ON> is set to "1" after about 100μs as initialize time of PLL, and operation of PLL is started.

Then, ***[CGPLL0SEL]***<PLL0SEL> is set to "1" after about 100μs as lock-up time.

Finally, ***[CGPLL0SEL]***<PLL0ST> is read and it checks having changed.

1.2.5.4. Procedures of Switching Starting and Stopping PLL Operation

(1) fc setting (PLL operation stopped → PLL operation started)

The example of switching procedure from the state of PLL operation stopped to the state of PLL operation started is as follows for the fc.

<< State before switching >>	
[CGPLL0SEL]<PLL0ON> = 0	The PLL operation is stopped.
[CGPLL0SEL]<PLL0SEL> = 0	The fosc is selected (PLL is unused.).
[CGPLL0SEL]<PLL0ST> = 0	The status of the clock selection indicates that the fosc is selected (PLL is unused.).
[CGSYSCR]<PLLREFSEL[2:0]> = 000	fosc is selected as PLL reference clock (f_{PLLREF}).

<< Example of switching procedure >>		
1	***[CGSYSCR]***<PLLREFSEL[2:0]> = xxx	Select the divided fosc as f_{PLLREF}.
2	***[CGPLL0SEL]***<PLL0SET[23:0]> = 0xXXX	Set PLL multiplication value (0xXXX).
3	Wait 100 μs or more.	Wait for the initialization time after a PLL multiplication value is set.
4	***[CGPLL0SEL]***<PLL0ON> = 1	Start the PLL operation.
5	Wait 100 μs or more.	Wait for the PLL output clock stable time (as lock-up time).
6	***[CGPLL0SEL]***<PLL0SEL> = 1	Select the f_{PLL}.
7	***[CGPLL0SEL]***<PLL0ST> is read.	Wait until the selection status changes under using PLL (***[CGPLL0SEL]***<PLL0ST> = 1).

Note: Procedure 1 to 5 are not required when the state before switching is ***[CGPLL0SEL]***<PLL0ON> = 1.
When switching from the state of PLL operation stopped to the state of PLL operation started while the PLL output clock is stable, only procedure 6 and 7 are required.

(2) fc setting (PLL operation oscillated → PLL operation stopped)

The example of switching procedure from the state of PLL operation oscillated to the state of PLL operation stopped is as follows for the fc.

<< State before switching >>	
[CGPLL0SEL]<PLL0ON> = 1	The PLL operation is oscillated.
[CGPLL0SEL]<PLL0SEL> = 1	The f_{PLL} is selected (PLL is used.).
[CGPLL0SEL]<PLL0ST> = 1	The status of the clock selection indicates that the f_{PLL} is selected (PLL is used).

<< Example of switching sequence >>		
1	***[CGPLL0SEL]***<PLL0SEL> = 0	Select the fosc (PLL is unused.).
2	***[CGPLL0SEL]***<PLL0ST> is read.	Wait until the selection status changes under not using PLL (***[CGPLL0SEL]***<PLL0ST> = 0).
3	***[CGPLL0SEL]***<PLL0ON> = 0	Stop the PLL operation.

1.2.6. System Clock

An internal high-speed oscillation clock and external high-speed oscillation clock (connected oscillator or clock input) can be used as a source of system clock.

The fc divided by setting of ***[CGSYSCR]***<GEAR[2:0]> can be used as a system clock. This is called as clock gear. Although a setting of clock gear can be changed during operation, after setting register before a clock actually changes, up to 16-clock time is required of fc. Check completion of a clock change by ***[CGSYSCR]***<GEARST[2:0]>.

Note: Do not change a clock gear during operation of peripheral functions, such as a timer counter.

1.2.6.1. Procedure of Setting System Clock

(1) fosc setting (Internal oscillator → External oscillator)

The example of switching procedure from the internal high-speed oscillator 1 (IHOSC1) to the external high-speed oscillator (EHOSC) is as follows for the fc.

<< State before switching >>	
[CGOSCCR]<IHOSC1EN> = 1	The internal high-speed oscillator 1 is oscillated.
[CGOSCCR]<OSCSEL> = 0	The internal high-speed oscillator 1 (IHOSC1) is selected as the high-speed oscillator for fosc.
[CGOSCCR]<OSCF> = 0	The oscillator selection status for fosc indicates that the internal high-speed oscillator 1 (IHOSC1) is selected.
An oscillator is connected to X1/X2 pin. (Note)	-

Note: Do not connect any devices except a oscillator.

<< Example of switching procedure >>		
1	***[PHPDN]***<bit[1:0]> = 00 ***[PHIE]***<bit[1:0]> = 00 ***[PHCR]***<bit[1:0]> = 00 ***[PHOD]***<bit[1:0]> = 00 ***[PHFR6]***<bit1> = 0 ***[PHFR7]***<bit1> = 0 ***[PHFR8]***<bit0> = 0	Disable pull-down resistors of X1 and X2 pins. Disable input control of X1 and X2 pins. Disable output control of X1 and X2 pins. Disable open-drain control of X1 and X2 pins. Function register 6 is set as the PORT. Function register 7 is set as the PORT. Function register 8 is set as the PORT.
2	***[CGOSCCR]***<EOSCEN[1:0]> = 01	Select an external high-speed oscillator as using an external high-speed oscillator (EHOSC).
3	***[CGWUPHCR]***<WUCLK> = 1 ***[CGWUPHCR]***<WUPT[15:4]> = arbitrary value	Use the clock of external high-speed oscillator (EHOSC) as the source clock of warming-up timer. Set the arbitrary value as oscillator stable time to warming-up timer.
4	***[CGWUPHCR]***<WUON> = 1	Start the warming-up timer.
5	***[CGWUPHCR]***<WUEF> is read.	Wait until warming-up operation is completed (***[CGWUPHCR]***<WUEF> = 0)
6	***[CGOSCCR]***<OSCSEL> = 1	Select the external high-speed oscillator (EHOSC) as oscillator for fosc.
7	***[CGOSCCR]***<OSCF> is read.	Wait until the status of the oscillator selection for fosc becomes that an external oscillator (EHOSC) is selected. (***[CGOSCCR]***<OSCF> = 1)
8	***[CGOSCCR]***<IHOSC1EN> = 0	Stop the internal high-speed oscillator 1.

(2) fosc setting (Internal oscillation → External clock input)

The example of switching procedure from the internal high-speed oscillator 1 (IHOSC1) to the external clock input (EHCLKIN) is as follows for the fc.

<< State before switching >>	
[CGOSCCR]<IHOSC1EN> = 1	The internal high-speed oscillator 1 is oscillated.
[CGOSCCR]<OSCSEL> = 0	The internal high-speed oscillator 1 (IHOSC1) is selected as the high-speed oscillator for fosc.
[CGOSCCR]<OSCF> = 0	The oscillator selection status for fosc indicates that the internal high-speed oscillator 1 (IHOSC1) is selected.
Input clock to EHCLKIN	Voltage level of clock must be within the proper voltage range.

<< Example of switching procedure >>		
1	***[PHPDN]***<bit[0]> = 0 ***[PHIE]***<bit[0]> = 0/1 ***[PHCR]***<bit[0]> = 0 ***[PHOD]***<bit[0]> = 0	Disable pull-down resistor of X1/EHCLKIN. The input control of X1/EHCLKIN pin is arbitrary. Disable output control of X1/EHCLKIN. Disable open-drain control of X1/EHCLKIN.
2	***[CGOSCCR]***<EOSCEN[1:0]> = 10	Select an external high-speed oscillator as using an external clock input pin (EHCLKIN).
3	***[CGOSCCR]***<OSCSEL> = 1	Select the external high-speed oscillator (EHOSC) as oscillator for fosc.
4	***[CGOSCCR]***<OSCF> is read.	Wait until the status of the oscillator selection for fosc becomes that an external oscillator (EHOSC) is selected. (***[CGOSCCR]***<OSCF> = 1)
5	***[CGOSCCR]***<IHOSC1EN> = 0	Stop the internal high-speed oscillator 1.

(3) fosc setting (External oscillator or external clock input → Internal oscillator)

The example of switching procedure from the external high-speed oscillator (EHOSC) or external clock input (EHCLKIN) to the internal high-speed oscillator 1 (IHOSC1).

<< State before switching >>	
[CGOSCCR]<EOSCEN[1:0]> = 01 or 10	The external high-speed oscillator (EHOSC) or the external clock input pin (EHCLKIN) is selected as oscillator for fosc.
[CGOSCCR]<OSCSEL> = 1	The external high-speed oscillator (EHOSC) is selected as the high-speed oscillator for fosc.
[CGOSCCR]<OSCF> = 1	The oscillator selection status for fosc indicates that the external high-speed oscillator (EHOSC) is selected.

<< Example of switching procedure >>		
1	***[CGWUPHCR]***<WUCLK>= 0	Use the clock of internal high-speed oscillator (IHOSC1) as the source clock of warming-up timer.
2	***[CGWUPHCR]***<WUPT[15:4]> = 0x000	Set "0x000" as oscillator stable time to warming-up timer.
3	***[CGOSCCR]***<IHOSC1EN> = 1	Start the internal high-speed oscillator 1.
4	***[CGWUPHCR]***<WUON> = 1	Start the warming-up timer.
5	***[CGWUPHCR]***<WUEF> is read.	Wait until warming-up operation is completed (***[CGWUPHCR]***<WUEF> = 0)
6	***[CGOSCCR]***<OSCSEL> = 0	Select the internal high-speed oscillator 1 (IHOSC1) as oscillator for fosc.
7	***[CGOSCCR]***<OSCF> is read.	Wait until the status of the oscillator selection for fosc becomes that an internal high-speed oscillator (IHOSC1) is selected. (***[CGOSCCR]***<OSCF> = 0)
8	***[CGOSCCR]***<EOSCEN[1:0]> = 00	Select external high-speed oscillator as using no external high-speed oscillator.

1.2.7. Clock Supply Setting Function

TMPM4L Group (1) has the clock supply supply/stop function for the peripheral circuits. To reduce the power consumption, it can stop supplying the clock to the peripheral functions that are not used.

Except some peripheral functions, clocks of the peripheral functions are not supplied after releasing reset.

In order to supply the clock of the peripheral function to be used, set the corresponding bit of ***[CGFSYSENA]***, ***[CGFSYSENB]***, ***[CGFCEN]*** and ***[CGSPCLKEN]*** to "1".

For details, refer to "1.4 Explanation of Register".

1.2.8. Clock Output Function

TMPM4L Group (1) has the clock output function to the pin. The high-speed oscillation clock "fosc", high-speed clock "fc", system clock "fsys" can be output from the SCOUT pin.

For details, refer to "1.4.2.5. *[CGSCOCR]* (SCOUT Output Control Register)".

The below table shows the use propriety state of SCOUT pin in each operation mode.

Table 1.5 List of Use Propriety in Each Operation Mode

SCOUT selection	Operation mode		
	NORMAL/IDLE mode	STOP1 mode	STOP2 mode
fosc	✓	-	-
fc	✓	-	-
fsys	✓	-	-

Note: ✓: available, -: not available

1.2.9. Prescaler Clock

Each peripheral function has a prescaler circuit to divide the ΦT0 clock. The ΦT0 clock which is input into the prescaler circuit can be divided by the divide rate specified by the ***[CGSYSCR]***<PRCK[3:0]>.

After releasing reset, fc is selected as ΦT0.

After writing register, the time of up to 512 fc clocks is required before a clock actually changes.

To confirm the completion of the clock change, check the status of ***[CGSYSCR]***<PRCKST[3:0]>.

Note: Do not change a prescaler clock during operation of peripheral functions, such as a timer counter.

1.3. Operation Mode

TMPM4L Group (1) has NORMAL mode and low-power consumption modes (IDLE, STOP1 and STOP2) as the operation mode. The power consumption can be reduced by changing operation mode according to directions for use.

1.3.1. Details of Operation Mode

1.3.1.1. Feature in Each Operation Mode

The feature in NORMAL and low-power consumption modes are as follows.

- NORMAL mode

  The CPU core and peripheral functions operate in the NORMAL mode. After releasing reset, TMPM4L Group (1) operates in NORMAL mode.

- Low-power consumption mode

  The feature in low-power consumption modes is as follows.

  – IDLE mode
  The CPU stops in the IDLE mode.
  The peripheral functions should perform operating or stopping by the register of each peripheral function, such as the clock supply setting function, etc.

Note: Note that the CPU cannot clear the watchdog timer in IDLE mode.

  – STOP1 mode
  All internal circuits including the internal oscillators stop.
  If the STOP1 mode is released, the internal high-speed oscillator 1 (IHOSC1) starts oscillation, and TMPM4L Group (1) returns to the NORMAL mode.
  Disable the interrupts which are not used for STOP1 release before transition to the STOP1 mode.

  – STOP2 mode
  It is the mode which holds a part of the function and cut off an internal electrical power source. STOP1 Consumption of electric power larger than the STOP2 mode can be held down. If the STOP2 mode is released, the power supply will be switched on to the main power domain, a reset sequence will be performed, and it will return to NORMAL mode.
  As for the main power domain, it is a function which does not supply a power supply in STOP2 mode.

Regarding of state of peripheral functions in the low-power consumption mode, refer to "1.3.1.4. Operation Status of Peripheral Functions in Low-power Consumption Mode".

1.3.1.2. Transition to and Return from Low-power Consumption Mode

In order to transit to each low-power consumption mode, the IDLE, STOP1, or STOP2 mode is selected by the standby control register ***[CGSTBYCR]***<STBY[1:0]>, and a WFI (Wait For Interrupt) command is executed. When the transition to the low-power consumption mode has been performed by WFI instruction, the returning from the low-power consumption mode can be performed by the reset or the interrupt generation. To return by interrupt, the preparation for releasing the low-power consumption mode is required beforehand. Refer to "Interrupts" chapter of the reference manual "Exception" for details.

Note1: TMPM4L Group (1) does not support a return by events; therefore, do not perform a transition to low-power consumption mode by WFE (Wait For Event).

Note2: TMPM4L Group (1) does not support low-power consumption mode by SLEEPDEEP of the Cortex-M4 (with FPU) processor core. Do not use the <SLEEPDEEP> bit of the system control register.

1.3.1.3. Selection of Low-power Consumption Mode

The low-power consumption mode is selected by ***[CGSTBYCR]***<STBY[1:0]>.
Following table shows the mode selected by <STBY[1:0]>.

Table 1.6 Low-power Consumption Mode Selection

Low-power consumption Mode	*[CGSTBYCR]*<STBY[1:0]>
IDLE mode	00
STOP1 mode	01
STOP2 mode	10

Note: Do not use the settings other than the above.

1.3.1.4. Operation Status of Peripheral Functions in Low-power Consumption Mode

The following Table 1.7 shows the operating status of the peripheral functions (block) in each operation mode.
In addition, after releasing reset, the clock supply status of the peripheral functions except some peripheral functions is not supplied.
If needed, set ***[CGFSYSENA]***, ***[CGFSYSENB]***, ***[CGFCEN]***, and ***[CGSPCLKEN]*** to enable clock supply.

Table 1.7 Operating Status of Peripheral Functions in Each Low-power Consumption Mode

Block		NORMAL mode	IDLE mode	STOP1 mode	STOP2 mode (Note1)
Processor core (including Debug)		✓	-	-	#
DMAC		✓	✓	-	#
I/O port	Pin state of PORT	✓	✓	✓	✓ (Note3)
	Registers	✓	✓	-	#
ADC		✓	✓	-	#
ASEL		✓	✓	-	#
DAC		✓	✓	-	#
COMP		✓	✓	-	#
UART		✓	✓	-	#
EI2C		✓	✓	-	#
TSPI		✓	✓	-	#
SMIF		✓	✓	-	#
A-PMD2		✓	✓	-	#
A-VE2		✓	✓	-	#
A-ENC2		✓	✓	-	#
T32A		✓	✓	-	#
TRGSEL		✓	✓	-	#
SAM		✓	✓	-	#
CRC		✓	✓	-	#
SIWDT		✓	✓ (Note2)	-	-
LVD		✓	✓	✓	✓
OFD		✓	✓	-	#
TRM		✓	N/A	-	#
CG		✓	✓	✓	#
PLL		✓	✓	-	#
RAM parity (RAMP)		✓	✓	-	#
External high-speed oscillator (EHOSC)		✓	✓	-	#
Internal high-speed oscillator 1 (IHOSC1)		✓	✓	-	#
Internal high-speed oscillator 2 (IHOSC2)		✓	✓	-	#
RLM		✓	✓	✓	✓
IA		✓	✓	✓	✓
IB		✓	✓	✓	#
DNF		✓	✓	✓	#
Flash		Can be accessed	Can be accessed (Note4)	Hold	Hold
RAM					#
VE RAM					#

✓: This peripheral function can be operated.

-: A clock to this peripheral function is stopped automatically after operation mode is transited to the target low-power consumption mode.

#: A power supply to this peripheral function is shut down automatically after operation mode is transited to the target low-power consumption mode. After returning to NORMAL mode, they are initialized by reset.

Note1: After confirming that the peripheral is stopped, operation mode is transited to the STOP2 mode.

Note2: Protect A mode only. In other cases, stop SIWDT before transiting to IDLE mode.

Note3: The state of PORTs, when ***[RLMSHTDNOP]***<PTKEEP> is set to "1", are held. The drive capacity of ports whose drive capacity can be selected is set to 1 mA not depending on setting of ***[DRVCR0]*** and ***[DRVCF1].***

Note4: Data is held when the peripheral functions which are access (read or write) (such as DMA, etc.) except CPU are not connected on the bus matrix.

1.3.2. Operation Mode State Transition

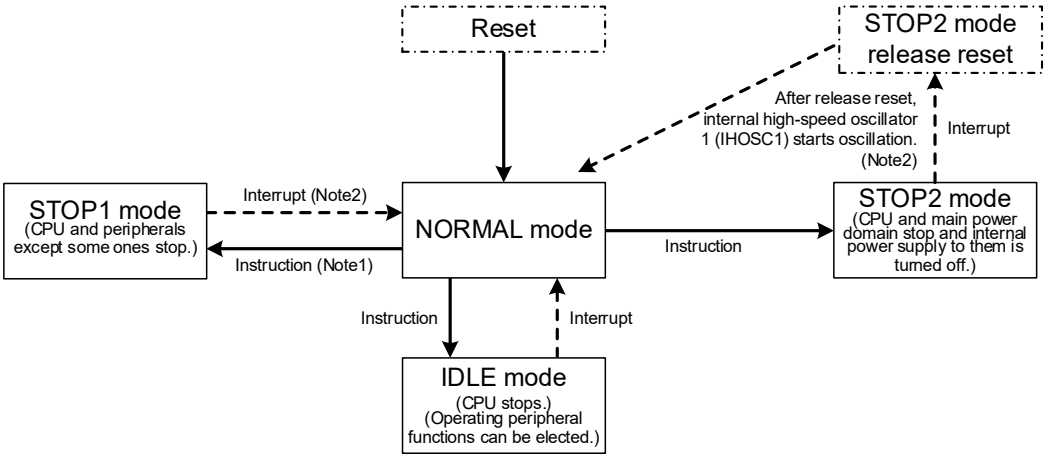

Figure 1.2 Operation Mode State Transition

Note1: Warming up is required at returning. A warming-up time must be set in the previous operation mode (NORMAL mode) before transiting to the STOP1 mode.

Note2: When TMPM4L Group (1) returns from STOP2 mode, it branches to the interrupt routine of reset. When it returns from the STOP1 mode, it branches to the service routine of interrupt source.

1.3.2.1. IDLE Mode Transition Flow

Perform the following procedure when transiting to the IDLE mode.

Because the IDLE mode is released by the interrupt, set the interrupt source setting before transiting to the IDLE mode. For the interrupts that can be used to release the IDLE mode, refer to "1.3.3.1. Release Source of Low-power Consumption Mode". Disable interrupts which do not use for releasing the IDLE mode and ones which cannot be used.

Transition flow (from NORMAL mode)		
1	***[SIWDxEN]***<WDTE> = 0	Disable SIWDT.
2	***[SIWDxCR]***<WDCR[7:0]> = 0xB1	Disable SIWDT.
3	***[FCSR0]***<RDYBSY> is read.	Wait until the Flash memory is Ready state (= 1).
4	***[CGSTBYCR]***<STBY[1:0]> = 00	Low-power consumption mode selection is set to IDLE mode.
5	***[CGSTBYCR]***<STBY[1:0]> is read.	Check that the value written in step 4 can be read.
6	WFI command execution	Transit to IDLE mode.

Note: When using the protect A mode of SIWDT, step 1 and 2 are not required.

1.3.2.2. STOP1 Mode Transition Flow

Perform the following procedure when transiting to STOP1 mode.

Because the STOP1 mode is released by an interrupt, set the interrupt source setting before transiting to STOP1 mode. For the interrupts that can be used to release the STOP1 mode, refer to "1.3.3.1. Release Source of Low-power Consumption Mode". Disable interrupts which do not use for releasing the STOP1 mode and ones which cannot be used.

Transition flow (from NORMAL mode)		
1	***[SIWDxEN]***<WDTE> = 0	Disable SIWDT.
2	***[SIWDxCR]***<WDCR[7:0]> = 0xB1	Disable SIWDT.
3	***[FCSR0]***<RDYBSY> is read.	Wait until the Flash memory is Ready state (= 1).
4	***[CGWUPHCR]***<WUEF> is read.	Wait until the warming-up operation is completed. (***[CGWUPHCR]*** <WUEF> = 0)
5	***[CGWUPHCR]***<WUCLK> = 0	Use the clock of internal high-speed oscillator (IHOSC1) as the source clock of warming-up timer.
	[CGWUPHCR]<WUPT[15:4]> = 0x000	Set "0x0000" to warming-up timer.
6	***[CGSTBYCR]***<STBY[1:0]> = 01	Low-power consumption mode selection is set to STOP1 mode.
7	***[CGPLL0SEL]***<PLL0SEL> = 0	Select the fosc (PLL is unused.).
8	***[CGPLL0SEL]***<PLL0ST> is read.	Wait until the selection status changes under not using PLL ([CGPLL0SEL]<PLL0ST> = 0).
9	***[CGPLL0SEL]***<PLL0ON> = 0	Stop the PLL operation.
10	***[CGOSCCR]***<IHOSC1EN> = 1	Start the internal high-speed oscillator 1.
11	***[CGWUPHCR]***<WUON> = 1	Start the warming-up timer.
12	***[CGWUPHCR]***<WUEF> is read.	Wait until the warming-up operation is completed. (***[CGWUPHCR]*** <WUEF> = 0)
13	***[CGOSCCR]***<OSCSEL> = 0	Select the internal high-speed oscillator 1 (IHOSC1) as oscillator for fosc.
14	***[CGOSCCR]***<OSCF> is read.	Wait until the status of the oscillator selection for fosc becomes that IHOSC1 is selected. (***[CGOSCCR]***<OSCF> = 0)
15	***[CGOSCCR]***<EOSCEN[1:0]> = 00	Use the external oscillator (EHOSC) as no oscillator.
16	***[CGOSCCR]***<IHOSC2EN> = 0	Stop the internal high-speed oscillator 2 (IHOSC2).
17	***[CGOSCCR]***<EOSCEN[1:0]> is read.	Check that the value written in step 15 can be read.
18	***[CGOSCCR]***<IHOSC2F> is read.	Wait until the stability flag of internal oscillation for IHOSC2 becomes "0".
19	WFI command execution	Transit to STOP1 mode.

1.3.2.3. STOP2 Mode Transition Flow

Set up the following procedure at transition to STOP2.

Because STOP2 mode is released by an interrupt, set the interrupt before transition STOP2 mode. For the interrupts that can be used to release the STOP2 mode, refer to "1.3.3.1. Release Source of Low-power Consumption Mode". Disables unused interrupts and unavailable interrupts for release STOP2.

Transition procedure (from NORMAL mode)		
1	***[SIWDxEN]***<WDTE> = 0	Disable SIWDT.
2	***[SIWDxCR]***<WDCR[7:0]> = 0xB1	Disable SIWDT.
3	***[FCSR0]***<RDYBSY> is read.	Wait until Flash becomes the Ready state (= 1).
4	[RLMSHTDNOP]<PTKEEP> = 1	IO control signal is made to hold.
5	***[CGSTBYCR]***<STBY[1:0]> = 10	Low-power consumption mode selection is set to STOP2 mode.
6	***[CGPLL0SEL]***<PLL0SEL> = 0	Select the PLL to "PLL is unused (fosc)".
7	***[CGPLL0SEL]***<PLL0ST> is read.	Wait until the PLL selection status for fsys becomes PLL unused. (= 0).
8	***[CGPLL0SEL]***<PLL0ON> = 0	Stop PLL for fsys.
9	[CGWUPHCR]<WUCLK> = 0 ***[CGWUPHCR]***<WUPT[15:4]> = 0x000	Set the warming-up clock selection to internal high-speed oscillator 1 (IHOSC1). Set "0x0000" to warming-up timer.
10	***[CGOSCCR]***<IHOSC1EN> = 1	Enable the internal high-speed oscillator 1.
11	***[CGWUPHCR]***<WUON> = 1	Start the high-speed oscillation warming-up timer
12	***[CGWUPHCR]***<WUEF> is read.	Wait until the warming-up timer status flag becomes ends (= 0).
13	***[CGOSCCR]***<OSCSEL> = 0	Set the high-speed oscillation selection for fosc to internal high-speed oscillator1 (IHOSC1).
14	***[CGOSCCR]***<OSCF> is read.	Wait until the high-speed oscillation selection status for fosc becomes internal high-speed oscillator1 (IHOSC1) (= 0).
15	***[CGOSCCR]***<EOSCEN[1:0]> = 00	Set the selection of an external oscillator operation to unused.
16	***[CGOSCCR]***<IHOSC2EN> = 0	The internal high-speed oscillator 2 is stopped.
17	***[CGOSCCR]***<EOSCEN[1:0]> is read.	The register writing of step 15 is checked (= 00).
18	***[CGOSCCR]***<IHOSC2F> is read.	Wait until the internal oscillation stable flag of the internal high-speed oscillator 2 becomes zero.
19	***[RLMRSTFLG0]***<STOP2RSTF> = 0 ***[RLMRSTFLG0]***< PINRSTF> = 0	A STOP2 mode reset flag/reset pin flag is cleared (Note).
20	WFI command execution	Transit to STOP2 mode.
21	Jump instruction	Return to step 20.

Note: Refer to the Reference Manual "Exception" for a reset flag register ***[RLMRSTFLG0]***.

1.3.3. Return from Low-power Consumption Mode

1.3.3.1. Release Source of Low-power Consumption Mode

The interrupt, non-maskable interrupt, and reset can perform return from a low-power consumption mode. The source which can be used to release the low-power consumption mode is depending on the low-power consumption mode.

For details, the following table is shown.

Table 1.8 List of Release Source

Low-power consumption mode			IDLE mode	STOP1 mode	STOP2 mode
Release source	Interrupt	INT00 to 20	✓	✓	✓
		INTT32A00ACCAP, INTT32A00BCAP, INTT32A01ACCAP, INTT32A01BCAP, INTT32A02ACCAP, INTT32A02BCAP, INTT32A03ACCAP, INTT32A03BCAP, INTT32A04ACCAP, INTT32A04BCAP, INTDMAATC, INTT32A00AC, INTT32A00B, INTT32A01AC, INTT32A01B, INTT32A02AC, INTT32A02B, INTT32A03AC, INTT32A03B, INTT32A04AC, INTT32A04B	✓	-	-
		INTVCN0, INTEMG0, INTOVV0, INTPWM0, INTENC00, INTENC01, INTCOMP0, INTCOMP1, INTCOMP2, INTCOMP3, INTCOMP4, INTCOMP5	✓	-	-
		INTADAPDA, INTADAPDB, INTADACP0, INTADACP1, INTADATRG, INTADASGL, INTADACNT, INTADBPDA, INTADBPDB, INTADBCP0, INTADBCP1, INTADBTRG, INTADBSGL, INTADBCNT	✓	-	-
		INTT0RX, INTT0TX, INTT0ERR, INTT1RX, INTT1TX, INTT1ERR, INTT2RX, INTT2TX, INTT2ERR	✓	-	-
		INTUART0RX, INTUART0TX, INTUART0ERR, INTUART1RX, INTUART1TX, INTUART1ERR, INTUART2RX, INTUART2TX, INTUART2ERR, INTUART3RX, INTUART3TX, INTUART3ERR, INTUART4RX, INTUART4TX, INTUART4ERR, INTUART5RX, INTUART5TX, INTUART5ERR	✓	-	-
		INTSMI0, INTI2C0BF, INTI2C0AL, INTI2C0, INTI2C1BF, INTI2C1AL, INTI2C1,	✓	-	-
		INTPARI, INTDMAAERR, INTFLCRDY	✓	-	-
	SysTick interrupt		✓	-	-
	Non-Maskable Interrupt (INTWDT0)		✓ (Note)	-	-
	Non-Maskable Interrupt (INTLVD)		✓	✓	✓
	Reset (SIWDT)		✓ (Note)	-	-
	Reset (LVD)		✓	✓	✓
	Reset (OFD)		✓	-	-
	Reset (SAM)		✓	-	-
	Reset (RESET_N pin)		✓	✓	✓

✓: After release the low-power consumption mode, the interrupt procedure will start.

-: It cannot be used for release the low-power consumption mode.

Note: Protected A mode only. In other cases, stop SIWDT before transition to IDLE mode.

- Released by an interrupt request

  When the interrupt request releases the low-power consumption mode, it is necessary to prepare so that interrupt request may be detected by the CPU. It is necessary that the interrupt request used for releasing STOP1 may be detected by the CPU and INTIF.

- Released by Non-Maskable Interrupt (NMI)

  The SIWDT interrupt (INTWDT0, Protect A mode only.) and the LVD interrupt (INTLVD) for the NMI sources can perform release from the low-power consumption mode.

- Released by reset

  The reset can perform release from all the low-power consumption modes.
  When released by reset, TMPM4L Group (1) operates in the NORMAL mode and it's registers will be initialized after releasing reset. For details, refer to "3.2.7.1. Reset Factors and Initialized Range".

- Released by SysTick interrupt

  SysTick interrupt can be used only in the IDLE mode.

Refer to "Interrupt" chapter of the reference manual "Exception" for details of interrupt.

1.3.3.2. Warming-up when Releasing Low-power Consumption Mode

Warming up may be required for the stability of internal circuits when the operation mode transits.
When the transition from STOP1 mode to NORMAL mode is performed, the internal oscillation is selected as the source clock of the warming-up timer automatically and the warming-up timer is started. A system clock is output after warming-up time is elapsed.

For this reason, before executing the command which the operation mode transits to the STOP1 mode by, set warming-up time to ***[CGWUPHCR]***<WUPT[15:4]>. For the setting value, refer to "1.2.4.3. Directions for Use of Warming-up Timer".

The following table shows the necessity of a warming-up setting at the time of each operation mode transition.

Table 1.9 Warming-up Time Setting

Operation mode transition	Warming-up setting
NORMAL → IDLE	Not required
NORMAL → STOP1	Not required
NORMAL → STOP2	Not required
IDLE → NORMAL	Not required
STOP1 → NORMAL	Required (automatic warming up)
STOP2 → RESET → NORMAL	Not required

1.3.3.3. Restart Operation from STOP2 Mode

The restart operation flow from STOP2 mode release factor interrupt generating is as follows.

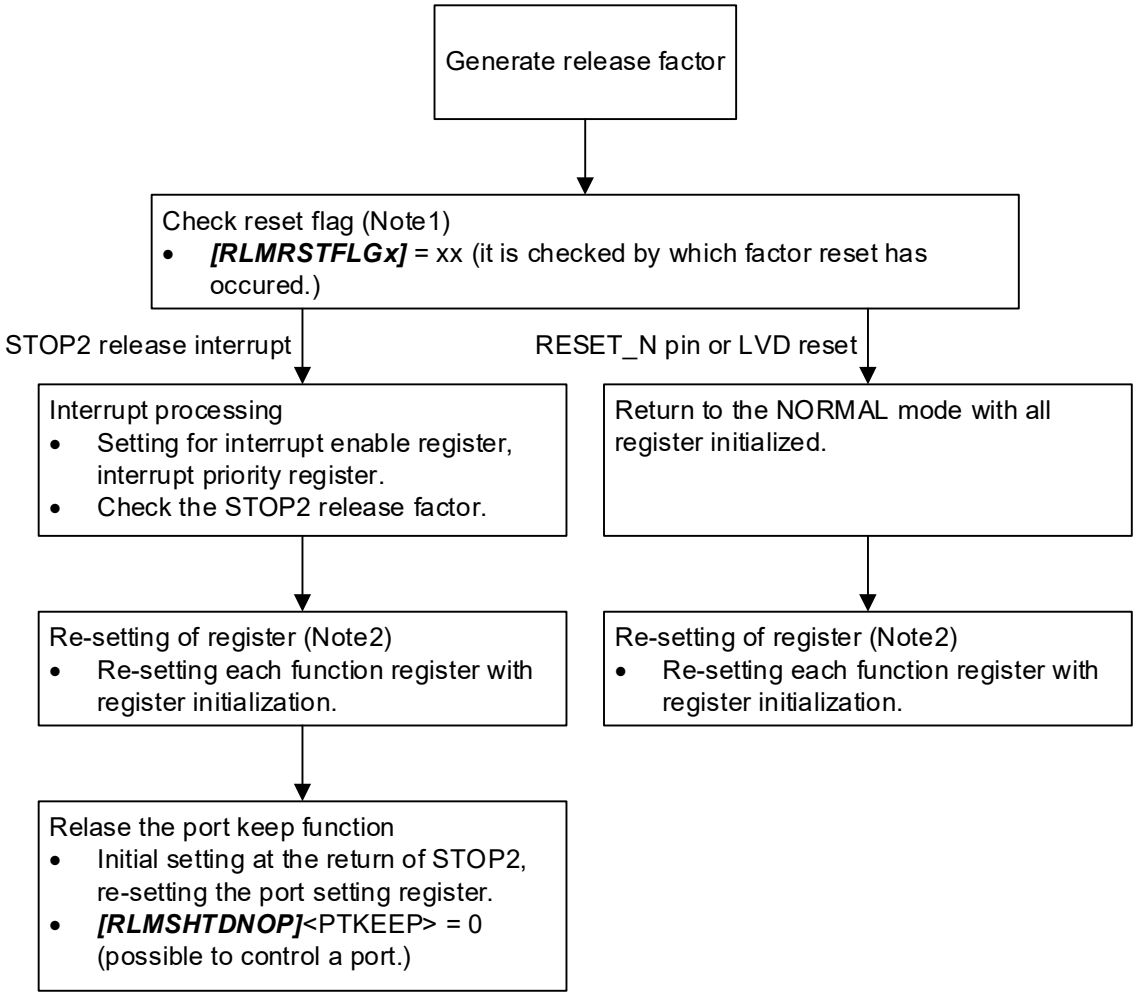

Figure 1.3 STOP2 Mode Restart Operation Flow

Note1: When STOP2 mode is released by RESET_N pin, as for a reset flag, both "STOP2 reset flag" and "reset pin flag" are materialized.

Note2: When STOP2 mode is released by LVD reset, as for a reset flag, both "STOP2 reset flag" and "reset pin flag" are materialized.

Note3: Register reset area is differ depending on the releasing STOP2 mode by an interrupt and the releasing STOP2 mode by the reset of RESET_N pin or LVD. Refer to "3.2.7.1. Reset Factors and Initialized Range of Circuits" for register reset area by each factor.

1.4. Explanation of Register

1.4.1. Register list

The register related to CG and its address information is shown below.

Peripheral function		Channel/unit	Base address
Clock control and operation mode	CG	–	0x40083000
Power control/reset	RLM	–	0x4003E400

1.4.1.1. Clock Control and Operation Mode

Register name		Address (Base+)
CG Write Protection Register	***[CGPROTECT]***	0x0000
Oscillation Control Register	***[CGOSCCR]***	0x0004
System Clock Control Register	***[CGSYSCR]***	0x0008
Standby Control Register	***[CGSTBYCR]***	0x000C
SCOUT Output Control Register	***[CGSCOCR]***	0x0010
PLL Selection Register	***[CGPLL0SEL]***	0x0020
High-speed Oscillation Warming-up Register	***[CGWUPHCR]***	0x0030
Clock Supply and Stop Register A for fsys	***[CGFSYSENA]***	0x0050
Clock Supply and Stop Register B for fsys	***[CGFSYSENB]***	0x0054
Clock Supply and Stop Register for fc	***[CGFCEN]***	0x0058
Clock Supply and Stop Register for ADC and Debug Circuit	***[CGSPCLKEN]***	0x005C

1.4.1.2. Power Control/reset

Register name		Address (Base+)
Power Supply Cut Off Control Register	***[RLMSHTDNOP]***	0x0001
RLM Write Protection Register	***[RLMPROTECT]***	0x000F

Note: Byte accessible registers. Bit band access cannot be performed.

1.4.2. Detail of Registers

1.4.2.1. *[CGPROTECT]* (CG Write Protection Register)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0".
7:0	PROTECT[7:0]	0xC1	R/W	Control write-protection for the CG register (all registers included except this register) 0xC1: CG registers are write-enabled. (Protect disabled) Other than 0xC1: Sets write protection (Protect enabled)

1.4.2.2. *[CGOSCCR]* (Oscillation Control Register)

Bit	Bit symbol	After reset	Type	Function
31:20	-	0	R	Read as "0".
19	IHOSC2F	0	R	Stability flag of internal oscillation for IHOSC2 0: Stopping or being in warming up 1: Stable oscillation
18:17	-	0	R	Read as "0".
16	IHOSC1F	1	R	Stability flag of internal oscillation for IHOSC1 (Note4) 0: Stopping or being in warming up 1: Stable oscillation
15:13	-	0	R	Read as "0".
12	-	0	R/W	Write as "0".
11:10	-	0	R	Read as "0".
9	OSCF	0	R	High-speed oscillator for fosc selection status. 0: Internal high-speed oscillator1 (IHOSC1) 1: External high-speed oscillator (EHOSC)
8	OSCSEL	0	R/W	Selection high-speed oscillation for fosc (Note1) 0: Internal high-speed oscillator1 (IHOSC1) 1: External high-speed oscillator (EHOSC)
7:4	-	0	R	Read as "0".
3	IHOSC2EN	0	R/W	Internal high-speed oscillator2 (IHOSC2) control (Note 2) 0: Stop 1: Oscillation
2:1	EOSCEN[1:0]	00	R/W	Selection operation of external high-speed oscillator (EHOSC) (Note3) 00: External high-speed oscillator is not used 01: Use as external high-speed oscillator (EHOSC) 10: Use as external clock input (EHCLKIN) 11: Reserved
0	IHOSC1EN	1	R/W	Internal high-speed oscillator1 (IHOSC1) control 0: Stop 1: Oscillation

Note1: When the setting is modified, confirm that the written value can be read from ***[CGOSCCR]***<OSCF> before executing the next operation.

Note2: Setting cannot be changed, when ***[SIWDxOSCCR]***<OSCPRO> is "1" (Write protection of SIWDT is enabled).

Note3: When EHOSC is used as the oscillator connection pin, set these bits to "01" (use as external high-speed oscillator).

Note4: To wait stabilizing oscillation of the internal high-speed oscillator1 (IHOSC1), use a warming-up timer and confirm ***[CGWUPHCR]***<WUEF> instead of <IHOSC1F>.

1.4.2.3. *[CGSYSCR]* (System Clock Control Register)

Bit	Bit symbol	After reset	Type	Functions
31:28	-	0	R	Read as "0".
27:24	PRCKST[3:0]	0000	R	Prescaler clock (ΦT0) selection status 0000: fc 0100: fc / 16 1000: fc / 256 0001: fc / 2 0101: fc / 32 1001: fc / 512 0010: fc / 4 0110: fc / 64 1010 to 1111: Reserved 0011: fc / 8 0111: fc / 128
23:19	-	0	R	Read as "0".
18:16	GEARST[2:0]	000	R	Selection status of the gear ratio of the system clock (fsys). 000: fc 100: fc / 16 001: fc / 2 101 to 111: Reserved 010: fc / 4 011: fc / 8
15:12	-	0	R	Read as "0".
11:8	PRCK[3:0]	0000	R/W	Select prescaler clock (ΦT0). 0000: fc 0100: fc / 16 1000: fc / 256 0001: fc / 2 0101: fc / 32 1001: fc / 512 0010: fc / 4 0110: fc / 64 1010 to 1111: Reserved 0011: fc / 8 0111: fc / 128 Selects a prescaler clock for the peripheral functions.
7:6	-	0	R/W	Write as "0".
5:3	PLLREFSEL[2:0]	000	R/W	Select PLL reference clock (f_{PLLREF}) 000: fosc 100 to 111: Reserved 001: fosc / 2 010: fosc / 3 011: fosc / 4
2:0	GEAR[2:0]	000	R/W	Select gear ratio of the system clock (fsys). 000: fc 100: fc / 16 001: fc / 2 101 to 111: Reserved 010: fc / 4 011: fc / 8

1.4.2.4. *[CGSTBYCR]* (Standby Control Register)

Bit	Bit symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1:0	STBY[1:0]	00	R/W	Select a low-power consumption mode. 00: IDLE 01: STOP1 10: STOP2 11: Reserved

1.4.2.5. *[CGSCOCR]* (SCOUT Output Control Register)

Bit	Bit symbol	After reset	Type	Functions
31:7	-	0	R	Read as "0".
6:4	SCODIV[2:0]	000	R/W	SCOUT division ratio selection (Note) 000: No dividing 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101 to 111: Reserved
3:1	SCOSEL[2:0]	000	R/W	SCOUT base clock selection (Note) 000: fosc 001: fc 010: Reserved 011: fsys 100 to 111: Reserved
0	SCOEN	0	R/W	SCOUT output enable control 0: Disabled 1: Enabled

Note: When "011: fsys" for SCOUT is selected by <SCOSEL[2:0]>, "000: No dividing" by <SCODIV[2:0]> cannot be selected.

1.4.2.6. *[CGPLL0SEL]* (PLL Selection Register)

Bit	Bit symbol	After reset	Type	Function
31:8	PLL0SET[23:0]	0x000000	R/W	PLL0 multiplication setting About a multiplication setting, refer to "1.2.5.2. Formula and Example of Setting Value for PLL Multiplication".
7:3	-	0	R	Read as "0".
2	PLL0ST	0	R	Clock selection status 0: fosc 1: f_{PLL}
1	PLL0SEL	0	R/W	Clock selection 0: fosc 1: f_{PLL}
0	PLL0ON	0	R/W	PLL operation 0: Stopped 1: Operated

1.4.2.7. *[CGWUPHCR]* (High-speed Oscillation Warming-up Register)

Bit	Bit symbol	After reset	Type	Function
31:20	WUPT[15:4]	0x800	R/W	Set the upper 12 bits of the 16 bits of calculation value of the warming-up timer. About setting of a warming-up timer, refer to "1.2.4.3. Directions for Use of Warming-up Timer".
19:16	WUPT[3:0]	0000	R/W	Set the lower 4 bits of the 16 bits of calculation value of the warming-up timer. It is fixed to "0000".
15:9	-	0	R	Read as "0".
8	WUCLK	0	R/W	Warming-up source clock selection (Note1) 0: Internal high-speed oscillator1 (IHOSC1) 1: External high-speed oscillator (EHOSC)
7:2	-	0	R	Read as "0".
1	WUEF	0	R	Status of the warming-up timer (Note2) 0: The end of warming-up operation 1: In warming-up operation
0	WUON	0	W	Warming-up timer control 0: Don't care 1: Warming-up operation start

Note1: Use the clock of internal high-speed oscillator 1 for warming up when the operation mode transits from STOP1 mode. Do not use the clock of external high-speed oscillator.

Note2: Do not modify the registers during the warming up (<WUEF> = 1). Set the registers when <WUEF> is "0".

1.4.2.8. *[CGFSYSENA]* (Clock Supply and Stop Register A for fsys)

Bit	Bit symbol	After reset	Type	Functions
31	IPENA31	0	R/W	T32A ch4 clock enable control 0: Stop clock. 1: Supply clock.
30	IPENA30	0	R/W	T32A ch3 clock enable control 0: Stop clock. 1: Supply clock.
29	IPENA29	0	R/W	T32A ch2 clock enable control 0: Stop clock. 1: Supply clock.
28	IPENA28	0	R/W	T32A ch1 clock enable control 0: Stop clock. 1: Supply clock.
27	IPENA27	0	R/W	T32A ch0 clock enable control 0: Stop clock. 1:Supply clock.
26	IPENA26	0	R/W	A-ENC2 ch0 clock enable control 0: Stop clock. 1: Supply clock.
25	IPENA25	0	R/W	A-PMD2 ch0 clock enable control 0: Stop clock. 1:Supply clock.
24	IPENA24	0	R/W	A-VE2 ch0 clock enable control 0: Stop clock. 1: Supply clock.
23	IPENA23	0	R/W	DMAC unit A clock enable control 0: Stop clock. 1: Supply clock.
22:9	-	0	R	Read as "0".
8	IPENA08	0	R/W	PORT J clock enable control 0: Stop clock. 1: Supply clock.
7	IPENA07	0	R/W	PORT H clock enable control 0: Stop clock. 1: Supply clock.
6	IPENA06	0	R/W	PORT G clock enable control 0: Stop clock. 1: Supply clock.
5	IPENA05	0	R/W	PORT F clock enable control 0: Stop clock. 1: Supply clock.
4	IPENA04	0	R/W	PORT E clock enable control 0: Stop clock. 1: Supply clock.
3	IPENA03	0	R/W	PORT D clock enable control 0: Stop clock. 1: Supply clock.
2	IPENA02	0	R/W	PORT C clock enable control 0: Stop clock. 1: Supply clock.
1	IPENA01	0	R/W	PORT B clock enable control 0: Stop clock. 1: Supply clock.
0	IPENA00	0	R/W	PORT A clock enable control 0: Stop clock. 1: Supply clock.

Note1: Even if the initial value of the register is set to clock stop, the clock is supplied during the reset.

Note2: Write "0" for bit of peripheral function that does not exist in each product.

1.4.2.9. *[CGFSYSENB]* (Clock Supply and Stop Register B for fsys)

Bit	Bit symbol	After reset	Type	Function
31	IPENB31	1	R/W	SIWDT ch0 clock enable control 0: Stop clock. 1: Supply clock.
30	-	0	R	Read as "0".
29	IPENB29	1	R/W	Write as "1"
28	-	0	R	Read as "0".
27	IPENB27	0	R/W	TRGSEL clock enable control 0: Stop clock. 1: Supply clock.
26	IPENB26	0	R/W	TRM clock enable control 0: Stop clock. 1: Supply clock.
25	IPENB25	0	R/W	OFD clock enable control 0: Stop clock. 1: Supply clock.
24	IPENB24	0	R/W	CRC clock enable control 0: Stop clock. 1: Supply clock.
23	IPENB23	0	R/W	RAM Parity clock enable control 0: Stop clock. 1: Supply clock.
22:18	-	0	R	Read as "0".
17	IPENB17	0	R/W	ASEL clock enable control 0: Stop clock. 1: Supply clock.
16	IPENB16	0	R/W	COMP clock enable control 0: Stop clock. 1: Supply clock.
15	IPENB15	0	R/W	DAC ch1 clock enable control 0: Stop clock. 1: Supply clock.
14	IPENB14	0	R/W	DAC ch0 clock enable control 0: Stop clock. 1: Supply clock.
13	IPENB13	0	R/W	ADC unit B clock enable control 0: Stop clock. 1: Supply clock.
12	IPENB12	0	R/W	ADC unit A clock enable control 0: Stop clock. 1: Supply clock.
11	IPENB11	0	R/W	EI2C ch1 clock enable control 0: Stop clock. 1: Supply clock.
10	IPENB10	0	R/W	EI2C ch0 clock enable control 0: Stop clock. 1: Supply clock.
9	IPENB09	0	R/W	UART ch5 clock enable control 0: Stop clock. 1: Supply clock.
8	IPENB08	0	R/W	UART ch4 clock enable control 0: Stop clock. 1: Supply clock.
7	IPENB07	0	R/W	UART ch3 clock enable control 0: Stop clock. 1: Supply clock.
6	IPENB06	0	R/W	UART ch2 clock enable control 0: Stop clock. 1: Supply clock.
5	IPENB05	0	R/W	UART ch1 clock enable control 0: Stop clock. 1: Supply clock.

Bit	Bit symbol	After reset	Type	Function
4	IPENB04	0	R/W	UART ch0 clock enable control 0: Stop clock. 1: Supply clock.
3	IPENB03	0	R/W	SMIF ch0 clock enable control 0: Stop clock. 1: Supply clock.
2	IPENB02	0	R/W	TSPI ch2 clock enable control 0: Stop clock. 1: Supply clock.
1	IPENB01	0	R/W	TSPI ch1 clock enable control 0: Stop clock. 1: Supply clock.
0	IPENB00	0	R/W	TSPI ch0 clock enable control 0: Stop clock. 1: Supply clock.

Note1: Even if the initial value of the register is set to clock stop, the clock is supplied during the reset.

Note2: Write "0" for bit of peripheral function that does not exist in each product.

1.4.2.10. *[CGFCEN]* (Clock Supply and Stop Register for fc)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0".
7	FCIPEN07	0	R/W	DNF clock enable control 0: Stop clock. 1: Supply clock.
6	FCIPEN06	0	R/W	Monitoring clock of OFD enable control 0: Stop clock. 1: Supply clock.
5:0	-	0	R	Read as "0".

Note: Even if the initial value of the register is set to clock stop, the clock is supplied during the reset.

1.4.2.11. *[CGSPCLKEN]* (Clock Supply Stop Register for ADC and Debug Circuit)

Bit	Bit symbol	After reset	Type	Function
31:18	-	0	R	Read as "0".
17	ADCKEN1	0	R/W	Enable the clock for ADC Unit B (Note2) 0: Clock stop 1: Clock supply
16	ADCKEN0	0	R/W	Enable the clock for ADC Unit A (Note2) 0: Clock stop 1: Clock supply
15:1	-	0	R	Read as "0".
0	TRCKEN	0	R/W	Enable the Clock for the Trace function of Debug circuit (Trace or SWV). 0: Clock stop 1: Clock supply

Note1: Even if the initial value of the register is set to clock stop, the clock is supplied during the reset.
Note2: When setting this bit to "0" (clock stop), make sure that AD conversion is stopped.

1.4.2.12. *[RLMSHTDNOP]* (Power Supply Cut Off Control Register)

Bit	Bit symbol	After reset	Type	Function
7	-	0	R/W	Write as "0".
6:5	-	0	R	Read as "0".
4	-	0	R/W	Write as "0".
3:1	-	0	R	Read as "0".
0	PTKEEP	0	R/W	I/O control signal holding control in STOP2 mode 0: Controlled by Port circuit 1: Held control signal at changing 0 → 1 This bit must be set before transition to STOP2 mode.

Note: Byte accessible registers. Bit band access cannot be performed.

1.4.2.13. *[RLMPROTECT]* (RLM Write Protection Register)

Bit	Bit symbol	After reset	Type	Function
7:0	PROTECT	0xC1	R/W	RLM register write protection control 0xC1: RLM register writing enabled (Protect disabled) Other than 0xC1: RLM register writing enabled (Protect enabled) Disable to write to [***RLMSHTDNOP***].

Note: Byte accessible registers. Bit band access cannot be performed.

2. Memory Map

2.1. Outlines

The memory maps for TMPM4L Group (1) are based on the Cortex-M4 (with FPU) processor core memory map.

The built-in ROM, built-in RAM and special function registers (SFR) of TMPM4L Group (1) are mapped to the Code, SRAM and peripheral regions of the Cortex-M4 (with FPU) respectively. The special function register (SFR) means the control registers of all input/output ports and peripheral functions.

Regarding the addresses of SFR, refer to the Reference Manual "Product Information".

The private peripheral bus is the processor core’s internal register region.

For more information on each region, refer to the " Arm Cortex-M4 Processor Technical Reference Manual".

Note that access to regions indicated as "Fault" causes a bus fault if bus faults are enabled, or causes a hard fault if bus faults are disabled. Also, do not access the vendor-specific region (Vender-Specific).

2.1.1. TMPM4LxFYA

- Code Flash: 256KB (Area0, Area1)
- RAM: 32KB
- Products: TMPM4L4FYAUG, TMPM4L2FYADUG, TMPM4L2FYAQG, TMPM4L1FYAUG

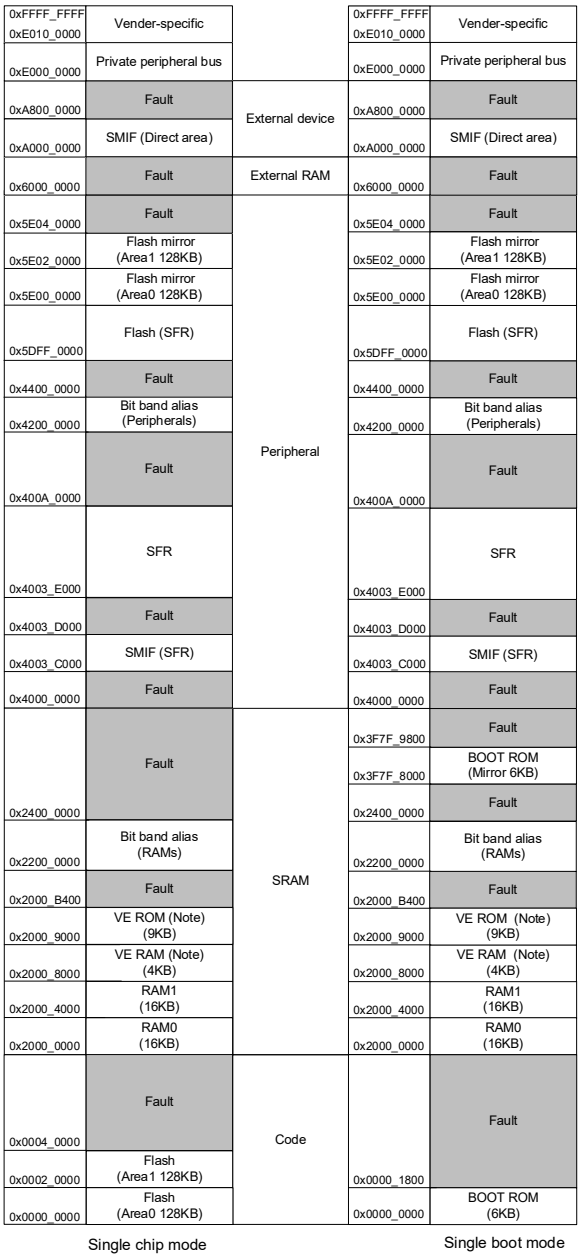

Figure 2.1 TMPM4LxFYA

Note: When ***[VExRAMTSKCONFG1]***<VERAMBUS> = 0, a bus manager can access VE RAM.
When ***[VExROMCONFG]***<VEROMBUS> = 0, a bus manager can access VE ROM.

2.1.2. TMPM4LxFWA

- Code Flash: 128KB (Area0)
- Data Flash: 64KB (Area1)
- RAM: 32KB
- Products: TMPM4L4FWAUG, TMPM4L2FWADUG, TMPM4L2FWAQG, TMPM4L1FWAUG

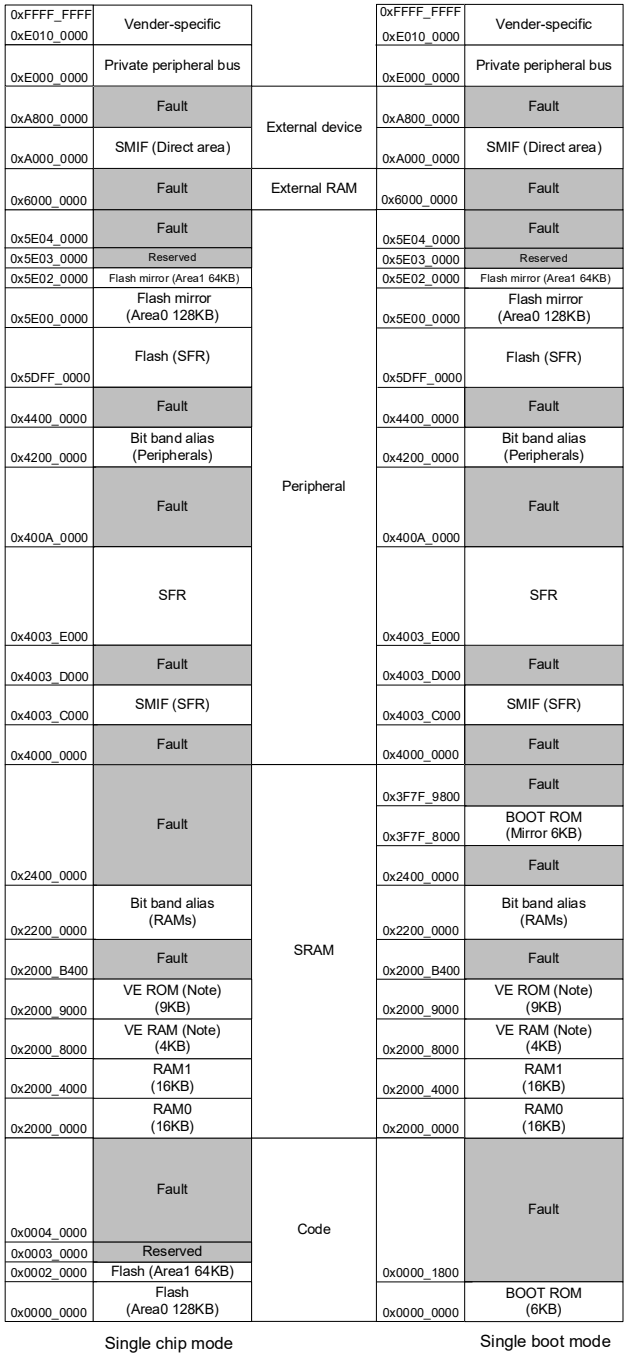

Figure 2.2 TMPM4LxFWA

Note: When ***[VExRAMTSKCONFG1]***<VERAMBUS> = 0, a bus manager can access VE RAM.
When ***[VExROMCONFG]***<VEROMBUS> = 0, a bus manager can access VE ROM.

2.2. Bus Matrix

TMPM4L Group (1) contains bus managers such as a CPU and DMA controller.

Bus managers connect to subordinate ports (S0 to S3) of Bus Matrix. In the bus matrix, manager ports (M0 to M13) connect to peripheral functions via connections described as (O or ●) in the following figure. "●" shows a connection to a mirror area.

While multiple subordinates are connected to the same bus manager line in the Bus Matrix, if multiple subordinate accesses are generated at the same time, a priority is given to access from a manager with the smallest subordinate number.

2.2.1. Configuration

2.2.1.1. Single Chip Mode

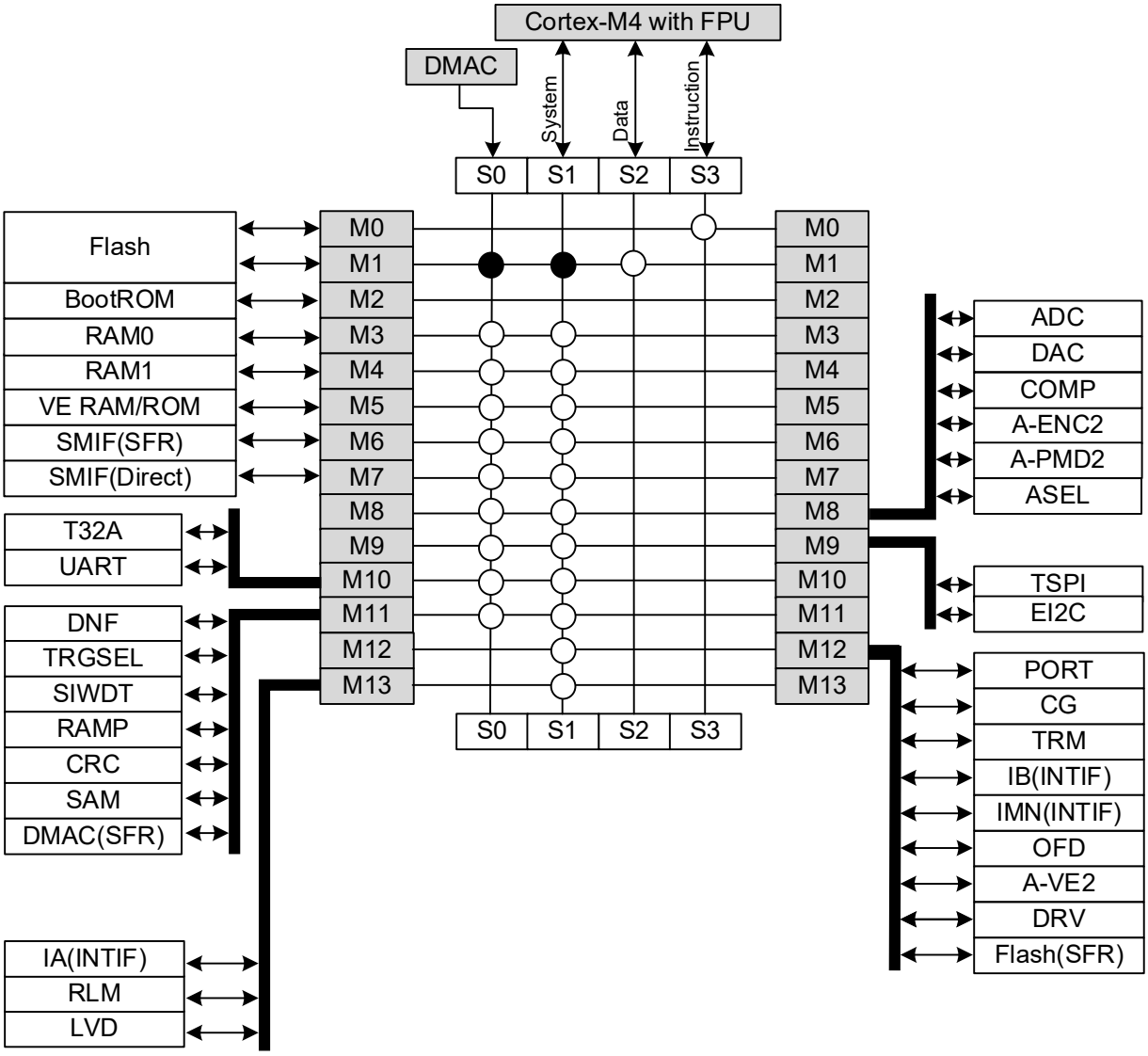

Figure 2.3 Single Chip Mode

2.2.1.2. Single Boot Mode

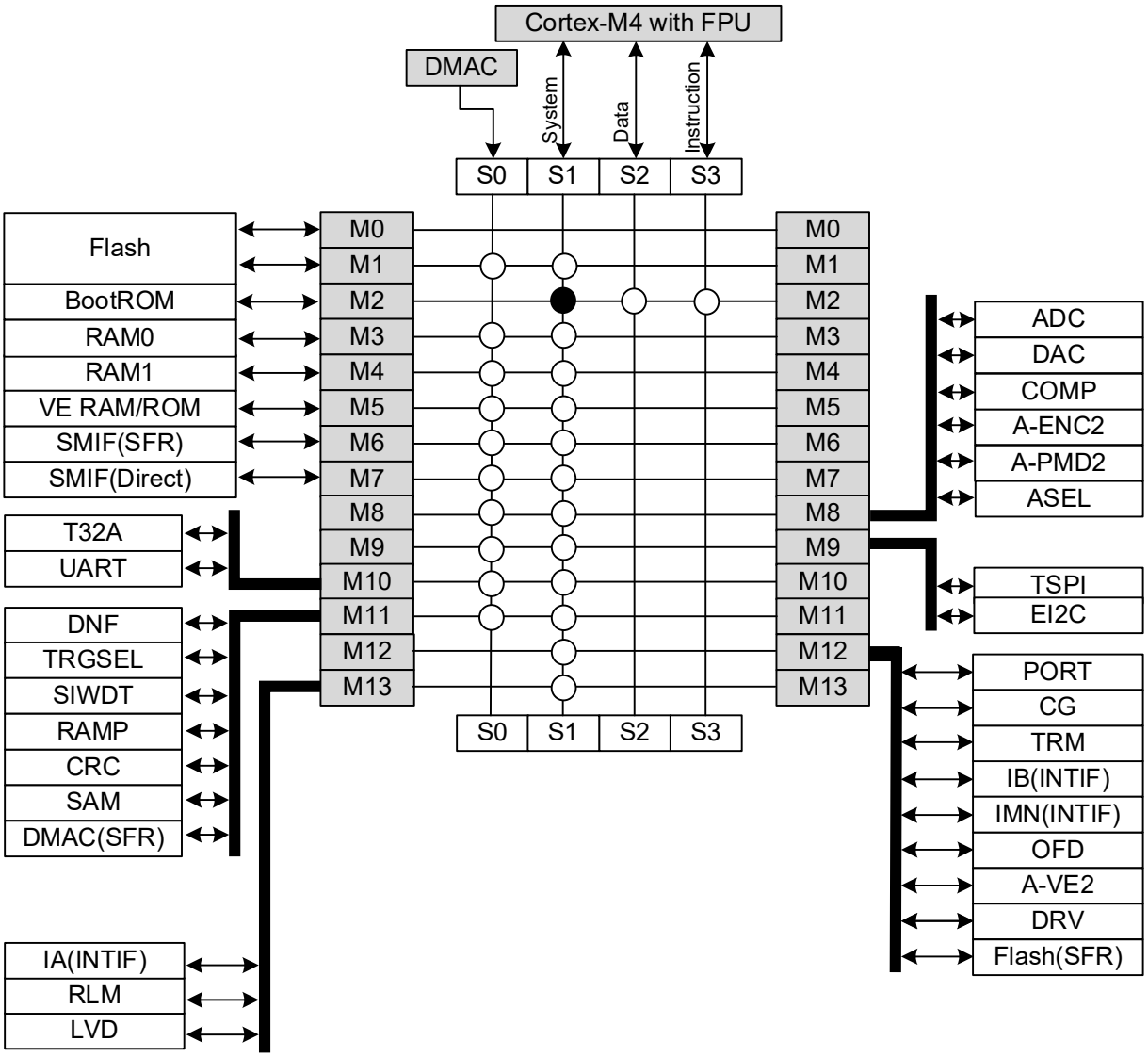

Figure 2.4 Single Boot Mode

3. Reset and Power Supply Control

3.1. Outlines

Function classification	Function	Operation description
Cold reset (Reset with turning on a power supply)	Power-on Reset	Reset which occurs at the time of a power supply turning on or turning off
	LVD reset	Reset which occurs when the voltage of power supply is the setting voltage or less
	Reset pin	Reset by a RESET_N pin
	PORF reset	Reset which occurs at the time of a power supply turning on or turning off PORF reset resets flash memory and debugging circuits with priority.
Warm reset (Reset without turning on a power supply)	Internal reset	Reset by SIWDT, OFD, LVD, LOCKUP, and <SYSRESETREQ>
	Reset pin	Reset by a RESET_N pin
Reset by releasing STOP2 mode	Interrupt	Reset to the main power domain (STOP2REQ) in returning from STOP2 mode
	LVD reset	Reset which occurs when the voltage of power supply is the setting voltage or less
	Reset pin	Reset by a RESET_N pin
Single boot starting	Reset pin	After reset is released, TMPM4L Group (1) starts from the internal boot ROM.

3.2. Description of Function and Operation

This chapter describes that the power supply turns on and turns off, and items related with the reset.

Note: Refer to "Electrical Characteristics" of a datasheet for the time and voltage of description of the symbol in a figure.
DVDD5 indicates a power supply pin for the digital circuit.

3.2.1. Cold Reset

When a power supply is turned on, the stabilization time for the built-in regulator, the built-in Flash memory, and the built-in high-speed oscillator is necessary. The TXZ+ family automatically inserts a wait time for the stabilization of these circuits.

When a power supply is turned on, make sure that the power supply voltage must be monotonically increased. If the power supply voltage drops and rises near the voltage level of POR and PORF detection/release voltage, it may not operate normally even if the power supply voltage rises to the guaranteed operating range thereafter.

3.2.1.1. Reset without Using RESET_N Pin

The LVD is enabled after initialization. Therefore, the LVD continuously resets TMPM4L Group (1) until a voltage of power supply exceeds the release voltage of LVD after releasing POR and PORF.
After releasing LVD reset, an internal reset is released after "Internal processing time" + "CPU operation wait time".

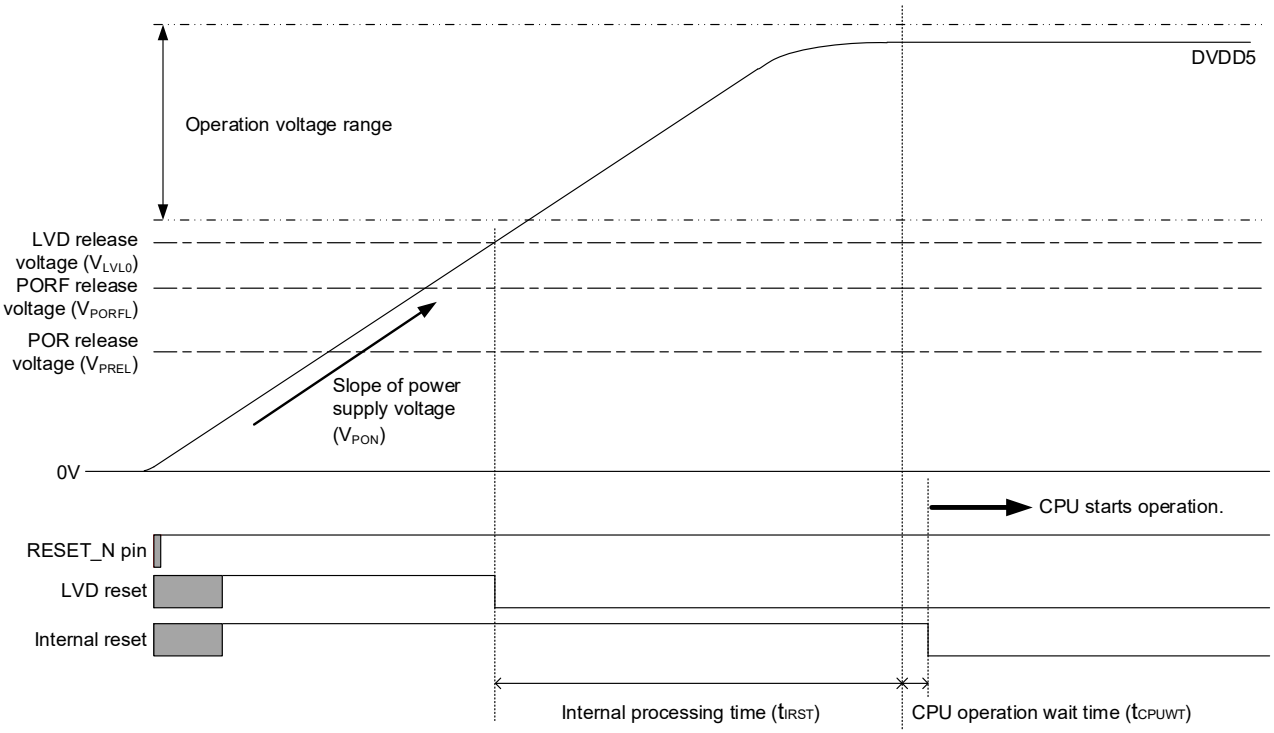

Figure 3.1 Reset without Using RESET_N Pin

Note: When the RESET_N pin is not used, "High" or opened level should be input to the RESET_N pin.

3.2.1.2. Reset by RESET_N Pin

When the power supply is turned on, the timing of reset release by using RESET_N pin can be controlled.

After a supply voltage exceeds the release voltage of the LVD and even after "Internal processing time" elapses, if the RESET_N pin is "Low", internal reset keeps asserting continuously. After a RESET_N pin becomes "High", the internal reset is released after "CPU operation wait time" has elapsed.

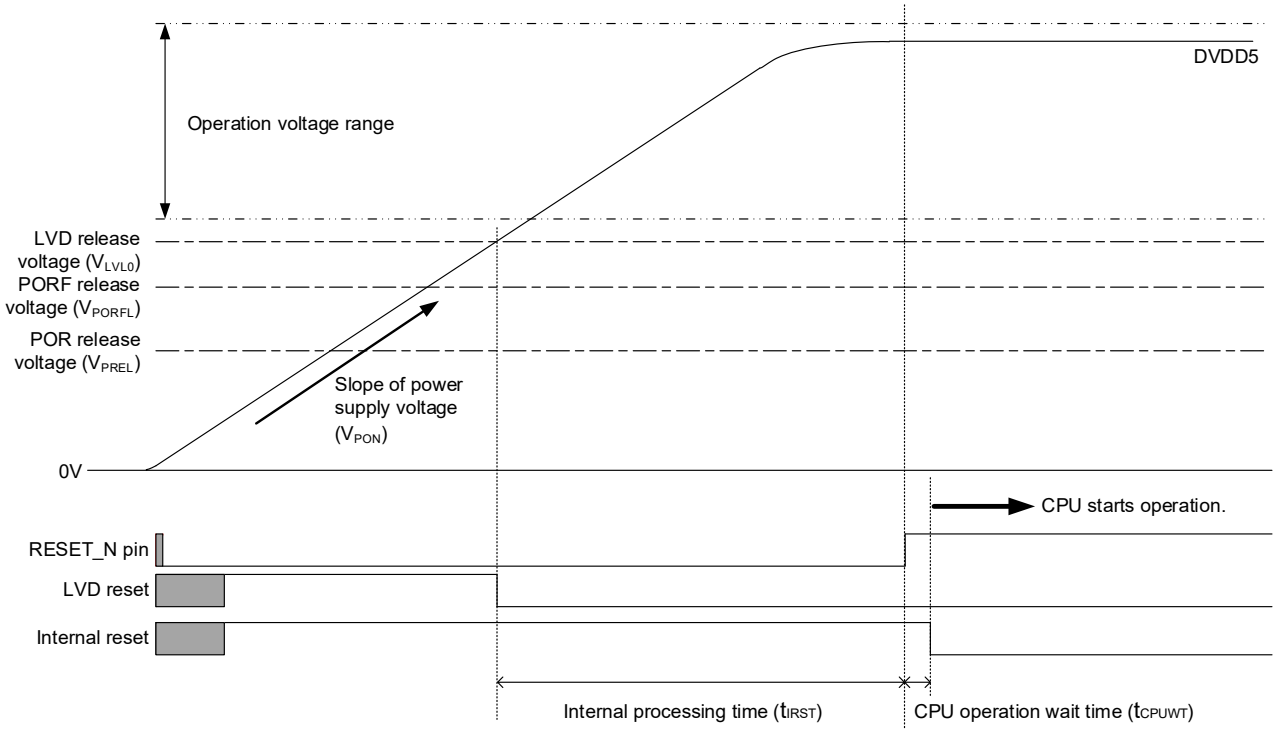

Figure 3.2 Reset by RESET_N pin (1)

If a RESET_N pin input change from "Low" to "High" during "Internal processing time", internal reset signal is released after "Internal processing time" + "CPU operation wait time" has elapsed.

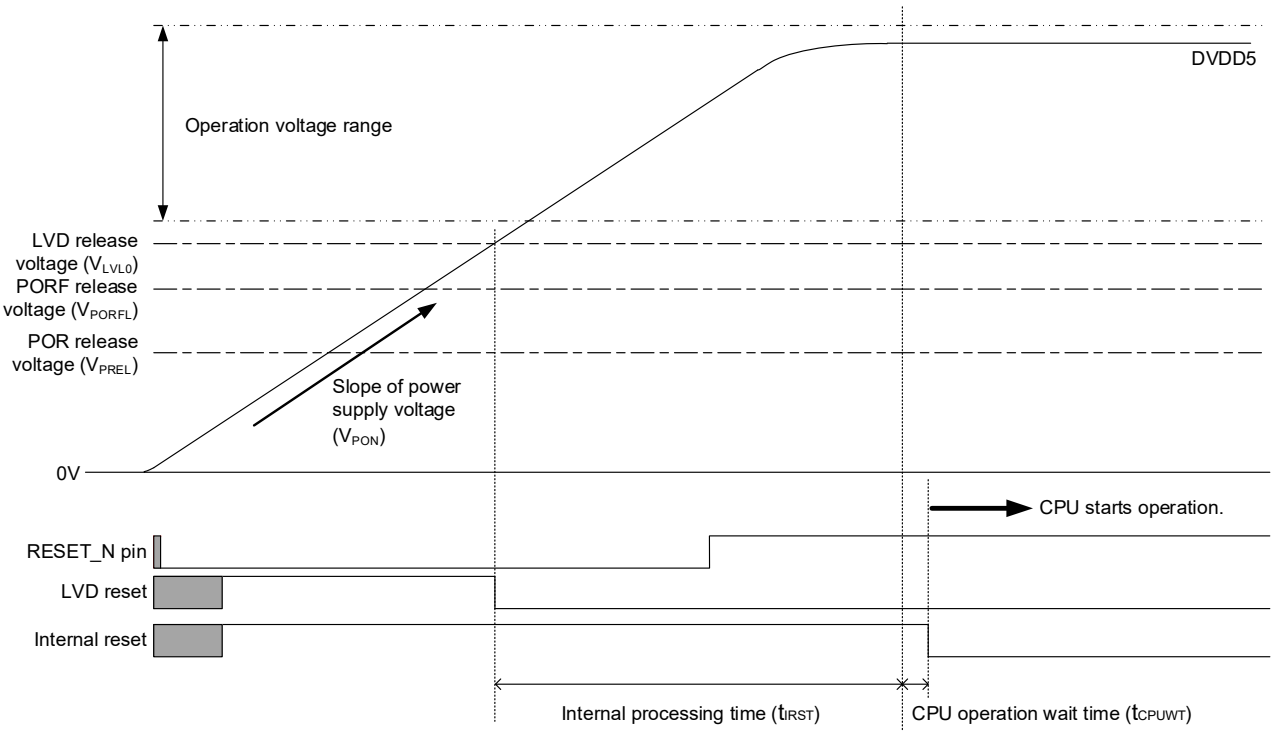

Figure 3.3 Reset by RESET_N Pin (2)

3.2.2. Warm Reset

3.2.2.1. Warm Reset by RESET_N Pin

When resetting with the RESET_N pin, set the RESET_N pin to "Low" for 17.2 µs or more while the power supply voltage is within the operating range.

When the "Low" period of the RESET_N pin is longer than "Internal processing time", after the RESET_N pin changes to "High", the internal reset is released after "CPU operation wait time" elapsed.

When the "Low" period of a RESET_N pin is shorter than "Internal processing time", a time of the internal reset is extended. It is released from a RESET_N pin changes to "Low" after "Internal processing time" + "CPU operation wait time" has elapsed.

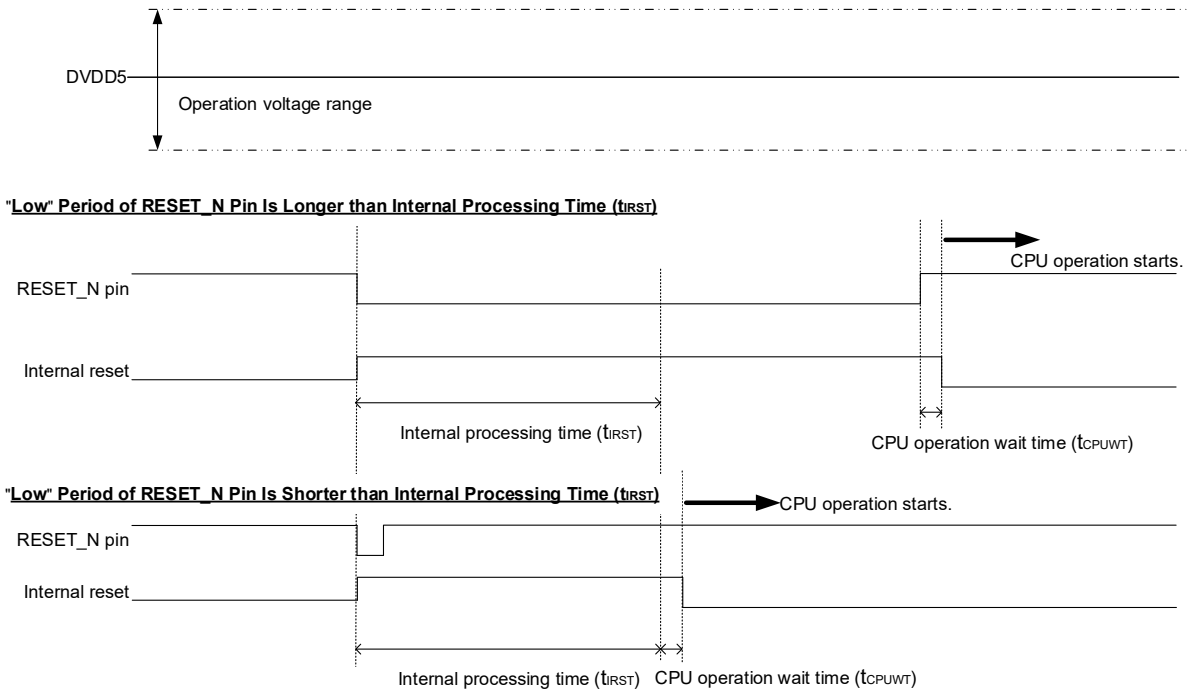

Figure 3.4 Warm Reset Operation

3.2.2.2. Warm Reset by LVD

If the period when a voltage of power supply is LVD detection/release voltage or less is longer than "Internal processing time", an internal reset is released after "Internal processing time". If it is shorter than "Internal processing time", an internal reset is released after "Internal processing time" + "CPU operation wait time".

3.2.2.3. Warm Reset by Other Internal Resets

When the reset by internal source, such as SIWDT, OFD, SAM, LOCKUP, and <SYSRESETREQ> occurs, the internal reset is released after "Internal processing time" + "CPU operation wait time" has elapsed.

3.2.3. Reset with Releasing STOP2 Mode

When a RESET_N pin changes "Low" or a LVD reset occurs, the STOP2 mode is released. And then, the main power domain circuits are supplied power and are reset. When a RESET_N pin changes "High" or the LVD reset is released, an operation mode is transited to NORMAL mode.

When an interrupt for releasing the STOP2 mode is asserted, the main power domain circuits are supplied power and are reset during releasing STOP2 mode sequence. Regarding of releasing STOP2 mode, refer to "1.3.3.3. Restart Operation from STOP2 Mode".

3.2.4. Start Up in Single Boot Mode

Regarding of the Single boot mode, refer to the reference manual "Flash Memory".
When the Secure Access Memory or Non-releasable Flash Protect is enabled, the Single boot mode dose not start. For details, refer to the reference manual "Security Function" and "Secure Access Memory".

3.2.4.1. Start Up Reset by RESET_N Pin

If a BOOT_N keeps "Low" and RESET_N pin changes "Low" to "High", the Single boot mode starts.
A BOOT_N pin is released after the CPU operation starts.

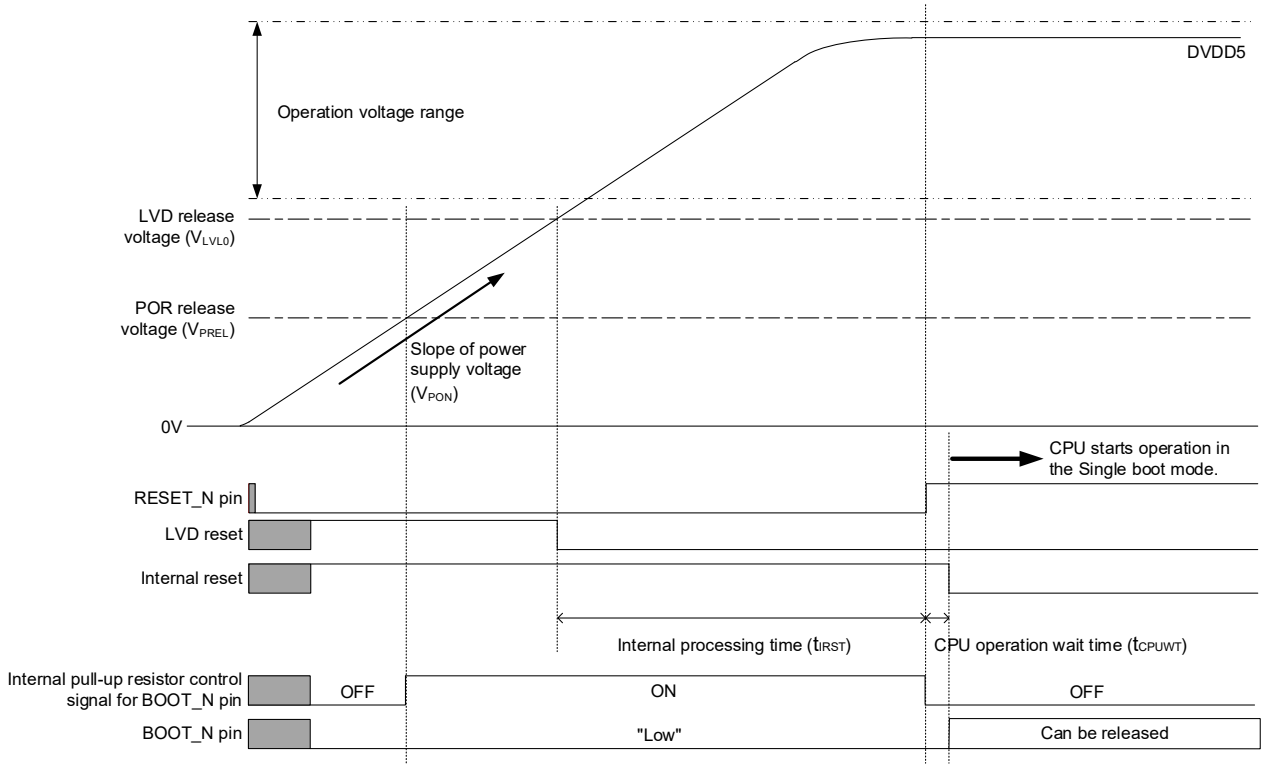

Figure 3.5 Single Boot Mode Start Up with RESET_N Pin When Power Is Turned On

3.2.4.2. Single Boot Mode Start Up when Power Supply Voltage Is Stable

When a power supply voltage is stable within an operating voltage range, a RESET_N pin keeps "Low" for "Internal processing time" or longer while the BOOT_N pin is input "Low". And release reset (a RESET_N pin is changed from "Low" to "High").

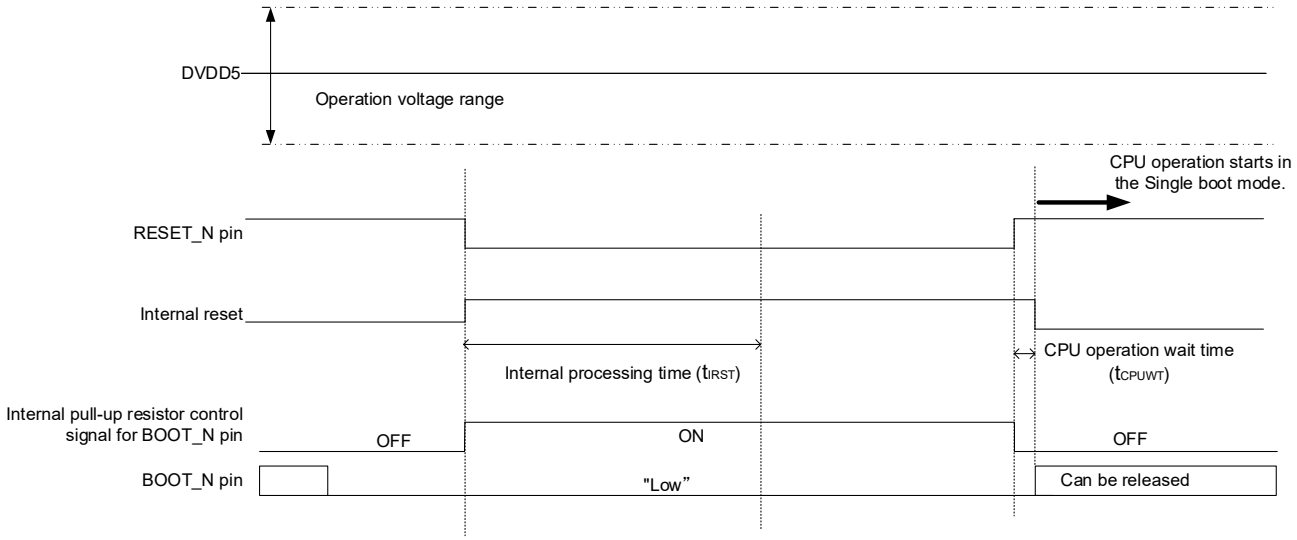

Figure 3.6 Single Boot Mode Start Up when Power Supply Voltage Is Stable

3.2.5. Power-on Reset Circuit

The power-on reset circuit (POR) generates a reset signal when the power supply is turned on or turned off.

Note: The power-on reset circuit may not operate correctly due to the fluctuation of the power supply. Equipment should be designed with full consideration of the electrical characteristics.

The power-on reset circuit consists of a detection voltage generation circuit, a reference voltage generation circuit, and a comparator.

The power supply voltage indicates a voltage of power supply for the digital circuit.

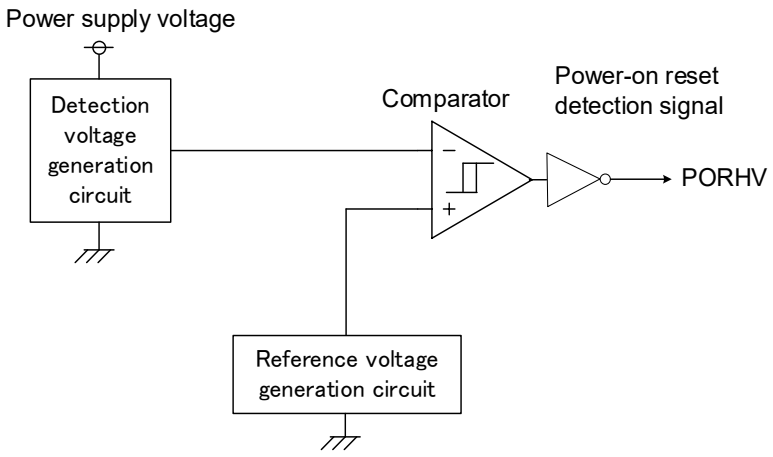

Figure 3.7 Power-on Reset Circuit

3.2.5.1. Operation when Power Supply is Turned On

When turn on power supply, while the power supply voltage is power-on reset release voltage (V_{PREL}) or lower, the power-on reset signal is generated. Refer to "Figure 3.1 Reset " for details.

While the power-on reset signal is generated, the CPU and peripheral functions are reset.

3.2.5.2. Operation when Power Supply is Turned Off

When turn off power supply or when the power supply voltage is power-on reset detection voltage (V_{PDET}) or lower, the power-on reset signal is generated.

While the power-on reset signal is generated, the CPU and peripheral functions are reset.

3.2.6. Turning Off and Re-turning On of Power Supply

When the power supply is turned off, the power supply voltage must be down gentler gradient than Max value of "Power gradient (V_{POFF})" specified in "Electrical Characteristics".

3.2.6.1. When Using External Reset Circuit or Built-in LVD Reset

When the power supply is turned off and the power supply voltage drops below the operation voltage range, the power supply voltage becomes the detection voltage of the external reset circuit or built-in LVD or lower, causing the reset occurs. From this reset sate, the power supply voltage must go up by keeping constraints as same as turning on the power supply.

3.2.6.2. When not Using External Reset Circuit and Built-in LVD Reset

When the power supply is turned off and the power supply voltage drops below the operation voltage range, the power supply voltage must drop the power-on reset detection voltage (V_{PDET}) or lower and this state must be kept for 200 µs or more. After that, the power supply voltage must go up by keeping rule as same as turning on the power supply.

If the power supply voltage drops below the power-on reset detection voltage (V_{PDET}) and this state cannot be kept for 200 µs or more, or if the same constraints as turning on the power supply cannot be kept, TMPM4L Group (1) may not operate properly.

3.2.7. After Reset Release

The control register of the Cortex-M4 (with FPU) processor core and control registers (SFR) of the peripheral functions are initialized by reset. But, initialized range of circuits is different depend on the reset factor.

Refer to "Table 3.1 Reset Factors and Initialized Range of Circuits" for the initialized range of circuit by each reset factor.

The reset factor when reset occurs can be checked by the reset flag registers which are ***[RLMRSTFLG0]*** and ***[RLMRSTFLG1]***. For details of ***[RLMRSTFLG0]*** and ***[RLMRSTFLG1]***, refer to the reference manual "Exception".

After reset is released, TMPM4L Group (1) starts operation by a clock of internal high-speed oscillator 1 (IHOSC1). The external high-speed oscillator clock and PLL multiple circuit should be set if necessary.

3.2.7.1. Reset Factors and Initialized Range of Circuits

The reset factors and initialized range of circuits are shown in Table 3.1.

Table 3.1 Reset Factors and Initialized Range of Circuits

Registers and peripheral functions		Reset source											
		STOP2 release			POR	Reset pin	OFD reset	SIWDT reset	LVD reset	PORF reset	<SYS RESET REQ> reset	LOCKUP Reset	SAM reset
		Interrupt source	Reset pin	LVD reset									
	Reset signal name	STOP2 REQ	RESET_N	LVD RSTOUT	PORHV	RESET_N	OFD RSTOUT	WDT RSTOUT	LVD RSTOUT	PORF RESET	SYS RESET REQ	LOCKUP RESET REQ	SAM RESET
Power control reset flags	*[RLMSHTDNOP] [RLMPROTECT]*	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	[RLMRSTFLG0] [RLMRSTFLG1]	-	-	-	✓	-	-	-	-	-	-	-	-
Interrupt control	*[IAIMCxx] [IANIC00]*	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	[IBIMCxxx] [IBNIC00]	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Flash memory	*[FCCPROMR]*	✓	✓	-	✓	-	-	-	-	✓	-	-	-
PORT	All registers	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
OFD		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVD		-	✓	-	✓	✓	-	-	-	-	-	-	-
Debug interface		✓	✓	-	✓	✓	-	-	-	✓	-	-	-
Others		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

✓: It is initialized.
-: It is not initialized.

Note: When reset is performed, the data of internal RAM will not be guaranteed.

4. Revision History

Table 4.1 Revision History

Revision	Date	Description
1.0	2026-01-30	- First release

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