32-bit RISC Microcontroller
Reference Manual

Advanced Encoder Input Circuit 2 (A-ENC2-A)

Revision 1.0

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
BEMF	Back Electromotive Force
BLDC	Brushless DC
CCW	Counterclockwise
CW	Clockwise
PMD	Programmable Motor Control Circuit
PWM	Pulse Width Modulation

1. Outlines

The advanced encoder input circuit operates as an input circuit for one channel (ENCxA, ENCxB, and ENCxZ pins). A list of functions is shown below.

Function category	Function	Operation
Sensor input	Encoder mode	Encoder mode is used connecting with an incremental encoder of AB or ABZ type. ● A-ENC2 detects the rotation edge of ENCxA and ENCxB pin inputs. The rotation direction is detected depending on a combination of them. ● A counter for the encoder mode is counted and down depending on the rotation direction. ● A counter for the encoder mode can be cleared by an arbitrary combination of ENCxA, ENCxB, and ENCxZ pin inputs. ● Count number in the encoder mode is up to 2^{32}. ● A valid level of ENCxZ pin input can be selected.
	Sensor mode (event count)	Sensor mode (event count) is used connecting with 2-phase (U and V) hall IC or 3-phase (U, V, and W) one. ● A-ENC2 detects the rotation edge of 2 signals, ENCxA and ENCxB pins, or 3 signals, ENCxA, ENCxB, and ENCxZ pin inputs. The rotation direction is detected depending on a combination of them. ● A counter for the sensor mode (event count) is counted and down depending on the rotation direction. ● Count number in the encoder mode is up to 2^{32}.
	Sensor mode (timer count)	Sensor mode (event count) is used connecting with 2-phase (U and V) hall IC or 3-phase (U, V, and W) one. ● A-ENC2 detects the rotation edge of 2 signals, ENCxA and ENCxB pin inputs, or 3 signals, ENCxA, ENCxB, and ENCxZ pin inputs. The rotation direction is detected depending on a combination of them. ● A counter for the sensor mode (timer count) is counted by fsys. ● A counter value is captured by the rotation edge. A time between the rotation edges can be measured by the captured value. ● A sensor less control for a brushless DC (BLDC) motor driven by a square wave is supported by PWM synchronous sampling mode.
	Sensor mode (phase count)	Sensor mode (event count) is used connecting with 2-phase (U and V) hall IC or 3-phase (U, V, and W) one. ● A-ENC2 detects the rotation edge of 2 signals, ENCxA and ENCxB pin inputs, or 3 signals, ENCxA, ENCxB, and ENCxZ pin inputs. The rotation direction is detected depending on a combination of them. ● A counter for the sensor mode (phase count) is counted and down depending on the clock of arbitrary frequency. ● A counter value is captured by the rotation edge. A time between the rotation edges can be measured by the captured value.
General purpose timer	Timer mode	Timer mode is used for 32-bit timer which counts by fsys. ● An edge to the ENCxZ pin input can be detected. ● A period between the edges can be measured by a 32-bit counter. ● The interrupts can be generated when the compare condition with a counter value and 3 registers is fulfilled.
Phase counter	Phase counter mode (phase measurement)	Phase counter mode (phase measurement) is used for 32-bit timer counted by a clock of arbitrary frequency. ● A counter for the phase counter mode (phase measurement) is counted by a clock of arbitrary frequency. ● An edge to the ENCxZ pin input can be detected. ● A counter value is captured by the edge of ENCxZ pin input. A time between the edges can be measured by the captured value. ● The interrupts can be generated when the compare condition with a counter value and 3 registers is fulfilled.

Function category	Function	Operation
	Phase counter mode (phase difference measurement)	Phase counter mode (phase difference measurement) is used for 32-bit timer counted by a clock of arbitrary frequency. ● A counter for the phase counter mode (phase difference measurement) is counted by a clock of arbitrary frequency. ● A counter is counted and down by a combination with the ENCxZ pin input and general-purpose timer output. ● An edge of general-purpose timer output can be detected. ● A counter value is captured by the edge of general-purpose timer output. A phase difference between the ENCxZ pin input and general-purpose timer output.
Noise Cancellation	Input circuit	The noise cancellation can sample the signals from ENCxA, ENCxB, and ENCxZ pin inputs by the clock divided fsys or one synchronized with PWM signal. ● A noise cancel time can be specified. ● When a sensor less control for a brushless DC (BLDC) motor driven is performed, only the induced voltage zero-cross of the Hi-Z phase can be detected.
Debug	Debug output	The internal signals of the A-ENC2 suitable for debugging can be output to outside of a device.

2. Configurations

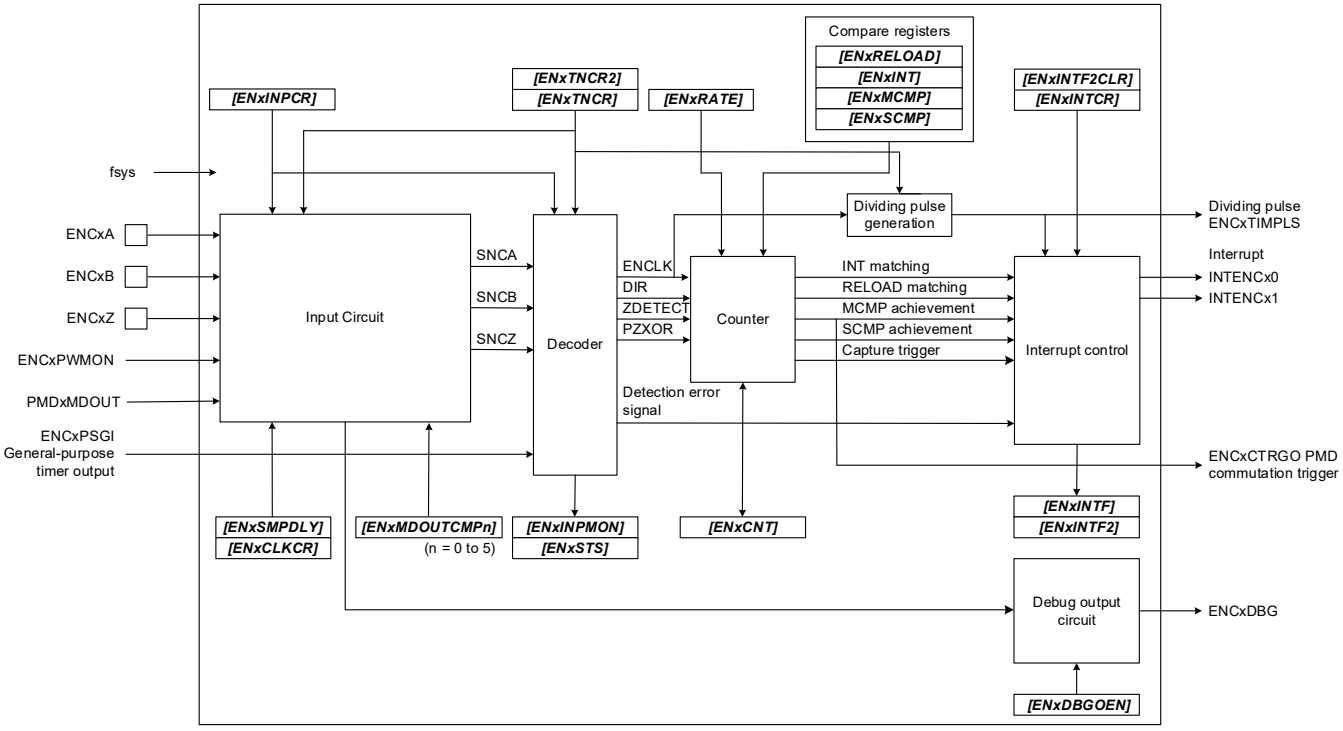

Figure 2.1 A-ENC2 Block Diagram

Table 2.1 List of Signals

No.	Symbol	Signal name	I/O	Reference manual
1	fsys	System clock	Input	Clock Control and Operation Mode
2	ENCxA	Encoder input A pin	Input	Data Sheet
3	ENCxB	Encoder input B pin	Input	Data Sheet
4	ENCxZ	Encoder input Z pin	Input	Data Sheet
5	ENCxPWMON	PWM signal for ENC	Input	Product Information
6	ENCxPSGI	General-purpose timer output signal	Input	Product Information
8	PMDxMDOUT	PWM output control	Input	Product Information
7	ENCxCTRGO	Commutation trigger for PMD	Output	Product Information
9	ENCxTIMPLS	Dividing pulse signal	Output	Product Information
10	INTENCx0	Encoder input interrupt 0	Output	Exception, Product Information
11	INTENCx1	Encoder input interrupt 1	Output	Exception, Product Information
12	ENCxDBG	Debug output	Output	Product Information

3. Function and Operation

3.1. Clock Supply

When A-ENC2-A is used, the corresponding clock enable bits should be set to "1" (Clock supply) in fsys supply stop register A (***[CGFSYSENA]*** and ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]*** and ***[CGFSYSMENB]***), fsys supply stop register C (***[CGFSYSMENC]***), and fc supply stop register (***[CGFCEN]***). The registers and the bit locations depend on each product. Some products do not have all registers. For the details, refer to the reference manual "Clock Control and Operation Mode".

3.2. Operation Mode

An operation mode is determined by ***[ENxTNCR]***<MODE[2:0]>, <P3EN>, <ZEN>. The other pin combination shown in the table below must not be used.
The operation mode settings are shown below.

Table 3.1 Operation Mode Setting

[ENxTNCR]			Input pins	Operation mode
<MODE[2:0]>	**<ZEN>**	**<P3EN>**		
000	0	0	ENCxA, ENCxB	Encoder mode (without ENCxZ pin)
	1		ENCxA, ENCxB, ENCxZ	Encoder mode (with ENCxZ pin)
001	0	0	ENCxA, ENCxB	Sensor mode (event count, 2-phase input)
		1	ENCxA, ENCxB, ENCxZ	Sensor mode (event count, 3-phase input)
010	0	0	ENCxA, ENCxB	Sensor mode (timer count, 2-phase input)
		1	ENCxA, ENCxB, ENCxZ	Sensor mode (timer count, 3-phase input)
011	0	0	-	Timer mode
	1		ENCxZ	Timer mode (with ENCxZ pin)
110	0	0	ENCxA, ENCxB	Sensor mode (phase count, 2-phase input)
		1	ENCxA, ENCxB, ENCxZ	Sensor mode (phase count, 3-phase input)
111	0	0	-	Phase counter mode (phase measurement)
	1		ENCxZ	Phase counter mode (phase measurement with ENCxZ pin)
	1	1	ENCxZ	Phase counter mode (phase difference measurement)

3.2.1. Encoder Mode

3.2.1.1. Features

The encoder mode supports a high-speed position sensor (phase judgement) such as an incremental encoder (it has A and B signals or A, B, and Z signals).

The signal A, B, and Z of an encoder are connected to ENCxA, ENCxB, and ENCxZ pins, respectively.

- A-ENC2 generates a rotation edge pulse by detecting the edge of signals from ENCxA and ENCxB pin inputs (2-phase decode).
- A 32-bit counter counts a rotation edge pulse.
- A-ENC2 detects the rotation direction of an encoder from ENCxA and ENCxB pin inputs.
- A-ENC2 detects the change in rotation direction. A-ENC2 reflects the detection result in a flag. A-ENC2 monitors the rotation direction and can generate an interrupt when A-ENC2 detects the other direction of rotation which is specified.
- The count up and down is controlled by the detected rotation direction.
- The reset condition of the counter can be specified.
- The error of ENCxA and ENCxB pin inputs can be detected.
- The counter value is captured by ***[ENxTNCR]***<SFTCAP> and it can be read from ***[ENxCNT]***<CNT[31:0]>.
- An interrupt occurs by the signal (ENCxTIMPLS) divided the rotation edge pulse.
- An interrupt occurs when A-ENC2 detects that the counter value satisfies the set condition.

3.2.1.2. Operations

A-ENC2 operates in the encoder mode when ***[ENxTNCR]***<MODE[2:0]> = 000, ***[ENxTNCR]***<ZEN> = arbitrary value, ***[ENxTNCR]***<P3EN> = 0.

In the encoder mode, the below functions can be set.

(1) Detection of a rotation direction
A phase between ENCxA and ENCxB pin inputs for detecting a rotation direction is set by ***[ENxTNCR2]***<ABREV>. And the rotation direction to detect and the value of ENCxA and ENCxB pin inputs (current or previous ones) can be selected by ***[ENxTNCR]***<DECMD[1:0]>. For details, refer to "3.3.2.1. Rotation Edge and Rotation Direction Detection".
A rotation direction is monitored by ***[ENxSTS]***<UD>. ***[ENxSTS]***<UD> is set to "0" when a rotation direction is CW direction and set to "1" when CCW direction.

(2) Control for ENCxZ pin input
ENCxZ pin input can be enabled and disabled by ***[ENxTNCR]***<ZEN>. When ***[ENxTNCR]***<ZEN> is "0", ENCxZ pin input is disabled. When it is "1", ENCxZ pin input is enabled.

When ENCxZ pin input is enabled, an active level of it can be selected by ***[ENxTNCR]***<ZEACT>. When ***[ENxTNCR]***<ZEACT> is "0", "High" to ENCxZ pin input is determined as an active level. When it is "1", "Low" is determined.
An active level input can be monitored by ***[ENxSTS]***<ZDET>.

(3) Counter operation
A counter in the encoder mode counts a rotation edge pulse (ENCLK).
For details, refer to "3.3.3.1. Encoder Mode and Sensor Mode (Event Count)".

A counter value and registers' values are compared by the condition set beforehand and the satisfaction of the conditions can be detected.

(a) Comparing condition for ***[ENxRELOAD]***<RELOAD[31:0]>
Only matching can be detected.

(b) Comparing condition for ***[ENxINT]***<INT[31:0]>
Only matching can be detected.

(c) Comparing condition for ***[ENxMCMP]***<MCMP[31:0]>
Only matching can be detected.

(d) Comparing condition for ***[ENxSCMP]***<SCMP[31:0]>
Only matching can be detected.

(4) Error detection
A skip judgment is performed in the encoder mode.
An abnormal input judgement is not performed in the encoder mode.
A bit reversed skip judgment is not performed in the encoder mode.
An edge detection error judgement is performed in the encoder mode.

(5) Interrupts
The interrupt signal INTENCx0 occurs synchronized with ENCxTIMPLS. When setting ***[ENxINTCR]***<TPLSIE> to "0", it is disabled. When setting to "1", it is enabled.

The conditions of comparing with the counter value and the registers, ***[ENxSCMP]***<SCMP[31:0]>, ***[ENxMCMP]***<MCMP[31:0]>, ***[ENxINT]***<INT[31:0]>, are set beforehand.
The interrupt signal INTENCx1 occurs when it is detected that the set conditions are fulfilled. When the corresponding bit in ***[ENxINTCR]*** is set to "0", it is disabled. When setting to "1", it is enabled.

The interrupt signal INTENCx0 occurs when errors are detected. When the corresponding bit in ***[ENxINTCR]*** is set to "0", it is disabled. When setting to "1", it is enabled.

For details, Refer to "3.3.4. Interrupt Control".

3.2.1.3. Examples of Operation

Figure 3.1 and Figure 3.2 are shown as the example of operation when ENCxZ pin input is enabled and a rotation direction is reversed midway.
The operation conditions are shown below.

(1) When ENCxA pin input is "High", ENCxB pin input is "Low", and ENCxZ pin input is "High", the counter is cleared. (***[ENxTNCR]***<ZEN> = 1, ***[ENxTNCR]***<ZEACT> = 0, ***[ENxTNCR]***<ABZCLRVAL[2:0]> = 101)

(2) When the value of counter becomes "0x000000002", an INT matching interrupt occurs.
(***[ENxINT]***<INT[31:0]> = 0x00000002, ***[ENxINTCR]***<CMPIE> = 1)

(3) The ENCxTIMPLS divided ENCLK by 2 is generated and the interrupt synchronized with ENCxTIMPLS occurs. (***[ENxTNCR]***<ENDEV[2:0]> = 001, ***[ENxINTCR]***<TPLSIE> = 1)

(4) When the value of counter becomes "0x000000380", the counter is cleared.
(***[ENxRELOAD]***<RELOAD[31:0]> = 0x00000380.)

(5) Rotation direction

(a) The state of ENCxA and ENCxB pin inputs are defined as CW direction when the ENCxA pin input is leading 90 degrees ahead of ENCxB pin input in phase. At this time, the counter counts up. The state when the ENCxA pin input is lagging 90 degrees behind ENCxB pin input is defined as CCW direction and the counter counts down. (***[ENxTNCR2]***<ABREV> = 0) ("Figure 3.1 CW Direction Means State that ENCxA Pin Input is Leading 90 Degrees Ahead of ENCxB Pin Input in Phase. (when *[ENxTNCR2]*<ABREV> is "0")")

(b) The state of ENCxA and ENCxB pin inputs are defined as CW direction when the ENCxA pin input is lagging 90 degrees behind of ENCxB pin input in phase. At this time, the counter counts up. The state when the ENCxA pin input is leading 90 degrees ahead of ENCxB pin input in phase is defined as CCW direction and the counter counts down. (***[ENxTNCR2]***<ABREV> = 1) ("Figure 3.2 CW Direction Means State that ENCxA Pin Input is Lagging 90 Degrees Behind of ENCxB Pin Input in Phase. (when *[ENxTNCR2]*<ABREV> is "1")")

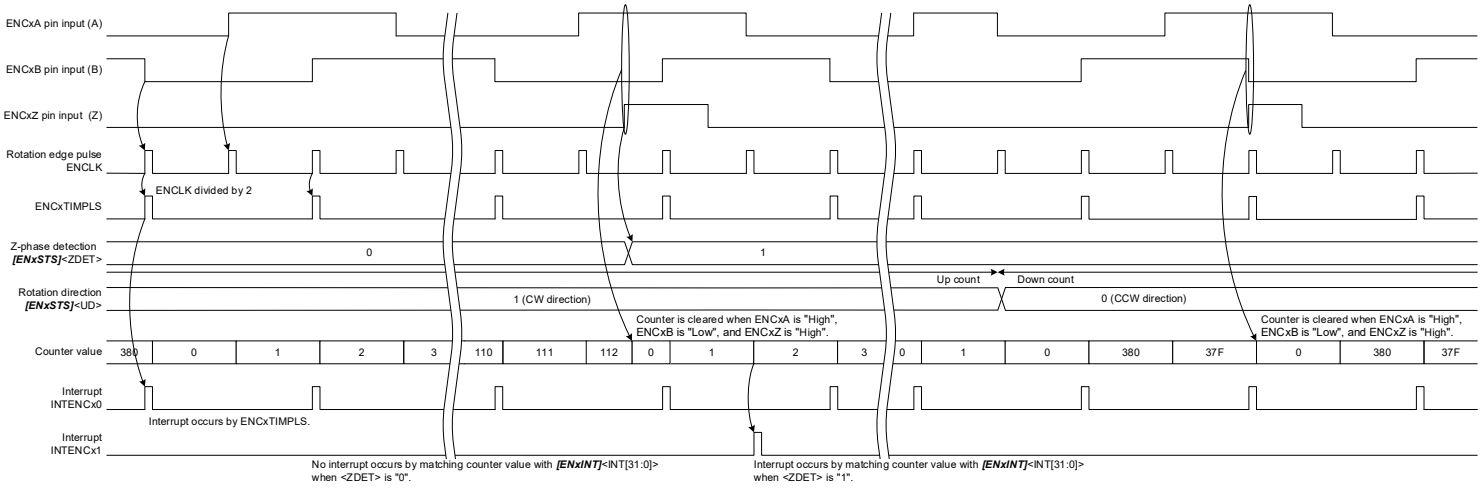

Figure 3.1 CW Direction Means State that ENCxA Pin Input is Leading 90 Degrees Ahead of ENCxB Pin Input in Phase. (when *[ENxTNCR2]*<ABREV> is "0")

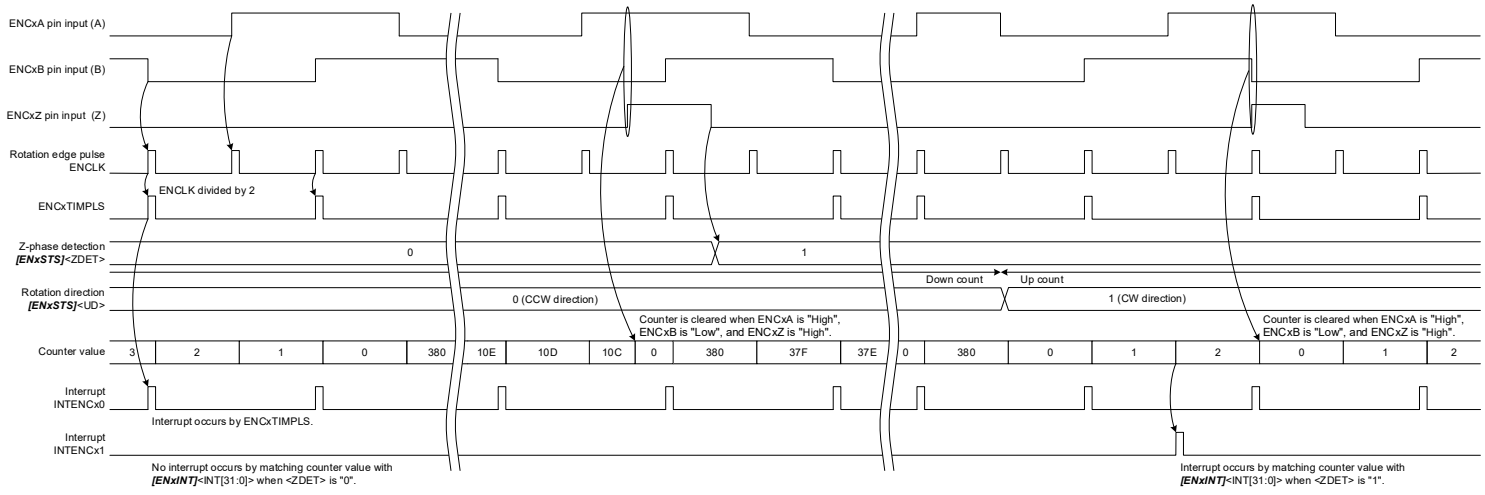

Figure 3.2 CW Direction Means State that ENCxA Pin Input is Lagging 90 Degrees Behind of ENCxB Pin Input in Phase. (when *[ENxTNCR2]*<ABREV> is "1")

Figure 3.3 shows the operation example when the ENCxZ pin input is disabled, the rotation direction is reversed midway, the counter is cleared by a software during counting.

The operation conditions are shown below.

(1) The counter is not cleared by the ENCxZ pin input. (***[ENxTNCR]***<ZEN> = 0)

(2) The counter is cleared by software. (***[ENxTNCR]***<ENCLR> = 1)

(3) When the value of counter becomes "0x000000002", an INT matching interrupt occurs. (***[ENxINT]***<INT[31:0]> = 0x00000002, ***[ENxINTCR]***<CMPIE> = 1)

(4) The ENCxTIMPLS divided ENCLK by 2 is generated and the interrupt synchronized with ENCxTIMPLS occurs. (***[ENxTNCR]***<ENDEV[2:0]> = 001, ***[ENxINTCR]***<TPLSIE> = 1)

(5) When the value of counter becomes "0x000000380", the counter is cleared. (***[ENxRELOAD]***<RELOAD[31:0]> = 0x00000380.)

(6) The state of ENCxA and ENCxB pin inputs are defined as CW direction when the ENCxA pin input is leading 90 degrees ahead of ENCxB pin input in phase. At this time, the counter counts up. The state when the ENCxA pin input is lagging ENCxB pin input is defined as CCW direction, and the counter counts down. (***[ENxTNCR2]***<ABREV> = 0)

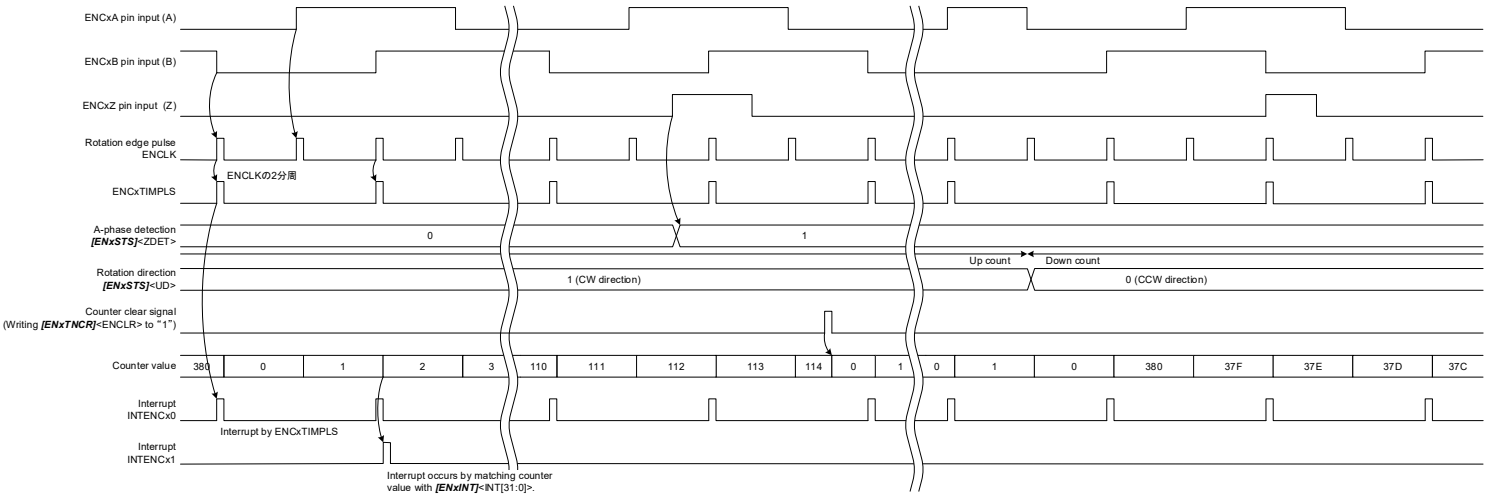

Figure 3.3 CW Direction Means State that ENCxA Pin Input is Leading 90 Degrees Ahead of ENCxB Pin Input in Phase. (when *[ENxTNCR]*<ZEN> is "0")

3.2.2. Sensor mode

The sensor mode supports a low-speed position sensor (zero-cross judgement) such as a 2-phase and 3-pahse Hall sensors.
The Hall sensor outputs (signal U, V, and W) are connected to ENCxA, ENCxB, and ENCxZ pins, respectively.

In the sensor mode, A-ENC2 performs the below operations.

(1) Event count

(2) Timer count
When the A-ENC2 performs as timer count, the zero cross detection mask control can be performed for the sensor less pulse drive which drives BLDC motor by a square pulse.

(3) Phase count
When the A-ENC2 performs as phase count, the zero cross detection mask control can be performed for the sensor less pulse drive which drives BLDC motor by a square pulse.

3.2.2.1. Event Count

(1) Features

- A-ENC2 generates a rotation edge pulse by detecting the edge of signals from ENCxA and ENCxB pin inputs (2-phase decode) or ENCxA, ENCxB, and ENCxZ pin inputs (3-phase decode).
- A-ENC2 detects the rotation direction of motor from ENCxA and ENCxB pin inputs or ENCxA, ENCxB, and ENCxZ pin inputs.
- The count up and down is controlled by the detected rotation direction.
- A-ENC2 detects the change in rotation direction. A-ENC2 reflects the detection result in a flag . A-ENC2 monitors the rotation direction and can generate an interrupt when A-ENC2 detects the other direction of rotation which is specified.
- The error of ENCxA, ENCxB, and ENCxZ pin inputs can be detected.
- The counter value is captured by ***[ENxTNCR]***<SFTCAP> and it can be read from ***[ENxCNT]***<CNT[31:0]>.
- An interrupt occurs by the signal (ENCxTIMPLS) divided the rotation edge pulse.
- An interrupt occurs when A-ENC2 detects that the counter value satisfies the set condition.

(2) Operations

A-ENC2 operates in the sensor mode (event count) when ***[ENxTNCR]***<MODE[2:0]> = 001, ***[ENxTNCR]***<ZEN> = 0, ***[ENxTNCR]***<P3EN> = arbitrary value.

In the sensor mode (event count), the below functions can be set.

(a) Detection of a rotation direction
The rotation direction to detect and the value of ENCxA, ENCxB, and ENCxZ pin inputs (current or previous ones) can be selected by ***[ENxTNCR]***<DECMD[1:0]>. For details, refer to "3.3.2.1. Rotation Edge and Rotation Direction Detection".
A rotation direction is monitored by ***[ENxSTS]***<UD>. ***[ENxSTS]***<UD> is set to "0" when a rotation direction is CW direction and set to "1" when CCW direction.

(b) Control for ENCxZ pin input
The ENCxZ pin input cannot be controlled.

(c) Counter operation
A counter in the sensor mode (event count) counts a rotation edge pulse (ENCLK).
For details, refer to "3.3.3.1. Encoder Mode and Sensor Mode (Event Count)".
The counter is cleared to "0x00000000" when ***[ENxTNCR]***<ENCLR> is set to "1".

A counter value and registers' values are compared by the condition set beforehand and the satisfaction of the conditions can be detected.

(i) Comparing condition for ***[ENxINT]***<INT[31:0]>
Only matching can be detected.

(ii) Comparing condition for ***[ENxMCMP]***<MCMP[31:0]>
Only matching can be detected.

(iii) Comparing condition for ***[ENxSCMP]***<SCMP[31:0]>
Only matching can be detected.

(d) Error detection
A skip judgment is performed in the sensor mode (event count).
An abnormal input judgement is not performed in the sensor mode (event count).
A bit reversed skip judgment is not performed in the sensor mode (event count).
An edge detection error judgement is performed in the sensor mode (event count).

(e) Interrupt
The interrupt signal INTENCx0 occurs synchronized with ENCxTIMPLS. When setting ***[ENxINTCR]***<TPLSIE> to "0", it is disabled. When setting to "1", it is enabled.

The conditions of comparing with the counter value and the registers, ***[ENxSCMP]***<SCMP[31:0]>, ***[ENxMCMP]***<MCMP[31:0]>, and ***[ENxINT]***<INT[31:0]>, are set beforehand.
The interrupt signal INTENCx1 occurs when it is detected that the set conditions are fulfilled. When the corresponding bit in ***[ENxINTCR]*** is set to "0", it is disabled. When setting to "1", it is enabled.

The interrupt signal INTENCx0 occurs when errors are detected. When the corresponding bit in ***[ENxINTCR]*** is set to "0", it is disabled. When setting to "1", it is enabled.

For details, Refer to "3.3.4. Interrupt Control".

(3) Examples of Operation

Figure 3.4 and Figure 3.5 are shown the example of operation.
The operation conditions are shown below.

(a) When the value of counter becomes "0x000000002", an INT matching interrupt occurs. (***[ENxINT]***<INT[31:0]> = 0x00000002, ***[ENxINTCR]***<CMPIE> = 1)

(b) The ENCxTIMPLS divided ENCLK by 2 is generated and the interrupt synchronized with ENCxTIMPLS occurs. (***[ENxTNCR]***<ENDEV[2:0]> = 001, ***[ENxINTCR]***<TPLSIE> = 1)

(c) Decode mode
(i) 2-phase decode
Decoded by 2-phase decode (***[ENxTNCR]***<P3EN> = 0) ("Figure 3.4 2-phase Decode (*[ENxTNCR]*<P3EN> = 0)")

(ii) 3-phase decode
Decoded by 3-phase decode (***[ENxTNCR]***<P3EN> = 1) ("Figure 3.5 3-phase Decode (*[ENxTNCR]*<P3EN> = 1)")

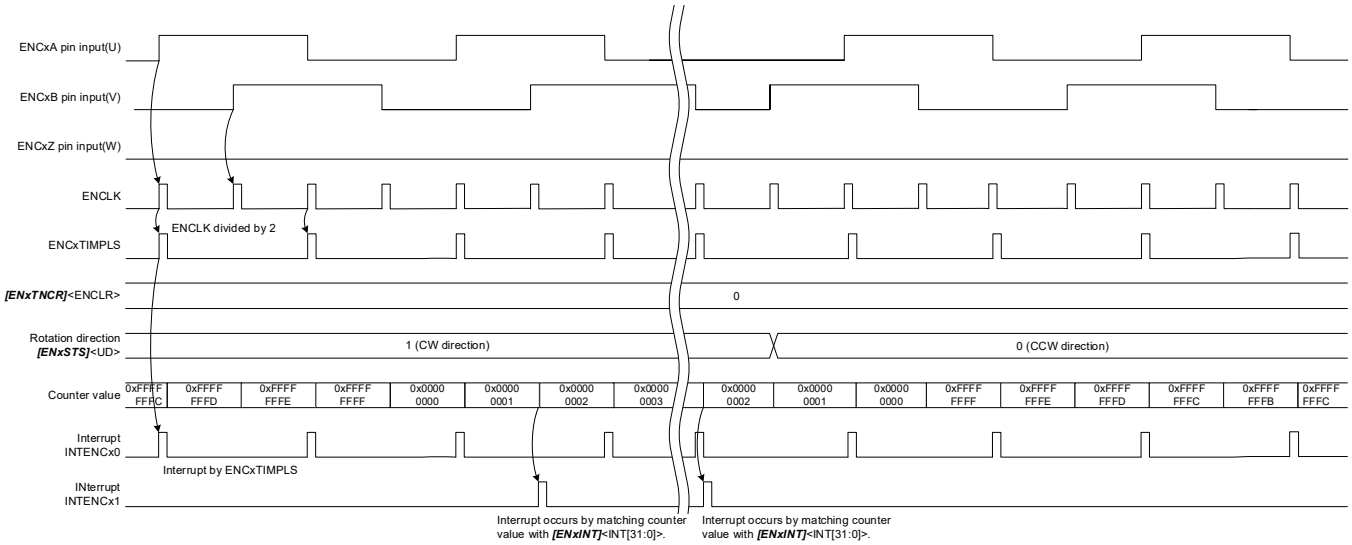

Figure 3.4 2-phase Decode (*[ENxTNCR]*<P3EN> = 0)

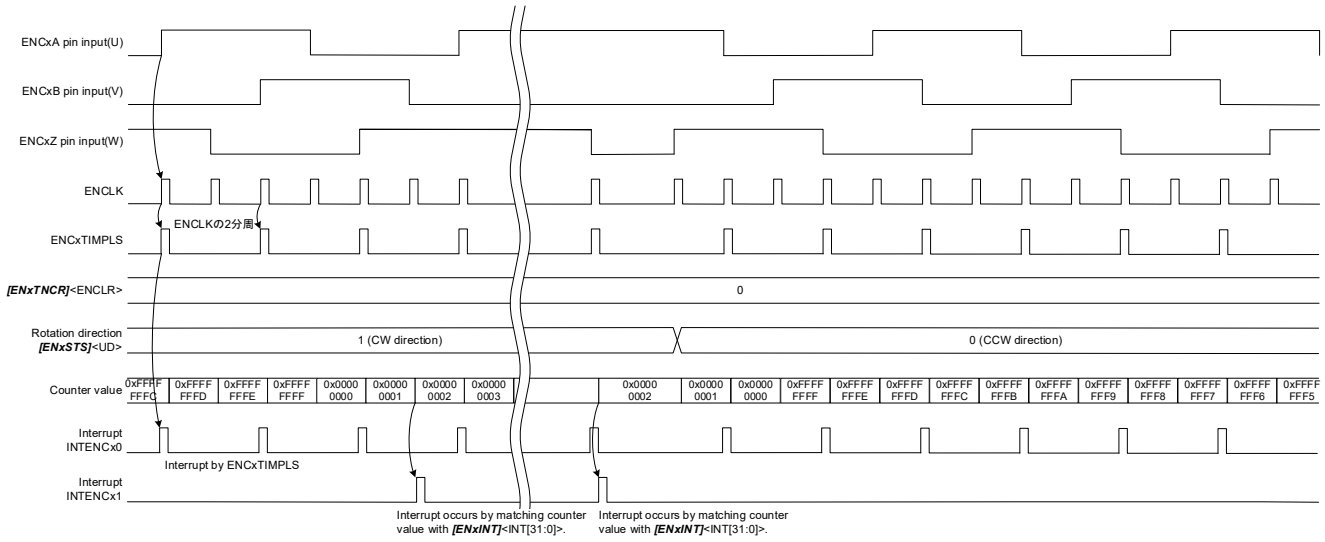

Figure 3.5 3-phase Decode (*[ENxTNCR]*<P3EN> = 1)

3.2.2.2. Timer Count

(1) Features

- A-ENC2 generates a rotation edge pulse by detecting the edge of signals from ENCxA and ENCxB pin inputs (2-phase decode) or ENCxA, ENCxB, and ENCxZ pin inputs (3-phase decode).
- A 32-bit counter counts up the fsys.
- A-ENC2 detects the rotation direction of motor from ENCxA and ENCxB pin inputs or ENCxA, ENCxB, and ENCxZ pin inputs.
- A-ENC2 detects the change in rotation direction. A-ENC2 reflects the detection result in a flag . A-ENC2 monitors the rotation direction and can generate an interrupt when A-ENC2 detects the other direction of rotation which is specified.
- The error of ENCxA, ENCxB, and ENCxZ pin inputs can be detected.
- The counter value is captured by ***[ENxTNCR]***<SFTCAP> and a rotation edge pulse and it can be read from ***[ENxCNT]***<CNT[31:0]>.
- An interrupt occurs when A-ENC2 detects that the counter value satisfies the set condition.

(2) Operations

A-ENC2 operates in the sensor mode (event count) when ***[ENxTNCR]***<MODE[2:0]> = 010, ***[ENxTNCR]***<ZEN> = 0, ***[ENxTNCR]***<P3EN> = arbitrary value.

In the sensor mode (timer count), the below functions can be set.

(a) Detection of a rotation direction
The rotation direction to detect and the value of ENCxA, ENCxB, and ENCxZ pin inputs (current or previous ones) can be selected by ***[ENxTNCR]***<DECMD[1:0]>. For details, refer to "3.3.2.1. Rotation Edge and Rotation Direction Detection".
A rotation direction is monitored by ***[ENxSTS]***<UD>. ***[ENxSTS]***<UD> is set to "0" when a rotation direction is CW direction and set to "1" when CCW direction.

(b) Control for ENCxZ pin input
The ENCxZ pin input cannot be controlled.

(c) Counter operation
A counter in the sensor mode (timer count) counts the fsys
For details, refer to "3.3.3.2. Sensor Mode (Timer Count) and Timer Mode".
The counter is cleared to "0x00000000" when ***[ENxTNCR]***<ENCLR> is set to "1".

A counter value and registers' values are compared by the condition set beforehand and the satisfaction of the conditions can be detected.

(i) Comparing condition for ***[ENxRELOAD]***<RELOAD[31:0]>
Only matching can be detected.

(ii) Comparing condition for ***[ENxINT]***<INT[31:0]>
Only matching can be detected.

(iii) Comparing condition for ***[ENxMCMP]***<MCMP[31:0]>
The comparing condition can be selected by ***[ENxTNCR]***<MCMPMD>.
When ***[ENxTNCR]***<MCMPMD> is "0", the comparing condition is matching with the counter value and ***[ENxMCMP]***<MCMP[31:0]>.
When it is "1", the comparing condition is that the counter value is ***[ENxMCMP]***<MCMP[31:0]> or more.

(iv) Comparing condition for ***[ENxSCMP]***<SCMP[31:0]>
The comparing condition can be selected by ***[ENxTNCR]***<SCMPMD>.
When ***[ENxTNCR]***<SCMPMD> is "0", the comparing condition is matching with the counter value and ***[ENxSCMP]***<MCMP[31:0]>.
When it is "1", the comparing condition is that the counter value is ***[ENxSCMP]***<MCMP[31:0]> or more.

(d) Error detection
A skip judgment is performed in the sensor mode (timer counter).
An abnormal input judgement is performed in the sensor mode (timer counter).
A bit reversed skip judgment is performed in the sensor mode (timer counter).
An edge detection error judgement is performed in the sensor mode (timer counter).

(e) Interrupt
The interrupt signal INTENCx0 occurs at capturing timing by the ENCLK. When setting ***[ENxINTCR]***<CAPIE> to "0", it is disabled. When setting to "1", it is enabled.

The conditions of comparing with the counter value and the registers, ***[ENxSCMP]***<SCMP[31:0]>, ***[ENxMCMP]***<MCMP[31:0]>, ***[ENxINT]***<INT[31:0]> and ***[ENxRELOAD]***<RELOAD[31:0]>, are set beforehand.
The interrupt signal INTENCx1 occurs when it is detected that the set conditions are fulfilled. When the corresponding bit in ***[ENxINTCR]*** is set to "0", it is disabled. When setting to "1", it is enabled.

The interrupt signal INTENCx0 occurs when errors are detected. When the corresponding bit in ***[ENxINTCR]*** is set to "0", it is disabled. When setting to "1", it is enabled.

For details, Refer to "3.3.4. Interrupt Control".

(3) Examples of Operation

Figure 3.6 and Figure 3.7 are shown the example of operation.
The operation conditions are shown below.

(a) When the value of counter becomes "0x000000002", an INT matching interrupt occurs. (***[ENxINT]***<INT[31:0]> = 0x00000002, ***[ENxINTCR]***<CMPIE> = 1)

(b) The interrupt occurs at capturing timing by ENCLK. (***[ENxTNCR]***<CAPIE> = 1)

(c) Decode mode
(i) 2-phase decode
Decoded by 2-phase decode (***[ENxTNCR]***<P3EN> = 0) ("Figure 3.6 2-phase Decode (*[ENxTNCR]*<P3EN> = 0)")

(ii) 3-phase decode
Decoded by 3-phase decode (***[ENxTNCR]***<P3EN> = 1) ("Figure 3.7 3-phase Decode (*[ENxTNCR]*<P3EN> = 1)")

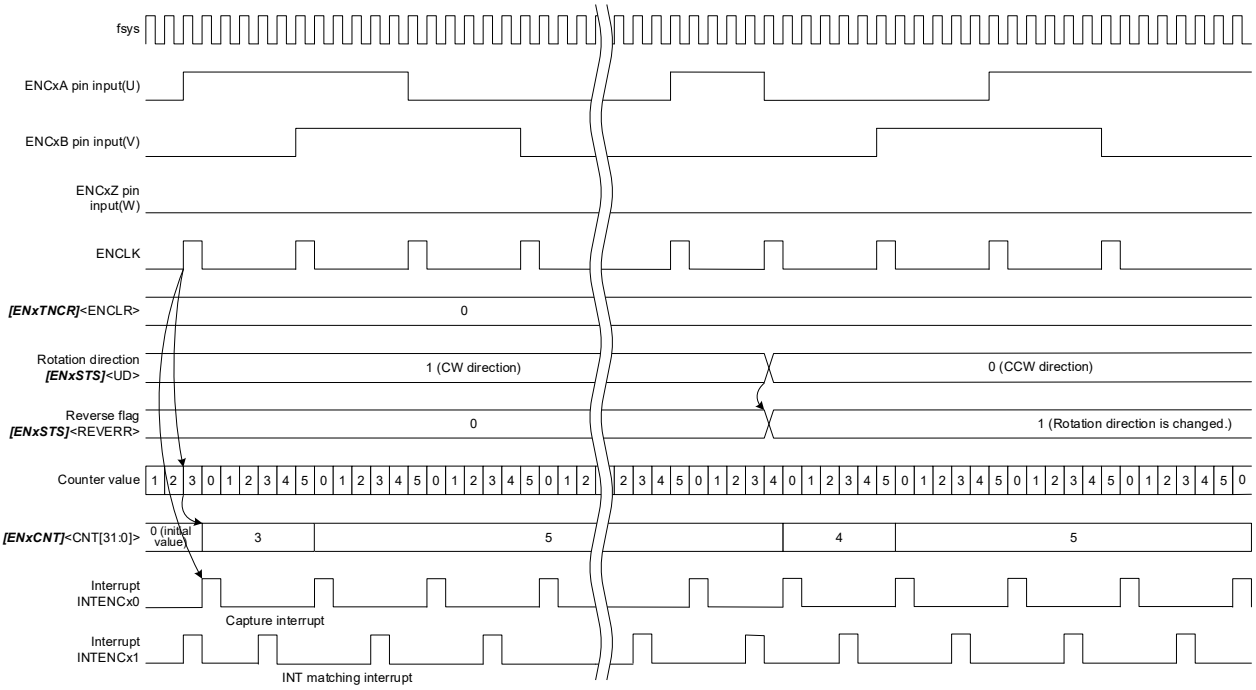

Figure 3.6 2-phase Decode (*[ENxTNCR]*<P3EN> = 0)

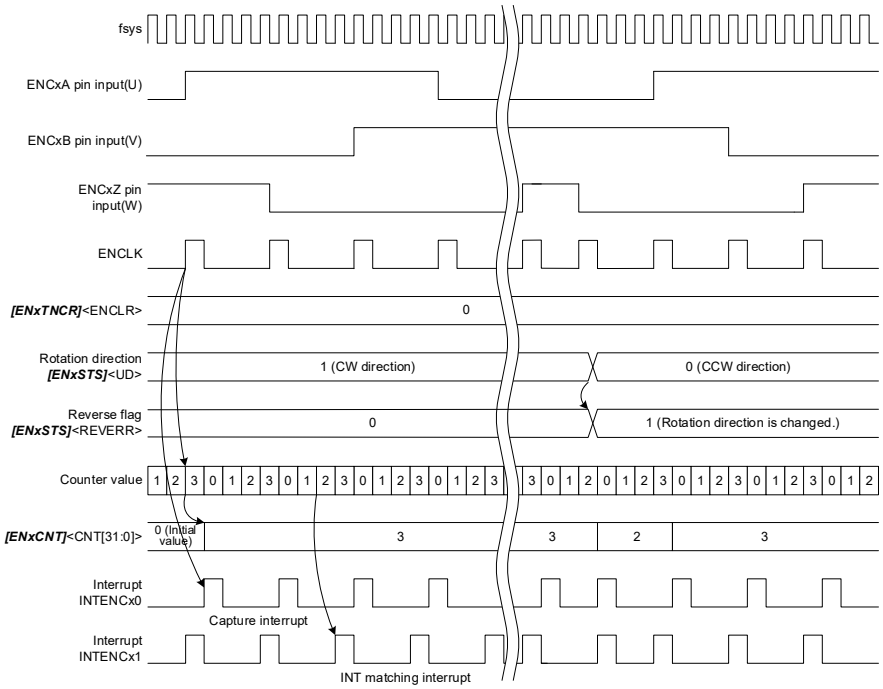

Figure 3.7 3-phase Decode (*[ENxTNCR]*<P3EN> = 1)

3.2.2.3. Phase count

(1) Features

- A-ENC2 generates a rotation edge pulse by detecting the edge of signals from ENCxA and ENCxB pin inputs (2-phase decode) or ENCxA, ENCxB, and ENCxZ pin inputs (3-phase decode).
- A 32-bit counter counts up and down the clock specified by ***[ENxTNCR]***<UDMD[1:0]> and ***[ENxRATE]***<RATE[15:0]>.
- A-ENC2 detects the rotation direction of motor from ENCxA and ENCxB pin inputs or ENCxA, ENCxB, and ENCxZ pin inputs.
- A-ENC2 detects the change in rotation direction. A-ENC2 reflects the detection result in a flag . A-ENC2 monitors the rotation direction and can generate an interrupt when A-ENC2 detects the other direction of rotation which is specified.
- The error of ENCxA, ENCxB, and ENCxZ pin inputs can be detected.
- The counter value is captured by ***[ENxTNCR]***<SFTCAP> and a rotation edge pulse and it can be read from ***[ENxCNT]***<CNT[31:0]>. An interrupt can occur at capturing timing by a rotation edge pulse.
- An interrupt occurs when A-ENC2 detects that the counter value satisfies the set condition.

(2) Operations

A-ENC2 operates in the sensor mode (phase count) when ***[ENxTNCR]***<MODE[2:0]> = 110, ***[ENxTNCR]***<ZEN> = 0, ***[ENxTNCR]***<P3EN> = arbitrary value.

In the sensor mode (phase count), the below functions can be set.

(a) Detection of a rotation direction
The rotation direction to detect and the value of ENCxA, ENCxB, and ENCxZ pin inputs (current or previous ones) can be selected by ***[ENxTNCR]***<DECMD[1:0]>. For details, refer to "3.3.2.1. Rotation Edge and Rotation Direction Detection".
A rotation direction is monitored by ***[ENxSTS]***<UD>. ***[ENxSTS]***<UD> is set to "0" when a rotation direction is CW direction and set to "1" when CCW direction.

(b) Control for ENCxZ pin input
The ENCxZ pin input cannot be controlled.

(c) Counter operation
A counter in the sensor mode (phase count) counts the clock specified with ***[ENxTNCR]***<UDMD[1:0]> and ***[ENxRATE]***<RATE[15:0]>.
For details, refer to "3.3.3.3. Sensor Mode (Phase Count) and Phase Counter Mode".
The counter is cleared to "0x00000000" when ***[ENxTNCR]***<ENCLR> is set to "1".

A counter value and registers' values are compared by the condition set beforehand and the satisfaction of the conditions can be detected.

(i) Comparing condition for ***[ENxRELOAD]***<RELOAD[31:0]>
Only matching can be detected.

(ii) Comparing condition for ***[ENxINT]***<INT[31:0]>
Only matching can be detected.

(iii) Comparing condition for ***[ENxMCMP]***<MCMP[31:0]>
Only matching can be detected.

(iv) Comparing condition for ***[ENxSCMP]***<SCMP[31:0]>
Only matching can be detected

.

(d) Error detection
A skip judgment is performed in 3-phase decode and the sensor mode (Phase count).
An abnormal input judgement is performed in the sensor mode (Phase count).
A bit reversed skip judgment is performed in the sensor mode (Phase count).
An edge detection error judgement is performed in the sensor mode (Phase count).

(e) Interrupt
The interrupt signal INTENCx0 occurs at capturing timing by ZDETECT. It is disabled when ***[ENxINTCR]***<CAPIE> is "0". It is enabled when ***[ENxINTCR]***<CAPIE> is "1".

The conditions of comparing with the counter value and the registers, ***[ENxSCMP]***<SCMP[31:0]>, ***[ENxMCMP]***<MCMP[31:0]>, ***[ENxINT]***<INT[31:0]>, and ***[ENxRELOAD]***<RELOAD[31:0]>, are set beforehand.
The interrupt signal INTENCx1 occurs when it is detected that the set conditions are fulfilled. When the corresponding bit in ***[ENxINTCR]*** is set to "0", it is disabled. When setting to "1", it is enabled.

For details, Refer to "3.3.4. Interrupt Control".

(3) Examples of Operation

Figure 3.8 and Figure 3.9 are shown the example of operation.
The operation conditions are shown below.

(a) When the value of counter becomes "0x000000002", an INT matching interrupt occurs. (***[ENxINT]***<INT[31:0]> = 0x00000002, ***[ENxINTCR]***<CMPIE> = 1)

(b) The interrupt occurs at capturing timing by ENCLK. (***[ENxTNCR]***<CAPIE> = 1)

(c) Decode mode
(i) 2-phase decode
Decoded by 2-phase decode (***[ENxTNCR]***<P3EN> = 0) ("Figure 3.8 2-phase Decode (*[ENxTNCR]*<P3EN> = 0)")

(ii) 3-phase decode
Decoded by 3-phase decode (***[ENxTNCR]***<P3EN> = 1) ("Figure 3.9 3-phase Decode (*[ENxTNCR]*<P3EN> = 1)")

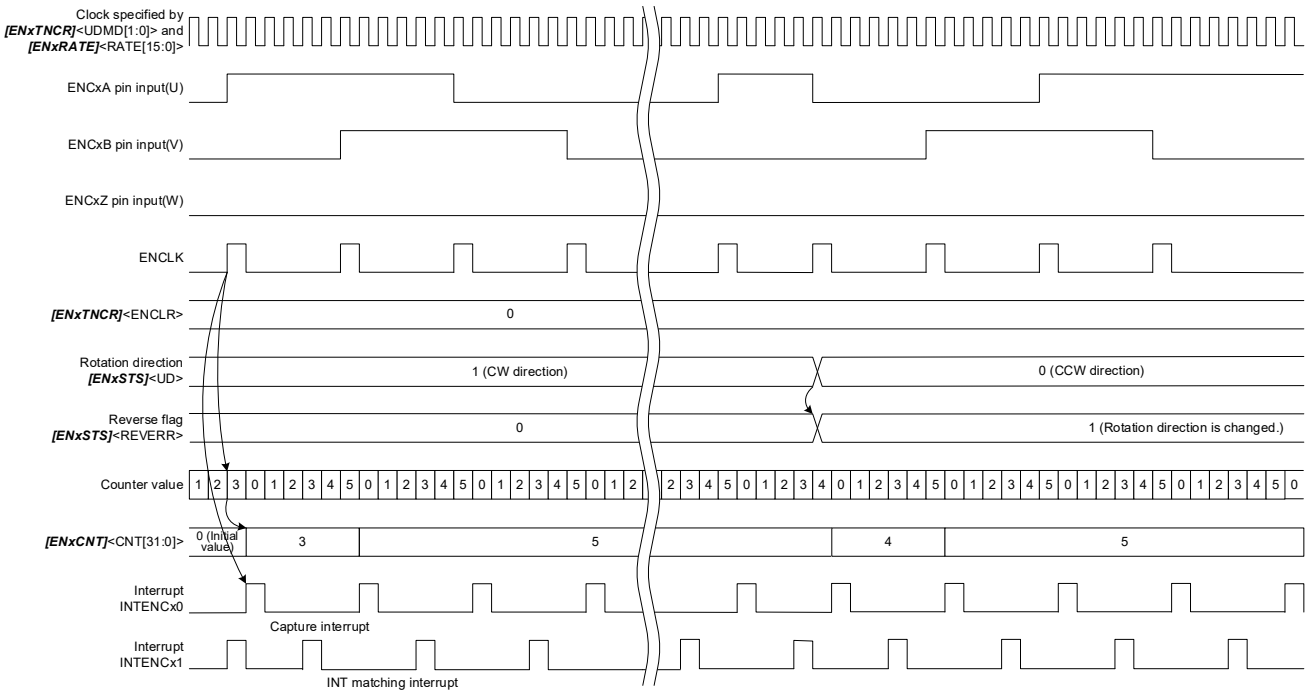

Figure 3.8 2-phase Decode (*[ENxTNCR]*<P3EN> = 0)

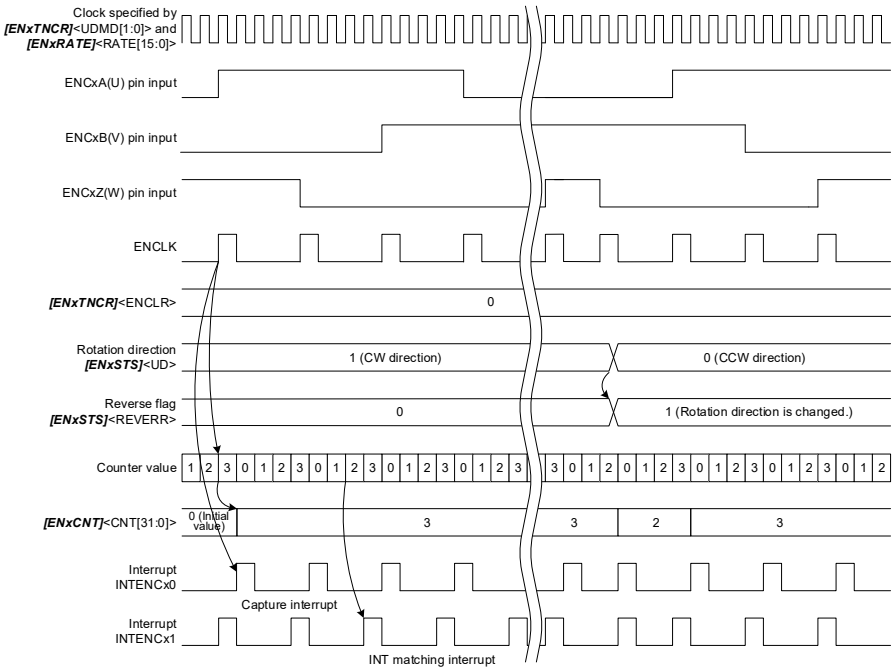

Figure 3.9 3-phase Decode (*[ENxTNCR]*<P3EN> = 1)

3.2.3. Timer Mode

3.2.3.1. Features

The timer mode can be used as a general 32-bit timer.

- The counter value is captured by ***[ENxTNCR]***<SFTCAP> and ZDETECT (edge detection signal of ENCxZ pin input) and it can be read from ***[ENxCNT]***<CNT[31:0]>.
- The condition to clear a counter is specified.
- An interrupt occurs when a counter value is captured by the ZDETECT (edge detection signal of ENCxZ pin input).
- An interrupt occurs when A-ENC2 detects that the counter value satisfies the set condition.

3.2.3.2. Operations

A-ENC2 operates in the timer mode when ***[ENxTNCR]***<MODE[2:0]> = 011, ***[ENxTNCR]***<ZEN> = arbitrary value, ***[ENxTNCR]***<P3EN> = 0.

In the timer mode, the functions below can be set.

(1) Detection of a rotation direction
In timer mode, a detection of a rotation direction is not performed.

(2) Control for ENCxZ pin input
ENCxZ pin input is used as an external trigger.
ENCxZ pin input can be enabled and disabled by ***[ENxTNCR]***<ZEN>. When ***[ENxTNCR]***<ZEN> is "0", ENCxZ pin input is disabled. When it is "1", ENCxZ pin input is enabled.

(3) Counter operation
A counter in the timer mode counts the fsys.
It always counts up.
For details, refer to "3.3.3.2. Sensor Mode (Timer Count) and Timer Mode".
The counter is cleared to "0x00000000" when ***[ENxTNCR]***<ENCLR> is set to "1".

A counter value and registers' values are compared by the condition set beforehand and the satisfaction of the conditions can be detected.

(a) Comparing condition for ***[ENxRELOAD]***<RELOAD[31:0]>
Only matching can be detected.

(b) Comparing condition for ***[ENxINT]***<INT[31:0]>
Only matching can be detected.

(c) Comparing condition for ***[ENxMCMP]***<MCMP[31:0]>
The comparing condition can be selected by ***[ENxTNCR]***<MCMPMD>.
When ***[ENxTNCR]***<MCMPMD> is "0", the comparing condition is matching with the counter value and ***[ENxMCMP]***<MCMP[31:0]>.
When it is "1", the comparing condition is that the counter value is ***[ENxMCMP]***<MCMP[31:0]> or more.

(d) Comparing condition for ***[ENxSCMP]***<SCMP[31:0]>
The comparing condition can be selected by ***[ENxTNCR]***<SCMPMD>.
When ***[ENxTNCR]***<SCMPMD> is "0", the comparing condition is matching with the counter value and ***[ENxSCMP]***<MCMP[31:0]>.
When it is "1", the comparing condition is that the counter value is ***[ENxSCMP]***<MCMP[31:0]> or more.

(4) Error detection
A skip judgment is not performed in the timer mode.
An abnormal input judgement is not performed in the timer mode.
A bit reversed skip judgment is not performed in the timer mode.
An edge detection error judgement is not performed in the timer mode.

(5) Interrupts
The interrupt signal INTENCx0 occurs at capturing timing by ZDETECT. It is disabled when ***[ENxINTCR]***<CAPIE> is "0". It is enabled when ***[ENxINTCR]***<CAPIE> is "1".

The conditions of comparing with the counter value and the registers, ***[ENxSCMP]***<SCMP[31:0]>, ***[ENxMCMP]***<MCMP[31:0]>, ***[ENxINT]***<INT[31:0]>, are set beforehand.
The interrupt signal INTENCx1 occurs when it is detected that the set conditions are fulfilled. When the corresponding bit in ***[ENxINTCR]*** is set to "0", it is disabled. When setting to "1", it is enabled.

For details, Refer to "3.3.4. Interrupt Control".

3.2.3.3. Example of Operation

Figure 3.10 is shown the example of operation when the ENCxZ pin input is disabled.
The operation conditions are shown below.

(1) When the value of counter becomes "0x000000006", an INT matching interrupt occurs. And the counter is not cleared at this time. (***[ENxINT]***<INT[31:0]> = 0x00000006, ***[ENxINTCR]***<CMPIE> = 1 ***[ENxTNCR]***<CMPSEL> = 1))

(2) When the value of counter becomes "0x000000032", an RELOAD matching interrupt occurs. At this time, a counter is cleared to "0x00000000" and is counted continuously. (***[ENxINT]***<RELOAD[31:0]> = 0x00000032, ***[ENxINTCR]***<RLDIE> = 1, ***[ENxTNCR]***<TOVMOD> = 0))

(3) A counter value is cleared to "0x00000000" by setting ***[ENxTNCR]***<ENCLR> to "1".

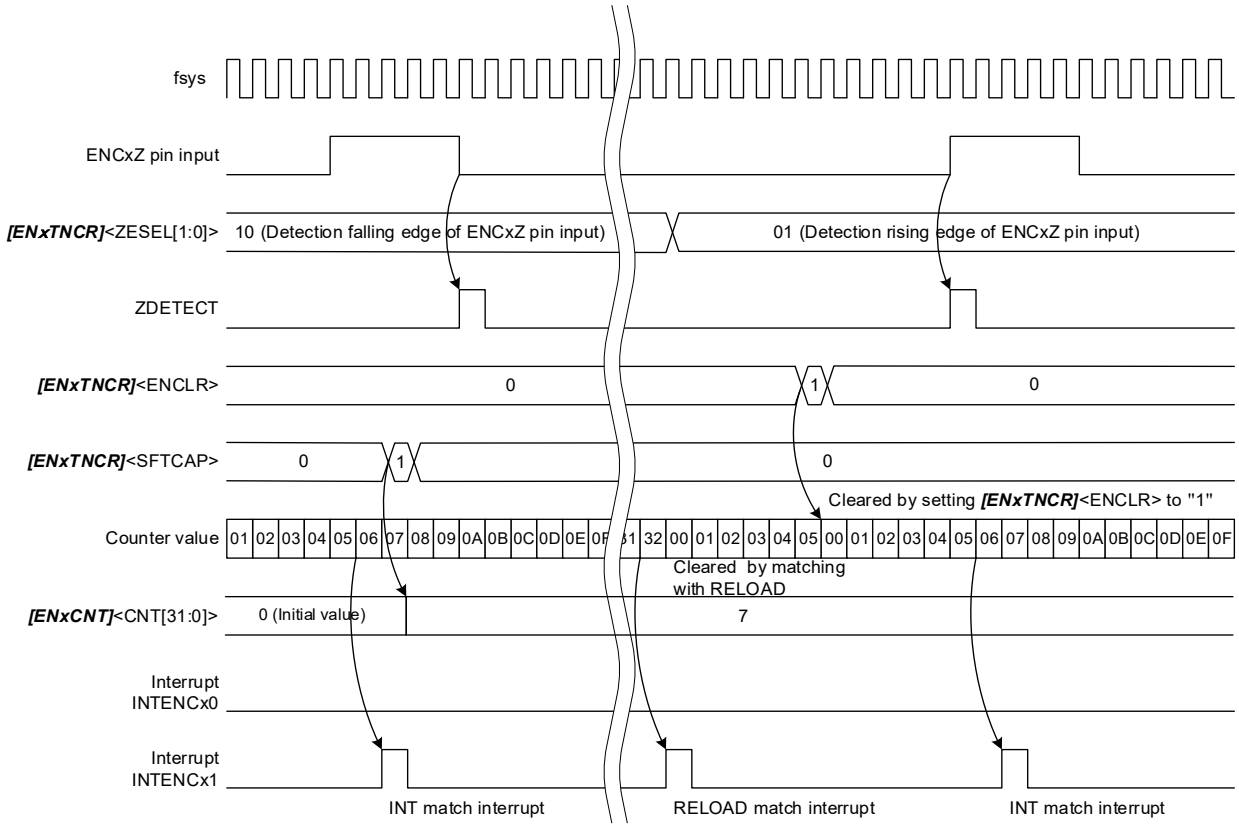

Figure 3.10 When ENCxZ Pin Input is Disabled. (*[ENxTNCR]*<ZEN> = 0)

Figure 3.11 is shown an example of operation when the ENCxZ pin input is enabled.
The operation conditions are shown below.

(1) When the value of counter becomes "0x000000006", an INT matching interrupt occurs. And the counter is not cleared at this time. (***[ENxINT]***<INT[31:0]> = 0x00000006, ***[ENxINTCR]***<CMPIE> = 1 ***[ENxTNCR]***<CMPSEL> = 1))

(2) When the value of counter becomes "0x000000032", an RELOAD matching interrupt occurs. At this time, a counter is cleared to "0x00000000" and is counted continuously. (***[ENxRELOAD]***<RELOAD[31:0]> = 0x00000032, ***[ENxINTCR]***<RLDIE> = 1, ***[ENxTNCR]***<TOVMOD> = 0))

(3) The value of the counter is captured, and a counter is cleared to "0x00000000" by the ZDETECT. A capture interrupt occurs. (***[ENxTNCR]***<TRGCAPMD> = 0, ***[ENxINTCR]***<CAPIE> = 1)

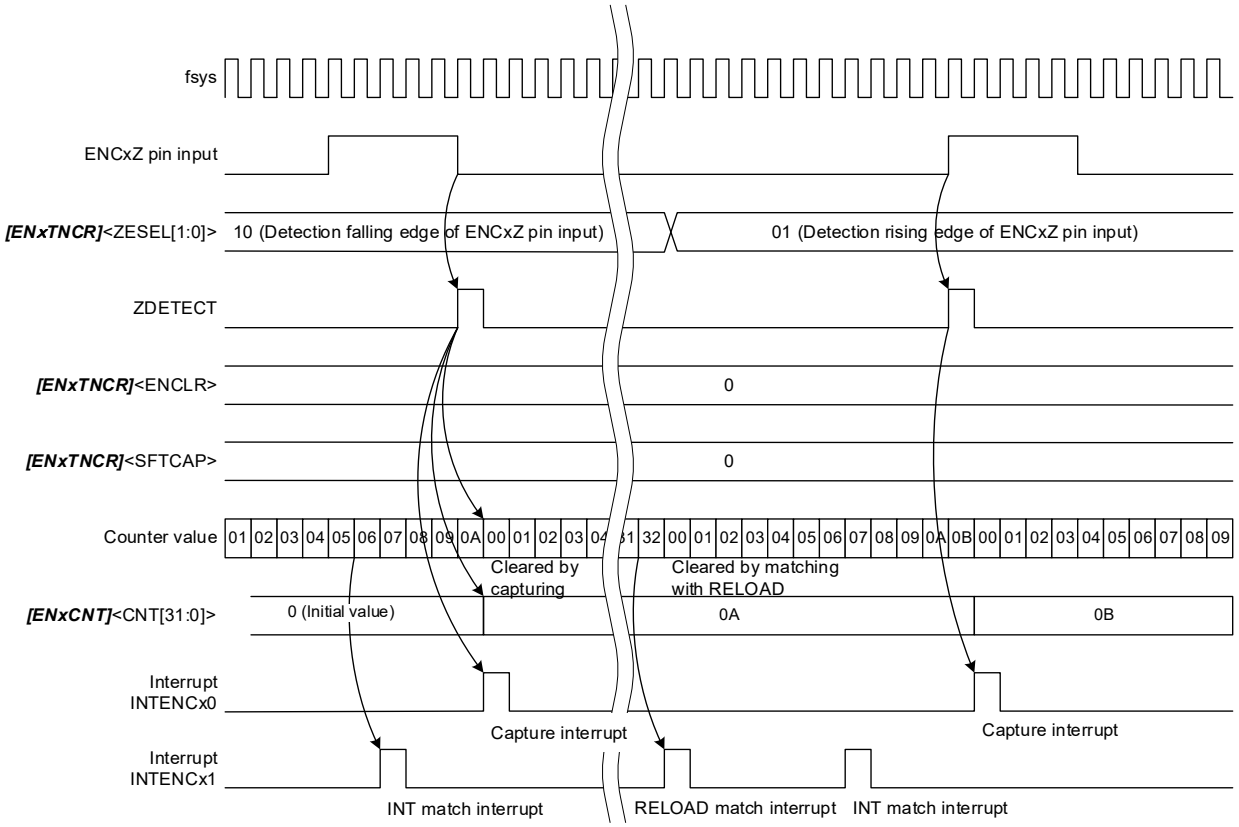

Figure 3.11 When ENCxZ Pin Input is Enabled. (*[ENxTNCR]*<ZEN> = 1)

3.2.4. Phase Counter Mode

In the phase counter mode, a counter counts up and down by the clock specified with ***[ENxRATE]***<RATE[15:0]>.

In the phase counter mode, A-ENC2 performs the below operations.

(1) Phase measurement

(2) Phase difference measurement
The phase difference between ENCxZ pin input and ENCxPSGI can be measured.

3.2.4.1. Phase Measurement

(1) Features

- The counter value is captured by ***[ENxTNCR]***<SFTCAP> and ZDETECT (edge detection signal of ENCxZ pin input) and it can be read from ***[ENxCNT]***<CNT[31:0]>.
- The factor to clear a counter is selected from a soft clear, compare match clear, or external trigger.
- An interrupt occurs when a counter value is captured by the ZDETECT (edge detection signal of ENCxZ pin input).
- An interrupt occurs when A-ENC2 detects that the counter value satisfies the set condition.

(2) Operations

A-ENC2 operates in the phase counter mode (phase measurement) when ***[ENxTNCR]***<MODE[2:0]> = 111, ***[ENxTNCR]***<ZEN> = arbitrary value, ***[ENxTNCR]***<P3EN> = 0.

In the phase counter mode (phase measurement), the below functions can be set.

(a) Detection of a rotation direction
In the phase counter mode (phase measurement), a detection of a rotation direction is not performed.

(b) Control for ENCxZ pin input
ENCxZ pin input is used as an external trigger.
ENCxZ pin input can be enabled and disabled by ***[ENxTNCR]***<ZEN>. When ***[ENxTNCR]***<ZEN> is "0", ENCxZ pin input is disabled. When it is "1", ENCxZ pin input is enabled.

(c) Counter operation
A counter in the phase counter mode (phase measurement) counts the clock specified by ***[ENxTNCR]***<UDMD[1:0]> and ***[ENxRATE]***<RATE[15:0]>.
For details, refer to "3.3.3.3. Sensor Mode (Phase Count) and Phase Counter Mode".

The counter is cleared to "0x00000000" when ***[ENxTNCR]***<ENCLR> is set to "1".

A counter value and registers' values are compared by the condition set beforehand and the satisfaction of the conditions can be detected.

(i) Comparing condition for ***[ENxRELOAD]***<RELOAD[31:0]>
Only matching can be detected.

(ii) Comparing condition for ***[ENxINT]***<INT[31:0]>
Only matching can be detected.

(iii) Comparing condition for ***[ENxMCMP]***<MCMP[31:0]>
Only matching can be detected.

(iv) Comparing condition for ***[ENxSCMP]***<SCMP[31:0]>
Only matching can be detected

(d) Error detection
A skip judgment is not performed in the phase counter mode (phase measurement).
An abnormal input judgement is not performed in the phase counter mode (phase measurement).
A bit reversed skip judgment is not performed in the phase counter mode (phase measurement).
An edge detection error judgement is not performed in the phase counter mode (phase measurement).

(e) Interrupts
The interrupt signal INTENCx0 occurs at capturing timing by ZDETECT. It is disabled when ***[ENxINTCR]***<CAPIE> is "0". It is enabled when ***[ENxINTCR]***<CAPIE> is "1".

The conditions of comparing with the counter value and the registers, ***[ENxSCMP]***<SCMP[31:0]>, ***[ENxMCMP]***<MCMP[31:0]>, ***[ENxINT]***<INT[31:0]>, and ***[ENxRELOAD]***<RELOAD[31:0]> are set beforehand.
The interrupt signal INTENCx1 occurs when it is detected that the set conditions are fulfilled. When the corresponding bit in ***[ENxINTCR]*** is set to "0", it is disabled. When setting to "1", it is enabled.

For details, Refer to "3.3.4. Interrupt Control".

(3) Examples of Operation

Figure 3.12 is shown the example of operation when the ENCxZ pin input is disabled.
The operation conditions are shown below.

(a) When the value of counter becomes "0x000000006", an INT matching interrupt occurs. And the counter is not cleared at this time. (***[ENxINT]***<INT[31:0]> = 0x00000006, ***[ENxINTCR]***<CMPIE> = 1 ***[ENxTNCR]***<CMPSEL> = 1))

(b) When the value of counter becomes "0x000000032", an RELOAD matching interrupt occurs. At this time, a counter is cleared to "0x00000000" and is counted continuously. (***[ENxINT]***<RELOAD[31:0]> = 0x00000032, ***[ENxINTCR]***<RLDIE> = 1, ***[ENxTNCR]***<TOVMOD> = 0))

(c) A counter value is cleared to "0x00000000" by setting ***[ENxTNCR]***<ENCLR> to "1".

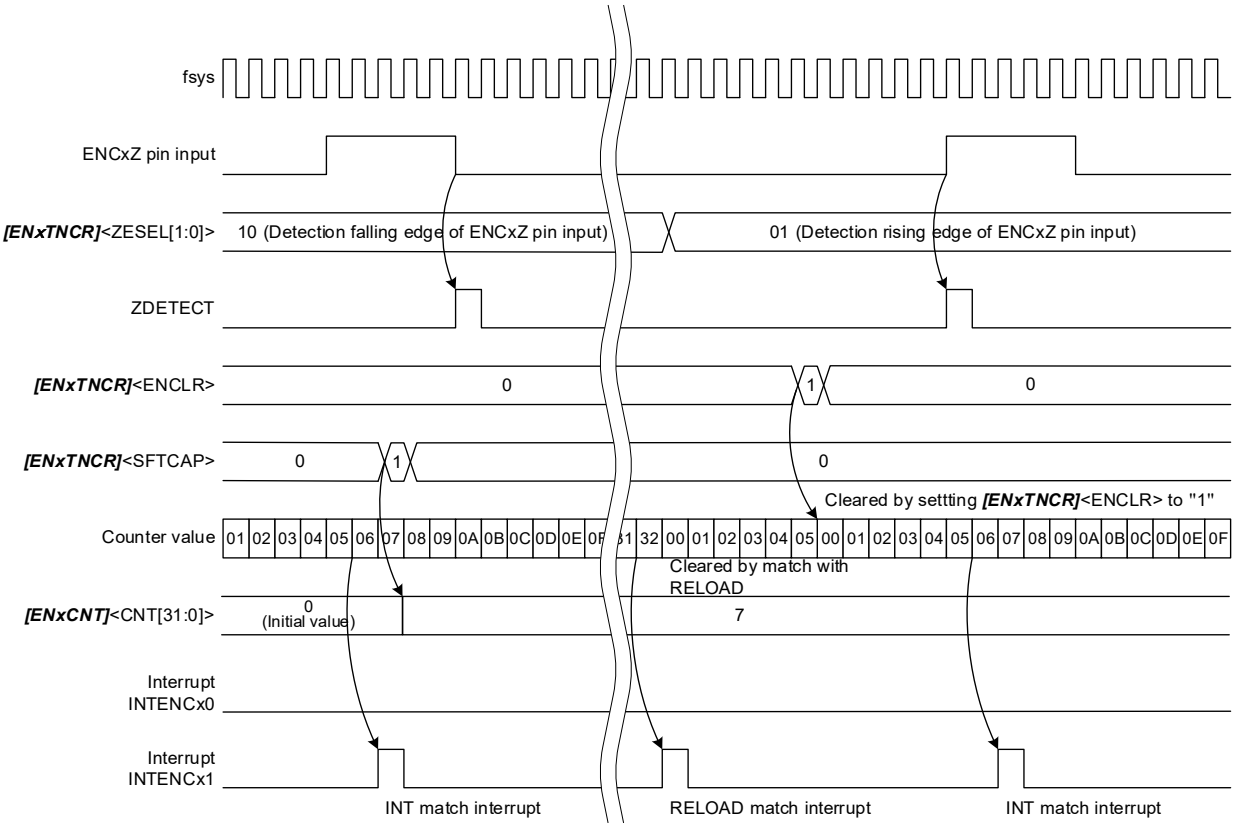

Figure 3.12 When ENCxZ Pin Input is Disabled. (*[ENxTNCR]*<ZEN> = 0)

Figure 3.13 is shown an example of operation when the ENCxZ pin input is enabled.
The operation conditions are shown below.

(a) When the value of counter becomes "0x000000006", an INT matching interrupt occurs. And the counter is not cleared at this time. (***[ENxINT]***<INT[31:0]> = 0x00000006, ***[ENxINTCR]***<CMPIE> = 1 ***[ENxTNCR]***<CMPSEL> = 1))

(b) When the value of counter becomes "0x000000032", an RELOAD matching interrupt occurs. At this time, a counter is cleared to "0x00000000" and is counted continuously. (***[ENxINT]***<RELOAD[31:0]> = 0x00000032, ***[ENxINTCR]***<RLDIE> = 1, ***[ENxTNCR]***<TOVMOD> = 0))

(c) The value of the counter is captured, and a counter is cleared to "0x00000000" by the ZDETECT. A capture interrupt occurs. (***[ENxTNCR]***<TRGCAPMD> = 0, ***[ENxINTCR]***<CAPIE> = 1)

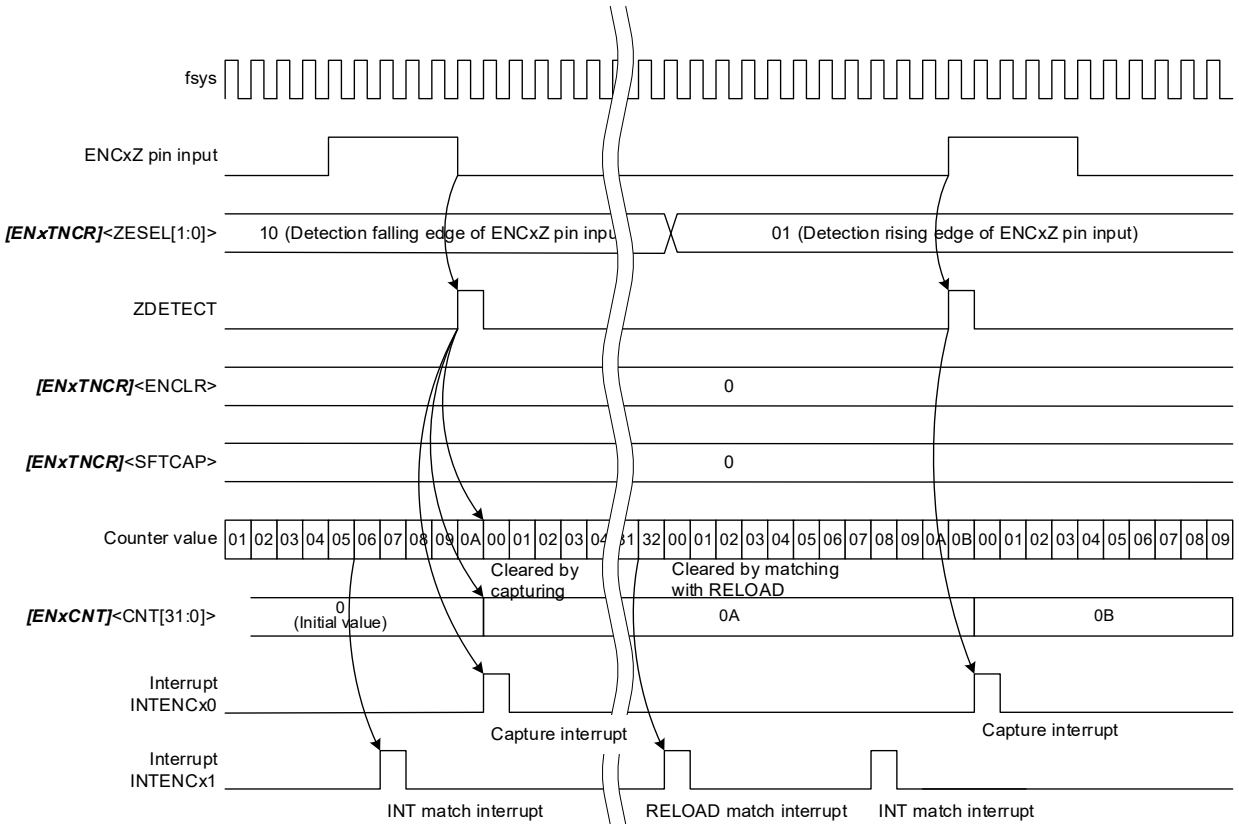

Figure 3.13 When ENCxZ Pin Input is Enabled. (*[ENxTNCR]*<ZEN> = 1)

3.2.4.2. Phase Difference Measurement

(1) Features

- A counter in the phase difference measurement mode, a counter counts up or down depending on the combination (PZAXOR) with ENCxZ pin input and ENCxPSGI.
- The counter value is captured by ***[ENxTNCR]***<SFTCAP> and ZDETECT (edge detection signal of ENCxPSGI) and it can be read from ***[ENxCNT]***<CNT[31:0]>.
- An interrupt occurs when a counter value is captured by the ZDETECT (edge detection signal of ENCxPSGI).
- An interrupt occurs when A-ENC2 detects that the counter value satisfies the set condition.

(2) Operations

A-ENC2 operates in the phase counter mode (phase measurement) when ***[ENxTNCR]***<MODE[2:0]> = 111, ***[ENxTNCR]***<ZEN> = 1, ***[ENxTNCR]***<P3EN> = 1.

[ENxRELOAD]<RELOAD[31:0]> is set that the capture value is "0x00000000" by the ENCxPSGI when the phase difference between ENCxZ pin input and ENCxPSGI is 1 / 4. The phase difference between ENCxZ pin input and ENCxPSGI can be calculated by the captured value as the variation from setting state.

In the phase counter mode (phase difference measurement), the below functions can be set.

(a) Detection of a rotation direction
In the phase counter mode (phase measurement), a detection of a rotation direction is not performed.

(b) Control for ENCxZ pin input
[ENxTNCR]<ZEN> must be set to "1" in the phase counter (phase difference measurement).

(c) Counter operation
A counter in the phase counter mode (phase measurement) counts the clock specified by ***[ENxRATE]***<RATE[15:0]>.
The up and down for counter is controlled by PZXOR.

For details, refer to "3.3.3.3. Sensor Mode (Phase Count) and Phase Counter Mode".

The counter is cleared to "0x00000000" when ***[ENxTNCR]***<ENCLR> is set to "1".

A counter value and registers' values are compared by the condition set beforehand and the satisfaction of the conditions can be detected.

(i) Comparing condition for ***[ENxRELOAD]***<RELOAD[31:0]>
Only matching can be detected.

(ii) Comparing condition for ***[ENxINT]***<INT[31:0]>
Only matching can be detected.

(iii) Comparing condition for ***[ENxMCMP]***<MCMP[31:0]>
Only matching can be detected.

(iv) Comparing condition for ***[ENxSCMP]***<SCMP[31:0]>
Only matching can be detected

(d) Error detection
A skip judgment is not performed in the phase counter mode (phase difference measurement).
An abnormal input judgement is not performed in the phase counter mode (phase difference measurement).
A bit reversed skip judgment is not performed in the phase counter mode (phase difference measurement).
An edge detection error judgement is not performed in the phase counter mode (phase difference measurement).

(e) Interrupts
The interrupt signal INTENCx0 occurs at capturing timing by ZDETECT. It is disabled when ***[ENxINTCR]***<CAPIE> is "0". It is enabled when ***[ENxINTCR]***<CAPIE> is "1".

The conditions of comparing with the counter value and the registers, ***[ENxSCMP]***<SCMP[31:0]>, ***[ENxMCMP]***<MCMP[31:0]>, ***[ENxINT]***<INT[31:0]>, and ***[ENxRELOAD]***<RELOAD[31:0]> are set beforehand.
The interrupt signal INTENCx1 occurs when it is detected that the set conditions are fulfilled. When the corresponding bit in ***[ENxINTCR]*** is set to "0", it is disabled. When setting to "1", it is enabled.

For details, Refer to "3.3.4. Interrupt Control".

(3) Example of operation

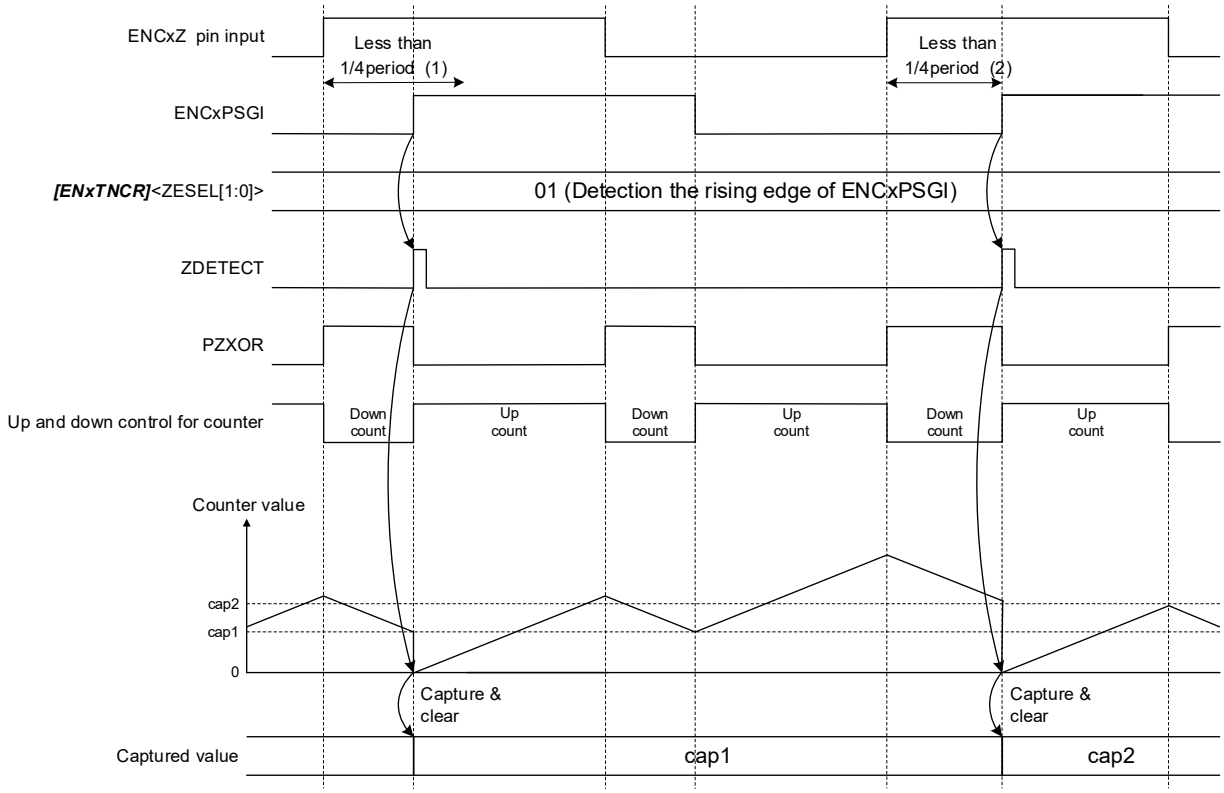

Figure 3.14 Operation in Phase Counter Mode (Phase Difference Measurement) (when Phase Difference is Less Than 1 / 4 Period)

3.3. Function Outlines for Each Circuit

3.3.1. Input Circuit

The input circuit performs an active level setting for ENCxZ pin input, a noise cancellation for ENCxA, ENCxB, and ENCxZ pin inputs by a digital noise filter, and BEMF detection phase limited control.

Debug output monitor
The signals of debug output monitor are shown below.
A symbol (a) to (d) indicates each signal in a figure.
a) BEMF filter input signals
b) Noise canceler input signals
c) Decoder input signals
d) Sampling signal for FF

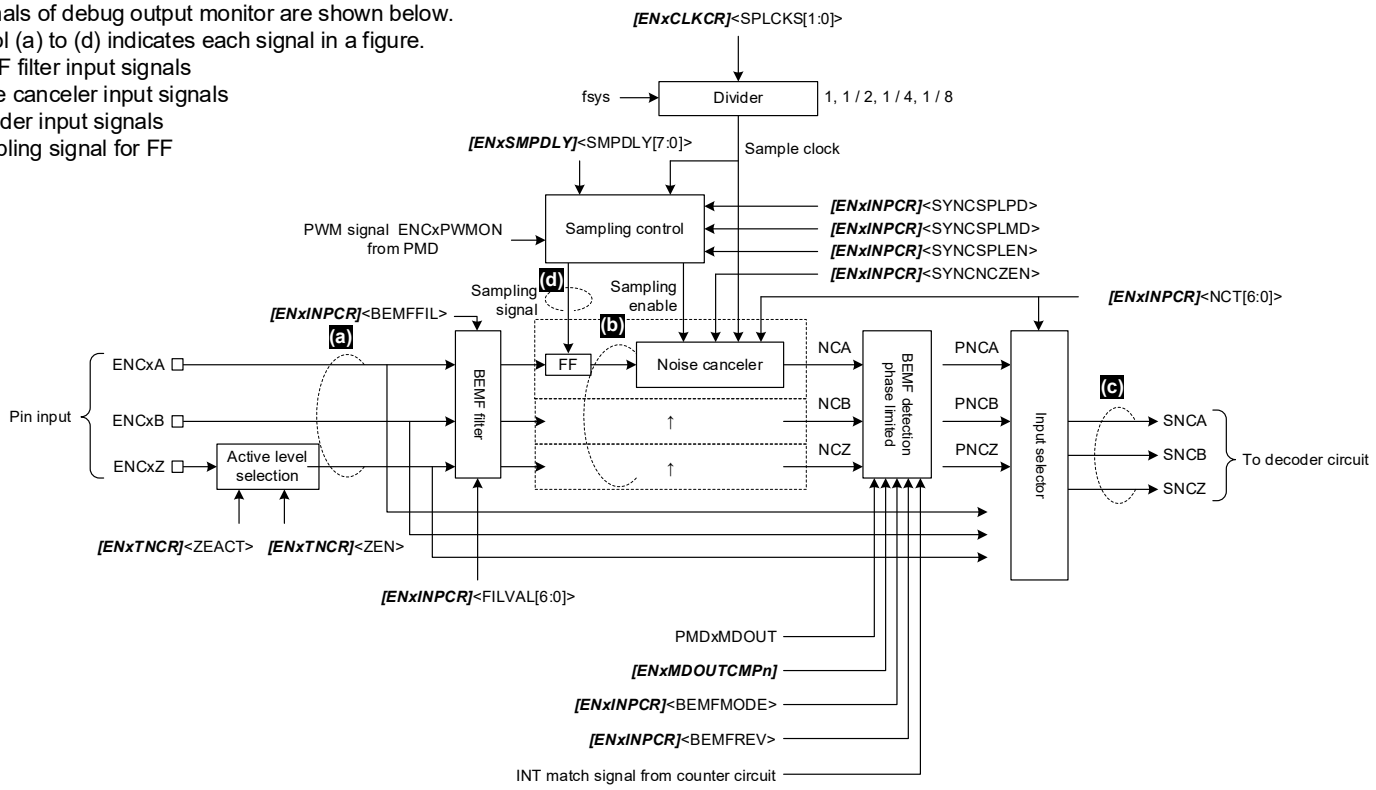

Figure 3.15 Configuration of Input Circuit

3.3.1.1. ENCxZ Pin Input Active Level Selection

Only in the encoder mode, an active level of ENCxZ pin input can be selected by ***[ENxTNCR]***<ZEACT>.
When ***[ENxTNCR]***<ZEACT> is set to "0", an active level is "High". When setting to "1", it is "Low".

3.3.1.2. Noise Filter

The A-ENC2 has the BEMF filter and noise canceler.
When ***[ENxINPCR]***<NCT[6:0]> is "0", both of them is disabled, an input to noise filter is output as it is.

(1) BEMF filter
The BEMF filter is enabled when ***[ENxINPCR]***<NCT[6:0]> is 0x01 or bigger, ***[ENxINPCR]***<FILVAL[6:0]> is 0x01 or bigger, and ***[ENxINPCR]***<BEMFFIL> is "1".
When the signals input to BEMF filter are sampled by fsys and they are matched times specified by ***[ENxINPCR]***<FILVAL[6:0]> continuously, the level of output signal from BEMF filter changes.
The out level of BEMF filter is "Low" after releasing reset.

(a) Sampling signal
The sampling signal of BEMF filter is fsys.

(b) Noise cancel operation
The noise cancel time is specified by ***[ENxINPCR]***<FILVAL[6:0]>.

Noise cancel time: ***[ENxINPCR]***<FILVAL[6:0]> × period of fsys

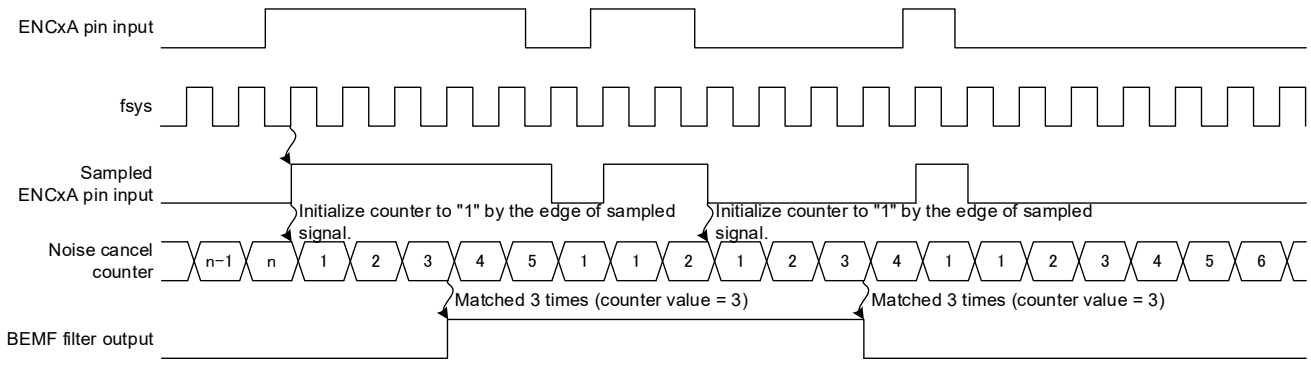

Figure 3.16 Noise Cancel Operation of BEMF Filter (*[ENxINPCR]*<FILVAL[6:0]> = 0x03)

(2) Noise canceler
The noise canceler is enabled ***[ENxINPCR]***<NCT[6:0]> is 0x01 or bigger.
The output signal of BEMF filter is sampled by the clock specified by ***[ENxCLKCR]***<SPLCKS[1:0]> and the sampling signal generated from ENCxPWMON.
When the sampled signals are matched times specified by ***[ENxINPCR]***<NCT[6:0]> continuously, the level of output signal from noise canceler changes.

(a) Sampling signal
The sampling signals are the clock specified by ***[ENxCLKCR]***<SPLCKS[1:0]> and the sampling signal generated from ENCxPWMON. The sampling signal depends on a sampling mode.

Note: The delay time of the first sampling may not be same as one specified by ***[ENxSMPDLY]***<SMPDLY[7:0]> after A-ENC2 operation is from disabled to enabled.

(i) Continuous sampling mode
When ***[ENxINPCR]***<SYNCSPLEN> is "0", a sampling mode is the continuous sampling mode. A sampling signal is a sample clock.

(ii) PWM synchronous sampling mode
When ***[ENxINPCR]***<SYNCSPLEN> is "1", a sampling mode is the PWM synchronous sampling mode. A sampling is synchronously performed with ENCxPWMON from PMD.

- PWM-on period sampling mode
When ***[ENxINPCR]***<SYNCSPLPD><SYNCSPLMD> is "00", a sampling mode is the PWM-on period sampling mode.
Only during ENCxPWMON is "High", an input signal of noise canceler is sampled by a sample clock.
The delay time after ENCxPWMON is becomes "High" before sampling starts is specified by ***[ENxSMPDLY]***<SMPDLY[7:0]>.

Delay time: ***[ENxSMPDLY]***<SMPDLY[7:0]> × period of sample clock

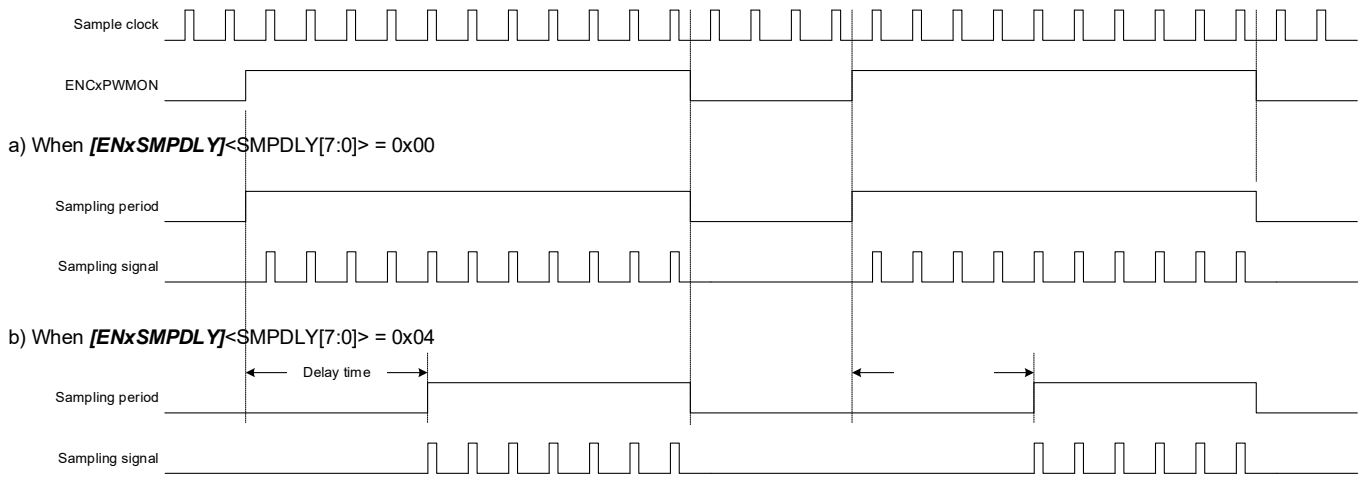

Figure 3.17 Sampling Signal in PWM-on Period Sampling Mode

- PWM-off period sampling mode
  When ***[ENxINPCR]***<SYNCSPLPD><SYNCSPLMD> is "10", a sampling mode is the PWM-off period sampling mode.
  Only during ENCxPWMON is "Low", an input signal of noise canceler is sampled by a sample clock.
  The delay time after ENCxPWMON is becomes "Low" before sampling starts is specified by ***[ENxSMPDLY]***<SMPDLY[7:0]>.

  Delay time: ***[ENxSMPDLY]***<SMPDLY[7:0]> × period of sample clock

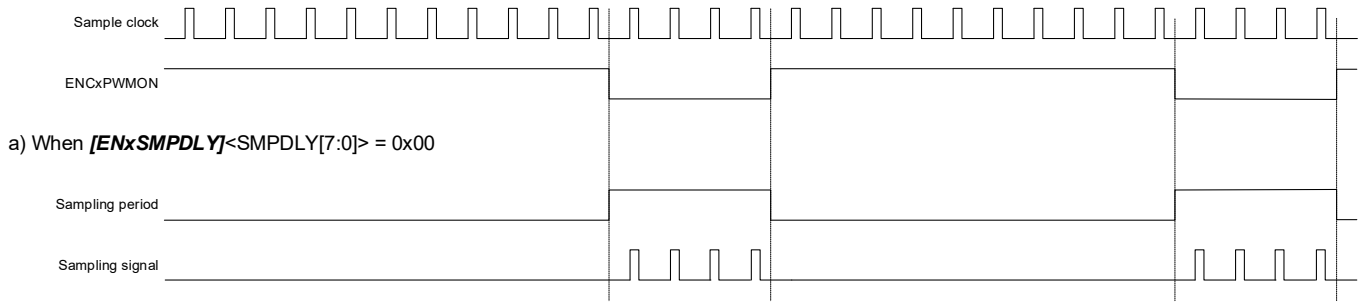

Figure 3.18 Sampling Signal in PWM-off Period Sampling Mode

- PWN-on edge sampling mode
  When ***[ENxINPCR]***<SYNCSPLPD><SYNCSPLMD> is "11", a sampling mode is the PWM-off period sampling mode.
  The sampling signal is ENCxPWMON. An input signal of noise canceler is sampled by the rising edge of ENCxPWMON.

- PWN-off edge sampling mode
  When ***[ENxINPCR]***<SYNCSPLPD><SYNCSPLMD> is "01", a sampling mode is the PWM-on period sampling mode.
  The sampling signal is ENCxPWMON. An input signal of noise canceler is sampled by the falling edge of ENCxPWMON.

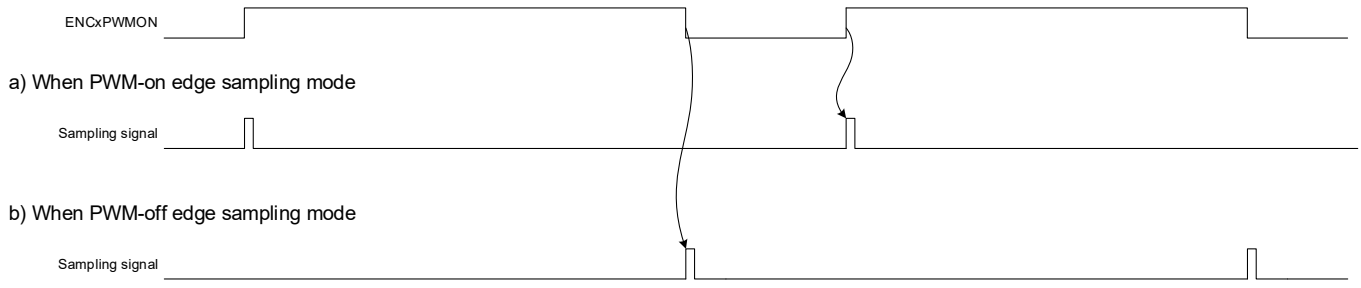

Figure 3.19 Sampling Signal in PWM-on Edge Sampling Mode and PWM-off Edge Sampling Mode

(b) Noise cancel operation
The noise cancel operation is performed only in the continuous sampling mode and PWM-on period sampling mode. The example of the output of BEMF filter for ENCxA pin input is shown below.

(i) In continuous sampling mode
The sample clock is used as a sampling signal.
The noise cancel time is specified by ***[ENxINPCR]***<FILVAL[6:0]>.

Noise cancel time: ***[ENxINPCR]***<NCT[6:0]> × period of sampling signal

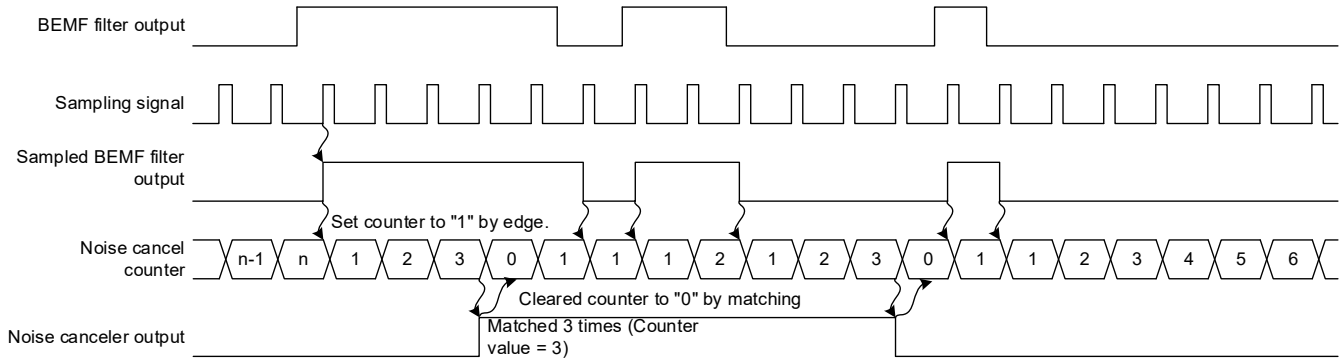

Figure 3.20 Noise Cancel Operation in Continuous Sampling Mode (*[ENxINPCR]*<NCT[6:0]> = 0x03)

(ii) In PWM-on period sampling mode
In PWM-on period sampling mode, the noise cancel operation is performed.
The sampling signal described in "(a) Sampling signal (ii)" is used.
A noise cancel counter is controlled by ***[ENxINPCR]***<SYNCNCZEN>.
When ***[ENxINPCR]***<SYNCNCZEN> is "0", a counter stops counting during the ENCxPWMON is "Low".
When ***[ENxINPCR]***<SYNCNCZEN> is "1", a counter is cleared to "0x00000000" during the ENCxPWMON is "Low".

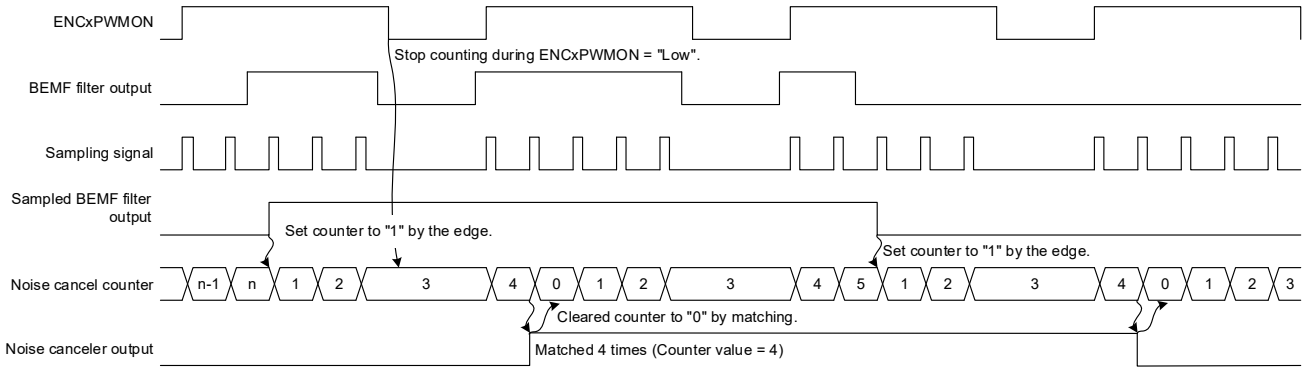

Figure 3.21 Noise Cancel Operation in PWM-on Period Sampling Mode (Counting Stop during PWM-off Period (*[ENxINPCR]*<SYNCNCZEN> = 0))

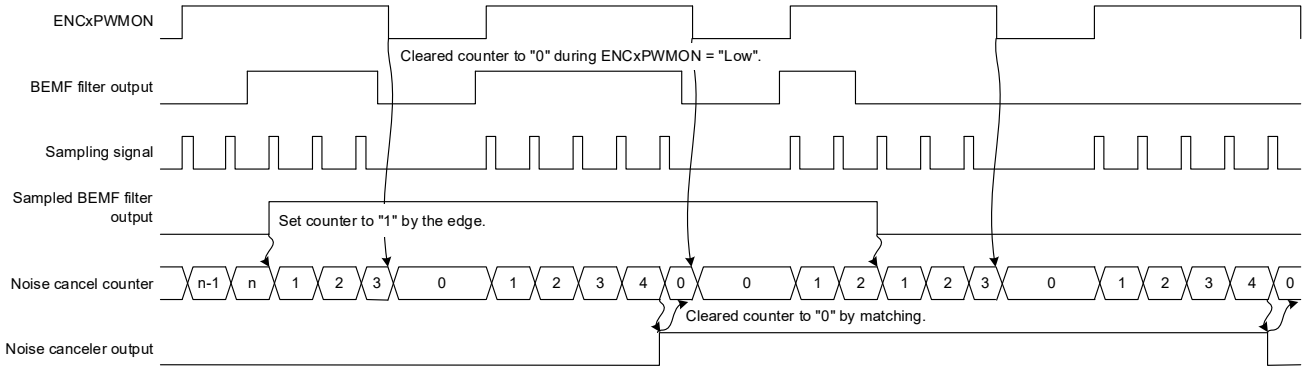

Figure 3.22 Noise Cancel Operation in PWM-on Period Sampling Mode (Cleared Counter during PWM-off Period (*[ENxINPCR]*<SYNCNCZEN> = 1))

3.3.1.3. BEMF Phase Detection Limited Control

The BEMF phase detection limited control can prevent the malfunction of A-ENC2 by detecting only the induced voltage zero-cross of the Hi-Z phase when A-ENC2 is used in sensor mode and the sensor-less square pulse drive is performed by zero-cross detection of induced voltage.

The BEMF phase detection limited control is enabled when ***[ENxINPCR]***<NCT[6:0]> is 0x01 or bigger and ***[ENxINPCR]***<BEMFFIL> is set to "1".

The target detection phase of induced voltage zero cross is determined and is output to the decoder depending on the phase determined by comparison with PMDxMDOUT from the PMD and ***[ENxMDOUTCMPn]*** (n = 0 to 5).

(1) Phase decision and detecting way

The six phases phase 0 to 5 are defined depending on the electric angle in 120-degree conduction control. And phase x is defined as the state when ***[ENxTNCR]***<ENRUN> is "0".

[ENxMDOUTCMPn] (n = 0 to 5) are assigned to each phase 0 to 5.

In ***[ENxMDOUTCMPn]***, the comparison conditions (such as the value compared with each signal of PMDxMDOUT from the PMD and the information of comparison enable/disable) are stored.

When modifying the PMDxMDOUT or ***[ENxMDOUTCMPn]***, the PMDxMDOUT is checked to fulfill the conditions in ***[ENxMDOUTCMPn]***. If fulfilled, the n is assigned as a current phase number. At this time, the phase number modified is stored as previous phase number.

Table 3.2 Decision of Electric Angle and Phase (CW Direction)

Electric angle (degree)	Phase
330 to 30	phase 0
30 to 90	phase 1
90 to 150	phase 2
150 to 210	phase 3
210 to 270	phase 4
270 to 330	phase 5

Note: If no condition is fulfilled, a previous phase number is retained as a current phase number.

(2) Phase and Output to Decoder
PNCA, PNCB, and PNCZ to decoder are defined by the combination with current and previous phase number and ***[ENxINPCR]***<BEMFREV>.
A detecting target phase of induced voltage zero cross is indicated as "L detect" and "H detect" in Table 3.3 and Table 3.4.

To avoid an error detection by the ringing generated at switching the energized phase, the previous of PNCA, PNCB, and PNCZ are output until INT match occurs, then the defined PNCA, PNCB, and PNCZ are output.

Table 3.3 Detecting Target Phase when *[ENxINPCR]*<BEMFREV> is "0" (CW Direction)

Previous phase	Current phase	PNCA	PNCB	PNCZ	Target range of electrical angel (degree)
phase 5	phase 0	(H→) L DETECT	H (Fixed)	L (Fixed)	330 to 30
phase 0	phase 1	L (Fixed)	H (Fixed)	(L→) H DETECT	30 to 90
phase 1	phase 2	L (Fixed)	(H→) L DETECT	H (Fixed)	90 to 150
phase 2	phase 3	(L→) H DETECT	L (Fixed)	H (Fixed)	150 to 210
phase 3	phase 4	H (Fixed)	L (Fixed)	(H→) L DETECT	210 to 270
phase 4	phase 5	H (Fixed)	(L→) H DETECT	L (Fixed)	270 to 330

Table 3.4 Detecting Target Phase when *[ENxINPCR]*<BEMFREV> is "1" (CCW Direction)

Previous phase	Current phase	PNCA	PNCB	PNCZ	Target range of electrical angel (degree)
phase1	phase0	(L→) H DETECT	H (Fixed)	L (Fixed)	210 to 150
phase0	phase5	H (Fixed)	(H→) L DETECT	L (Fixed)	150 to 90
phase5	phase4	H (Fixed)	L (Fixed)	(L→) H DETECT	90 to 30
phase4	phase3	(H→) L DETECT	L (Fixed)	H (Fixed)	30 to 330
phase3	phase2	L (Fixed)	(L→) H DETECT	H (Fixed)	330 to 270
phase2	phase1	L (Fixed)	H (Fixed)	(H→) L DETECT	270 to 210

Note1: PNCA, PNCB, and PNCZ does not match the values in Table 3.3and Table 3.4 until the combination with previous phase and current phase are matched with one in Table 3.3 and Table 3.4 after setting ***[ENxTNCR]***<ENRUN> to "1"

Note2: The PNCA, PNCB, and PNCZ keep the decides ones in spite of the changing inputs of BEMF detection phase limited circuit after PNCA, PNCB, and PNCZ are decided by the 3.3.1.3. BEMF Phase Detection Limited Control.

3.3.1.4. Debug Output Monitor

The internal signals in the input circuit can be monitored via PMDxDEBUG pin. The signals monitored as a debug monitor signal are shown in Figure 3.15. The output for each debug monitor signal can be enabled and disabled by the corresponding bit field of ***[ENxDBGOEN]***.

Regarding PMDxDEBUG pin output, refer to the reference manual "Advanced Motor Control Circuit 2".

Note1: When ***[ENxDBGOEN]***<BEMF150> is set to "1", other bits must be set to "0".

Note2: When ***[ENxDBGOEN]***<BEMF120> is set to "1", other bits must be set to "0".

3.3.2. Decoder

A rotation edge detection and generation of edge pulse are performed by the decoder depending on SNCA, SNCB, and SNCZ via the input circuit.

And a zero cross detection mask for sensor-less square pulse drive is also performed.

The error detection (skip judgement, abnormal input judgement, reversed skip judgement, and edge detection error judgement) for the encoder inputs is performed by SNCA, SNCB, and SNCZ.

The edge detection of ENCxZ pin input is performed from SNCZ

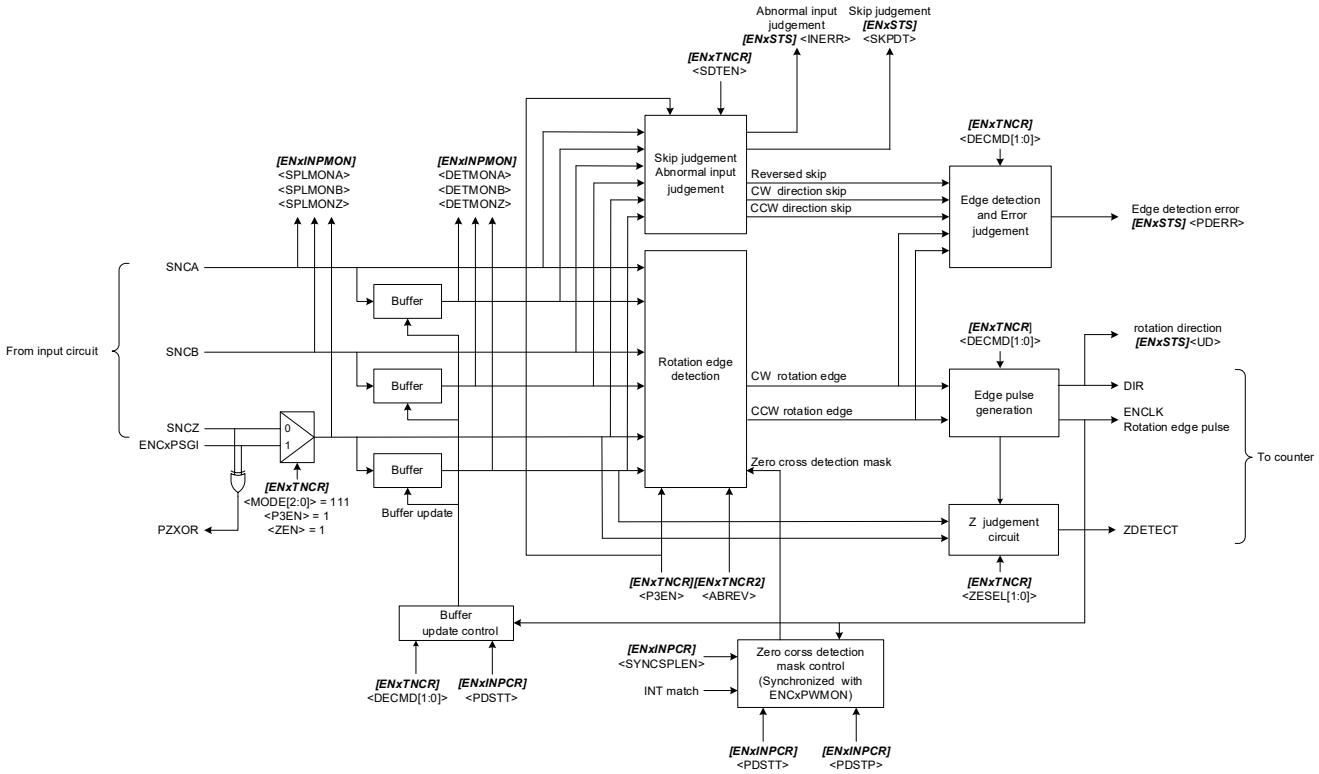

Figure 3.23 Configuration of Decoder

3.3.2.1. Rotation Edge and Rotation Direction Detection

A rotation edge and rotation direction detection are described for each decode mode.

(1) 2-phase decode mode (***[ENxTNCR]***<P3EN> = 0)
2-phase decode mode is used in the encoder mode, sensor mode (event count, timer count, phase count), and timer mode.

A rotation edge and rotation direction are detected by the below transition in the 2-phase decode mode. The transition with SNCA and SNCB can be changed by ***[ENxTNCR2]***<ABREV>.

(a) CW direction (***[ENxTNCR2]***<ABREV> = 0)
The transition of (A) → (B), (B) → (C), (C) → (D), and (D) → (A) are detected as a rotation edge. A rotation direction is decided as a CW direction when a transition order is this case and set ***[ENxSTS]***<UD> to "1".

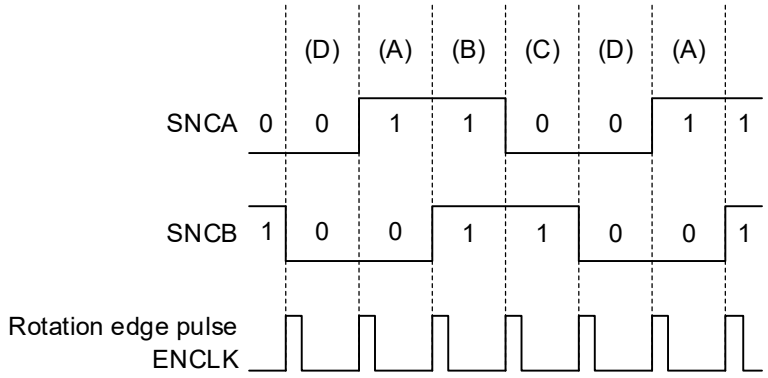

Figure 3.24 SNCA and SNCB Waveform in CW Direction and Rotation Edge Pulse (*[ENxTNCR2]*<ABREV> = 0)

(b) CW direction (***[ENxTNCR2]***<ABREV> = 1)
The transition of (A) → (D), (D) → (C), (C) → (B), and (B) → (A) are detected as a rotation edge. A rotation direction is decided as a CW direction when a transition order is this case and set ***[ENxSTS]***<UD> to "1".

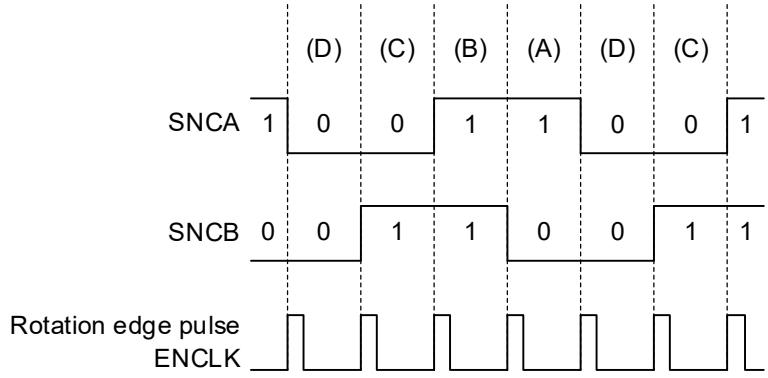

Figure 3.25 SNCA and SNCB Waveform in CW Direction and Rotation Edge Pulse (*[ENxTNCR2]*<ABREV> = 1)

(c) CCW direction (***[ENxTNCR2]***<ABREV> = 0)
The transition of (D) → (C), (C) → (B), (B) → (A), and (A) → (D) are detected as a rotation edge. A rotation direction is decided as a CCW direction when a transition order is this case and set ***[ENxSTS]***<UD> to "0".

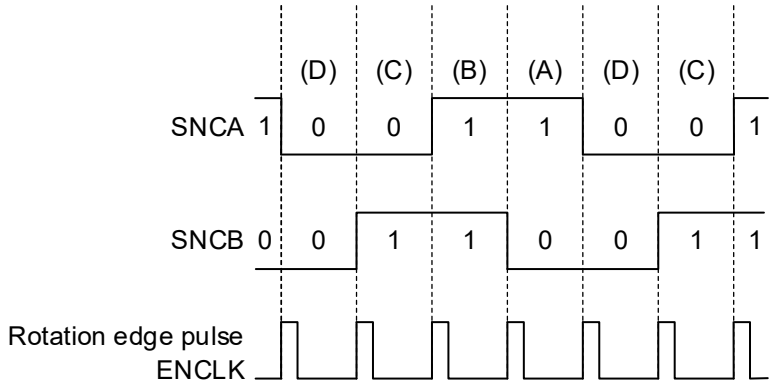

Figure 3.26 SNCA and SNCB Waveform in CCW Direction and Rotation Edge Pulse (*[ENxTNCR2]*<ABREV> = 0)

(d) CCW direction (***[ENxTNCR2]***<ABREV> = 1)
The transition of (D) → (A), (A) → (B), (B) → (C), and (C) → (D) are detected as a rotation edge. A rotation direction is decided as a CCW direction when a transition order is this case and set ***[ENxSTS]***<UD> to "0".

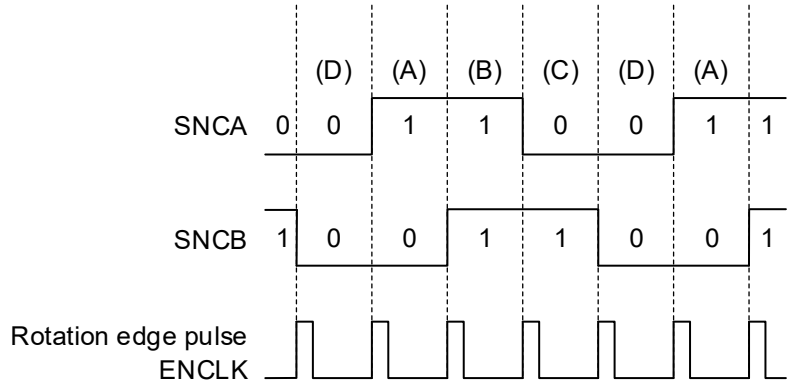

Figure 3.27 SNCA and SNCB Waveform in CCW Direction and Rotation Edge Pulse (*[ENxTNCR2]*<ABREV> = 1)

(2) 3-phase decode mode (***[ENxTNCR]***<P3EN> = 1)
3-phase decode mode is used in the encoder mode, sensor mode (event count, timer count, phase count), and timer mode.

A rotation edge and rotation direction are detected by the below transition in the 3-phase decode mode.

(a) CW direction
The transition of (A) → (B), (B) → (C), (C) → (D), (D) → (E), (E) → (F) and (F) → (A) are detected as a rotation edge. A rotation direction is decided as a CW direction when a transition order is this case and set ***[ENxSTS]***<UD> to "1".

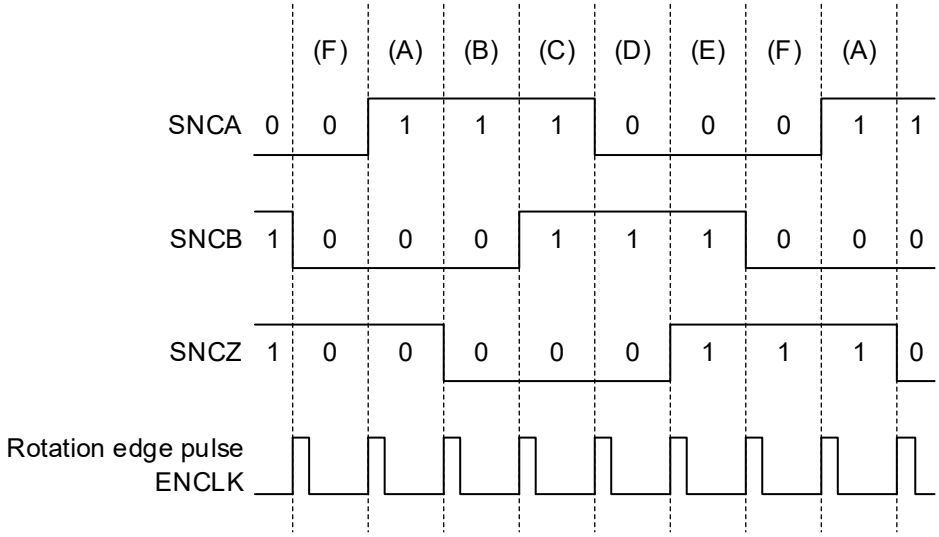

Figure 3.28 SNCA, SNCB and SNCZ Waveform in CW Direction and Rotation Edge Pulse

(b) CCW direction
The transition of (F) → (E), (E) → (D), (D) → (C), (C) → (B), (B) → (A) and (A) → (F) are detected as a rotation edge. A rotation direction is decided as a CCW direction when a transition order is this case and set ***[ENxSTS]***<UD> to "0".

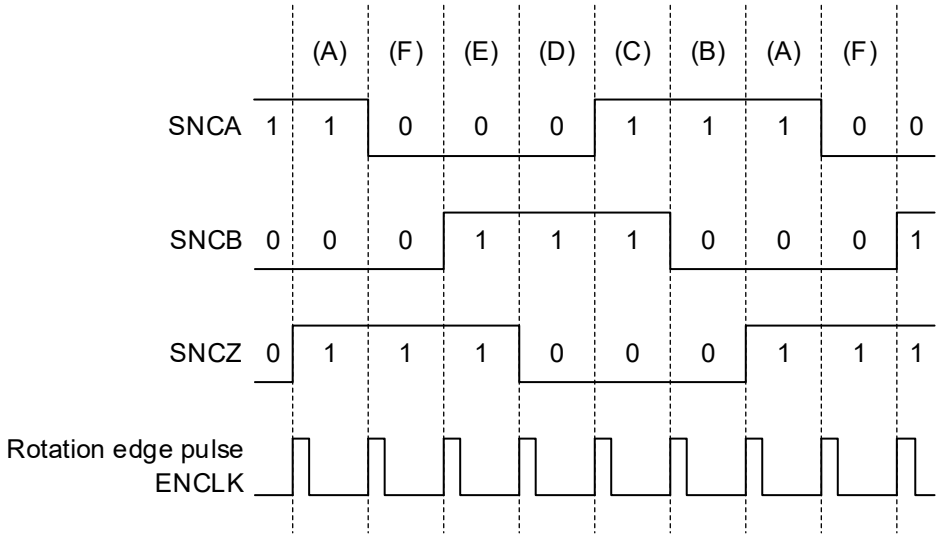

Figure 3.29 SNCA, SNCB and SNCZ Waveform in CCW Direction and Rotation Edge Pulse

3.3.2.2. Z Judgement Circuit

The Z judgement circuit detects the edge of SNCZ.

(1) Encoder mode
The Z judgement circuit detects the rising edge of SNCZ in CW direction and the falling edge of SNCZ in CCW direction. ZDETECT is asserted when detecting the edge and ***[ENxSTS]***<ZDET> is set to "1" at this time.

(2) Timer mode and Phase counter mode
The detection edge of SNCZ can be selected by ***[ENxTNCR]***<ZESEL[1:0]> among a rising edge, falling edge, and both edges. ZDETECT is asserted when detecting the edge.

3.3.2.3. Skip Judgement and Abnormal Input Judgement

(1) Skip judgement
Unexpected transition of SNCA, SNCB, SNCZ generation can be detected in the 3-phase decode mode of sensor mode. This is called as the skip judgement.
When ***[ENxSTS]***<SDTEN> is set to "1", the detection of the skip judgement is enabled.
When the below transits are detected, the decoder judges a generation of unexpected transition and ***[ENxSTS]***<SKPDT> is set to "1". At this time, when ***[ENxINTCR]***<ERRIE> is "1", a detection error interrupt is output from INTENCx0. And also, ***[ENxINTF2]***<ERRF2> is set to "1".

Note: (A) to (F) indicate same ones in Figure 3.28 and Figure 3.29.

(a) CW direction
(A) → (C), (B) → (D), (C) → (E), (D) → (F), (E) → (A) , and (F) → (B)

(b) CCW direction
(A) → (E), (B) → (F), (C) → (A), (D) → (B), (E) → (C) , and (F) → (D)

(2) Reserved judgement
In the 2-phase and 3-phase decode mode, to reverse all of the signals of decoding simultaneously can be detected. This is called as the reversed judgement.

Note: (A) to (F) indicate same ones in Figure 3.28 and Figure 3.29.

(a) 2-phase decode
(A) → (C), (B) → (D), (C) → (A), and (D) → (B)

(b) 3-phase decode
(A) → (D), (D) → (A), (B) → (E), (E) → (B), (C) → (F) , and (F) → (C)

(3) Abnormal input judgement
In 3-phase decode of the sensor mode, changing all of signals SNCA, SNCB, and SNCZ to "0" or "1" simultaneously can be detected. This is called the abnormal input judgement.
When the abnormal input judgement occurs, ***[ENxSTS]***<INERR> is set to "1". At this time, when ***[ENxINTCR]***<ERRIE> is "1", a detection error interrupt is output from INTENCx0. And also, ***[ENxINTF2]***<ERRF2> is set to "1".

3.3.2.4. Edge Detection Error Judgement

In the sensor mode (event count, timer count, phase count), the detection of the direction other than specified one can be judged. This is the edge detection error judgement.

To enable the edge detection error judgement, set ***[ENxTNCR]***<SDTEN> to "1".

The rotation direction to detect is specified by ***[ENxTNCR]<DECMD[1:0]>***.

(1) ***[ENxTNCR]***<DECMD[1:0]> = 01 (detecting only CW direction)
When CCW direction is detected, the edge detection error occurs.

(2) ***[ENxTNCR]***<DECMD[1:0]> = 10 (detecting only CCW direction)
When CW direction is detected, the edge detection error occurs.

Note: When ***[ENxTNCR]***<DECMD[1:0]> = 00 or 11, no edge detection is performed.

When the edge detection error, skip judgement, or reserved judgement occurs, ***[ENxSTS]***<PDERR> is set to "1". At this time, when ***[ENxINTCR]***<ERRIE> is "1", a detection error interrupt is output from INTENCx0. And also, ***[ENxINTF2]***<ERRF2> is set to "1".

3.3.2.5. Examples of Skip Judgement and Edge Detection Error

In the encoder mode and 3-phase decode mode of sensor mode, the combination (A) to (F) shown in Figure 3.28 and Figure 3.29 is shown in about the skip judgement and edge error judgement.

Table 3.5 Skip Judgement and Edge Detection Error Judgement in Detecting CW Direction (*[ENxTNCR]*<DECMD[1:0]> = 01)

		Current state					
		(A)	(B)	(C)	(D)	(E)	(F)
Previous state	(A)	-	Direction of expectation	SKPDT	PDERR	PDERR SKPDT	PDERR
	(B)	PDERR	-	Direction of expectation	SKPDT	PDERR	PDERR SKPDT
	(C)	PDERR SKPDT	PDERR	-	Direction of expectation	SKPDT	PDERR
	(D)	PDERR	PDERR SKPDT	PDERR	-	Direction of expectation	SKPDT
	(E)	SKPDT	PDERR	PDERR SKPDT	PDERR	-	Direction of expectation
	(F)	Direction of expectation	SKPDT	PDERR	PDERR SKPDT	PDERR	-

-: No combination, SKPDT: Skip judgement, PDEER: Edge detection error judgement

Table 3.6 Skip Judgement and Edge Detection Error Judgement in Detecting CCW Direction (*[ENxTNCR]*<DECMD[1:0]> = 10)

		Current state					
		(A)	(B)	(C)	(D)	(E)	(F)
Previous state	(A)	-	PDERR	PDERR SKPDT	PDERR	SKPDT	Direction of expectation
	(B)	Direction of expectation	-	PDERR	PDERR SKPDT	PDERR	SKPDT
	(C)	SKPDT	Direction of expectation	-	PDERR	PDERR SKPDT	PDERR
	(D)	PDERR	SKPDT	Direction of expectation	-	PDERR	PDERR SKPDT
	(E)	PDERR SKPDT	PDERR	SKPDT	Direction of expectation	-	PDERR
	(F)	PDERR	PDERR SKPDT	PDERR	SKPDT	Direction of expectation	-

-: No combination, SKPDT: Skip judgement, PDEER: Edge detection error judgement

3.3.2.6. Buffer Update Control

The buffer update control controls an update timing of the buffer which keeps SNCA, SNCB, and SNCZ for using a rotation direction detection.

An update timing is specified by ***[ENxTNCR]***<DECMD[1:0]>.

(1) ***[ENxTNCR]***<DECMD[1:0]> = 00
A buffer is always updated by fsys.
A rotation direction is judged by detecting a change of SNCA, SNCB, and SNCZ.

(2) ***[ENxTNCR]***<DECMD[1:0]> ≠ 00
The buffer is updated at detecting a rotation edge.
A rotation direction is judged by detecting a change of SNCA, SNCB, and SNCZ at detecting a rotation edge (in ***[ENxINPMON]***<DETMONA>, <DETMONB>, and <DETMONZ>) and the current ones (***[ENxINPMON]***<SPLMONA>, <SPLMONB>, and<SPLMONZ>).

3.3.2.7. Zero Cross Detection Mask Control

To perform the sensor-less square pulse drive by driving the BLDC by square pulse, the zero cross detection mask control is used in the sensor mode (timer count and phase count).

The zero cross detection mask control is enabled in PWM synchronous sampling mode (***[ENxINPCR]***<SYNCSPLEN> = 1).

The zero cross detection mask control controls the stopping and starting of detection rotation edge.
It is controlled by setting ***[ENxINPCR]***<PDSTT> or <PDSTP> to "1" or hardware.

(1) Staring or re-starting of rotation edge detection
The rotation edge detection starts or re-starts by setting ***[ENxINPCR]***<PDSTT> to "1" or by the INT match signal from the counter.

(2) Stopping or terminating of rotation edge detection
The rotation edge detection stops or terminates by setting ***[ENxINPCR]***<PDSTP> to "1" or by the rotation edge detection from the decoder.

3.3.3. Counter

The counter has a 32-bit up and down counter which can be preset, a compare function, and capture function. Each circuit is used depending on the operation mode of A-ENC2.

3.3.3.1. Encoder Mode and Sensor Mode (Event Count)

The counter in the encoder mode and sensor mode (event count) has a 32-bit counter controlled by ENCLK and DIR from the decoder, the compare function compared the value of each ***[ENxRELOAD]***<RELOAD[31:0]>, ***[ENxINT]***<INT[31:0]>, ***[ENxMCMP]***<MCMP[31:0]>, and ***[ENxSCMP]***<SCMP[31:0]> and the value of 32-bit up and down counter and capture function.

(1) 32-bit counter
When DIR = 0, a 32-bit counter counts up by ENCLK.
When DIR = 1, it counts down by ENCLK.

When it stops, a value can be preset to it. The read value can be preset to it when the encoder read the absolute position is connected with the A-ENC2.

The clear and load operation of 32-bit counter are shown below.

(a) Encoder mode (***[ENxTNCR]***<MODE[2:0]> = 000)
(i) Clearing 32-bit counter

- At matching with a counter value and ***[ENxRELOAD]***<RELAOD[31:0]> when DIR = 1
- At matching with states of SNCA, SNCB, and SNCZ and ***[ENxTNCR2]***<ABZCLRVAL[2:0]> When ***[ENxTNCR]***<ZEN> is "1", the zero position of encoder can be specified by the combination of SNCA, SNCB, and SNCZ.

Table 3.7 Setting Value of *[ENxTNCR2]*<ABZCLRVAL[2:0]> and Condition of Clearing Counter

[ENxTNCR2]<ABZCLRVAL[2:0]>	Condition of clearing counter		
	SNCA	SNCB	SNCZ
000	0	0	0
001	0	0	1
010	0	1	0
011	0	1	1
100	1	0	0
101	1	0	1
110	1	1	0
111	1	1	1

Figure 3.30 shows an enlarged timing chart of timing for clearing counter. It shows that the falling edge of signal B is shaken back and forth against the rising edge of signal Z.

In the left figure of Figure 3.30, because of matching the counter clear condition and the values of A, B, and Z, clear the counter to "0".
In the right figure of Figure 3.30, after the counter value "F" equals ***[ENxRELOAD]***<RELOAD[31:0]>, the counter value is cleared because ENCLK occurred due to the falling edge of the signal B. After that, the counter is cleared again because the counter clear condition matches the input values of A, B, and Z.

- When ***[ENxRELOAD]***<RELOAD[31:0]> = 0x0000000F and ***[ENxTNCR2]***<ABZCLRVAL[2:0]> = 001

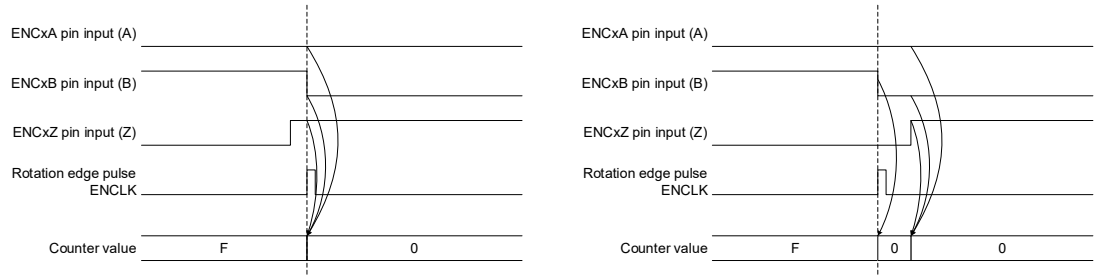

Figure 3.30 Example of Operation when Connecting with Incremental Encoder of ABZ Type

- At setting ***[ENxTNCR]***<ENCLR> to "1"

(ii) Loading the value of ***[ENxRELOAD]***<RELOAD[31:0]> to the counter

- At deciding that the counter value is "0" when DIR = 0

(b) Sensor mode (event count) (***[ENxTNCR]***<MODE[2:0]> = 001)
(i) Clearing 32-bit counter

- At the next ENCLK after the value of counter becomes "0xFFFFFFFF" when DIR = 1
- At setting ***[ENxTNCR]***<ENCLR> to "1"

(ii) Loading 32-bit counter to "0xFFFFFFFF"

At the next ENCLK after the value of counter becomes "0" when DIR = 0

(2) Compare function

- Perform match comparison with the counter value and ***[ENxRELOAD]***<RELOAD[31:0]>.
- Perform match comparison with the counter value and ***[ENxINT]***<INT[31:0]>.
- Perform match comparison with the counter value and ***[ENxMCMP]***<MCMP[31:0]>.
  When ***[ENxINTCR]***<MCMPIE> is "1", the compare result is output to ENCxCTRG0.
- Perform match comparison with the counter value and ***[ENxSCMP]***<SCMP[31:0]>.

Note: When ***[ENxTNCR]***<ZEN> is "1" in the encoder mode, the result of compare the counter value with ***[ENxINT]***<INT[31:0]>, ***[ENxMCMP]***<MCMP[31:0]>, and ***[ENxSCMP]***<SCMP[31:0]> is ignored until ***[ENxSTS]***<ZDET> becomes "1".

(3) Capture function
The value of counter at setting ***[ENxTNCR]***<SFTCAP> to "1" is captured to ***[ENxCNT]***<CNT[31:0]>.

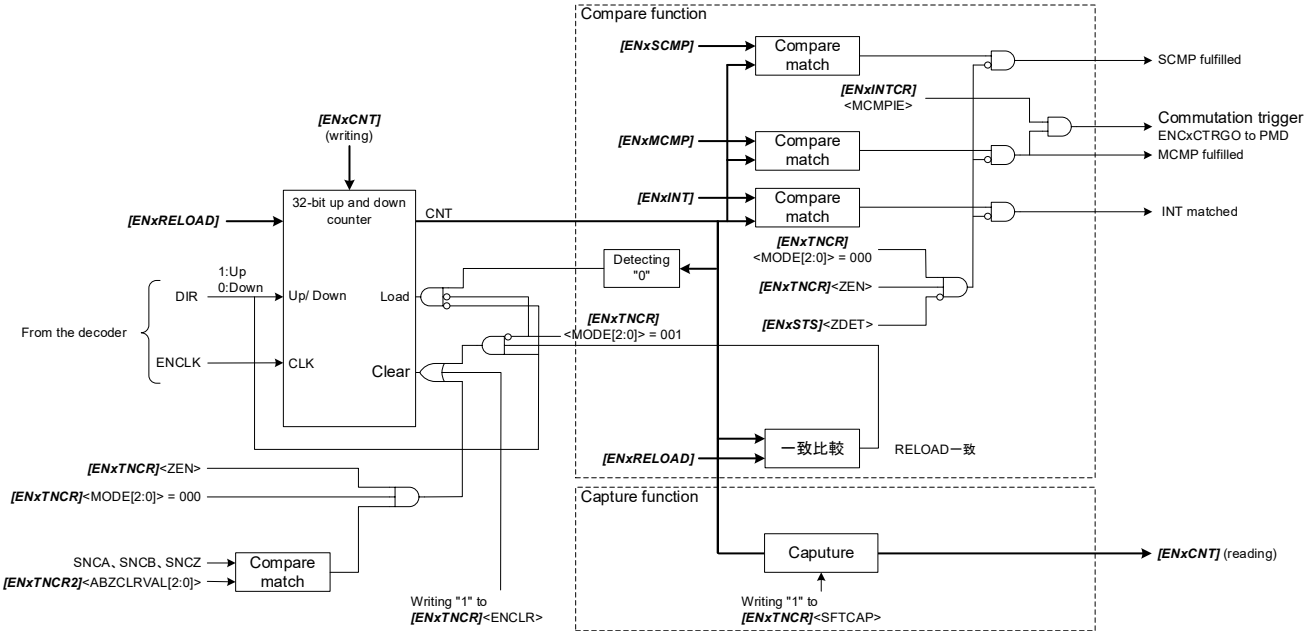

Figure 3.31 Configuration of Counter (in Encoder Mode and Sensor Mode (Event Count))

3.3.3.2. Sensor Mode (Timer Count) and Timer Mode

The counter in the sensor mode (timer count) and timer mode has a 32-bit counter controlled by fsys, the compare function compared the value of each ***[ENxRELOAD]***<RELOAD[31:0]>, ***[ENxINT]***<INT[31:0]>, ***[ENxMCMP]***<MCMP[31:0]>, and ***[ENxSCMP]***<SCMP[31:0]> and the value of 32-bit up and down counter and capture function.

(1) 32-bit counter
A 32-bit counter counts up by fsys.

When it stops, a value can be preset to it.

The clear operation of 32-bit counter is shown below.

(a) Sensor mode (timer counter) (***[ENxTNCR]***<MODE[2:0]> = 010)
(i) Clearing 32-bit counter

- At generating ENCLK when ***[ENxTNCR]***<TRGCAPMD> is "0"
- At setting ***[ENxTNCR]***<ENCLR> to "1"

(b) Timer mode (***[ENxTNCR]***<MODE[2:0]> = 011)
(i) Clearing 32-bit counter

- At matching with the counter value and ***[ENxINT]***<INT[31:0]> when ***[ENxTNCR]***<CMPSEL> is "0"
- At matching with the counter value and ***[ENxRELOAD]***<RELOAD[31:0]> when ***[ENxTNCR]***<CMPSEL> is "1" and ***[ENxTNCR]***<TOVMD> is "0"
- At changing ZDETECT, output from Z judgement circuit of the decoder to "1" when ***[ENxTNCR]***<TRGCAPMD> is "0" and ***[ENxTNCR]***<ZEN> is "1"
- At setting ***[ENxTNCR]***<ENCLR> to "1"

(2) Compare function

- Perform match comparison with the counter value and ***[ENxRELOAD]***<RELOAD[31:0]>.
- Perform match comparison with the counter value and ***[ENxINT]***<INT[31:0]>.
- Perform match comparison with the counter value and ***[ENxMCMP]***<MCMP[31:0]> when ***[ENxTNCR]***<MCMPMD> is "0".
  Perform magnitude comparison with the counter value and ***[ENxMCMP]***<MCMP[31:0]> when ***[ENxTNCR]***<MCMPMD> is "1".
  When ***[ENxINTCR]***<MCMPIE> is "1", the compare result is output to ENCxCTRG0.
- Perform match comparison with the counter value and ***[ENxSCMP]***<SCMP[31:0]> when ***[ENxTNCR]***<SCMPMD> is "0".
  Perform magnitude comparison with the counter value and ***[ENxSCMP]***<SCMP[31:0]> when ***[ENxTNCR]***<SCMPMD> is "1".

(3) Capture function
The counter value is captured to ***[ENxCNT]***<CNT[31:0]> at the below timings.

(a) Sensor mode (timer count) (***[ENxTNCR]***<MODE[2:0]> = 010)

- At generating ENCLK
- At setting ***[ENxTNCR]***<SFTCAP> to "1"

(b) Timer mode (***[ENxTNCR]***<MODE[2:0]> = 011)

- At changing ZDETECT, output from Z judgement circuit of the decoder to "1" when ***[ENxTNCR]***<TRGCAPMD> is "0" and ***[ENxTNCR]***<ZEN> is "1"
- At setting ***[ENxTNCR]***<SFTCAP> to "1"

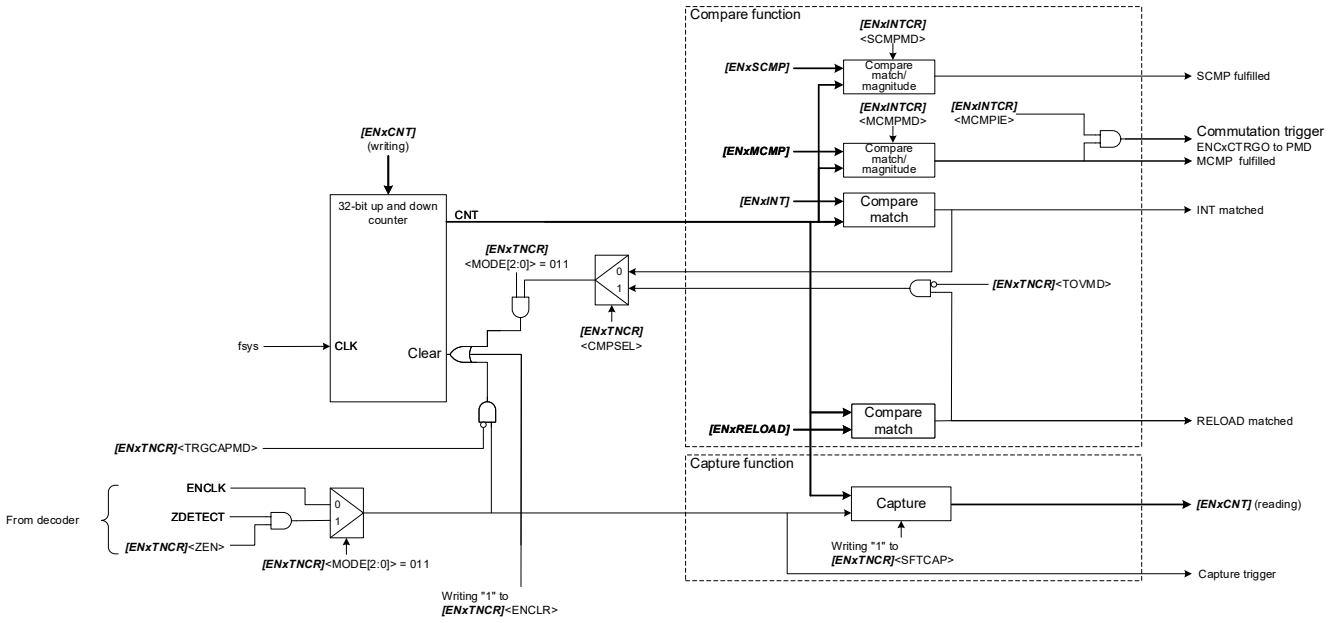

Figure 3.32 Configuration of Counter (in Sensor Mode (Timer Count) and Timer Mode)

3.3.3.3. Sensor Mode (Phase Count) and Phase Counter Mode

The counter in the sensor mode (phase count) and phase counter mode has a clock generator controlled by fsys and PZXOR from the decoder, a 32-bit counter controlled by the clock and up/down signal from a clock generator, the compare function compared the value of each ***[ENxRELOAD]***<RELOAD[31:0]>, ***[ENxINT]***<INT[31:0]>, ***[ENxMCMP]***<MCMP[31:0]>, and ***[ENxSCMP]***<SCMP[31:0]> and the value of 32-bit up and down counter and capture function.

(1) 32-bit counter
When 32-bit counter stops, a value can be preset to it.

A 32-bit counter is controlled by the clock and up and down signal which are setting by ***[ENxRATE]***<RATE[15:0]>, ***[ENxTNCR]***<UDMD[1:0]>, and PZXOR.

[ENxRATE]<RATE[15:0]> is handled as an unsigned binary or two's complement.
The "n" shows a number which ***[ENxRATE]***<RATE[15:0]> indicates. A clock frequency is fsys × |n| / 2^{16}.

For details of ***[ENxRATE]***<RATE[15:0]> and clock frequency, refer to "4.2.6. *[ENxRATE]* (Phase Count Rate Register)".

(a) Sensor mode (phase count) (***[ENxTNCR]***<MODE[2:0]> = 110) and phase counter mode (phase measurement) (***[ENxTNCR]***<MODE[2:0]> = 111, ***[ENxTNCR]***<ZEN> = arbitrary value, and ***[ENxTNCR]***<P3EN> = 0)

(i) When ***[ENxTNCR]***<UDMD[1:0]> is "00"
Counting up

(ii) When ***[ENxTNCR]***<UDMD[1:0]> is "01"
Counting down

(iii) When ***[ENxTNCR]***<UDMD[1:0]> is others
Counting up when n is a positive number
Counting down when n is a negative number

(b) Phase counter mode (phase difference measurement) (***[ENxTNCR]***<MODE[2:0]> = 111, ***[ENxTNCR]***<ZEN> = 1, and ***[ENxTNCR]***<P3EN> = 1)

A value of ***[ENxRATE]***<RATE[15:0]> is used as 2-complementary n.

(i) When PZXOR is "0"
Counting up

(ii) When PZXOR is "1"
Counting down

The clear and load operations of 32-bit counter are shown below.

(a) Sensor mode (phase count) (***[ENxTNCR]***<MODE[2:0]> = 110)
(i) Clearing 32-bit counter

- At generating ENCLK when ***[ENxTNCR]***<TRGCAPMD> is "0"
- At matching with the counter value and ***[ENxRELOAD]***<RELOAD[31:0]> in counting up when ***[ENxTNCR]***<TOVMD> is "0"
- At setting ***[ENxTNCR]***<ENCLR> to "1"

(ii) Loading the value of ***[ENxRELOAD]***<RELOAD[31:0]> to the counter

- At judging that a counter value is matched with "0" in counting down.

(b) Phase counter mode (***[ENxTNCR]***<MODE[2:0]> = 111)

(i) Clearing 32-bit counter

- At changing ZDETECT, output from Z judgement circuit of the decoder to "1" when ***[ENxTNCR]***<TRGCAPMD> is "0" and ***[ENxTNCR]***<ZEN> is "1"
- At matching with the counter value and ***[ENxRELOAD]***<RELOAD[31:0]> in counting up when ***[ENxTNCR]***<TOVMD> is "0"
- At setting ***[ENxTNCR]***<ENCLR> to "1"

(ii) Loading the value of ***[ENxRELOAD]***<RELOAD[31:0]> to the counter

- At judging that a counter value is matched with "0" in counting down.

(2) Compare function

- Perform match comparison with the counter value and ***[ENxRELOAD]***<RELOAD[31:0]>.
- Perform match comparison with the counter value and ***[ENxINT]***<INT[31:0]>.
- Perform match comparison with the counter value and ***[ENxMCMP]***<MCMP[31:0]>. When ***[ENxINTCR]***<MCMPIE> is "1", the compare result is output to ENCxCTRG0.
- Perform match comparison with the counter value and ***[ENxSCMP]***<SCMP[31:0]>.

(3) Capture function

The counter value is captured to ***[ENxCNT]***<CNT[31:0]> at the below timings.

(a) Sensor mode (phase count) (***[ENxTNCR]***<MODE[2:0]> = 110)

- At generating ENCLK when ***[ENxTNCR]***<TRGCAPMD> is "0"
- At setting ***[ENxTNCR]***<SFTCAP> to "1"

(b) Phase counter mode (***[ENxTNCR]***<MODE[2:0]> = 111)

- At changing ZDETECT, output from Z judgement circuit of the decoder to "1" when ***[ENxTNCR]***<TRGCAPMD> is "0" and ***[ENxTNCR]***<ZEN> is "1"
- At setting ***[ENxTNCR]***<SFTCAP> to "1"

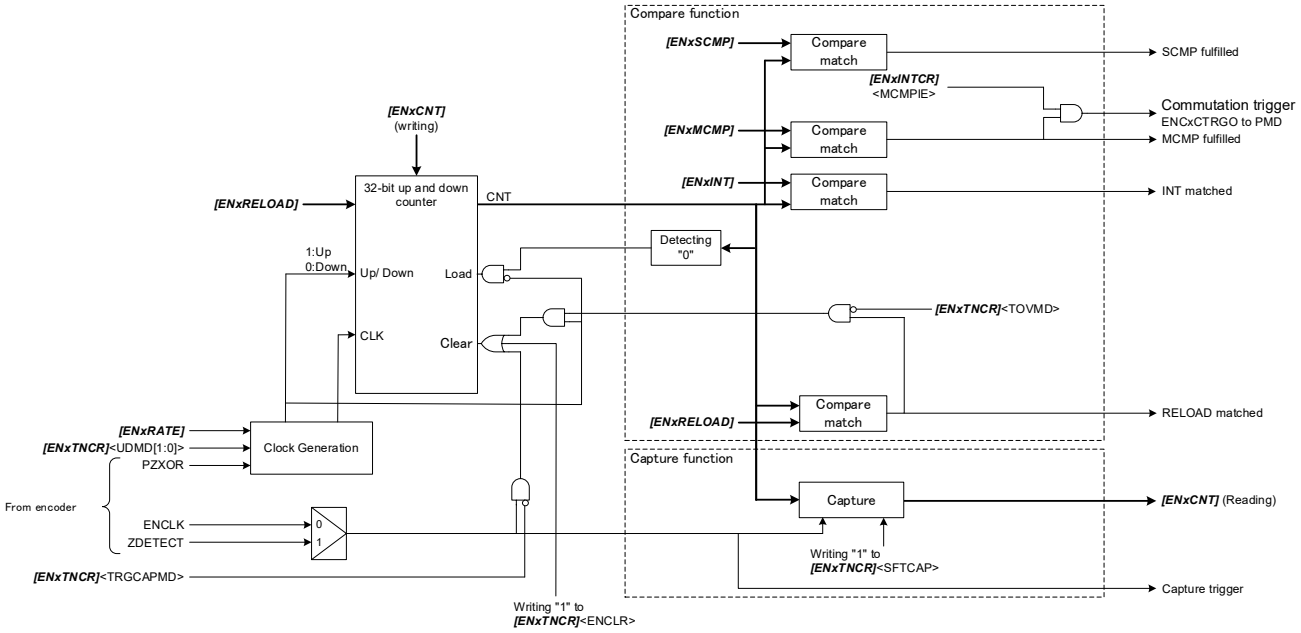

Figure 3.33 Configuration of Counter (in Sensor Mode (Phase Count) and Phase Counter Mode)

3.3.4. Interrupt Control

The generation of interrupt for each interrupt factor can be specified by ***[ENxINTCR]***. When a corresponding bit field of ***[ENxINTCR]*** is "0", the generation of interrupt is disabled. When it is "1", the generation of interrupt is enabled, and the corresponding interrupt signal occurs.

The generation of interrupt factors can be monitored by ***[ENxINTF]*** and ***[ENxINTF2]***.

A bit field of ***[ENxINTF]*** is set to "1" by generation of interrupt factors in spite of the corresponding bit field of ***[ENxINTCR]***.

It is cleared to "0" when ***[ENxINTF]*** is read or the corresponding bit field of ***[ENxINTFCLR]*** is set to "1". And then, it is also cleared to "0" when ***[ENxTNCR]***<ENRUN> is "0".

A bit field of ***[ENxINTF2]*** is set to "1" by generation of interrupt factor when the corresponding bit field of ***[ENxINTCR]*** is "1". It is not set to "1" when the corresponding bit field of ***[ENxINTCR]*** is "0".

It is cleared to "0" when the corresponding bit field of ***[ENxINTFCLR]*** is set to "1". And then, it is also cleared to "0" when ***[ENxTNCR]***<ENRUN> is "0".

Table 3.8 List of Interrupt Factors

Interrupt factor	Description	Operation mode	*[ENxINTCR]*	*[ENxINTF]*	*[ENxINTF2]*	Interrupt signal
Dividing pulse	Inform generating ENCxTIMPLS.	Encoder mode Sensor mode (event count)	<TPLSIE>	<TPLSF>	<TPLSF2>	INTENCx0
Capture	Inform capturing by ZDETECT.	Timer mode Phase counter mode	<CAPIE>	<CAPF>	<CAPF2>	INTENCx0
	Inform capturing by ENCLK.	Sensor mode (timer count, phase count)				
Detection error	Inform generating edge detection error (***[ENxSTS]***<PDERR>) or skip judgement (***[ENxSTS]***<SKPDT>)	Encoder mode Sensor mode (event count, timer count, phase count)	<ERRIE>	<ERRF>	<ERRF2>	INTENCx0
INT matched	Inform matching with ***[ENxINT]***<INT[31:0]> and counter value.	All operation mode	<CMPIE>	<INTCPF>	<INTCPF2>	INTENCx1
RELOAD matched	Inform matching with ***[ENxRELOAD]***<RELOAD[31:0]> and counter value.	Sensor mode (timer count, phase count) Timer mode Phase counter mode (phase measurement, phase difference measurement)	<RLDIE>	<RLDCPF>	<RLDCPF2>	INTENCx1
MCMP fulfilled	Inform matching with ***[ENxMCMP]***<MCMP[31:0]> and counter value when ***[ENxTNCR]***<MCMPMD> is "0". Inform that a counter value becomes ***[ENxMCMP]***<MCMP[31:0]> or bigger when ***[ENxTNCR]***<MCMPMD> is "1".	Sensor mode (timer count) Timer mode	<MCMPIE>	<MCMPF>	<MCMPF2>	INTENCx1
	Inform matching with ***[ENxMCMP]***<MCMP[31:0]> and counter value.	Encoder mode Sensor mode (event count, timer count, phase count) Phase counter mode (phase measurement, phase difference measurement)				
SCMP fulfilled	Inform matching with ***[ENxSCMP]***<SCMP[31:0]> and counter value when ***[ENxTNCR]***<SCMPMD> is "0". Inform that a counter value becomes ***[ENxSCMP]***<SCMP[31:0]> or bigger when ***[ENxTNCR]***<SCMPMD> is "1".	Sensor mode (timer count) Timer mode	<SCMPIE>	<SCMPF>	<SCMPF2>	INTENCx1
	Inform matching with ***[ENxSCMP]***<SCMP[31:0]> and counter value.	Encoder mode Sensor mode (event count, timer count, phase count) Phase counter mode (phase measurement, phase difference measurement)				

Table 3.9 Interrupt Factors in Each Operation Mode

Operation mode	Interrupt factor
Encoder mode	Dividing pulse, detection error, INT matched, MCMP fulfilled, SCMP fulfilled
Sensor mode (event count)	Dividing pulse, detection error, INT matched, MCMP fulfilled, SCMP fulfilled
Sensor mode (timer count)	Capture, detection error, INT matched, RELOAD matched, MCMP fulfilled, SCMP fulfilled
Sensor mode (phase count)	Capture, detection error, INT matched, RELOAD matched, MCMP fulfilled, SCMP fulfilled
Timer mode	Capture, INT matched, RELOAD matched, MCMP fulfilled, SCMP fulfilled
Phase counter mode (phase measurement, phase difference measurement)	Capture, INT matched, RELOAD matched, MCMP fulfilled, SCMP fulfilled

4. Registers

4.1. List of Registers

The registers and addresses of A-ENC2 are shown below.

Peripheral function		Channel/unit	Base address
			TYPE1
Advanced encoder input circuit 2	A-ENC2-A	ch0	0x40068800
		ch1	0x40068900
		ch2	0x40068A00
		ch3	0x40068B00

Note: The built-in channel, unit and base address are depending on each product. For details of them, refer to the reference manual "Product Information".

Register name		Address (Base+)
Control Register	***[ENxTNCR]***	0x0000
RELOAD Comparison Register	***[ENxRELOAD]***	0x0004
INT Comparison Register	***[ENxINT]***	0x0008
Counter Register	***[ENxCNT]***	0x000C
MCMP Comparison Register	***[ENxMCMP]***	0x0010
Phase Count Rate Register	***[ENxRATE]***	0x0014
Status Register	***[ENxSTS]***	0x0018
Input Procedure Control Register	***[ENxINPCR]***	0x001C
Sample Delay Register	***[ENxSMPDLY]***	0x0020
Input Monitor Register	***[ENxINPMON]***	0x0024
Sample Clock Control Register	***[ENxCLKCR]***	0x0028
Interrupt Control Register	***[ENxINTCR]***	0x002C
Interrupt Flag Register	***[ENxINTF]***	0x0030
SCMP Comparison Register	***[ENxSCMP]***	0x0034
Debug Output Control Register	***[ENxDBGOEN]***	0x0038
Control Register 2	***[ENxTNCR2]***	0x003C
MDOUT Comparison Phase 0 Register	***[ENxMDOUTCMP0]***	0x0040
MDOUT Comparison Phase 1 Register	***[ENxMDOUTCMP1]***	0x0044
MDOUT Comparison Phase 2 Register	***[ENxMDOUTCMP2]***	0x0048
MDOUT Comparison Phase 3 Register	***[ENxMDOUTCMP3]***	0x004C
MDOUT Comparison Phase 4 Register	***[ENxMDOUTCMP4]***	0x0050
MDOUT Comparison Phase 5 Register	***[ENxMDOUTCMP5]***	0x0054
Interrupt Flag Register 2	***[ENxINTF2]***	0x0058
Interrupt Flag Clear Register	***[ENxINTFCLR]***	0x005C

Note: When ***[ENxTNCR]***<ENRUN> is "1", the registers and bit fields which can be re-written are followings; ***[ENxTNCR]***<SFTCAP>, <ENRUN>, <ENCLR>, ***[ENxINPCR]***<PDSTP>, <PDSTT>, ***[ENxRELOAD]***, ***[ENxINT]***, ***[ENxMCMP]***, ***[ENxSCMP]***, ***[ENxINTFCLR]***.
Re-writing to others is prohibited.

4.2. Detail of Registers

In this section, the description of a bit field whose operation is depended on an operation mode of A-ENC2 is shown with operation mode with symbol **[]**.

4.2.1. *[ENxTNCR]* (Control Register)

Bit	Bit symbol	After reset	Type	Function
31:30	-	0	R	Read as "0".
29	SCMPMD	0	R/W	Compare mode setting for ***[ENxSCMP]***<SCMPCNT[31:0]> and counter value **[Sensor mode (timer count)]**, **[Timer mode]** 0: Match comparison mode (counter value = ***[ENxSCMP]***<SCMPCNT[31:0]>) 1: Magnitude comparison mode (counter value ≥ ***[ENxSCMP]***<SCMPCNT[31:0]>) **[Encoder mode]**, **[Sensor mode (event count**, **phase count)]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** Match comparison mode is selected in spite of setting. Arbitrary value: No meaning
28	CMPSEL	0	R/W	Clear condition setting for counter value **[Timer mode]** When ***[ENxTNCR]***<TOVMD> is "0" 0: Counter value is cleared to "0x00000000" when a counter value and ***[ENxINT]***<INT[31:0]> are matched. The counting is continued. 1: Counter value is cleared to "0x00000000" when a counter value and ***[ENxRELOAD]***<RELOAD[31:0]> are matched. The counting is continued. When ***[ENxTNCR]***<TOVMD> is "1" 0: Counter value is cleared to "0x00000000" when a counter value and ***[ENxINT]***<INT[31:0]> are matched. The counting is stopped when a counter value and ***[ENxRELOAD]***<RELOAD[31:0]> are matched. If ***[ENxINT]***<INT[31:0]> equals ***[ENxRELOAD]***<RELOAD[31:0]>, the counter is cleared. 1: The counting is stopped when a counter value and ***[ENxRELOAD]***<RELOAD[31:0]> are matched. A counter value is not cleared. **[Encoder mode**, **Sensor mode (phase count)]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** Counter value is cleared to "0x00000000" when a counter value and ***[ENxRELOAD]***<RELOAD[31:0]> are matched and a rotation direction is CW direction. Arbitrary value: No meaning **[Sensor mode (event count**, **timer count)]** The counter value is not cleared. Arbitrary value: No meaning

Bit	Bit symbol	After reset	Type	Function
27:26	UDMD[1:0]	00	R/W	Up or down setting for counting 32-bit up and down counter **[Sensor mode (phase count)], [Phase counter mode (phase measurement)]** 00: 32-bit up and down counter counts up. 01: 32-bit up and down counter counts down. 10 or 11: Refer to "3.3.3.3. Sensor Mode (Phase Count) and Phase Counter Mode". **[Encoder mode], [Sensor mode (event count, timer count)], [Timer mode], [Phase counter mode (phase difference measurement)]** Arbitrary value: No meaning
25	TOVMD	0	R/W	Counting operation setting when ***[ENxRELOAD]***<RELOAD[31:0]> and counter value are matched **[Sensor mode (timer count)], [Timer mode]** 0: Counting is continued. 1: Counting is stopped. When "counting is stopped" is specified, counter value is cleared to "0x00000000" by setting ***[ENxTNCR]***<ENCLR> to "1" and release matching with ***[ENxTNCR]***<ENCLR> and counter value to restart counting from stopping count. **[Timer mode], [Sensor mode (phase count)], [Phase counter mode (phase measurement)]** 0: Counter value is cleared to "0x00000000" and counting is continued. 1: Counting is stopped. When "counting is stopped" is specified, counter value is cleared to "0x00000000" by setting ***[ENxTNCR]***<ENCLR> to "1" and release matching with ***[ENxTNCR]***<ENCLR> and counter value to restart counting from stopping count. **[Encoder mode]** The following operations are performed in spite of setting. (1) The counter value is cleared, and counting is continued when a rotation direction is CW direction. (2) Counting is continued when the rotation direction is CCW direction. Arbitrary value: No meaning **[Sensor mode (event count)], [Phase counter mode (phase difference measurement)]** In these operation modes, matching with ***[ENxRELOAD]***<RELOAD[31:0]> and counter value cannot be performed. Arbitrary value: No meaning
24	MCMPMD	0	R/W	Compare mode setting for ***[ENxMCMP]***<MCMPCNT[31:0]> and counter value **[Sensor mode (timer count)], [Timer mode]** 0: Match comparison mode (counter value = ***[ENxMCMP]***<MCMPCNT[31:0]>) 1: Magnitude Comparison mode (counter value ≥ ***[ENxMCMP]***<MCMPCNT[31:0]>) **[Encoder mode], [Sensor mode (event count, phase count)], [Phase counter mode (phase measurement, phase difference measurement)]** Match comparison mode is selected in spite of setting. (counter value = ***[ENxMCMP]***<MCMPCNT[31:0]>) Arbitrary value: No meaning

Bit	Bit symbol	After reset	Type	Function
23:22	DECMD[1:0]	00	R/W	Signals of rotation direction detection and detection rotation direction setting **[Encoder mode]**, **[Sensor mode (event count**, **timer count**, **phase count)]** 00: Edges of CW and CCW direction are detected. Changing input signals (SNCA, SNCB, and SNCZ) are detected. 01: Only edge of CW direction is detected. Changing between SNCA, SNCB, and SNCZ and states of ones when the previous edge is detected. (Detection result is held.) 10: Only edge of CCW direction is detected. Changing between SNCA, SNCB, and SNCZ and states of ones when the previous edge is detected. (Detection result is held.) 11: Edges of CW and CCW direction are detected. Changing between SNCA, SNCB, and SNCZ and states of ones when the previous edge is detected. (Detection result is held.) **[Timer mode]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** Write as "00.
21	SDTEN	0	R/W	Detection setting for the skip judgement and edge detection error judgement **[Encoder mode]** No skip judgement is performed. 0: Edge detection error judgement is disabled. 1: Edge detection error judgement is enabled. **[Sensor mode (event count**, **timer count**, **phase count)]** The skip judgement and edge detection error judgement are performed. 0: Judgement is disabled. 1: Judgement is enabled. **[Timer mode]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** Write as "0".
20	-	0	R	Read as "0".
19:17	MODE[2:0]	000	R/W	Operation mode setting **[Encoder mode]**, **[Sensor mode (event count**, **Timer mode**, **phase count)]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** The operation mode is determined by ***[ENxTNCR]***<MODE[2:0]>, <P3EN>, and <ZEN>. For details, refer to "Table 3.1 Operation Mode Setting". 000: Encoder mode 001: Sensor mode (event count) 010: Sensor mode (timer count) 011: Timer mode 100: Reserved 101: Reserved 110: Sensor mode (phase count) 111: Phase counter mode

Bit	Bit symbol	After reset	Type	Function
16	P3EN	0	R/W	Decode mode setting (2-phase or 3-phase input selection) The operation mode is determined by ***[ENxTNCR]***<MODE[2:0]>, <P3EN>, and <ZEN>. For details, refer to "Table 3.1 Operation Mode Setting". **[Sensor mode (event count, timer count, phase count)]** 0: 2-phase decode 1: 3-phase decode **[Encoder mode, Timer mode], [Phase counter mode (phase measurement)]** Write as "0". **[Phase counter mode (phase different measurement)]** Write as "1".
15:13	-	0	R	Read as "0".
12	TRGCAPMD	0	R/W	Operation selection at trigger capture This bit field does not influence the operation of soft capture. **[Sensor mode (timer count, phase count)], [Timer mode], [Phase counter mode (phase measurement, phase difference measurement)]** Trigger capture operation is selected at detection of rotation edge. 0: Capturing and clearing a counter 1: Only capturing **[Encoder mode], [Sensor mode (event count)]** In these modes, no capture function is performed. Arbitrary value: No meaning
11	SFTCAP	0	W	Execution setting for soft capture Read as "0". **[Sensor mode (timer count, phase count)], [Timer mode,], [Phase counter mode (phase measurement, phase difference measurement)]** 0: No meaning 1: Capturing counter value To read captured value, read ***[ENxCNT]***<CNT[31:0]>. **[Encoder mode], [Sensor mode (event count)]** Write as "0".
10	ENCLR	0	W	Counter clear setting Read as "0". ***[ENxTNCR]***<SFTCAP> and <ENCLR> are not set to "1" simultaneously. **[Encoder mode], [Sensor mode (event count, Timer mode, phase count)], [Timer mode], [Phase counter mode (phase measurement, phase difference measurement)]** 0: No meaning 1: A counter is cleared to "0x00000000". The cleared counter restarts count again.

Bit	Bit symbol	After reset	Type	Function
9:8	ZESEL[1:0]	00	R/W	Detection edge selection when ENCxZ pin input is enabled. (***[ENxTNCR]***<ZEN> = 1) **[Timer mode], [Phase counter mode (phase measurement, phase difference measurement)]** 00: Reserved 01: Rising edge detection 10: Falling edge detection 11: Both edge detection **[Encoder mode], [Sensor mode (event count, timer count, phase count)]** Write as "00".
7	ZEN	0	R/W	ENCxZ pin input control setting The operation mode is determined by ***[ENxTNCR]***<MODE[2:0]>, <P3EN>, and <ZEN>. For details, refer to "Table 3.1 Operation Mode Setting". **[Encoder mode], [Timer mode], [Phase counter mode (phase measurement)]** 0: ENCxZ pin input is disabled. 1: ENCxZ pin input is enabled. **Sensor mode (event count, timer count, phase count)]** Write as "0". **[Phase counter mode (phase difference measurement)]** Write as "1".
6	ENRUN	0	R/W	A-ENC2 operation control setting **[Encoder mode], [Sensor mode (event count, Timer mode, phase count)], [Timer mode], [Phase counter mode (phase measurement, phase difference measurement)]** 0: A-ENC2 operation is disabled. 1: A-ENC2 operation is enabled.
5	ZEACT	0	R/W	Active level selection of ENCxZ pin input This bit field is valid when ***[ENxTNCR]***<ZEN> is "1". **[Encoder mode]** 0: "High" active is selected. 1: "Low" active is selected. **[Sensor mode (event count, timer count, phase count)], [Timer mode], [Phase counter mode (phase measurement, phase difference measurement)]** "High" active is always selected in spite of setting. Arbitrary value: No meaning
4:3	-	0	R	Read as "0".

Bit	Bit symbol	After reset	Type	Function
2:0	ENDEV[2:0]	000	R/W	Dividing ratio of rotation edge pulse (ENCLK) setting for the dividing output (ENCxTIMPLS) A rotation edge pulse is divided by this bit field setting and it is used for interrupt source. **[Encoder mode]**, **[Sensor mode (event count)]** 000: Divided by 1 100: Divided by 16 001: Divided by 2 101: Divided by 32 010: Divided by 4 110: Divided by 64 011: Divided by 8 111: Divided by 128 **[Sensor mode (timer count**, **phase count)**, **[Timer mode]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** Arbitrary value: No meaning

Note: When ***[ENxTNCR]***<ENRUN> is set to "1", other bit fields in this register do not changed simultaneously. Only when ***[ENxTNCR]***<ENRUN> is "0", other bit fields can be changed.

4.2.2. *[ENxRELOAD]* (RELOAD Comparison Register)

Bit	Bit symbol	After reset	Type	Function
31:0	RELOAD[31:0]	0x00000000	R/W	The operation of this register is changed by operation mode. **[Encoder mode]** Number of input pulse for one rotation × 4 - 1 Maximum number of count is set. During counting up, when a counter value matched with ***[ENxRELOAD]***<RELOAD[31:0]>, a counter value is cleared to "0x00000000". And also, during counting down, a counter value becomes "0x00000000", a counter value is set to a value of ***[ENxRELOAD]***<RELOAD[31:0]>. **[Sensor mode (event count)]**, **[Phase counter mode (phase difference measurement)]** This register is not used. **[Sensor mode (timer count)]**, **[Timer mode]** A comparison value with counter value When ***[ENxINTCR]***<RLDIE> is "1", at matching a counter value with ***[ENxRELOAD]***<RELOAD[31:0]> interrupt INTENCx1 occurs. **[Sensor mode (phase count)]**, **[Phase counter mode (phase measurement)]** Maximum number of count During counting up, when a counter value matched with ***[ENxRELOAD]***<RELOAD[31:0]>, a counter value is cleared to "0x00000000". And also, during counting down, a counter value becomes "0x00000000", a counter value is set to a value of ***[ENxRELOAD]***<RELOAD[31:0]>. When ***[ENxINTCR]***<RLDIE> is "1", at matching a counter value with ***[ENxRELOAD]***<RELOAD[31:0]> interrupt INTENCx1 occurs. When ***[ENxTNCR]***<TOVMD> is "1" (Stopping count at RELOAD matching), do not set ***[ENxMCMP]***<MCMP[31:0]> and ***[ENxRELOAD]***<RELOAD[31:0]> to same value.

4.2.3. *[ENxINT]* (INT Comparison Register)

Bit	Bit symbol	After reset	Type	Function
31:0	INT[31:0]	0x00000000	R/W	Setting value to compare with a counter value **[Encoder mode]** When a counter value and ***[ENxINT]***<INT[31:0]> are matched, ***[ENxINTF]***<INTCPF> is set to "1". At this time, when ***[ENxINTCR]***<CMPIE> is "1", an interrupt INTENCx1 occurs depending on the value of ***[ENxTNCR]***<ZEN>. (1) When ***[ENxTNCR]***<ZEN> is "0" An interrupt INTENCx1 occurs when ***[ENxINTF]***<INTCPF> is set to "1". (2) When ***[ENxTNCR]***<ZEN> is "1" An interrupt INTENCx1 occurs when ***[ENxINTF]***<INTCPF> and ***[ENxSTS]***<ZDET> are "1". When ***[ENxSTS]***<ZDET> is "0", no interrupt INTENCx1 occurs. **[Sensor mode (event count, timer count)], [Timer mode]** When a counter value and ***[ENxINT]***<INT[31:0]> are matched, ***[ENxINTF]***<INTCPF> is set to "1". At this time, when ***[ENxINTCR]***<CMPIE> is "1", an interrupt INTENCx1 occurs. **[Sensor mode (phase count)], [Phase counter mode (phase measurement, phase difference measurement)]** When a counter value and ***[ENxINT]***<INT[31:0]> are matched, ***[ENxINTF]***<INTCPF> is set to "1". At this time, when ***[ENxINTCR]***<CMPIE> is "1", an interrupt INTENCx1 occurs. However, when all of the conditions below are fulfilled, no interrupt INTENCx1 occurs. (1) ***[ENxTNCR]***<TOVMD> is "1". (Stopping counter when ***[ENxRELOAD]***<RELOAD[31:0]> and counter value are matched.) (2) Setting values in ***[ENxINT]***<INT[31:0]> and ***[ENxRELOAD]***<RELOAD[31:0]> are same.

4.2.4. *[ENxCNT]* (Counter Register)

Bit	Bit symbol	After reset	Type	Function
31:0	CNT[31:0]	0x00000000	R/W	Setting pre-set value for counter Reading captured value The captured value remained in spite of the value of ***[ENxTNCR]***<ENRUN>. ***[ENxCNT]***<CNT[31:0]> is initialized by only reset. **[Encoder mode]**, **[Sensor mode (event count)]** The value of counter which counts up and down a rotation edge pulse (ENCLK) is captured when ***[ENxTNCR]***<SFTCAP> is set to "1". This is called as "soft capture". The captured value is read from ***[ENxCNT]***<CNT[31:0]>. **[Sensor mode (timer count**, **phase count)]** The counter value is captured by rotation edge pulse (ENCLK). And when ***[ENxTNCR]***<SFTCAP> is set to "1", a counter value is captured. The captured value is read from ***[ENxCNT]***<CNT[31:0]>. **[Timer mode]**, **[Phase counter mode (phase measurement)]** When ***[ENxTNCR]***<SFTCAP> is set to "1", a counter value is captured. And when ***[ENxTNCR]***<ZEN> is "1", a counter value is captured by the detection edge of ENCxZ pin input specified by ***[ENxTNCR]***<ZESEL[1:0]>. The captured value is read from ***[ENxCNT]***<CNT[31:0]>. **[Phase counter mode (phase difference measurement)]** When ***[ENxTNCR]***<SFTCAP> is set to "1", a counter value is captured. And when ***[ENxTNCR]***<ZEN> is "1", a counter value is captured by the detection edge of ENCxPSGI specified by ***[ENxTNCR]***<ZESEL[1:0]>. The captured value is read from ***[ENxCNT]***<CNT[31:0]>.

4.2.5. *[ENxMCMP]* (MCMP Comparison Register)

Bit	Bit symbol	After reset	Type	Function
31:0	MCMP[31:0]	0x00000000	R/W	Setting value to compare with a counter value A compare condition is specified by ***[ENxTNCR]***<MCMPMD>. **[Sensor mode (timer count)]**, **[Timer mode]** A counter value and ***[ENxMCMP]***<MCMP[31:0]> are compared. When the specified condition is fulfilled, ***[ENxINTF]***<MCMPF> is set to "1". At this time, a signal which is generated by fulfilling the specified condition is out to ENCxCTRGO. When ***[ENxINTCR]***<MCMPIE> is "1", an interrupt INTENCx1 occurs. Only the first condition fulfilled is available for setting ***[ENxMCMP]***<MCMP[31:0]>. Other conditions fulfilled is ignored. (1) Match comparison mode (***[ENxTNCR]***<MCMPMD> = 0) A condition fulfilled signal occurs when a counter value and ***[ENxMCMP]***<MCMP[31:0]> are matched. (2) Magnitude comparison mode (***[ENxTNCR]***<MCMPMD> = 1) A condition fulfilled signal occurs when a counter value is ***[ENxMCMP]***<MCMP[31:0]> or more. **[Encoder mode]**, **[Sensor mode (event count)]** A counter value and ***[ENxMCMP]***<MCMP[31:0]> are compared. When they are matched, ***[ENxINTF]***<MCMPF> is set to "1".When ***[ENxINTCR]***<MCMPIE> is "1", an interrupt INTENCx1 occurs. **[Sensor mode (phase count)]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** A counter value and ***[ENxMCMP]***<MCMP[31:0]> are compared. When they are matched, ***[ENxINTF]***<MCMPF> is set to "1".When ***[ENxINTCR]***<MCMPIE> is "1", an interrupt INTENCx1 occurs. When ***[ENxTNCR]***<TOVMD> is "1" (Stopping count at RELOAD matching), do not set ***[ENxMCMP]***<MCMP[31:0]> and ***[ENxRELOAD]***<RELOAD[31:0]> to same value.

4.2.6. *[ENxRATE]* (Phase Count Rate Register)

Bit	Bit symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:0	RATE[15:0]	0x0000	R/W	Frequency setting of the clock used for counting 32-bit up and down counter ***[ENxRATE]***<RATE[15:0]> is handled as an unsigned binary or two's complement. The "n" shows a number which ***[ENxRATE]***<RATE[15:0]> indicates. A clock frequency is fsys × |n| / 2^{16}. When n is "0", a 32-bit up and down counter is not changed. ***[ENxRATE]***<RATE[15:0]> is handled as shown below. **[Sensor mode (phase count)]**, **[Phase counter mode (phase measurement)]** (1) When ***[ENxTNCR]***<UDMD[1:0]> = 00 or 01 ***[ENxRATE]***<RATE[15:0]> is handled as unsigned binary. A value range is from 0 (0x0000) to 2^{16} -1 (0xffff). (2) When ***[ENxTNCR]***<UDMD[1:0]> = 10 or 11 ***[ENxRATE]***<RATE[15:0]> is handled as two's complementary. A value range is from 0 (0x0000) to 2^{15} -1 (0x7fff) and -2^{15} (0x8000) to -1 (0xffff). **[Phase counter mode (phase difference measurement)]** ***[ENxRATE]***<RATE[15:0]> is handled as unsigned binary. A value range is from 0 (0x0000) to 2^{16} -1 (0xffff). **[Encoder mode]**, **[Sensor mode (event count**, **timer count)]**, **[Timer mode]** Arbitrary value: No meaning

4.2.7. *[ENxSTS]* (Status Register)

All bit fields in ***[ENxSTS]*** are clear to "0" by reading ***[ENxSTS]***.

Bit	Bit symbol	After reset	Type	Function
31:15	-	0	R	Read as "0".
14	REVERR	0	R	Rotation direction reverse flag (Note) This bit field is cleared when ***[ENxTNCR]***<ENRUN> is "0". **[Sensor mode (timer count, phase count)]** The flag indicated that the rotation direction is changed. (Note) 0: - 1: Rotation direction changed (***[ENxSTS]***<UD> = 0 → 1 or 1 → 0) **[Encoder mode], [Sensor mode (event count)], [Timer mode], [Phase counter mode (phase measurement, phase difference measurement)]** No meaning
13	UD	0	R	Rotation direction flag This bit field is cleared when ***[ENxTNCR]***<ENRUN> is "0". **[Encoder mode], [Sensor mode (event count, timer count, phase count)]** 0: CCW direction is detected. 1: CW direction is detected. **[Timer mode], [Phase counter mode (phase measurement, phase difference measurement)]** No meaning
12	ZDET	0	R	ENCxZ pin input valid edge detection flag This bit field is cleared when ***[ENxTNCR]***<ENRUN> is "0". **[Encoder mode]** 0: No detection of ENCxZ pin input valid edge after A-ENC2 operation is enabled. 1: Detection of ENCxZ pin input valid edge after A-ENC2 operation is enabled. When a valid edge of ENCxZ pin input depending on a rotation direction (rising edge for CW direction, falling edge for CCW direction) is detected, <ZDET> is set to "1". **Sensor mode (event count, timer count, phase count)], [Timer mode], [Phase counter mode (phase measurement, phase different measurement]** No meaning
11:3	-	0	R	Read as "0".
2	SKPDT	0	R	Skip judgement flag when the skip judgement is enabled. (***[ENxTNCR]***<SDTEN> = 1) **[Sensor mode (event count, timer count, phase count)]** 0: No skip judgement 1: Skip judgement **[Encoder mode], [Timer mode], [Phase counter mode (phase measurement, phase difference measurement)]** No meaning

Bit	Bit symbol	After reset	Type	Function
1	PDERR	0	R	Edge detection error flag **[Encoder mode]**, **[Sensor mode (event count**, **timer count**, **phase count)]** 0: No error detected 1: Error detected When the direction except decoder detection direction selected by ***[ENxTNCR]***<DECMD[1:0]>, <PDERR> is set to "1". **[Timer mode]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** No meaning
0	INERR	0	R	Input error detection flag **[Sensor mode (event count**, **timer count**, **phase count)]** 0: No input error detected 1: Input error detected In 3-phase decode mode, when all of ENCxA, ENCxB, and ENCxZ pin inputs are changed to "Low" or "High" at once, It is decided that ENCxA, ENCxB, and ENCxZ pin inputs has errors, and <INERR> is set to "1". **[Encoder mode]**, **[Timer mode]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** No meaning

Note: After an operation mode (***[ENxTNCR]***<MODE[2:0]>) of A-ENC2 is changed, all bit fields are cleared to "0" by reading ***[ENxSTS]*** at first.

4.2.8. *[ENxINPCR]* (Input Process Control Register)

Bit	Bit symbol	After reset	Type	Function
31:25	-	0	R	Read as "0".
24	BEMFREV	0	R/W	Rotation detection selection for BEMF **[Sensor mode (timer count)]** 0: CW direction 1: CCW direction This bit field is available only when ***[ENxINPCR]***<BEMFMODE> is "1". **[Encoder mode**, **Sensor mode (event count**, **phase count)]**, **[Timer mode]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** Write as "0".
23	-	0	R	Read as "0".
22:16	FILVAL[6:0]	0x00	R/W	Noise cancellation time of BEMF filter setting **[Sensor mode (timer count)]** Setting range: 0 to 127 ("0x00" to "0x7F") Cancellation time: Setting value × 1 / fsys When the signals input to BEMF filter are sampled and they are matched times specified by ***[ENxINPCR]***<FILVAL[6:0]> continuously, the output signal from BEMF filter changes. If ***[ENxINPCR]***<FILVAL[6:0]> is set to "0", the input signal to BEMF filter is output as it is. This bitfield is valid only when ***[ENxINPCR]***<NCT[6:0]> ≠ 0 and ***[ENxINPCR]***<BEMFFIL> = 1. **[Encoder mode]**, **[Sensor mode (event count**, **phase count)]**, **[Timer mode]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** Setting range: 0 to 127 ("0x00" to "0x7F") Cancellation time: Setting value × 1 / fsys When the signals input to BEMF filter are sampled and they are matched times specified by ***[ENxINPCR]***<FILVAL[6:0]> continuously, the output signal from BEMF filter changes. If ***[ENxINPCR]***<FILVAL[6:0]> is set to "0", the input signal to BEMF filter is output as it is. This bitfield is valid only when ***[ENxINPCR]***<NCT[6:0]> ≠ 0, ***[ENxINPCR]***<BEMFFIL> = 1, and ***[ENxINPCR]***<SYNCSPLEN> = 0.
15	-	0	R	Read as "0".

Bit	Bit symbol	After reset	Type	Function
14:8	NCT[6:0]	0x00	R/W	Noise cancellation time setting **[Encoder mode]**, **[Sensor mode (event count**, **timer count**, **phase count)]**, **[Timer mode]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** (1) When PWM synchronous sampling mode (***[ENxINPCR]***<SYNCSPLEN> = 1) Setting range: 0 to 127 ("0x00" to "0x7F") Cancellation time : Setting value × period of sampling signal Period of sampling signal: A) When PWN-on period sampling and PMW-off period sampling: Refer to "4.2.11. *[ENxCLKCR]* (Sample Clock Control Register)". B) When PWM-on edge sampling and PWN-off edge sampling: ENCxPWMON (2) Others Setting range: 0 to 127 ("0x00" to "0x7F") Cancellation time : Setting value × period of sampling signal Period of sampling signal: Refer to "4.2.11. *[ENxCLKCR]* (Sample Clock Control Register)". When the signal input to noise canceler is sampled by sampling signal and they are matched times specified by ***[ENxINPCR]***<NCT[6:0]> continuously, the output signal from noise canceler changes. If ***[ENxINPCR]***<NCT[6:0]> is set to "0x00", the input signal to noise canceler is output as it is.
7	PDSTP	0	W	Rotation edge detection stop or terminate setting in PWM synchronous sampling mode of the zero-cross signal mask control Read as "0". ***[ENxINPCR]***<PDSTP> and ***[ENxINPCR]***<PDSTT> must not be set to "1" simultaneously. **[Sensor mode (timer count**, **phase count)]** 0: No meaning 1: STOP or terminate rotation edge detection **[Encoder mode]**, **[Sensor mode (event count]**, **[Timer mode]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** Write as "0".
6	PDSTT	0	W	Rotation edge detection start or re-start setting in PWM synchronous sampling mode of the zero-cross signal mask control Read as "0". ***[ENxINPCR]***<PDSTP> and ***[ENxINPCR]***<PDSTT> must not be set to "1" simultaneously. **[Sensor mode (timer count**, **phase count)]** 0: No meaning 1: Start or re-start rotation edge **[Encoder mode]**, **[Sensor mode (event count]**, **[Timer mode]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** Write as "0".

Bit	Bit symbol	After reset	Type	Function
5	BEMFFIL	0	R/W	BEMF filter enable setting **[Sensor mode (timer count)]** 0: BEMF filter disabled (an input signal is output as it is.) 1: BEMF filter enabled When ***[ENxINPCR]***<NCT[6:0]> is 0x01 or bigger and ***[ENxINPCR]***<BEMFFIL> is set to "1", the BEMF filter is enabled. Just after ***[ENxINPCR]***<BEMFFIL> is set to "1", until the signals input to BEMF filter are sampled by fsys and they are matched times specified by ***[ENxINPCR]***<FILVAL[6:0]> continuously, the BEMF filter's output is undefined. **[Encoder mode]**, **[Sensor mode (event count**, **phase count)]**, **[Timer mode]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** 0: BEMF filter disabled (an input signal is output as it is.) 1: BEMF filter enabled When ***[ENxINPCR]***<NCT[6:0]> is not 0x00, ***[ENxINPCR]***<SYNCSPLEN> is "0", and ***[ENxINPCR]***<BEMFFIL> is set to "1", the BEMF filter is enabled. Just after ***[ENxINPCR]***<BEMFFIL> is set to "1", until the signals input to BEMF filter are sampled and they are matched times specified by ***[ENxINPCR]***<FILVAL[6:0]> continuously, the BEMF filter's output is undefined.
4	BEMFMODE	0	R/W	BEMF detection phase limited control enable setting **[Sensor mode (timer count)]** 0: Disabled 1: Enabled When ***[ENxINPCR]***<NCT[6:0]> is 0x01 or bigger, ***[ENxINPCR]***<BEMFFIL> is set to "1", the BEMF detection phase limited control is enabled. **[Encoder mode]**, **[Sensor mode (event count**, **phase count)**, **[Timer mode]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** Write as "0".
3	SYNCSPLPD	0	R/W	Sampling mode selection in PWM synchronous sampling mode (***[ENxINPCR]***<SYNCSPLEN> = 1) **[Sensor mode (timer count)]** <SYNCSPLPD> <SYNCSPLMD> Sampling mode 0 0 PWM-on period sampling 0 1 PWM-off edge sampling 1 0 PWM-off period sampling 1 1 PWM-on edge sampling **[Encoder mode]**, **[Sensor mode (event count**, **phase count)]**, **[Timer mode]**, **[phase counter (phase measurement**, **phase different measurement)]** Arbitrary value: No meaning

Bit	Bit symbol	After reset	Type	Function
2	SYNCNCZEN	0	R/W	Noise filter counter control setting when the noise canceler is used as PWM-on period sampling **[Sensor mode (timer count)]** 0: No meaning 1: PWM-off period clear Only when ***[ENxINPCR]***<SYNCSPLEN> = 1, ***[ENxINPCR]***<SYNCSPLPD> = 0, and ***[ENxINPCR]***<SYNCSPLMD> = 0, value of ***[ENxINPCR]***<SYNCNCZEN> is valid. **[Encoder mode]**, **[Sensor mode (event count**, **phase count)]**, **[Timer mode]**, **[Phase counter (phase measurement**, **phase different measurement)]** Arbitrary value: No meaning
1	SYNCSPLMD	0	R/W	**[Sensor mode (timer count)]** Refer to ***[ENxINPCR]***<SYNCSPLPD> in this section. **[Encoder mode]**, **[Sensor mode (event count**, **phase count)]**, **[Timer mode]**, **[Phase counter (phase measurement**, **phase different measurement)]** Arbitrary value: No meaning
0	SYNCSPLEN	0	R/W	Sampling mode selection and zero-cross signal mask control enable setting **[Sensor mode (timer count)]** 0: Continuous sampling and zero-cross signal mask control disabled 1: Continuous sampling and zero-cross signal mask control enabled This bit field selects the sampling mode of noise canceler. When this is used, ***[ENxINPCR]***<NCT[6:0]> is set 0x01 or bigger. When this bit field is set to "0", an input signal to the noise canceler is sampling by the sample clock specified by ***[ENxCLKCR]***<SPLCKS[1:0]>. When it is set to "1", an input signal to the noise canceler is sampling by the ENCxPWMON from the PMD synchronously. **[Encoder mode]**, **[Sensor mode (event count**, **phase count)]**, **[Timer mode]**, **[Phase counter (phase measurement**, **phase different measurement)]** Write as "0".

4.2.9. *[ENxSMPDLY]* (Sample Delay Register)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0".
7:0	SMPDLY[7:0]	0x00	R/W	Delay time setting of sampling start **[Sensor mode (event count, timer count, phase count)]** Setting range: 0 to 255 ("0x00" to "0xFF") Delay time: Setting value × sample clock period Sample clock period: Refer to "4.2.11. *[ENxCLKCR]* (Sample Clock Control Register)". Set a delay time from PWM on to start sampling when PWM-on period sampling (***[ENxINPCR]***<SYNCSPLEN> = 1, ***[ENxINPCR]***<SYNCSPLPD><SYNCSPLMD> = 00) **[Encoder mode], [Timer mode], [Phase counter (phase measurement, phase different measurement)]** Arbitrary value: No meaning

Note: After A-ENC2 is enabled (setting ***[ENxTNCR]***<ENRUN> to "1" after setting to "0"), the first sample delay time may be not same as the value specified by ***[ENxSMPDLY]***<SMPDLY[7:0]>.

4.2.10. *[ENxINPMON]* (Input Monitor Register)

Bit	Bit symbol	After reset	Type	Function
31:7	-	0	R	Read as "0".
6	DETMONZ	0	R	SNCZ, is the signal output from input selector for ENCxZ pin input, status monitor at detecting rotation edge **[Encoder mode]**, **[Sensor mode (event count**, **Timer mode**, **phase count)]**, **[Timer mode]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** (1) When ***[ENxTNCR]***<ENRUN> = 0, or ***[ENxTNCR]***<DECMD[1:0]> = 00 or ***[ENxINPCR]***<PDSTT> = 0 → 1 This bit field indicates a value of ***[ENxINPMON]***<SPLMONZ> at previous fsys. (2) When ***[ENxTNCR]***<DECMD[1:0]> ≠ 01 A) From ***[ENxTNCR]***<ENRUN> = 0 → 1 or ***[ENxINPCR]***<PDSTT> = 0 → 1 to the first rotation edge detection This bit field indicates a value of ***[ENxINPMON]***<SPLMONZ> at previous fsys. B) Since then This bit field indicates a value of ***[ENxINPMON]***<SPLMONZ> at detecting a rotation edge. (3) Others This bit field indicates a value of SNCZ at detecting a rotation edge.
5	DETMONB	0	R	SNCB, is the signal output from input selector for ENCxB pin input, status monitor at detecting rotation edge **[Encoder mode]**, **[Sensor mode (event count**, **Timer mode**, **phase count)]**, **[Timer mode]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** (1) When ***[ENxTNCR]***<ENRUN> = 0, or ***[ENxTNCR]***<DECMD[1:0]> = 00 or ***[ENxINPCR]***<PDSTT> = 0 → 1 This bit field indicates a value of ***[ENxINPMON]***<SPLMONB> at previous fsys. (2) When ***[ENxTNCR]***<DECMD[1:0]> ≠ 01 A) From ***[ENxTNCR]***<ENRUN> = 0 → 1 or ***[ENxINPCR]***<PDSTT> = 0 → 1 to the first rotation edge detection This bit field indicates a value of ***[ENxINPMON]***<SPLMONB> at previous fsys. B) Since then This bit field indicates a value of ***[ENxINPMON]***<SPLMONB> at detecting a rotation edge. (3) Others This bit field indicates a value of SNCB at detecting a rotation edge.

Bit	Bit symbol	After reset	Type	Function
4	DETMONA	0	R	SNCA, is the signal output from input selector for ENCxA pin input, status monitor at detecting rotation edge **[Encoder mode]**, **[Sensor mode (event count**, **Timer mode**, **phase count)]**, **[Timer mode]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** (1) When ***[ENxTNCR]***<ENRUN> = 0, or ***[ENxTNCR]***<DECMD[1:0]> = 00 or ***[ENxINPCR]***<PDSTT> = 0 → 1 This bit field indicates a value of ***[ENxINPMON]***<SPLMONA> at previous fsys. (2) When ***[ENxTNCR]***<DECMD[1:0]> ≠ 01 A) From ***[ENxTNCR]***<ENRUN> = 0 → 1 or ***[ENxINPCR]***<PDSTT> = 0 → 1 to the first rotation edge detection This bit field indicates a value of ***[ENxINPMON]***<SPLMONA> at previous fsys. B) Since then This bit field indicates a value of ***[ENxINPMON]***<SPLMONA> at detecting a rotation edge. (3) Others This bit field indicates a value of SNCA at detecting a rotation edge.
3	-	0	R	Read as "0".
2	SPLMONZ	0	R	This bit field indicates the status of input circuit output signal (SNCZ).
1	SPLMONB	0	R	This bit field indicates the status of input circuit output signal (SNCB).
0	SPLMONA	0	R	This bit field indicates the status of input circuit output signal (SNCA).

4.2.11. *[ENxCLKCR]* (Sample Clock Control Register)

Bit	Bit symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1:0	SPLCKS[1:0]	00	R/W	Sampling frequency Setting **[Encoder mode]**, **[Sensor mode (event count**, **Timer mode**, **phase count)]**, **[Timer mode]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** 00: fsys 01: fsys / 2 10: fsys / 4 11: fsys / 8 The sampling frequency of ENCxA, ENCxB, and ENCxZ pin inputs is specified. However, in PWM synchronous sampling mode (***[ENxINPCR]***<SYNCSPLEN> = 1), when PWM-off edge sampling mode or PWM-on edge sampling mode (***[ENxINPCR]***<SYNCSPLPD><SYNCSPLMD> = 01 or 11), ***[ENxCLKCR]***< SPLCKS[1:0]> has no meaning because a sampling clock is ENCxPWMON.

4.2.12. *[ENxINTCR]* (Interrupt Control Register)

Bit	Bit symbol	After reset	Type	Function
31:7	-	0	R	Read as "0".
6	SCMPIE	0	R/W	SCMP fulfilled interrupt enable setting 0: Disabled 1: Enabled When this bit field is set to "1", interrupt INTENCx1 occurs when SCMP fulfilled condition is satisfied. It is valid in all operation modes of A-ENC2.
5	MCMPIE	0	R/W	MCMP fulfilled interrupt enable setting 0: Disabled 1: Enabled When this bit field is set to "1", interrupt INTENCx1 occurs when MCMP fulfilled condition is satisfied. It is valid in all operation modes of A-ENC2.
4	RLDIE	0	R/W	RELOAD match interrupt enable setting 0: Disabled 1: Enabled When this bit field is set to "1", at matching timing with counter value and ***[ENxRELOAD]***<RELOAD[31:0]>, interrupt INTENCx1 occurs. In Sensor mode (timer count, phase count), Timer mode, Phase counter mode (phase measurement, phase different measurement), it is valid.
3	CMPIE	0	R/W	INT match interrupt enable setting 0: Disabled 1: Enabled When this bit field is set to "1", at matching timing with counter value and ***[ENxINT]***<INT[31:0]>, interrupt INTENCx1 occurs. It is valid in all operation modes of A-ENC2.
2	ERRIE	0	R/W	Detection error interrupt enable setting 0: Disabled 1: Enabled When this bit field is to "1", at detecting edge detection error (***[ENxSTS]***<PDERR>) or skip judgement (***[ENxSTS]***<SKPDT>), interrupt INTENCx0 occurs. In Encoder mode, Sensor mode (event count, timer count, phase count), it is valid.
1	CAPIE	0	R/W	Capture interrupt enabled setting 0: Disabled 1: Enabled When this bit field is to "1", at capturing a count value by an external trigger (ENCxZ pin input) or a rotation edge pulse (ENCLK), interrupt INTENCx0 occurs. In Timer mode, Sensor mode (timer count, phase count), Phase counter mode (phase measurement, phase different measurement), it is valid.
0	TPLSIE	0	R/W	Division interrupt enable setting 0: Disabled 1: Enabled When this bit field is to "1", interrupt INTENCx0 occurs by the pulse that divided a rotation edge pulse (ENCLK) by ***[ENxTNCR]***<ENDEV[2:0]> setting. In Timer mode, Sensor mode (timer count, phase count), Phase counter mode (phase measurement, phase different measurement), it is valid.

Note: Regarding of the factors and operation modes of each interrupt, refer to "3.3.4. Interrupt Control".

4.2.13. *[ENxINTF]* (Interrupt Flag Register)

A bit field in ***[ENxINTF]*** is set to "1" when an interrupt request occurs in spite of the corresponding bit field of ***[ENxINTCR]***.
All bit fields are cleared to "0" by reading ***[ENxINTF]*** or setting a corresponding bit field of ***[ENxINTFCLR]***.
And when ***[ENxTNCR]***<ENRUN> is set to "0", they are also cleared to "0".

Bit	Bit symbol	After reset	Type	Function
31:7	-	0	R	Read as "0".
6	SCMPF	0	R	SCMP fulfilled flag 0: No satisfaction 1: Satisfied In all operation modes of A-ENC2, this bit field is set to "1".
5	MCMPF	0	R	MCMP fulfilled flag 0: No satisfaction 1: Satisfied In all operation modes of A-ENC2, this bit field is set to "1".
4	RLDCPF	0	R	RELOAD match flag 0: No matching 1: Matched In Sensor mode (timer count, phase count), Timer mode, Phase counter mode (phase measurement, phase difference count), this bit field is set to "1".
3	INTCPF	0	R	INT match flag 0: No matching 1: Matched In all operation modes of A-ENC2, this bit field is set to "1".
2	ERRF	0	R	Detection error flag 0: No detection 1: Detected In Encoder mode, Sensor mode (event count, timer count, phase count), this bit field is set to "1".
1	CAPF	0	R	Capture flag 0: No capturing 1: Captured In Sensor mode (timer count, phase count), Timer mode, Phase counter mode (phase measurement, phase difference count), this bit field is set to "1".
0	TPLSF	0	R	Division flag 0: No dividing 1: Dived In Encoder mode, Sensor mode (event count), this bit field is set to "1".

Note: Regarding of the factors and operation modes of each interrupt, refer to "3.3.4. Interrupt Control".

4.2.14. *[ENxSCMP]* (SCMP Compare Register)

Bit	Bit symbol	After reset	Type	Function
31:0	SCMP[31:0]	0x00000000	R/W	Setting value to compare with a counter value A comparing condition is specified by ***[ENxTNCR]***<SCMPMD>. **[Sensor mode (timer count)]**, **[Timer mode]** A counter value and ***[ENxSCMP]***<SCMP[31:0]> are compared. When the specified condition is fulfilled, ***[ENxINTF]***<SCMPF> is set to "1". When ***[ENxINTCR]***<SCMPIE> is "1", an interrupt INTENCx1 occurs. Only the first condition fulfilled is available for setting ***[ENxSCMP]***<SCMP[31:0]>. Other conditions fulfilled is ignored. (1) Match comparison mode (***[ENxTNCR]***<SCMPMD> = 0) A condition fulfilled signal occurs when a counter value and ***[ENxSCMP]***<SCMP[31:0]> are matched. (2) Magnitude comparison mode (***[ENxTNCR]***<SCMPMD> = 1) A condition fulfilled signal occurs when a counter value is ***[ENxSCMP]***<SCMP[31:0]> or more. **[Encoder mode]**, **[Sensor mode (event count**, **phase count)]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** A counter value and ***[ENxSCMP]***<SCMP[31:0]> are compared. When they are matched, ***[ENxINTF]***<SCMPF> is set to "1".When ***[ENxINTCR]***<SCMPIE> is "1", an interrupt INTENCx1 occurs.

4.2.15. *[ENxDBGOEN]* (Debug Output Control Register)

Bit	Bit symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15	BEMF150 (Note1)	0	R/W	Output setting of synthesized signal of each internal signal in square pulse drive This bit field enables an output of the signals for debugging a program of 150-degree conduction control. 0: Disabled 1: Enabled A output signal is "Low" at detecting a zero crossing → a output signal is "High" at the first phase change → a short output signal is "Low" at the second phase change → a short output signal is "Low" at releasing mask → a output signal is "Low" at detecting a zero crossing, repeated
14	BEMF120 (Note2)	0	R/W	Output setting of synthesized signal of each internal signal in square pulse drive This bit field enables an output of the signals for debugging a program of 120-degree conduction control. 0: Disabled 1: Enabled A output signal is "Low" at detecting a zero crossing → a output signal is "High" at the phase change → a short output signal is "Low" at releasing mask → a output signal is "Low" at detecting a zero crossing, repeated
13	ISCKE	0	R/W	Output enable setting for FF sampling signal When the output is enabled, the signal (d) in Figure 3.15 Configuration of Input Circuit" is output. 0: Disabled 1: Enabled
12	-	0	R/W	Write as "0".
11	ENOUTZ	0	R/W	Output enable setting for SNCZ signal to the decoder When the output is enabled, the signal (c) in "Figure 3.15 Configuration of Input Circuit" is output. 0: Disabled 1: Enabled
10	ENOUTB	0	R/W	Output enable setting for SNCB signal to the decoder When the output is enabled, the signal (c) in "Figure 3.15 Configuration of Input Circuit" is output. 0: Disabled 1: Enabled
9	ENOUTA	0	R/W	Output enable setting for SNCA signal to the decoder When the output is enabled, the signal (c) in "Figure 3.15 Configuration of Input Circuit" is output. 0: Disabled 1: Enabled
8	SMPOUTZ	0	R/W	Output enable setting for the signal input to a noise canceler of ENCxZ pin input When the output is enabled, the signal (b) in "Figure 3.15 Configuration of Input Circuit" is output. 0: Disabled 1: Enabled
7	SMPOUTB	0	R/W	Output enable setting for the signal input to a noise canceler of ENCxB pin input When the output is enabled, the signal (b) in "Figure 3.15 Configuration of Input Circuit" is output. 0: Disabled 1: Enabled

Bit	Bit symbol	After reset	Type	Function
6	SMPOUTA	0	R/W	Output enable setting for the signal input to a noise canceler of ENCxA pin input When the output is enabled, the signal (b) in "Figure 3.15 Configuration of Input Circuit" is output. 0: Disabled 1: Enabled
5:3	-	0	R	Read as "0".
2	METOUTZ	0	R/W	Output enable setting for the signal input to a BEMF filter of ENCxZ pin input When the output is enabled, the signal (a) in "Figure 3.15 Configuration of Input Circuit" is output. 0: Disabled 1: Enabled
1	METOUTB	0	R/W	Output enable setting for the signal input to a BEMF filter of ENCxB pin input When the output is enabled, the signal (a) in "Figure 3.15 Configuration of Input Circuit" is output. 0: Disabled 1: Enabled
0	METOUTA	0	R/W	Output enable setting for the signal input to a BEMF filter of ENCxA pin input When the output is enabled, the signal (a) in "Figure 3.15 Configuration of Input Circuit" is output. 0: Disabled 1: Enabled

Note1: When ***[ENxDBGOEN]***<BEMF150> is set to "1", other bits must be set to "0".

Note2: When ***[ENxDBGOEN]***<BEMF120> is set to "1", other bits must be set to "0".

4.2.16. *[ENxTNCR2]* (Control Register 2)

Bit	Bit symbol	After reset	Type	Function
31:5	-	0	R	Read as "0".
4	ABREV	0	R/W	Phase setting for ENCxA and ENCxB pin inputs when a rotation direction is CW direction **[Encoder mode]**, **[Sensor mode (event count**, **timer count)]**, **[Timer mode]** 0: CW direction: a phase of ENCxA pin input is 90 degrees ahead the ENCxB pin input 1: CCW direction: a phase of ENCxA pin input is 90 degrees behind the ENCxB pin input **[Sensor mode (phase count)]**, **[Phase counter mode (phase measurement**, **phase measurement)]** Write as "0".
3	-	0	R	Read as "0".
2:0	ABZCLRVAL[2:0]	001	R/W	Counter reset condition setting **[Encoder mode]**, **[Sensor mode (event count**, **timer count)]**, **[Timer mode]** 0: "Low" 1: "High" ABZCLRVAL[2]: Specify SNCA state ABZCLRVAL[1]: Specify SNCB state ABZCLRVAL[0]: Specify SNCZ state When ***[ENxTNCR]***<ZEACT> = 1 and <ABZCLRVAL[2:0]> = 001, a counter is cleared by satisfaction below condition. ENCxZ pin input = "Low" ENCxB pin input = "Low" ENCxA pin input = "Low" **[Sensor mode (phase count)]**, **[Phase counter mode (phase measurement**, **phase difference measurement)]** Arbitrary value: No meaning

4.2.17. *[ENxMDOUTCMPn]* (MDOUT Compare Phase n Register, n = 0 to 5)

When ***[ENxINPCR]***<BEMFMODE> is "1", the setting of these registers is valid. And PMDxMDOUT and ***[ENxMDOUTCMPn]*** are compared.
When all bits 16 to 26 in ***[ENxMDOUTCMPn]*** is "0", The matching result is fulfilled in spite of the actual compare result.

Bit	Bit symbol	After reset	Type	Function
31:27	-	0	R	Read as "0".
26	WPWMCMPEN	0	R/W	Enable setting for comparing with WPWM of PMDxMDOUT and ***[ENxMDOUTCMPn]***<WPWMCMP> 0: Disabled 1: Enabled
25	WOC1CMPEN	0	R/W	Enable setting for comparing with WOC1 of PMDxMDOUT and ***[ENxMDOUTCMPn]***<WOC1CMP> 0: Disabled 1: Enabled
24	WOC0CMPEN	0	R/W	Enable setting for comparing with WOC0 of PMDxMDOUT and ***[ENxMDOUTCMPn]***<WOC0CMP> 0: Disabled 1: Enabled
23	-	0	R	Read as "0".
22	VPWMCMPEN	0	R/W	Enable setting for comparing with VPWM of PMDxMDOUT and ***[ENxMDOUTCMPn]***<VPWMCMP> 0: Disabled 1: Enabled
21	VOC1CMPEN	0	R/W	Enable setting for comparing with VOC1 of PMDxMDOUT and ***[ENxMDOUTCMPn]***<VOC1CMP> 0: Disabled 1: Enabled
20	VOC0CMPEN	0	R/W	Enable setting for comparing with VOC0 of PMDxMDOUT and ***[ENxMDOUTCMPn]***<VOC0CMP> 0: Disabled 1: Enabled
19	-	0	R	Read as "0".
18	UPWMCMPEN	0	R/W	Enable setting for comparing with UPWM of PMDxMDOUT and ***[ENxMDOUTCMPn]***<UPWMCMP> 0: Disabled 1: Enabled
17	UOC1CMPEN	0	R/W	Enable setting for comparing with UOC1 of PMDxMDOUT and ***[ENxMDOUTCMPn]***<VOC1CMP> 0: Disabled 1: Enabled
16	UOC0CMPEN	0	R/W	Enable setting for comparing with UOC0 of PMDxMDOUT and ***[ENxMDOUTCMPn]***<VOC0CMP> 0: Disabled 1: Enabled
15:11	-	0	R	Read as "0".
10	WPWMCMP	0	R/W	Comparison value with WPWM of PMDxMDOUT setting
9	WOC1CMP	0	R/W	Comparison value with WOC1 of PMDxMDOUT setting
8	WOC0CMP	0	R/W	Comparison value with WOC0 of PMDxMDOUT setting
7	-	0	R	Read as "0".
6	VPWMCMP	0	R/W	Comparison value with VPWM of PMDxMDOUT setting
5	VOC1CMP	0	R/W	Comparison value with VOC1 of PMDxMDOUT setting
4	VOC0CMP	0	R/W	Comparison value with VOC0 of PMDxMDOUT setting
3	-	0	R	Read as "0".
2	UPWMCMP	0	R/W	Comparison value with UPWM of PMDxMDOUT setting
1	UOC1CMP	0	R/W	Comparison value with UOC1 of PMDxMDOUT setting

Bit	Bit symbol	After reset	Type	Function
0	UOC0CMP	0	R/W	Comparison value with UOC0 of PMDxMDOUT setting

4.2.18. *[ENxINTF2]* (Interrupt Flag Register 2)

A bit field in ***[ENxINTF2]*** is set to "1" when the generation condition of each interrupt is fulfilled at setting the corresponding bit field in ***[ENxINTCR]*** to"1".

It is cleared to "0" by setting a corresponding bit field of ***[ENxINTFCLR]*** to "1". And when ***[ENxTNCR]***<ENRUN> is set to "0", they are also cleared to "0".

Bit	Bit symbol	After reset	Type	Function
31:7	-	0	R	Read as "0".
6	SCMPF2	0	R	SCMP fulfilled flag 0: No satisfaction 1: Satisfied In all operation modes of A-ENC2, this bit field is set to "1".
5	MCMPF2	0	R	MCMP fulfilled flag 0: No satisfaction 1: Satisfied In all operation modes of A-ENC2, this bit field is set to "1".
4	RLDCPF2	0	R	RELOAD match flag 0: No matching 1: Matched In Sensor mode (timer count, phase count), Timer mode, Phase counter mode (phase measurement, phase difference count), this bit field is set to "1".
3	INTCPF2	0	R	INT match flag 0: No matching 1: Matched In all operation modes of A-ENC2, this bit field is set to "1".
2	ERRF2	0	R	Detection error flag 0: No detection 1: Detected In Encoder mode, Sensor mode (event count, timer count, phase count), this bit field is set to "1".
1	CAPF2	0	R	Capture flag 0: No capturing 1: Captured In Sensor mode (timer count, phase count), Timer mode, Phase counter mode (phase measurement, phase difference count), this bit field is set to "1".
0	TPLSF2	0	R	Division flag 0: No dividing 1: Dived In Encoder mode, Sensor mode (event count), this bit field is set to "1".

Note: Regarding of the factors and operation modes of each interrupt, refer to "3.3.4. Interrupt Control".

4.2.19. *[ENxINTFCLR]* (Interrupt Flag Clear Register)

Bit	Bit symbol	After reset	Type	Function
31:7	-	0	R	Read as "0".
6	SCMPFXCR	0	W	Clear setting for SCMP fulfilled flag Read as "0". 0: No meaning 1: ***[ENxINTF]***<SCMPF> and ***[ENxINTF2]***<SCMPF2> are cleared to "0".
5	MCMPFXCR	0	W	Clear setting for SCMP fulfilled flag Read as "0". 0: No meaning 1: ***[ENxINTF]***<MCMPF> and ***[ENxINTF2]***<MCMPF2> are cleared to "0".
4	RLDCPFXCR	0	W	Clear setting for RELOAD match flag Read as "0". 0: No meaning 1: ***[ENxINTF]***<RLDCPF> and ***[ENxINTF2]***<RLDCPF2> are cleared to "0".
3	INTCPFXCR	0	W	Clear setting for INT match flag Read as "0". 0: No meaning 1: ***[ENxINTF]***<INTCPF> and ***[ENxINTF2]***<INTCPF2> are cleared to "0".
2	ERRFXCR	0	W	Clear setting for detection error flag Read as "0". 0: No meaning 1: ***[ENxINTF]***<ERRF> and ***[ENxINTF2]***<ERRF2> are cleared to "0".
1	CAPFXCR	0	W	Clear setting for capture flag Read as "0". 0: No meaning 1: ***[ENxINTF]***<CAPF> and ***[ENxINTF2]***<CAPF2> are clear to "0".
0	TPLSFXCR	0	W	Clear setting for division flag Read as "0". 0: No meaning 1: ***[ENxINTF]***<TPLSF> and ***[ENxINTF2]***<TPLSF2> are cleared to "0".

5. Precaution for Usage

Confirm that ***[ENxTNCR]***<ENRUN> is "0" when the clock supply is stopped. It is also required when the operation mode of MCU is changed to STOP1 mode or STOP2 mode.

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.0	2026-02-20	- First release

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