

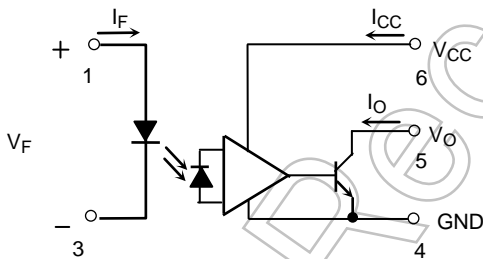
TLP113

Isolated Line Receiver
 Microprocessor System Interface
 Simplex / Multiplex Data Transmission
 Computer-Peripheral Interface
 Digital Isolation For A / D, D / A Conversion

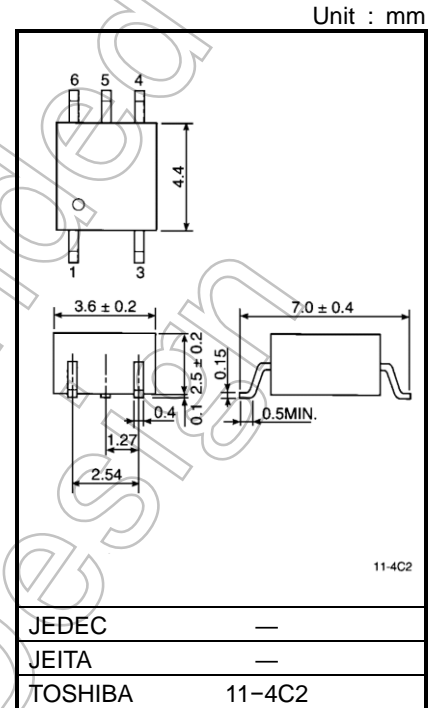
The TOSHIBA mini flat coupler TLP113 is a small outline coupler, suitable for surface mount assembly. TLP113 consists of an infrared emitting diode, optically coupled to an integrated high gain, high speed photodetector whose output is an open collector with schottky clamped transistor. TLP113 : Mini Flat Package, 5Pin, one circuit.

- Input current thresholds: $I_F=10\text{mA}(\text{max})$
- Switching speed: 10MBd(typ.)
- TTL / LSTTL compatible: $V_{CC}=5\text{V}$
- Guaranteed performance over temp.: 0 to 70°C
- Isolation voltage: 2500Vrms(min)
- UL- recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349

Schematic

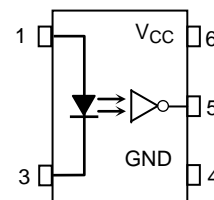


(Note) A 0.1μF bypass capacitor must be connected between pins 4 and 6.



Weight: 0.09 g (typ.)

Pin Configuration(top view)



- 1 : Anode
- 3 : Cathode
- 4 : GND
- 5 : Output (Open collector)
- 6 : V_{CC}

TRUTH TABLE (Positive Logic)

INPUT	OUTPUT
H	L
L	H

Start of commercial production
 1988-04

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
LED	Forward current	I _F	20	mA
	Forward current derating (Ta ≥ 85 °C)	I _F /°C	-1.6	mA/°C
	Pulse forward current (Note 1)	I _{FP}	40	mA
	Peak transient forward current (Note 2)	I _{FPT}	1	A
	Reverse voltage	V _R	5	V
	Diode power dissipation	PD	40	mW
	Diode power dissipation derating (Ta ≥ 85°C)	ΔPD/°C	-1.0	mW/°C
Detector	Output current	I _O	25	mA
	Output voltage	V _O	7	V
	Supply voltage (60 s maximum)	V _{CC}	7	V
	Output power dissipation	P _O	40	mW
	Output power dissipation derating (Ta ≥ 85 °C)	P _O /°C	-5.7	mW/°C
Operating temperature range		T _{opr}	-40 to 85	°C
Storage temperature range		T _{stg}	-55 to 125	°C
Lead solder temperature (10 s)		T _{sol}	260	°C
Isolation voltage (AC, 60 s., RH ≤ 60 %) (Note 3)		BV _S	2500	V _{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: 50 % duty cycle, 1 ms pulse width.

Note 2: Pulse width ≤ 1 μs, 300 pps.

Note 3: This device is regarded as a two terminal device: pins 1 and 3 are shorted together, as are pins 4, 5 and 6.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Input voltage, low level	V _{FL}	-3	0	1.0	V
Input current, high level	I _{FH}	13*	16	20	mA
Supply voltage**	V _{CC}	4.5	5	5.5	V
Fan out (TTL load)	N	—	—	8	—
Operating temperature	T _{opr}	0	—	70	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

* 13mA is a guard banded value which allows for at least 20 % CTR degradation.
Initial input current threshold value is 10 mA or less.

**This item denotes operating ranges, not meaning of recommended operating conditions.

Electrical Characteristics(unless otherwise specified, Ta=0 to 70°C, Vcc=4.5 to 5.5V, VFL ≤ 1.0V)

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Forward voltage	V _F	I _F = 10 mA, Ta = 25 °C	—	1.65	1.80	V
Forward voltage temperature coefficient	ΔV _F /ΔTa	I _F = 10 mA	—	-2	—	mV / °C
Reverse current	I _R	V _R = 5 V, Ta = 25 °C	—	—	10	μA
Capacitance between terminals	C _T	V _F = 0 V, f = 1 MHz, Ta = 25 °C	—	45	—	pF
High level output current	I _{OH}	V _F = 1.0 V, V _O = 5.5 V	—	—	250	μA
		V _F = 1.0 V, V _O = 5.5 V, Ta = 25 °C	—	0.5	10	
Low level output voltage	V _{OL}	I _F = 10 mA I _{OL} = 13 mA(sinking)	—	0.4	0.6	V
"H level output → L level output" input current	I _{FH}	I _{OL} = 13 mA(sinking) V _{OL} = 0.6 V	—	—	10	mA
High level supply current	I _{CCH}	V _{CC} = 5.5 V, I _F = 0 mA	—	7	15	mA
Low level supply current	I _{CCL}	V _{CC} = 5.5 V, I _F = 16 mA	—	12	18	mA
Input-output insulation leakage current	I _S	V _S = 3540 V, t = 5 s Ta = 25 °C (Note 1)	—	—	100	μA
Isolation resistance	R _S	R.H. ≤ 60 %, V _S = 500 VDC Ta = 25 °C (Note 1)	5×10 ¹⁰	10 ¹⁴	—	Ω
Stray capacitance between input to output	C _S	V _S = 0 V, f = 1 MHz Ta = 25 °C (Note 1)	—	0.8	—	pF

* All typical values are V_{CC} = 5 V, Ta = 25 °C

Note1: Device considered a two-terminal device: Pins 1 and 3 shorted together, and pins 4, 5 and 6 shorted together.

Switching Characteristics (Vcc=5V, Ta=25°C)

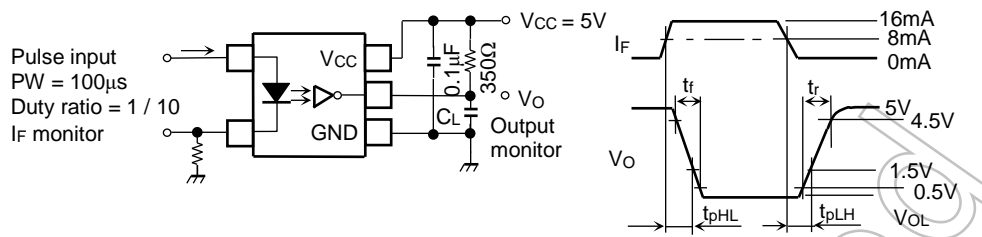
Characteristics	Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time (H→L)	t _{pHL}	1	I _F = 0 → 16 mA C _L = 15 pF, R _L = 350 Ω	—	60	120	ns
Propagation delay time (L→H)	t _{pLH}	1	I _F = 16 → 0 mA C _L = 15 pF, R _L = 350 Ω	—	60	120	ns
Output rise-fall time (10-90%)	t _r , t _f	1	R _L = 350 Ω, C _L = 15 pF I _F = 0 ↔ 16 mA	—	30	—	ns
Common mode transient immunity at high output level	CM _H	2	I _F = 0 mA, V _{CM} = 200V _{p-p} V _{O(min)} = 2 V, R _L = 350 Ω	—	200	—	V / μs
Common mode transient immunity at low output level	CM _L	2	I _F = 16 mA, V _{CM} = 200 V _{p-p} V _{O(max)} = 0.8 V, R _L = 350 Ω	—	-500	—	V / μs

Note: The V_{CC} supply voltage to each TLP113 isolator must be bypassed by 0.1 μF capacitor, this can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to package V_{CC} and GND pins of each device.

Note: CM_H is the maximum rising common mode voltage waveform (voltage/time) that can keep high level (V_O > 2.0 V)

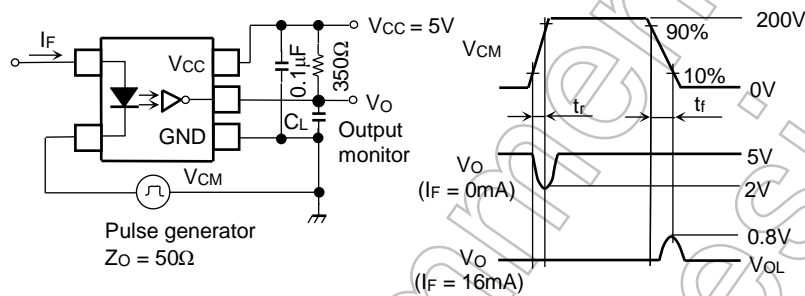
Note: CM_L is the maximum falling common mode voltage waveform (voltage/time) that can keep low level (V_O < 0.8 V).

Test Circuit 1: Switching Time Test Circuit



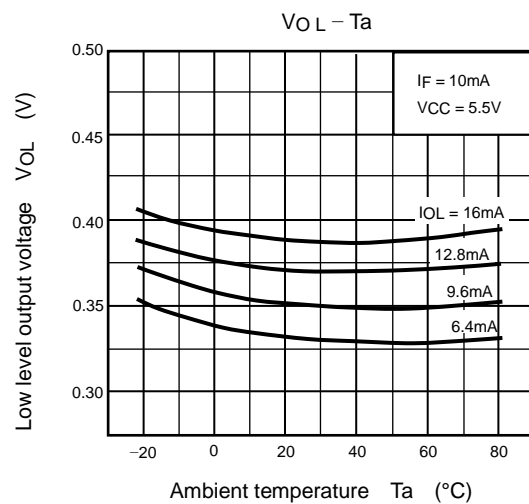
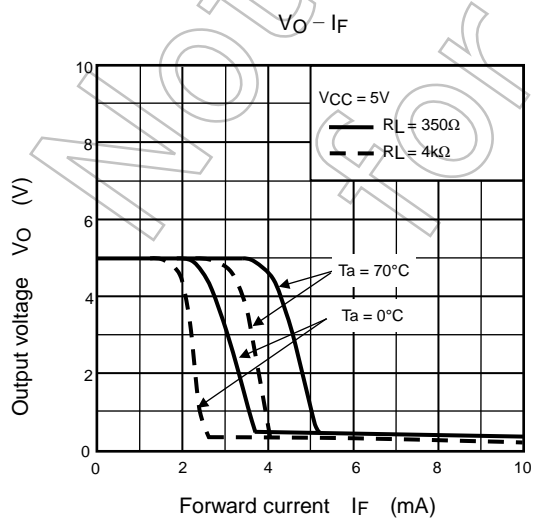
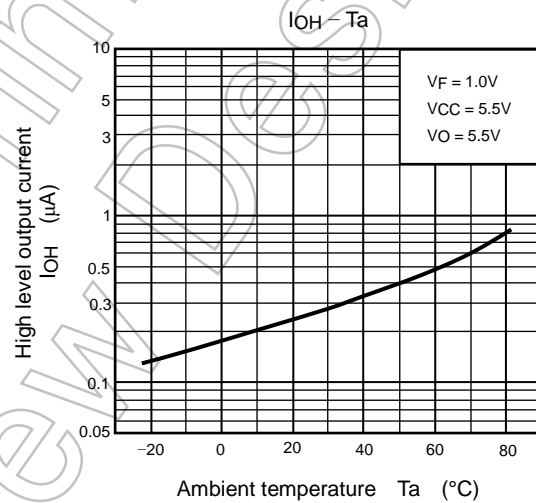
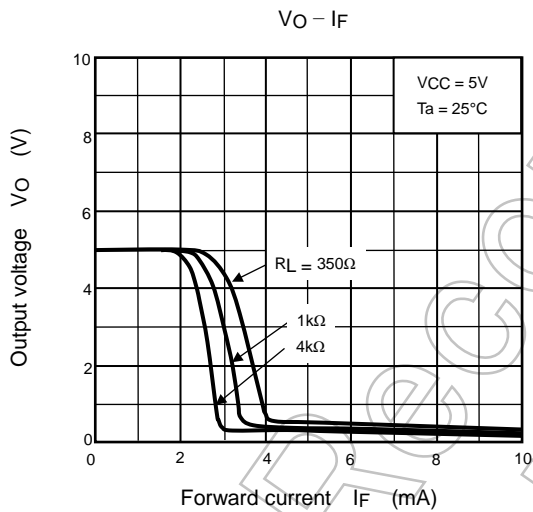
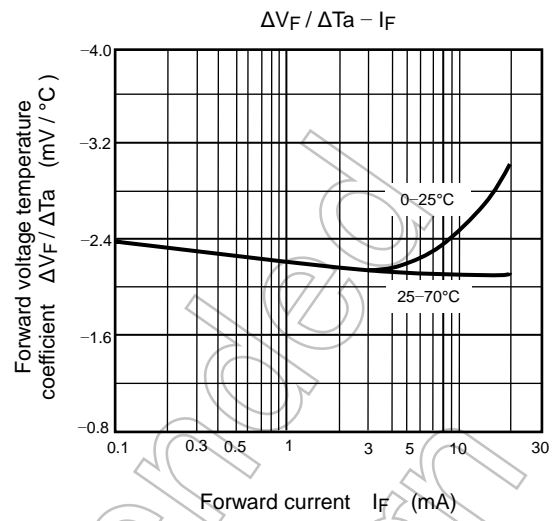
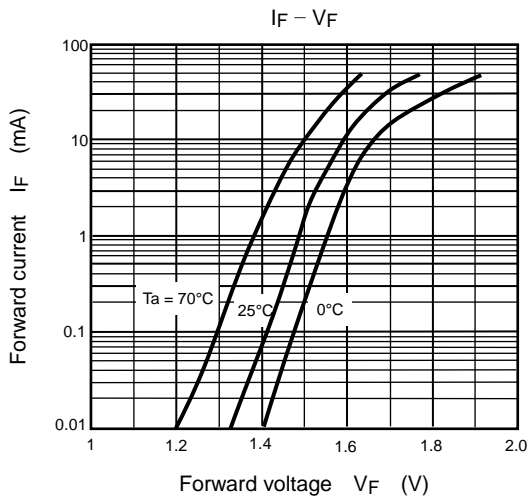
CL is approximately 15pF which includes probe and stray wiring capacitance.

Test Circuit 2: Common Mode Transient Immunity Test Circuit

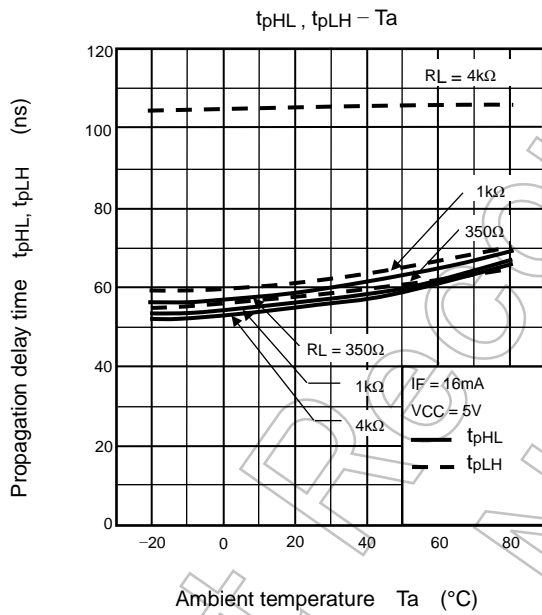
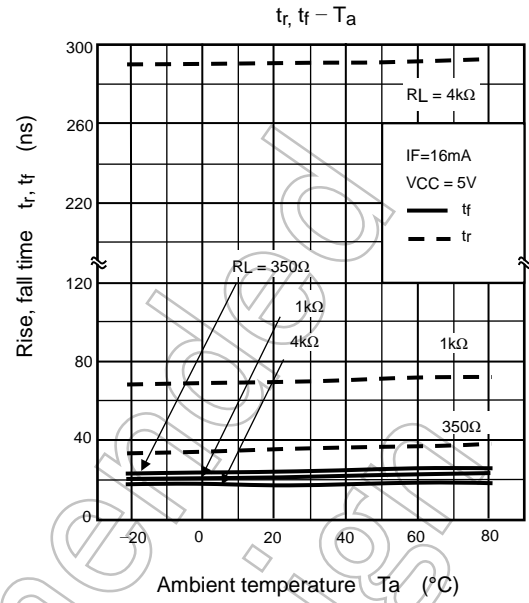
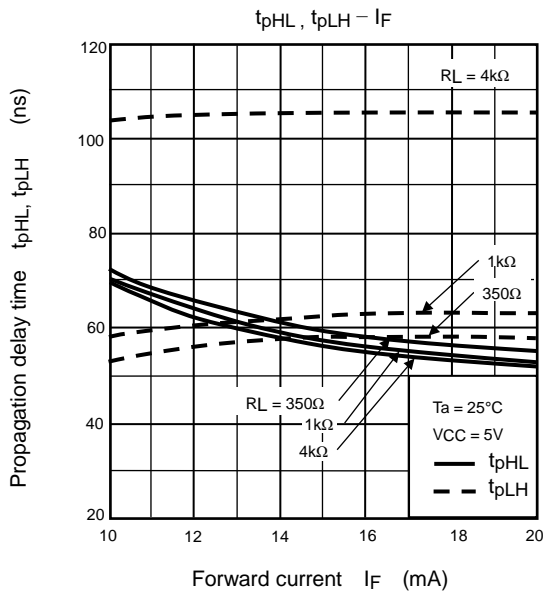


$$CM_H = \frac{160(V)}{t_r(\mu s)}, CM_L = \frac{160(V)}{t_f(\mu s)}$$

CL is approximately 15pF which includes probe and stray wiring capacitance.



NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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