

LOW POWER QUAD CHANNEL DIGITAL ISOLATORS

# DCL341x0B

**DCL341L0B/DCL341H0B**

## 1. Applications

- Industrial automation systems
- Motor control
- Inverter
- Switching power supply

## 2. Description

DCL341L0B/DCL341H0B are low power quad-channel digital isolators. Outstanding performance characteristics are achieved by Toshiba CMOS technology and the magnetic coupling structure. In addition, they comply with UL 1577 and has a 3000V<sub>rms</sub> rating as an isolation voltage. These products can operate with a temperature range of -40 to 125 °C and a wide supply voltage of 2.25 to 5.5 V.

## 3. Features

Data rate	: Up to 25 Mbps
Supply voltage	: 2.25 V to 5.5 V
Temperature Range	: -40 °C to 125 °C
Propagation Delay	: 32 ns Typ. (5.0 V operation)
Default Output	: High and Low Options
High CMTI(min.)	: ±30 kV/μs
Withstand Voltage	: 3 kV <sub>rms</sub>
Package	: 16pin SSOP (16LD QSOP)
Safety-Related Certification	: UL1577, CQC, VDE DIN EN 60747-17
UL	: UL1577, File No. E519997
cUL	: CSA Component Acceptance Service Notice No. 5A
VDE	: DIN EN IEC 60747-17 (VDE 0884-17) (Planning)
CQC	: GB 4943.1-2022 (Planning)

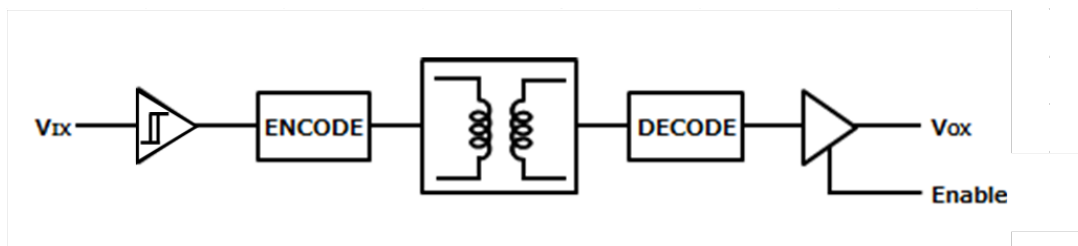
Start of commercial production

2026-04

**Table of Contents**

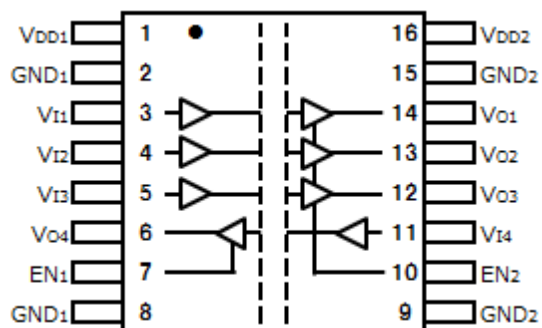
<b>1.</b>	<b>Applications.....</b>	<b>1</b>
<b>2.</b>	<b>Description .....</b>	<b>1</b>
<b>3.</b>	<b>Features .....</b>	<b>1</b>
<b>4.</b>	<b>Internal Circuit.....</b>	<b>3</b>
<b>5.</b>	<b>Pin configuration and Functions.....</b>	<b>3</b>
<b>5.1.</b>	<b>Pin Functions.....</b>	<b>4</b>
<b>6.</b>	<b>Functional Description .....</b>	<b>5</b>
<b>7.</b>	<b>Absolute Maximum Ratings (Ta = 25 °C).....</b>	<b>6</b>
<b>8.</b>	<b>Recommended Operating Conditions (Note) .....</b>	<b>6</b>
<b>9.</b>	<b>Electrical Characteristics .....</b>	<b>7</b>
<b>9.1.</b>	<b>Electrical Characteristics – 5 V Supply.....</b>	<b>7</b>
<b>9.2.</b>	<b>Electrical Characteristics – 3.3 V Supply .....</b>	<b>8</b>
<b>9.3.</b>	<b>Electrical Characteristics – 2.5 V Supply .....</b>	<b>9</b>
<b>9.4.</b>	<b>Supply Current Characteristics – 5 V Supply .....</b>	<b>10</b>
<b>9.5.</b>	<b>Supply Current Characteristics – 3.3 V Supply .....</b>	<b>11</b>
<b>9.6.</b>	<b>Supply Current Characteristics – 2.5 V Supply .....</b>	<b>12</b>
<b>10.</b>	<b>Insulation Specifications .....</b>	<b>13</b>
<b>11.</b>	<b>Safety Limiting Values .....</b>	<b>14</b>
<b>12.</b>	<b>Test Circuit .....</b>	<b>15</b>
<b>13.</b>	<b>Characteristics Curves (Note) .....</b>	<b>17</b>
<b>14.</b>	<b>Package Information .....</b>	<b>18</b>
<b>15.</b>	<b>Ordering guide .....</b>	<b>19</b>
	<b>RESTRICTIONS ON PRODUCT USE.....</b>	<b>20</b>

## 4. Internal Circuit



## 5. Pin configuration and Functions

DCL341L0B / DCL341H0B



## 5.1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	DCL341L0B DCL341H0B		
V <sub>DD1</sub>	1	-	Power Supply, side 1
GND <sub>1</sub>	2,8	-	GND connection for V <sub>DD1</sub> , side 1
V <sub>I1</sub>	3	I	Input, Channel1
V <sub>I2</sub>	4	I	Input, Channel2
V <sub>I3</sub>	5	I	Input, Channel3
V <sub>I4</sub>	11	I	Input, Channel4
EN <sub>1</sub>	7	I	Output enable 1. Input pins on side 1 are enabled when EN <sub>1</sub> is high, and in high impedance state when EN <sub>1</sub> is low.
GND <sub>2</sub>	9,15	-	GND connection for V <sub>DD2</sub> , side 2
EN <sub>2</sub>	10	I	Output enable 2. Output pins on side 2 are enabled when EN <sub>2</sub> is high, and in high impedance state when EN <sub>2</sub> is low.
V <sub>O4</sub>	6	O	Output, Channel4
V <sub>O3</sub>	12	O	Output, Channel3
V <sub>O2</sub>	13	O	Output, Channel2
V <sub>O1</sub>	14	O	Output, Channel1
V <sub>DD2</sub>	16	-	Power Supply, side 2

## 6. Functional Description

### DCL341L0B/DCL341H0B

V <sub>DDI</sub>	V <sub>DDO</sub>	OUTPUT ENABLE (ENx)	INPUT (V <sub>IX</sub> )	OUTPUT (V <sub>OX</sub> )	DESCRIPTION
PU	PU	H	L	L	Normal Operation
			H	H	
		L	L or H	Z	Output Disable mode
PU	PD	X	L or H	Undetermined	When V <sub>DDO</sub> is unpowered, a channel output is undetermined.
PD	PU	H	X	Default	Default mode DCL34xL0B=L , DCL34xH0B=H
		L		Z	Output Disable mode
PD	PD	X	X	Undetermined	When V <sub>DDO</sub> is unpowered, a channel output is undetermined.

PU= Powered up (V<sub>DD</sub>≥2.25 V), PD= Powered down (V<sub>DD</sub><2.25 V→0V), H= High level, L= Low level, X= Don't Care

V<sub>DDI</sub>, V<sub>DDO</sub>: Supply voltages on the input and output sides of each channel.

ENx : Output enable signal on the same side as the V<sub>OX</sub> output.

V<sub>IX</sub>, V<sub>OX</sub> : Input and output signals of each channel.

When the input pin (V<sub>IX</sub>) on the power-off side is set to "H", power is supplied to the device via the ESD circuit, so use is prohibited. Don't leave the Input pin (V<sub>IX</sub>) and Enable pin (ENx) on the power ON side open because terminal circuits don't have pull-down resistor or pull-down resistor inside.

## 7. Absolute Maximum Ratings (Ta = 25 °C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power supply voltage	V <sub>DD1</sub> , V <sub>DD2</sub>	-0.5	6.0	V
Input Voltage	V <sub>I</sub>	-0.5	V <sub>DDX</sub> +0.5 <sup>(1)</sup>	V
Output Voltage	V <sub>O</sub>	-0.5	V <sub>DDX</sub> +0.5 <sup>(1)</sup>	V
Output Current	I <sub>O</sub>	-15	15	mA
Storage Temperature	T <sub>stg</sub>	-65	150	°C
Operating Temperature	T <sub>opr</sub>	-40	125	°C
Soldering Temperature (10 s)	T <sub>sol</sub>	-	260	°C
Maximum Withstanding Isolation Voltage (1 min.)	BV <sub>S</sub>	-	3000	V <sub>rms</sub>

1: Maximum voltage must not exceed 6 V. X = 1 or 2.

## 8. Recommended Operating Conditions (Note)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power supply voltage	V <sub>DD1</sub> , V <sub>DD2</sub>	2.25	5.5	V
Junction Temperature	T <sub>J</sub>	-40	150	°C
Operating Temperature	T <sub>opr</sub>	-40	125	°C

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this data sheet should also be considered.

Note: A ceramic capacitor (0.1 μF) should be connected between pin 1 (V<sub>DD1</sub>) and pin 2 (GND<sub>1</sub>) for V<sub>DD1</sub> and between pin 16 (V<sub>DD2</sub>) and pin 15 (GND<sub>2</sub>) for V<sub>DD2</sub> and should be the layout on the IC as close as possible (less than 10 mm). Otherwise, the IC may not switch properly.

## 9. Electrical Characteristics

### 9.1. Electrical Characteristics – 5 V Supply

All typical specifications are at  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 5\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operating range of  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ , and  $-40\text{ }^\circ\text{C} \leq T_a \leq 125\text{ }^\circ\text{C}$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
<b>DC SPECIFICATIONS</b>							
Output Voltage Logic High	$V_{IX} = H, I_{OH} = -20\text{ }\mu\text{A}$	-	$V_{OH}$	$V_{DDO}^{(1)}-0.1$	$V_{DDO}^{(1)}$	-	V
	$V_{IX} = H, I_{OH} = -4\text{ mA}$			$V_{DDO}^{(1)}-0.4$	$V_{DDO}^{(1)}-0.2$	-	
Output Voltage Logic Low	$V_{IX} = L, I_{OL} = 20\text{ }\mu\text{A}$	-	$V_{OL}$	-	0.0	0.1	V
	$V_{IX} = L, I_{OL} = 4\text{ mA}$			-	0.2	0.4	
Output impedance	-	-	$Z_O$	-	50	-	$\Omega$
High-level input voltage	-	-	$V_{IH}$	$0.7 \cdot V_{DD1}^{(1)}$	-	-	V
Low-level input voltage	-	-	$V_{IL}$	-	-	$0.3 \cdot V_{DD1}^{(1)}$	V
Input Voltage Hysteresis	-	-	$V_{HYS}$	-	0.44	-	V
Input Current	$V_I = V_{DD1}^{(1)}$ or 0 V	-	$I_i$	-	-	$\pm 1$	$\mu\text{A}$
<b>SWITCHING SPECIFICATIONS</b>							
Data Rate	-	-	$t_{bps}$	DC	-	25	Mbps
Pulse Width	-	-	PW	40	-	-	ns
Propagation Delay	50 kHz, Duty = 50 %, $t_r = t_f = 2\text{ ns}$ , $C_L = 15\text{ pF}$	Fig. 12-1	$t_{PHL}, t_{PLH}$	-	-	46	ns
<b>DC~10Mbps</b>							
Pulse Width Distortion	$ t_{PHL} - t_{PLH} $	Fig. 12-1	PWD	-	-	8.0	ns
Propagation Delay Skew <sup>(2)</sup> (Between any two units)	-	-	$t_{PSK}$	-	-	16	ns
Channel Matching	Same Direction	-	$t_{skCD}$	-	-	5.0	ns
	Opposing Direction	-	$t_{skOD}$	-	-	7.0	
<b>DC~25Mbps</b>							
Pulse Width Distortion	$ t_{PHL} - t_{PLH} $	Fig. 12-1	PWD	-	-	13	ns
Propagation Delay Skew <sup>(2)</sup> (Between any two units)	-	-	$t_{PSK}$	-	-	21	ns
Channel Matching	Same Direction	-	$t_{skCD}$	-	-	10	ns
	Opposing Direction	-	$t_{skOD}$	-	-	12	
Output Rise Time	10 % - 90 %	Fig. 12-1	$t_r$	-	2.0	-	ns
Output Fall Time	90 % - 10 %	Fig. 12-1	$t_f$	-	2.0	-	ns
Enable 3-state output enable time <sup>(3)</sup>	50 kHz, Duty = 50 %, $t_r = t_f = 2\text{ ns}$ , $C_L = 15\text{ pF}$	Fig. 12-3	$t_{PZL}, t_{PZH}$	-	-	10	ns
Enable 3-state output disable time		Fig. 12-3	$t_{PLZ}, t_{PHZ}$	-	-	15	
Default output delay time from input power loss	$V_{DD1} < 2.25\text{ V} \rightarrow 0\text{ V}$		$t_{DO}$	-	-	25	$\mu\text{s}$
Time from PU <sup>(4)</sup> to valid output data			$t_{PU}$	-	-	30	$\mu\text{s}$
Common mode transient immunity	$V_I = V_{DD1}$ or 0 V, $V_{CM} = 1000\text{ V}$ , $T_a = 25\text{ }^\circ\text{C}$	Fig. 12-5	$ CMTI $	30	-	-	kV/ $\mu\text{s}$

1:  $V_{DD1}$  = Input-side  $V_{DDX}$ ,  $V_{DDO}$  = Output-side  $V_{DDX}$  2: Propagation delay difference (between parts) is applied under the same operating conditions (power supply voltage, input current, temperature conditions, etc.).

3: When ENx signal is changed from Low to High, the output signal ( $V_{OX}$ ) is valid after the output enable time. The output signal ( $V_{OX}$ ) within the output enable time is undefined.

4: PU = Powered up ( $V_{DD} \geq 2.25\text{ V}$ ), After VDD is set powered up, normal operation become valid 30  $\mu\text{s}$  later.

## 9.2. Electrical Characteristics – 3.3 V Supply

All typical specifications are at  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 3.3\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operating range of  $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ , and  $-40\text{ }^\circ\text{C} \leq T_a \leq 125\text{ }^\circ\text{C}$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
<b>DC SPECIFICATIONS</b>							
Output Voltage Logic High	$V_{IX} = H, I_{OH} = -20\text{ }\mu\text{A}$	-	$V_{OH}$	$V_{DDO}^{(1)}-0.1$	$V_{DDO}^{(1)}$	-	V
	$V_{IX} = H, I_{OH} = -4\text{ mA}$			$V_{DDO}^{(1)}-0.4$	$V_{DDO}^{(1)}-0.2$	-	
Output Voltage Logic Low	$V_{IX} = L, I_{OL} = 20\text{ }\mu\text{A}$	-	$V_{OL}$	-	0.0	0.1	V
	$V_{IX} = L, I_{OL} = 4\text{ mA}$			-	0.2	0.4	
Output impedance	-	-	$Z_o$	-	50	-	$\Omega$
High-level input voltage	-	-	$V_{IH}$	$0.7 \cdot V_{DDI}^{(1)}$	-	-	V
Low-level input voltage	-	-	$V_{IL}$	-	-	$0.3 \cdot V_{DDI}^{(1)}$	V
Input Voltage Hysteresis	-	-	$V_{HYS}$	-	0.25	-	V
Input Current	$V_I = V_{DDI}^{(1)}$ or 0 V	-	$I_I$	-	-	$\pm 1$	$\mu\text{A}$
<b>SWITCHING SPECIFICATIONS</b>							
Data Rate	-	-	$t_{bps}$	DC	-	25	Mbps
Pulse Width	-	-	PW	40	-	-	ns
Propagation Delay	50 kHz, Duty = 50 %, $t_r = t_f = 2\text{ ns}$ , $C_L = 15\text{ pF}$	Fig. 12-1	$t_{PHL}, t_{PLH}$	-	-	52	ns
<b>DC~10Mbps</b>							
Pulse Width Distortion	$ t_{PHL} - t_{PLH} $	Fig. 12-1	PWD	-	-	8.0	ns
Propagation Delay Skew <sup>(2)</sup> (Between any two units)	-	-	$t_{PSK}$	-	-	19	ns
Channel Matching	Same Direction	-	$t_{skCD}$	-	-	5.0	ns
	Opposing Direction	-	$t_{skOD}$	-	-	9.0	
<b>DC~25Mbps</b>							
Pulse Width Distortion	$ t_{PHL} - t_{PLH} $	Fig. 12-1	PWD	-	-	13	ns
Propagation Delay Skew <sup>(2)</sup> (Between any two units)	-	-	$t_{PSK}$	-	-	24	ns
Channel Matching	Same Direction	-	$t_{skCD}$	-	-	10	ns
	Opposing Direction	-	$t_{skOD}$	-	-	14	
Output Rise Time	10 % - 90 %	Fig. 12-1	$t_r$	-	2.0	-	ns
Output Fall Time	90 % - 10 %	Fig. 12-1	$t_f$	-	2.0	-	ns
Enable 3-state output enable time <sup>(3)</sup>	50 kHz, Duty = 50 %, $t_r = t_f = 2\text{ ns}$ , $C_L = 15\text{ pF}$	Fig. 12-3	$t_{PZL}, t_{PZH}$	-	-	15	ns
Enable 3-state output disable time		Fig. 12-3	$t_{pLZ}, t_{pHZ}$	-	-	20	ns
Default output delay time from input power loss	$V_{DDI} < 2.25\text{ V} \rightarrow 0\text{ V}$	-	$t_{DO}$	-	-	30	$\mu\text{s}$
Time from PU <sup>(4)</sup> to valid output data	-	-	$t_{PU}$	-	-	30	$\mu\text{s}$
Common mode transient immunity	$V_I = V_{DDI}$ or 0 V, $V_{CM} = 1000\text{ V}$ , $T_a = 25\text{ }^\circ\text{C}$	Fig. 12-5	CMTI	30	-	-	kV/ $\mu\text{s}$

1:  $V_{DDI}$  = Input-side  $V_{DDX}$ ,  $V_{DDO}$  = Output-side  $V_{DDX}$  2: Propagation delay difference (between parts) is applied under the same operating conditions (power supply voltage, input current, temperature conditions, etc.).

3: When ENx signal is changed from Low to High, the output signal ( $V_{OX}$ ) is valid after the output enable time. The output signal ( $V_{OX}$ ) within the output enable time is undefined.

4: PU = Powered up ( $V_{DD} \geq 2.25\text{ V}$ ), After VDD is set powered up, normal operation become valid 30  $\mu\text{s}$  later.

## 9.3. Electrical Characteristics – 2.5 V Supply

All typical specifications are at  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 2.5\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operating range of  $2.25\text{ V} \leq V_{DD1} \leq 2.75\text{ V}$ ,  $2.25\text{ V} \leq V_{DD2} \leq 2.75\text{ V}$ , and  $-40\text{ }^\circ\text{C} \leq T_a \leq 125\text{ }^\circ\text{C}$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
<b>DC SPECIFICATIONS</b>							
Output Voltage Logic High	$V_{IX} = H$ , $I_{OH} = -20\text{ }\mu\text{A}$	-	$V_{OH}$	$V_{DDO}^{(1)}-0.1$	$V_{DDO}^{(1)}$	-	V
	$V_{IX} = H$ , $I_{OH} = -4\text{ mA}$	-		$V_{DDO}^{(1)}-0.4$	$V_{DDO}^{(1)}-0.2$	-	
Output Voltage Logic Low	$V_{IX} = L$ , $I_{OL} = 20\text{ }\mu\text{A}$	-	$V_{OL}$	-	0.0	0.1	V
	$V_{IX} = L$ , $I_{OL} = 4\text{ mA}$	-		-	0.2	0.4	
Output impedance	-	-	$Z_o$	-	50	-	$\Omega$
High-level input voltage	-	-	$V_{IH}$	$0.7 \cdot V_{DDI}^{(1)}$	-	-	V
Low-level input voltage	-	-	$V_{IL}$	-	-	$0.3 \cdot V_{DDI}^{(1)}$	V
Input Voltage Hysteresis	-	-	$V_{HYS}$	-	0.22	-	V
Input Current	$V_I = V_{DDI}^{(1)}$ or 0 V	-	$I_I$	-	-	$\pm 1$	$\mu\text{A}$
<b>SWITCHING SPECIFICATIONS</b>							
Data Rate	-	-	$t_{bps}$	DC	-	25	Mbps
Pulse Width	-	-	PW	40	-	-	ns
Propagation Delay	50 kHz, Duty = 50 %, $t_r = t_f = 2\text{ ns}$ , $C_L = 15\text{ pF}$	Fig. 12-1	$t_{PHL}$ , $t_{PLH}$	-	-	63	ns
<b>DC~10Mbps</b>							
Pulse Width Distortion	$ t_{PHL} - t_{PLH} $	Fig. 12-1	PWD	-	-	8.0	ns
Propagation Delay Skew <sup>(2)</sup> (Between any two units)	-	-	$t_{PSK}$	-	-	24	ns
Channel Matching	Same Direction	-	$t_{skCD}$	-	-	7.0	ns
	Opposing Direction	-	$t_{skOD}$	-	-	11	
<b>DC~25Mbps</b>							
Pulse Width Distortion	$ t_{PHL} - t_{PLH} $	Fig. 12-1	PWD	-	-	13	ns
Propagation Delay Skew <sup>(2)</sup> (Between any two units)	-	-	$t_{PSK}$	-	-	29	ns
Channel Matching	Same Direction	-	$t_{skCD}$	-	-	12	ns
	Opposing Direction	-	$t_{skOD}$	-	-	16	
Output Rise Time	10 % - 90 %	Fig. 12-1	$t_r$	-	2.0	-	ns
Output Fall Time	90 % - 10 %	Fig. 12-1	$t_f$	-	2.0	-	ns
Enable 3-state output enable time <sup>(3)</sup>	50 kHz, Duty = 50 %, $t_r = t_f = 2\text{ ns}$ , $C_L = 15\text{ pF}$	Fig. 12-3	$t_{pZL}$ , $t_{pZH}$	-	-	20	ns
Enable 3-state output disable time		Fig. 12-3	$t_{pLZ}$ , $t_{pHZ}$	-	-	25	ns
Default output delay time from input power loss	$V_{DDI} < 2.25\text{ V} \rightarrow 0\text{ V}$	-	$t_{DO}$	-	-	40	$\mu\text{s}$
Time from PU <sup>(4)</sup> to valid output data	-	-	$t_{PU}$	-	-	30	$\mu\text{s}$
Common mode transient immunity	$V_I = V_{DDI}$ or 0 V, $V_{CM} = 1000\text{ V}$ , $T_a = 25\text{ }^\circ\text{C}$	Fig. 12-5	CMTI	30	-	-	kV/ $\mu\text{s}$

1:  $V_{DDI}$  = Input-side  $V_{DDX}$ ,  $V_{DDO}$  = Output-side  $V_{DDX}$  2: Propagation delay difference (between parts) is applied under the same operating conditions (power supply voltage, input current, temperature conditions, etc.).

3: When ENx signal is changed from Low to High, the output signal ( $V_{OX}$ ) is valid after the output enable time. The output signal ( $V_{OX}$ ) within the output enable time is undefined.

4: PU = Powered up ( $V_{DD} \geq 2.25\text{ V}$ ), After VDD is set powered up, normal operation become valid 30  $\mu\text{s}$  later.

## 9.4. Supply Current Characteristics – 5 V Supply

All typical specifications are at  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 5\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operating range of  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ , and  $-40\text{ }^\circ\text{C} \leq T_a \leq 125\text{ }^\circ\text{C}$ , unless otherwise noted.

### (1) DCL341x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current ( DC Signal )	EN1,EN2 = High Enable VI = 0 or 1	I <sub>DD1(Q)</sub>	-	305	645	μA
		I <sub>DD2(Q)</sub>	-	340	940	μA
1 Mbps	f <sub>CLK</sub> = 500 kHz, duty = 50 % cycle square wave. No load	I <sub>DD1(1)</sub>	-	440	790	μA
		I <sub>DD2(1)</sub>	-	495	1105	μA
1 Mbps	f <sub>CLK</sub> = 500 kHz, duty = 50 % cycle square wave. C <sub>L</sub> = 15 pF	I <sub>DD1(1)</sub>	-	490	845	μA
		I <sub>DD2(1)</sub>	-	625	1240	μA
25 Mbps	f <sub>CLK</sub> = 12.5 MHz, duty = 50 % cycle square wave. C <sub>L</sub> = 15 pF	I <sub>DD1(25)</sub>	-	9.1	12.7	mA
		I <sub>DD2(25)</sub>	-	8.8	11.4	mA

## 9.5. Supply Current Characteristics – 3.3 V Supply

All typical specifications are at  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 3.3\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operating range of  $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ , and  $-40\text{ }^\circ\text{C} \leq T_a \leq 125\text{ }^\circ\text{C}$ , unless otherwise noted.

### (1) DCL341x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current ( DC Signal )	EN1,EN2 = High Enable VI = 0 or 1	I <sub>DD1(Q)</sub>	-	235	505	μA
		I <sub>DD2(Q)</sub>	-	260	745	μA
1 Mbps	f <sub>CLK</sub> = 500 kHz, duty = 50 % cycle square wave. No load	I <sub>DD1(1)</sub>	-	320	580	μA
		I <sub>DD2(1)</sub>	-	360	845	μA
1 Mbps	f <sub>CLK</sub> = 500 kHz, duty = 50 % cycle square wave. C <sub>L</sub> = 15 pF	I <sub>DD1(1)</sub>	-	350	620	μA
		I <sub>DD2(1)</sub>	-	445	950	μA
25 Mbps	f <sub>CLK</sub> = 12.5 MHz, duty = 50 % cycle square wave. C <sub>L</sub> = 15 pF	I <sub>DD1(25)</sub>	-	6.5	9.6	mA
		I <sub>DD2(25)</sub>	-	5.8	7.8	mA

## 9.6. Supply Current Characteristics – 2.5 V Supply

All typical specifications are at  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 2.5\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operating range of  $2.25\text{ V} \leq V_{DD1} \leq 2.75\text{ V}$ ,  $2.25\text{ V} \leq V_{DD2} \leq 2.75\text{ V}$ , and  $-40\text{ }^\circ\text{C} \leq T_a \leq 125\text{ }^\circ\text{C}$ , unless otherwise noted

### (1) DCL341x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current ( DC Signal )	EN1,EN2 = High Enable VI = 0 or 1	I <sub>DD1(Q)</sub>	-	210	455	μA
		I <sub>DD2(Q)</sub>	-	240	690	μA
1 Mbps	f <sub>CLK</sub> = 500 kHz, duty = 50 % cycle square wave. No load	I <sub>DD1(1)</sub>	-	280	520	μA
		I <sub>DD2(1)</sub>	-	310	765	μA
1 Mbps	f <sub>CLK</sub> = 500 kHz, duty = 50 % cycle square wave. C <sub>L</sub> = 15 pF	I <sub>DD1(1)</sub>	-	305	545	μA
		I <sub>DD2(1)</sub>	-	375	845	μA
25 Mbps	f <sub>CLK</sub> = 12.5 MHz, duty = 50 % cycle square wave. C <sub>L</sub> = 15 pF	I <sub>DD1(25)</sub>	-	5.7	8.4	mA
		I <sub>DD2(25)</sub>	-	4.6	6.3	mA

## 10. Insulation Specifications

PARAMETER	Symbol	TEST CONDITIONS	VALUE	UNIT
Minimum External Clearance	CLR	Shortest terminal-to-terminal distance through air	3.7	mm
Minimum External Creepage	CPG	Shortest terminal-to-terminal distance across the package surface	3.4	mm
Distance Through The Insulation	DTI	Minimum internal gap	8.5	μm
Comparative Tracking Index	CTI		400	V
Material Group	-	According to IEC 60664-1	II	-
Overvoltage Category Per IEC 60664-1	-	Rated main voltage ≤ 300 V <sub>RMS</sub>	I-III	-
<b>DIN EN IEC 60747-17; (VDE 0884-17)</b>				
Maximum Repetitive Peak Isolation Voltage	V <sub>IORM</sub>	AC voltage (bipolar)	566	V <sub>PK</sub>
Maximum Transient Isolation Voltage	V <sub>IOTM</sub>	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification), V <sub>TEST</sub> = 1.2 x V <sub>IOTM</sub> , t = 1 s (100 % production)	4243	V <sub>PK</sub>
Maximum Impulse Voltage	V <sub>IMP</sub>	IEC 62368-1 1.2/50 μs waveform	4000	V <sub>PK</sub>
Maximum surge isolation voltage	V <sub>IOSM</sub>	Test method per IEC 61000-4-5, 1.2/50 μs waveform, V <sub>IOSM</sub> ≥ 1.3 x V <sub>IMP</sub> (qualification)	5200	V <sub>PK</sub>
Apparent charge measuring voltage	V <sub>pd(m)</sub>	Method A, After Input/Output safety test subgroup 2&3, V <sub>ini,a</sub> = V <sub>IOTM</sub> , V <sub>pd(m)</sub> = 1.2 x V <sub>IORM</sub> t <sub>ini</sub> = 60 s, t <sub>m</sub> = 10 s, partial discharge < 5 pC	680	V <sub>PK</sub>
		Method A, After environmental tests subgroup 1, V <sub>ini,a</sub> = V <sub>IOTM</sub> , V <sub>pd(m)</sub> = 1.6 x V <sub>IORM</sub> t <sub>ini</sub> = 60 s, t <sub>m</sub> = 10 s, partial discharge < 5 pC	906	
		Method B1; At routine test (100 % production) and preconditioning (type test) V <sub>ini,b</sub> ≥ 1.2 x V <sub>IOTM</sub> , V <sub>pd(m)</sub> = 1.875 x V <sub>IORM</sub> t <sub>ini,b</sub> = 1 s, t <sub>m</sub> = 1 s partial discharge < 5 pC	1062	
Barrier capacitance, input to output	C <sub>IO</sub>	f = 1 MHz	1.7	pF
Input Capacitance	C <sub>I</sub>	Side 1 input : V <sub>Ix</sub>	1.8	pF
		Side 2 input : V <sub>Ix</sub>	4.2	pF
Isolation Resistance	R <sub>IO</sub>	V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25 °C	>10 <sup>12</sup>	Ω
		V <sub>IO</sub> = 500 V, 100 °C ≤ T <sub>A</sub> ≤ 125 °C	>10 <sup>11</sup>	
		V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150 °C	>10 <sup>9</sup>	
Pollution Degree	-	-	2	-
Climatic Category	-	-	40/125/21	-
<b>UL 1577</b>				
Maximum Withstanding Isolation Voltage	V <sub>ISO</sub>	V <sub>TEST</sub> = V <sub>ISO</sub> , t = 60 s (qualification), V <sub>TEST</sub> = 1.2 x V <sub>ISO</sub> , t = 1 s (100 % production)	3000	V <sub>rms</sub>

## 11. Safety Limiting Values

PARAMETER	Symbol	TEST CONDITIONS	Value	Unit
Safety Input, Output or Supply Current	I <sub>S</sub>	V <sub>DD1</sub> = V <sub>DD2</sub> = 5.5 V, T <sub>J</sub> = 150 °C, T <sub>a</sub> = 25 °C	287	mA
		V <sub>DD1</sub> = V <sub>DD2</sub> = 3.6 V, T <sub>J</sub> = 150 °C, T <sub>a</sub> = 25 °C	439	mA
		V <sub>DD1</sub> = V <sub>DD2</sub> = 2.75 V, T <sub>J</sub> = 150 °C, T <sub>a</sub> = 25 °C	575	mA
Safety Input, Output or Total Power	P <sub>S</sub>	T <sub>J</sub> = 150 °C, T <sub>a</sub> = 25 °C	1580	W
Maximum Safety Temperature	T <sub>S</sub>	-	150	°C

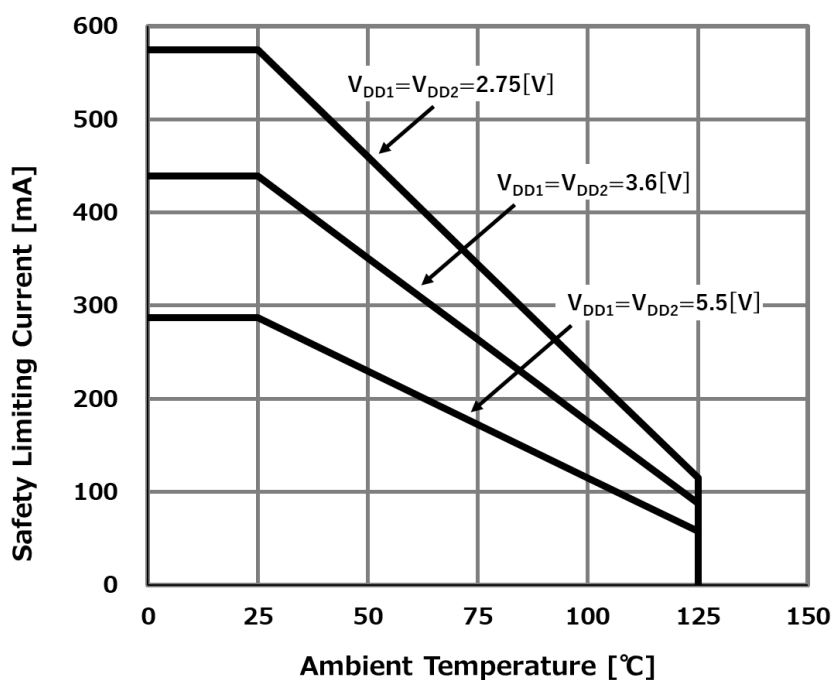
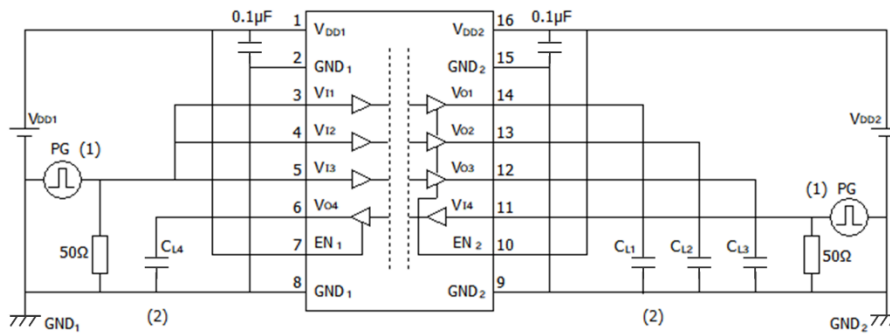


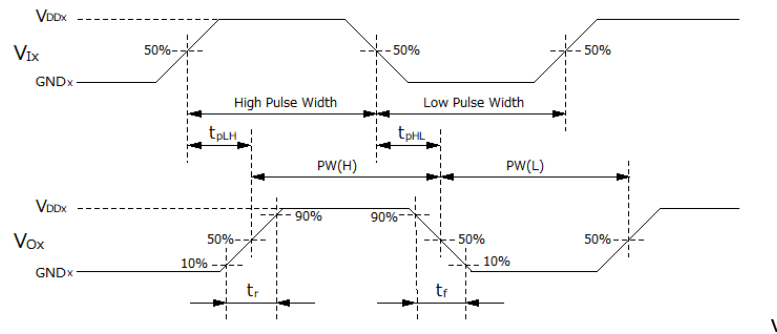
Fig. 11.1 Thermal Derating Curve for Safety Limiting Current-Ta

## 12. Test Circuit

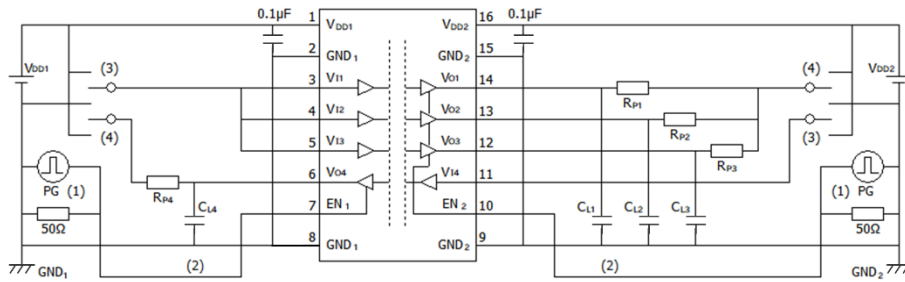


**Fig. 12-1: DCL341L0B/DCL341H0B Switching Test Circuit**

- 1: The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 50 \text{ kHz}$ , 50 % duty cycle,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ ,  $Z_o = 50 \Omega$ . At the input,  $50 \Omega$  resistor is required to terminate input generator signal. It is needed not in actual application.
- 2:  $C_{Lx} = 15 \text{ pF}$  includes instrumentation and fixture capacitance.

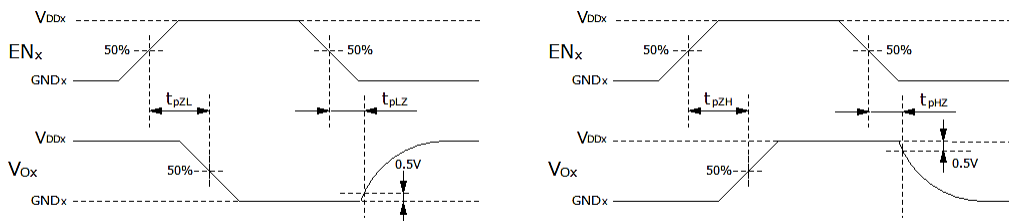


**Fig. 12-2: DCL341x0B Switching Waveforms**

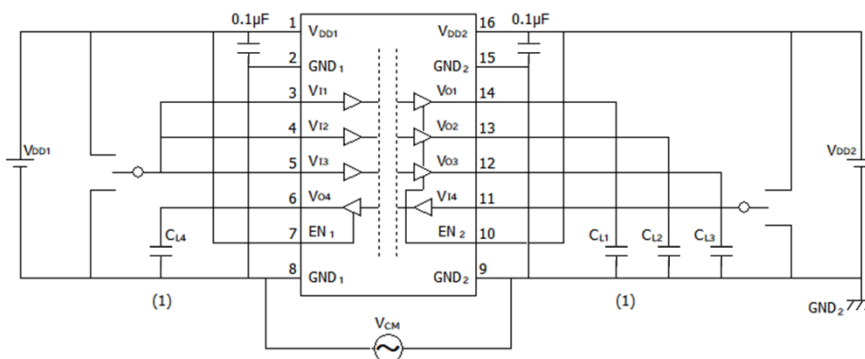


**Fig. 12-3: DCL341L0B/DCL341H0B Enable Propagation Delay Time Test Circuit**

- 1: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50 % duty cycle,  $t_r \leq 2$  ns,  $t_f \leq 2$  ns,  $Z_O = 50 \Omega$ . At the input, 50 Ω resistor is required to terminate input generator signal. It is needed not in actual application.
- 2:  $C_{LX} = 15$  pF includes instrumentation and fixture capacitance.
- 3: GND for  $t_{pZL}$ ,  $t_{PLZ}$ ,  $V_{DD}$  for  $t_{pZH}$ ,  $t_{PHZ}$
- 4:  $V_{DD}$  for  $t_{pZL}$ ,  $t_{PLZ}$ , GND for  $t_{pZH}$ ,  $t_{PHZ}$ .



**Fig. 12-4: DCL341L0B/DCL341H0B Enable Propagation Delay Time Waveforms**



**Fig. 12-5: DCL341L0B/DCL341H0B Common-Mode Transient Immunity Test Circuit**

- 1:  $C_{LX} = 15$  pF includes instrumentation and fixture capacitance.
- 2: Apply  $V_{CM}$  with reference to the GND terminal on the output terminal side of the IC. The GND on the IC input terminal side is isolated from the output terminal side. Depending on which channel is being measured,  $V_{CM}$  may be applied with reference to GND<sub>1</sub> or with reference to GND<sub>2</sub>.

## 13. Characteristics Curves (Note)

Note: The following characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

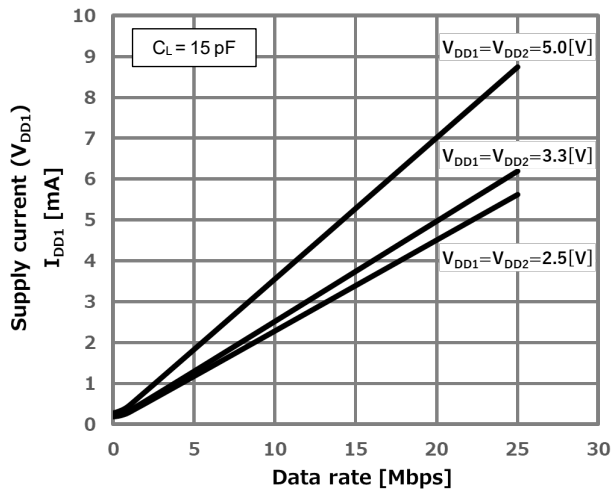


Fig.13.1. DCL341x0B  $I_{DD1}$  Supply Current - Data rate

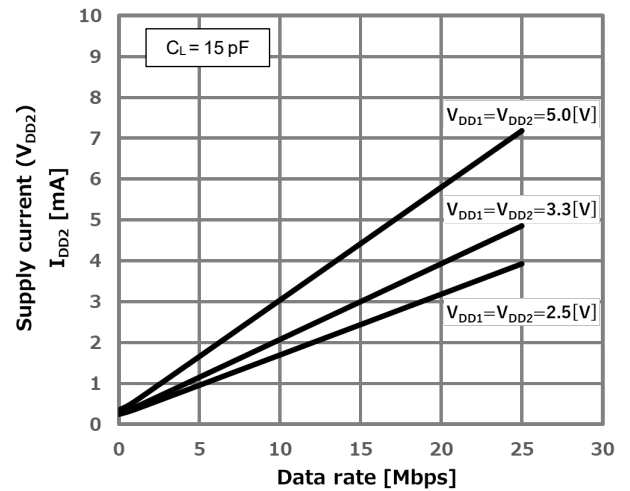


Fig.13.2. DCL341x0B  $I_{DD2}$  Supply Current - Data rate

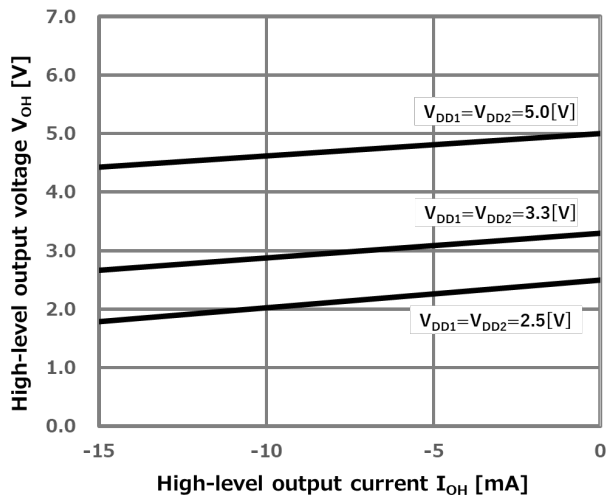


Fig.13.3.  $V_{OH} - I_{OH}$

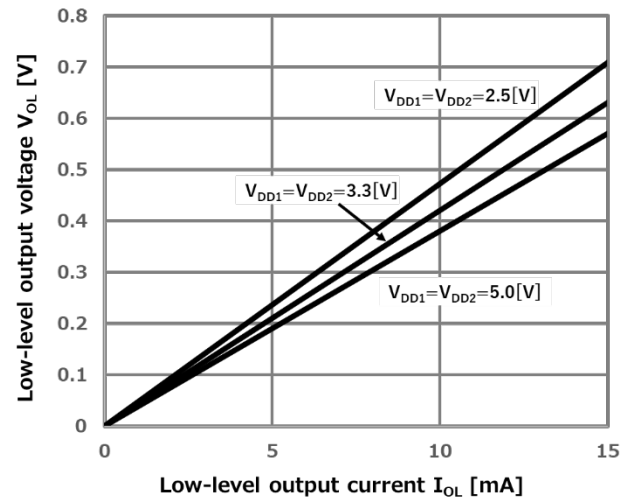


Fig.13.4.  $V_{OL} - I_{OL}$

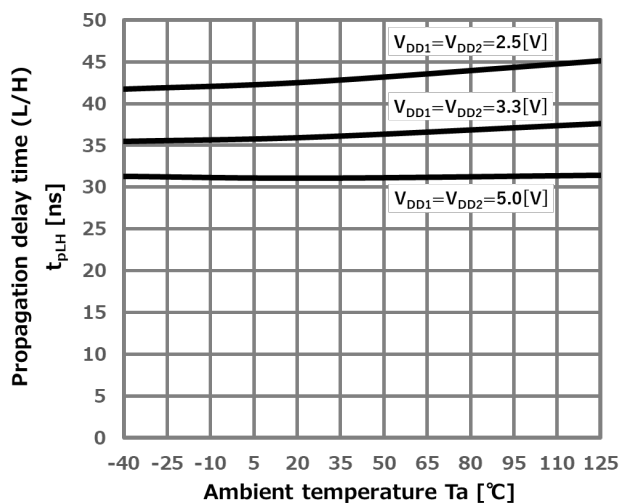


Fig.13.5. Propagation Delay Time  $t_{pHL} - T_a$

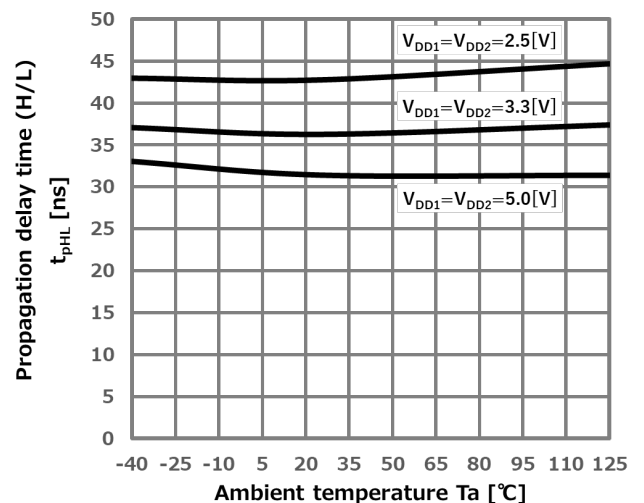


Fig.13.6. Propagation Delay Time  $t_{pLH} - T_a$

## 14. Package Information

Package Name	SSOP16 (P-SSOP16-0405-0.64-001)
Implementation category	Surface Mount
Pin Number	16
Package Dimension Width × Length × Height (mm)	3.9 (Typ.) × 4.9 (Typ.) × 1.75 (Max)
Package Dimension(mm) / Land Pattern Example (mm)	<p>Package Dimension</p> <p>Land Pattern Dimensions (for reference only)</p> <p>Notes : Land Pattern Dimensions</p> <ul style="list-style-type: none"> <li>• All linear dimensions are given in millimeters unless otherwise specified.</li> <li>• This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only. TOSHIBA is not responsible for any incorrect or incomplete drawings and information.</li> <li>• You are solely responsible for all aspects of your own land pattern, including but not limited to soldering processes.</li> <li>• The drawing shown may not accurately represent the actual shape or dimensions.</li> <li>• Before creating and producing designs and using, customers must also refer to and comply with the latest versions of all relevant TOSHIBA information and the instructions for the application that Product will be used with or for.</li> </ul>

## 15. Ordering guide

Model	V <sub>DD1</sub> end Number of inputs	V <sub>DD2</sub> end Number of inputs	Default Output	Data rate [Mbps]	Control signal	Temperature range [°C]	Package
DCL341L0B	3	1	L	25	Output Enable	-40~125	SSOP16
DCL341H0B	3	1	H	25	Output Enable	-40~125	SSOP16

## RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as "TOSHIBA". Hardware, software and systems described in this document are collectively referred to as "Product".

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**

Toshiba Electronic Devices & Storage Corporation

<https://toshiba.semicon-storage.com/>