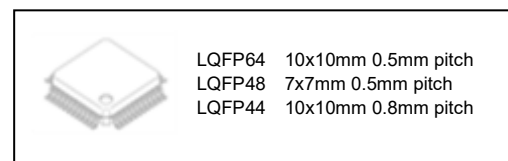


## CMOS Digital Integrated Circuit Silicon Monolithic

# TMPM4H Group(1)

## General Description

- Arm® Cortex®-M4 processor with FPU, Operation frequency: 1 to 120MHz.  
Operation voltage: 2.7 to 5.5 V
- Flash memory: 256 KB.
- Package: 44 to 64 pins, 3 types of packages are available.



## Applications

Widely used for consumer products and industrial products including home appliances, OA equipment, household equipment and AV devices.

## Features

- Arm Cortex-M4 processor with FPU
  - Operating frequency: 1 to 120MHz
  - Support Memory Protection Unit (MPU)
- Operating voltage and low-power consumption mode
  - Operating voltage: 2.7 to 5.5V
  - Low-power consumption mode: IDLE mode and STOP1 mode
- Operating temperature: -40 to 105°C
- Internal memory
  - Code flash: 256 KB, rewrite frequencies: up to 100,000 times
  - RAM: 18KB, support parity
- Clock
  - External high-speed oscillator (EHOSC): 6 to 24MHz (ceramic and crystal oscillator)
  - External high-speed clock input (EHCLKIN): 6 to 24MHz
  - Internal high-speed oscillator (IHOSC1): 10 MHz, support user trimming
  - PLL: 120MHz
- Oscillation frequency detector (OFD): Abnormal system clock detection
- Voltage detection circuit (LVD): 8 levels, Interrupt or reset signal selectale
- Interrupt
  - External factors: 9 to 11 (support noise filter (analog/digital))
  - Internal: 63 to 66 factors
- I/O port: 33 to 51 ports
  - Support pull-up and up-down register, open-drain output, and 5V tolerant input
- Onchip debug (JTAG/SW), non-break debug interface (RAM monitor)
- Trigger selection circuit (TRGSEL)
  - Expand trigger request of DMA controller, timer counter and etc.
- DMA controller (DMAC)
  - Trigger requests: 27 to 32 factors by internal and external triggers
- CRC calculation circuit (CRC): 1 channel
  - CRC32 and CRC16
- Asynchronous serial communication circuit (UART): 3 to 4 channels
  - Up to 5Mbps, support FIFO (transmission: 8 stages, reception: 8 stages)
- Serial peripheral interface (TSPI): 2 to 4 channel/s
  - Only SIO mode, up to 20Mbps, support FIFO (transmission: 16 bits × 8 stages, reception: 16 bits × 8 stages)
- I<sup>2</sup>C Interface
  - I<sup>2</sup>C Interface (I2C): 1 channel, support multi controller
  - I<sup>2</sup>C Interface version A (EI2C): 1 channel, support multi controller and 10-bit addressing
- 12-bit analog to digital converter (ADC): 1 unit, 9 to 12 analog inputs
  - Conversion time: 0.73μs at f<sub>SCLK</sub> = 30MHz
  - Self-diagnosis support function
- Advanced programmable motor control circuit (A-PMD): 1 channel
  - Synchronized operation with 3-phase complementary PWM output and 12-bit ADC
  - PFC: support 3-phase interleaved PFC control
  - Emergency stop function by external inputs (EMG pin, OVV pin)

Start of commercial production  
 2026-08

- 32-bit timer event counter (T32A)
  - 6 channels as 32-bit timer, 12 channels as 16-bit timer
  - Interval timer, event counter, input capture, 2-phase plus count, PPG output, synchronous start, and trigger start and stop
- Clock selective watchdog timer (SIWDT): 1 channel
  - Clock other than the system clock can be selected as source clock.
  - Clear window, interrupt or reset output selectable

## Products Lists Categorized by Functions

The product under development is contained in this table.

For the newest status of each product, please contact your sales representative.

**Table 1.1 Products Lists**

| Built-in Functions            |                                  | TMPM4H4FYUG                                | TMPM4H2FYDUG                             | TMPM4H1FYUG                                |
|-------------------------------|----------------------------------|--|--|--|
| Memory                        | Code Flash (KB)                  | 256  | 256                                      | 256  |
|                               | RAM (KB)                         | 18   | 18                                       | 18   |
| I/O port                      | PORT (pin)                       | 51   | 37                                       | 33   |
| External interrupt            | Factors                          | 11   | 10                                       | 9  |
|                               | Pins                             | 16   | 12                                       | 11   |
| DMA                           | DMAC (ch)                        | 32   | 27                                       | 27   |
| Timer function                | T32A (ch)                        | 6  | 6  | 6  |
| Serial communication function | UART (ch)                        | 4  | 3  | 3  |
|                               | I2C/EI2C (ch)                    | 1 / 1                                      | 1 / 1                                    | 1 / 1                                      |
|                               | TSPI (ch)                        | 4  | 2  | 2  |
| Analog function               | 12-bit ADC (No. of analog input) | 12   | 10                                       | 9  |
| Motor control function        | A-PMD (ch)                       | 1  | 1  | 1  |
| Other function                | CRC                              | 1  | 1  | 1  |
|                               | RAMP (ch)                        | 1  | 1  | 1  |
| System function               | LVD                              | 1  | 1  | 1  |
|                               | SIWDT (ch)                       | 1  | 1  | 1  |
|                               | OFD                              | 1  | 1  | 1  |
|                               | POR                              | 1  | 1  | 1  |
| Debug interface               | DEBUG                            | JTAG/SW<br>TRACE(4bits)<br>NBDIF           | JTAG/SW                                  | JTAG/SW                                    |
| Package                       | Package type                     | LQFP64<br>(10 mm x 10 mm,<br>0.5 mm pitch) | LQFP48<br>(7 mm x 7 mm,<br>0.5 mm pitch) | LQFP44<br>(10 mm x 10 mm,<br>0.8 mm pitch) |
|                               | Package name                     | P-LQFP64-1010-0.50-003                     | P-LQFP48-0707-0.50-002                   | P-LQFP44-1010-0.80-003                     |

## Contents

|   |    |
|---|----|
| General Description.....  | 1  |
| Applications .....  | 1  |
| Features .....  | 1  |
| Products Lists Categorized by Functions .....                         | 3  |
| Contents .....  | 4  |
| List of Figures.....  | 7  |
| List of Tables .....  | 8  |
| Preface .....   | 9  |
| Conventions.....  | 9  |
| Terms and Abbreviations.....  | 11 |
| 1. Block Diagram.....   | 12 |
| 2. Pin Assignment.....  | 13 |
| 2.1. LQFP64 .....   | 13 |
| 2.2. LQFP48 .....   | 14 |
| 2.3. LQFP44 .....   | 15 |
| 3. Memory Map .....   | 16 |
| 4. Pin Description.....   | 17 |
| 4.1. Functional Pin Names and Functions .....                         | 17 |
| 4.1.1. Function Pins of Peripheral .....                              | 17 |
| 4.1.2. Debug Pins .....   | 18 |
| 4.1.3. Control Pins .....   | 19 |
| 4.1.4. Power Supply Pins .....  | 19 |
| 4.1.5. Capacitors between Power Supply Pins.....                      | 20 |
| 4.2. Functional Pins and Ports Assignment (in pin number order) ..... | 21 |
| 4.3. Ports .....  | 27 |
| 4.3.1. Port Specification Table.....                                  | 28 |
| 5. Functional Description and Operation Description .....             | 30 |
| 5.1. Reference Manuals .....  | 30 |
| 5.2. Processor Core.....  | 31 |
| 5.2.1. Core Information.....  | 31 |
| 5.2.2. Configurable Options.....                                      | 31 |
| 5.3. Clock Control and Operating Mode (CG).....                       | 32 |
| 5.4. Flash Memory (256KB) .....                                       | 32 |
| 5.5. Oscillator.....  | 33 |
| 5.6. Trimming Circuit (TRM) .....                                     | 33 |
| 5.7. Oscillation Frequency Detector (OFD).....                        | 33 |
| 5.8. Voltage Detection Circuit (LVD) .....                            | 34 |
| 5.9. Digital Noise Filter Circuit (DNF) .....                         | 34 |

|   |    |
|---|----|
| 5.10. Debug Interface (DEBUG).....                              | 35 |
| 5.10.1. Non-break Debug Interface (NBDIF) .....                 | 35 |
| 5.11. DMA Controller (DMAC).....                                | 36 |
| 5.12. Asynchronous Serial Communication Circuit (UART) .....    | 36 |
| 5.13. Serial Peripheral Interface (TSPI) .....                  | 37 |
| 5.14. I <sup>2</sup> C Interface.....                           | 37 |
| 5.14.1. I <sup>2</sup> C Interface (I2C).....                   | 38 |
| 5.14.2. I <sup>2</sup> C Interface Version A (EI2C).....        | 38 |
| 5.15. 12-bit Analog to Digital Converter (ADC) .....            | 39 |
| 5.16. Advanced Programmable Motor Control Circuit (A-PMD) ..... | 39 |
| 5.17. 32-bit Timer Event Counter (T32A).....                    | 40 |
| 5.18. Clock Selective Watchdog Timer (SIWDT).....               | 41 |
| 5.19. CRC Calculation Circuit (CRC) .....                       | 41 |
| 5.20. RAM Parity (RAMP).....                                    | 41 |
| 5.21. Measures for Security Risk .....                          | 42 |
| 5.21.1. Outline .....   | 42 |
| 5.21.2. Disclaimer.....   | 42 |
| 6. Equivalent Circuit.....                                      | 43 |
| 6.1. Port .....   | 43 |
| 6.2. Power Supply Pin for Analog.....                           | 46 |
| 6.3. Control Pins .....   | 47 |
| 6.4. Clock Control Pins .....                                   | 47 |
| 7. Electrical Characteristics.....                              | 48 |
| 7.1. Absolute Maximum Ratings.....                              | 48 |
| 7.2. DC Electrical Characteristics (1/2) .....                  | 49 |
| 7.3. DC Electrical Characteristics (2/2) .....                  | 53 |
| 7.3.1. Current Consumption .....                                | 53 |
| 7.3.2. Analog Current Consumption .....                         | 54 |
| 7.4. Power Supply Voltage Fluctuation .....                     | 55 |
| 7.5. Characteristics of Internal Processing at RESET .....      | 55 |
| 7.6. Characteristics of Power-on Reset.....                     | 56 |
| 7.7. Characteristics of PORF.....                               | 56 |
| 7.8. Characteristics of Voltage Detection Circuit.....          | 57 |
| 7.9. 12-bit AD Converter Characteristics.....                   | 58 |
| 7.9.1. AD Converter Characteristics .....                       | 58 |
| 7.9.2. Reference Power Supply .....                             | 58 |
| 7.10. AC Electrical Characteristics .....                       | 59 |
| 7.10.1. Serial Peripheral Interface (TSPI).....                 | 59 |
| 7.10.2. I <sup>2</sup> C Interface (I2C).....                   | 64 |
| 7.10.3. I <sup>2</sup> C Interface Version A (EI2C).....        | 66 |
| 7.10.4. 32-bit Timer Event Counter (T32A).....                  | 68 |
| 7.10.5. External Interrupt.....                                 | 69 |

|  |    |
|--|----|
| 7.10.6. Trigger Selection Circuit (TRGSEL).....              | 70 |
| 7.10.7. Debug Communication .....                            | 71 |
| 7.10.8. NBD Interface .....                                  | 74 |
| 7.10.9. SCOUT Pin.....                                       | 75 |
| 7.10.10. External Clock Input .....                          | 76 |
| 7.11. Noise Filter (Analog) Characteristics.....             | 76 |
| 7.12. Flash Memory Characteristics.....                      | 77 |
| 7.12.1. Code Flash .....                                     | 77 |
| 7.12.2. Chip Erase.....                                      | 77 |
| 7.13. Regulator Characteristics .....                        | 77 |
| 7.14. Oscillation Circuit Characteristics.....               | 78 |
| 7.14.1. Internal Oscillator.....                             | 78 |
| 7.14.2. External Oscillator .....                            | 78 |
| 7.14.3. Oscillation Circuit.....                             | 79 |
| 7.14.4. Ceramic Oscillator .....                             | 79 |
| 7.14.5. Crystal Oscillator .....                             | 79 |
| 7.14.6. Precautions for Designing Printed Circuit Board..... | 79 |
| 8. Package Dimensions .....                                  | 80 |
| 8.1. P-LQFP64-1010-0.50-003.....                             | 80 |
| 8.2. P-LQFP48-0707-0.50-002.....                             | 81 |
| 8.3. P-LQFP44-1010-0.80-003.....                             | 82 |
| 9. Precautions .....   | 83 |
| 10. Revision History .....                                   | 84 |
| Appendix.....  | 85 |
| List of All Pins .....                                       | 85 |
| Part Naming Conventions.....                                 | 87 |
| RESTRICTIONS ON PRODUCT USE.....                             | 88 |

## List of Figures

|             |  |    |
|-------------|--|----|
| Figure 1.1  | Block Diagram of TMPM4H Group(1).....                            | 12 |
| Figure 3.1  | Example of TMPM4HxFY .....                                       | 16 |
| Figure 4.1  | Connection Diagram of Capacitors between Power Supply Pins ..... | 20 |
| Figure 5.1  | Measures for Security Risk.....                                  | 42 |
| Figure 7.1  | Power Supply Fluctuation Rate .....                              | 55 |
| Figure 7.2  | 1st Clock Edge Sampling (Controller) .....                       | 62 |
| Figure 7.3  | 2nd Clock Edge Sampling (Controller) .....                       | 62 |
| Figure 7.4  | 1st Clock Edge Sampling (Target).....                            | 63 |
| Figure 7.5  | 2nd Clock Edge Sampling (Target) .....                           | 63 |
| Figure 7.6  | AC Timing of I2C.....  | 65 |
| Figure 7.7  | AC timing of EI2C .....  | 67 |
| Figure 7.8  | Count Pulse Input .....  | 69 |
| Figure 7.9  | JTAG/SWD Signal Waveform.....                                    | 72 |
| Figure 7.10 | Trace Signal Waveform .....                                      | 73 |
| Figure 7.11 | AC Timing of NBDIF .....   | 74 |
| Figure 7.12 | SCOUT Waveform Output.....                                       | 75 |
| Figure 7.13 | External Clock Input Waveform .....                              | 76 |
| Figure 7.14 | Example of Oscillation Circuit.....                              | 79 |

## List of Tables

|            |  |    |
|------------|--|----|
| Table 1.1  | Products Lists.....  | 3  |
| Table 4.1  | Functional Pin Names and Functions .....                             | 17 |
| Table 4.2  | Debug Pin Names and Functions .....                                  | 18 |
| Table 4.3  | Control Pin Names and Functions .....                                | 19 |
| Table 4.4  | Power Supply Pin Names and Functions .....                           | 19 |
| Table 4.5  | Signal Connection List (1/6).....                                    | 21 |
| Table 4.6  | Signal Connection List (2/6).....                                    | 22 |
| Table 4.7  | Signal Connection List (3/6).....                                    | 23 |
| Table 4.8  | Signal Connection List (4/6).....                                    | 24 |
| Table 4.9  | Signal Connection List (5/6).....                                    | 25 |
| Table 4.10 | Signal Connection List (6/6).....                                    | 26 |
| Table 4.11 | Port Names and Specifications of Port A, B, C, D, E, F, G .....      | 28 |
| Table 4.12 | Port Names and Specifications of Port H, J, K, L .....               | 29 |
| Table 5.1  | Reference Manuals for TMPM4H Group(1).....                           | 30 |
| Table 5.2  | Core Revision.....   | 31 |
| Table 5.3  | Configurable Options and Their Implementations .....                 | 31 |
| Table 5.4  | Built-in Oscillator .....  | 33 |
| Table 5.5  | Built-in TRM.....  | 33 |
| Table 5.6  | Built-in OFD.....  | 33 |
| Table 5.7  | Built-in LVD .....   | 34 |
| Table 5.8  | Number of External Interrupts (Number of Built-in DNF).....          | 34 |
| Table 5.9  | Built-in Debug Interface .....                                       | 35 |
| Table 5.10 | Built-in DMAC.....   | 36 |
| Table 5.11 | Built-in UART .....  | 36 |
| Table 5.12 | Built-in TSPI .....  | 37 |
| Table 5.13 | Built-in I2C/EI2C.....   | 37 |
| Table 5.14 | Number of Analog Inputs .....  | 39 |
| Table 5.15 | Built-in A-PMD.....  | 39 |
| Table 5.16 | Built-in T32A.....   | 40 |
| Table 5.17 | Built-in SIWDT.....  | 41 |
| Table 5.18 | Built-in CRC.....  | 41 |
| Table 5.19 | Built-in RAMP .....  | 41 |
| Table 5.20 | Access Paths and Protection Targets (1).....                         | 42 |
| Table 5.21 | Access Paths and Protection Targets (2).....                         | 42 |
| Table 7.1  | Absolute Maximum Ratings .....                                       | 48 |
| Table 7.2  | IDD Measurement Condition (Pin Setting and Oscillation Circuit)..... | 53 |
| Table 7.3  | IDD Measurement Condition (CPU and Peripheral Function).....         | 54 |
| Table 10.1 | Revision History .....   | 84 |

## Preface

### Conventions

- Numeric formats follow the rules as shown below:
 

|              |              |   |
|--------------|--------------|---|
| Hexadecimal: | 0xABC        |   |
| Decimal:     | 123 or 0d123 | - Only when it needs to be explicitly shown that they are decimal numbers.                              |
| Binary:      | 0b111        | - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence. |
- "\_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].  
 Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by *[ ]* defines the register.  
 Example: *[ABCD]*
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.  
 Example: *[XYZ1]*, *[XYZ2]*, *[XYZ3]* → *[XYZn]*
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...  
 Example: *[ADACR0]*, *[ADBCR0]*, *[ADCCR0]* → *[ADxCR0]*
- In case of channel, "x" means 0, 1, and 2, ...  
 Example: *[T32A0RUNA]*, *[T32A1RUNA]*, *[T32A2RUNA]* → *[T32AxRUNA]*
- The bit range of a register is written like as [m: n].  
 Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.  
 Example: *[ABCD]*<EFG> = 0x01 (hexadecimal), *[XYZn]*<VW> = 1 (binary)
- Word and byte represent the following bit length.
 

|              |         |
|--------------|---------|
| Byte:        | 8 bits  |
| Half word:   | 16 bits |
| Word:        | 32 bits |
| Double word: | 64 bits |
- Properties of each bit in a register are expressed as follows:
 

|      |                              |
|------|------------------------------|
| R:   | Read only                    |
| W:   | Write only                   |
| R/W: | Read and write are possible. |
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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\*\*\*\*\*



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**Terms and Abbreviations**

Some of abbreviations used in this document are as follows:

|        |   |
|--------|---|
| ADC    | Analog to Digital Converter                 |
| A-PMD  | Advanced Programmable Motor Control Circuit |
| CRC    | Cyclic Redundancy Check                     |
| DMAC   | Direct Memory Access Controller             |
| DNF    | Digital Noise Filter                        |
| EHOSC  | External High-speed Oscillator              |
| EI2C   | Inter-integrated Circuit Version A          |
| Fm     | Fast Mode of I <sup>2</sup> C Interface     |
| IHOSC  | Internal High-speed Oscillator              |
| INT    | Interrupt                                   |
| I2C    | Inter-integrated Circuit                    |
| LVD    | Voltage Detection Circuit                   |
| NBDIF  | Non-break Debug Interface                   |
| NMI    | Non-maskable Interrupt                      |
| OFD    | Oscillation Frequency Detector              |
| POR    | Power-on Reset Circuit                      |
| RAMP   | RAM Parity                                  |
| SIWDT  | Clock Selective Watchdog Timer              |
| TRGSEL | Trigger Selection Circuit                   |
| TRM    | Trimming Circuit                            |
| TSPI   | Serial Peripheral Interface                 |
| T32A   | 32-bit Timer Event Counter                  |
| UART   | Asynchronous Serial Communication Circuit   |

## 1. Block Diagram

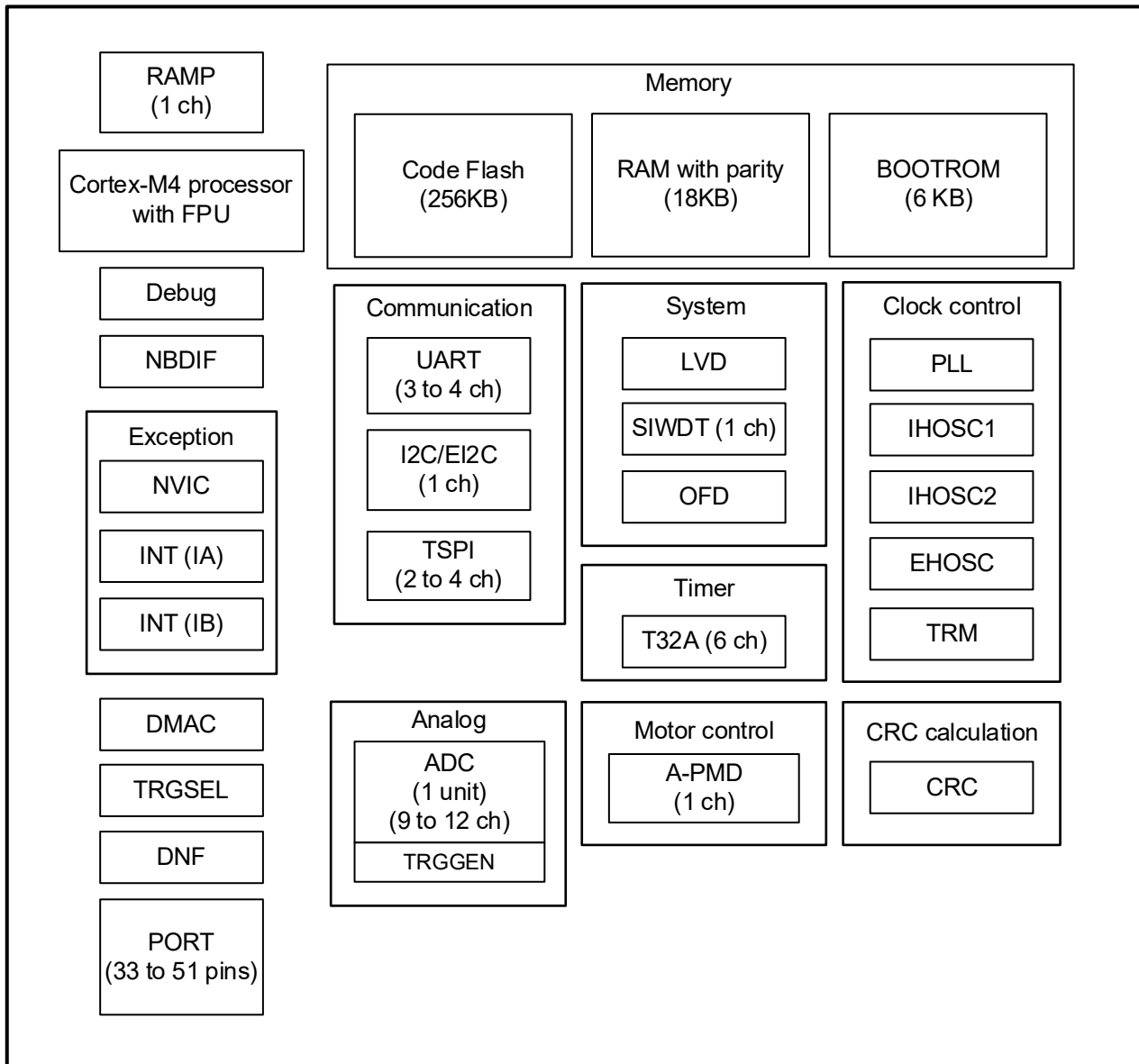
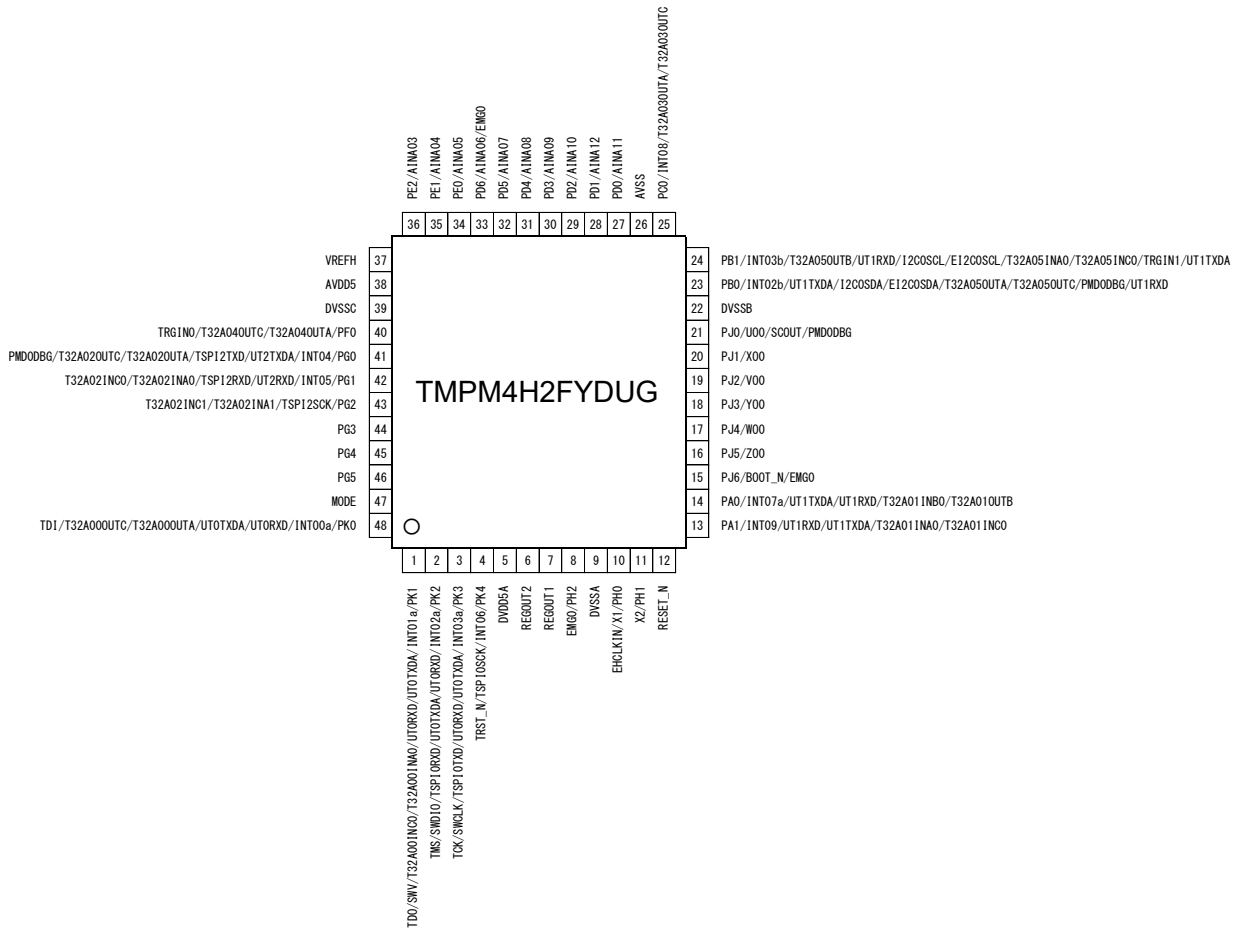


Figure 1.1 Block Diagram of TPM4H Group(1)



## 2.2. LQFP48





## 3. Memory Map

|            |                                 |              |            |                           |                                 |
|------------|---------------------------------|--------------|------------|---------------------------|---------------------------------|
| 0xFFFFFFFF | Vendor-Specific                 | System level | 0xFFFFFFFF | Vendor-Specific           |                                 |
| 0xE0100000 | CPU Register Region             |              | 0xE0100000 | CPU Register Region       |                                 |
| 0xE0000000 | Fault                           | Peripheral   | 0xE0000000 | Fault                     |                                 |
| 0x5E040000 | Code Flash (Mirror 256KB)       |              | 0x5E040000 | Code Flash (Mirror 256KB) |                                 |
| 0x5E000000 | Flash (SFR)                     |              | 0x5E000000 | Flash (SFR)               |                                 |
| 0x5DFF0000 | Fault                           |              | 0x5DFF0000 | Fault                     |                                 |
| 0x44000000 | Bit Band Alias (SFR)            |              | 0x44000000 | Bit Band Alias (SFR)      |                                 |
| 0x42000000 | Fault                           |              | 0x42000000 | Fault                     |                                 |
| 0x40100000 | SFR                             |              | 0x40100000 | SFR                       |                                 |
| 0x4003E000 | Fault                           |              | 0x4003E000 | Fault                     |                                 |
| 0x40000000 | BOOT ROM                        |              | 0x40000000 | BOOT ROM (Mirror 6KB)     |                                 |
| 0x3F7F9800 | Fault                           |              | 0x3F7F9800 | Fault                     |                                 |
| 0x3F7F8000 | Fault                           |              | 0x3F7F8000 | Fault                     |                                 |
| 0x24000000 | Bit Band Alias (RAM/Backup RAM) |              | SRAM       | 0x24000000                | Bit Band Alias (RAM/Backup RAM) |
| 0x22000000 | Fault                           |              |            | 0x22000000                | Fault                           |
| 0x20004800 | RAM2 (10KB)                     |              |            | 0x20004800                | RAM2 (10KB)                     |
| 0x20002000 | RAM1 (4KB)                      | 0x20002000   |            | RAM1 (4KB)                |                                 |
| 0x20010000 | RAM0 (4KB)                      | 0x20010000   |            | RAM0 (4KB)                |                                 |
| 0x20000000 | Fault                           | 0x20000000   |            | Fault                     |                                 |
| 0x00040000 | Code Flash (256KB)              | Code         | 0x00001800 | BOOT ROM (6KB)            |                                 |
| 0x00000000 |                                 |              | 0x00000000 |                           |                                 |

Single chip mode

Single BOOT mode

**Figure 3.1 Example of TMPM4HxFY**

Note1: Fault, Reserved: Please do not access their region.

Note2: For details of Single Chip Mode and Single Boot Mode, refer to the Reference Manual "Flash Memory".

## 4. Pin Description

### 4.1. Functional Pin Names and Functions

#### 4.1.1. Function Pins of Peripheral

Table 4.1 Functional Pin Names and Functions

| Peripheral function                                 | Pin name             | Input or Output                    | Function   |
|---|----------------------|------------------------------------|--|
| Clock control and operation mode (CG)               | SCOUT                | Output                             | Output pin for the system clock  |
| Interrupt control (IA/IB)                           | INTx                 | Input                              | External interrupt input pin<br>External input pin provides the noise filter (analog/digital). |
| 32-bit timer event counter (T32A)                   | T32AxINA0            | Input                              | 16-bit timer A input capture input pin 0   |
|   | T32AxINA1            | Input                              | 16-bit timer A input capture input pin 1   |
|   | T32AxOUTA            | Output                             | 16-bit timer A output pin  |
|   | T32AxINB0            | Input                              | 16-bit timer B input capture input pin 0   |
|   | T32AxINB1            | Input                              | 16-bit timer B input capture input pin 1   |
|   | T32AxOUTB            | Output                             | 16-bit timer B output pin  |
|   | T32AxINC0            | Input                              | 32-bit timer input capture input pin 0   |
|   | T32AxINC1            | Input                              | 32-bit timer input capture input pin 1   |
|   | T32AxOUTC            | Output                             | 32-bit timer output pin  |
| Serial peripheral interface (TSPI)                  | TSPIxRXD             | Input                              | Data input pin   |
|   | TSPIxTXD             | Output                             | Data output pin  |
|   | TSPIxSCK             | I/O                                | Clock input/output pin   |
| Asynchronous serial communication circuit (UART)    | UTxRXD               | Input                              | Data input pin   |
|   | UTxTXDA              | Output                             | Data output pin A  |
| I <sup>2</sup> C interface (I2C/EI2C)               | I2CxSDA/<br>EI2CxSDA | I/O                                | Data input/output pin  |
|   | I2CxSCL/<br>EI2CxSCL | I/O                                | Clock input/output pin   |
| Advanced programmable motor control circuit (A-PMD) | EMGx                 | Input                              | Emergency state detection input pin  |
|   | OVVx                 | Input                              | Overvoltage detection input pin  |
|   | UOx                  | Output                             | U-phase output pin   |
|   | VOx                  | Output                             | V-phase output pin   |
|   | WOx                  | Output                             | W-phase output pin   |
|   | XOx                  | Output                             | X-phase output pin   |
|   | YOx                  | Output                             | Y-phase output pin   |
|   | ZOx                  | Output                             | Z-phase output pin   |
| PMDxDBG   | Output               | Debug output pin for motor control |  |
| 12-bit analog to digital converter (ADC)            | AINAx                | Input                              | Analog input pin   |
| Trigger selection circuit (TRGSEL)                  | TRGINx               | Input                              | External trigger input pin   |

Note: "x" means channel number, unit number or interrupt number.

## 4.1.2. Debug Pins

**Table 4.2 Debug Pin Names and Functions**

| Debug PORT | Pin name   | Input or Output | Function                                |
|------------|------------|-----------------|---|
| JTAG       | TMS        | Input           | JTAG test mode selection input pin      |
|            | TCK        | Input           | JTAG serial clock input pin             |
|            | TDO        | Output          | JTAG serial data output pin             |
|            | TDI        | Input           | JTAG serial data input pin              |
|            | TRST_N     | Input           | JTAG test reset input pin               |
| SW         | SWDIO      | I/O             | Serial wire data input/output pin       |
|            | SWCLK      | Input           | Serial wire clock input pin             |
|            | SWV        | Output          | Serial wire viewer output pin           |
| TRACE      | TRACECLK   | Output          | Trace clock output pin                  |
|            | TRACEDATA0 | Output          | Trace data output pin 0                 |
|            | TRACEDATA1 | Output          | Trace data output pin 1                 |
|            | TRACEDATA2 | Output          | Trace data output pin 2                 |
|            | TRACEDATA3 | Output          | Trace data output pin 3                 |
| NBDIF      | NBDSYNC    | Input           | Non-break debug synchronous input pin   |
|            | NBDCLK     | Input           | Non-break debug clock input pin         |
|            | NBDDATA0   | I/O             | Non-break debug data input/output pin 0 |
|            | NBDDATA1   | I/O             | Non-break debug data input/output pin 1 |
|            | NBDDATA2   | I/O             | Non-break debug data input/output pin 2 |
|            | NBDDATA3   | I/O             | Non-break debug data input/output pin 3 |

## 4.1.3. Control Pins

**Table 4.3 Control Pin Names and Functions**

|             | Pin name | Input or Output | Function   |
|-------------|----------|-----------------|--|
| Control Pin | X1       | Input           | High-speed oscillator connection pin   |
|             | X2       | Output          | High-speed oscillator connection pin   |
|             | EHCLKIN  | Input           | External clock input pin   |
|             | BOOT_N   | Input           | BOOT mode control pin<br>The BOOT mode control pin is sampled on the rising edge of the RESET_N pin input. It is not sampled by internal reset factor. If the BOOT mode control pin is "Low" level, the MCU enters single boot mode. If it is "High" level, the MCU enters single chip mode.<br>For details of single boot mode, refer to the Reference Manual "Flash Memory". |
|             | RESET_N  | Input           | Reset signal input pin   |
|             | MODE     | Input           | Mode Pin<br>This pin must be fixed to "Low" level.   |

## 4.1.4. Power Supply Pins

**Table 4.4 Power Supply Pin Names and Functions**

|              | Pin name   | Function   |
|--------------|--|--|
| Power Supply | DVDD5A (Note1)<br>DVDD5B (Note1)<br>DVDD5C (Note1) | Power supply pins for digital<br>DVDD5A/B/C supplies the power to the following pins:<br>PA to PC, PF to PL, MODE, RESET_N   |
|              | DVSSA (Note2)<br>DVSSB (Note2)<br>DVSSC (Note2)    | GND pins for digital   |
|              | REGOUT1 (Note3)                                    | Capacitor for a regulator connection pin (Note4)   |
|              | REGOUT2 (Note3)                                    | Capacitor for a regulator connection pin (Note4)   |
|              | AVDD5/VREFH  | Power supply pin for analog (AVDD5) and reference power pin for analog (VREFH) for analog are assigned to same pin.<br>AVDD5 supplies the power to the following pins:<br>PD, PE |
|              | AVSS   | GND pin for analog, this pin is shared with an analog reference GND pin (VREFL).   |

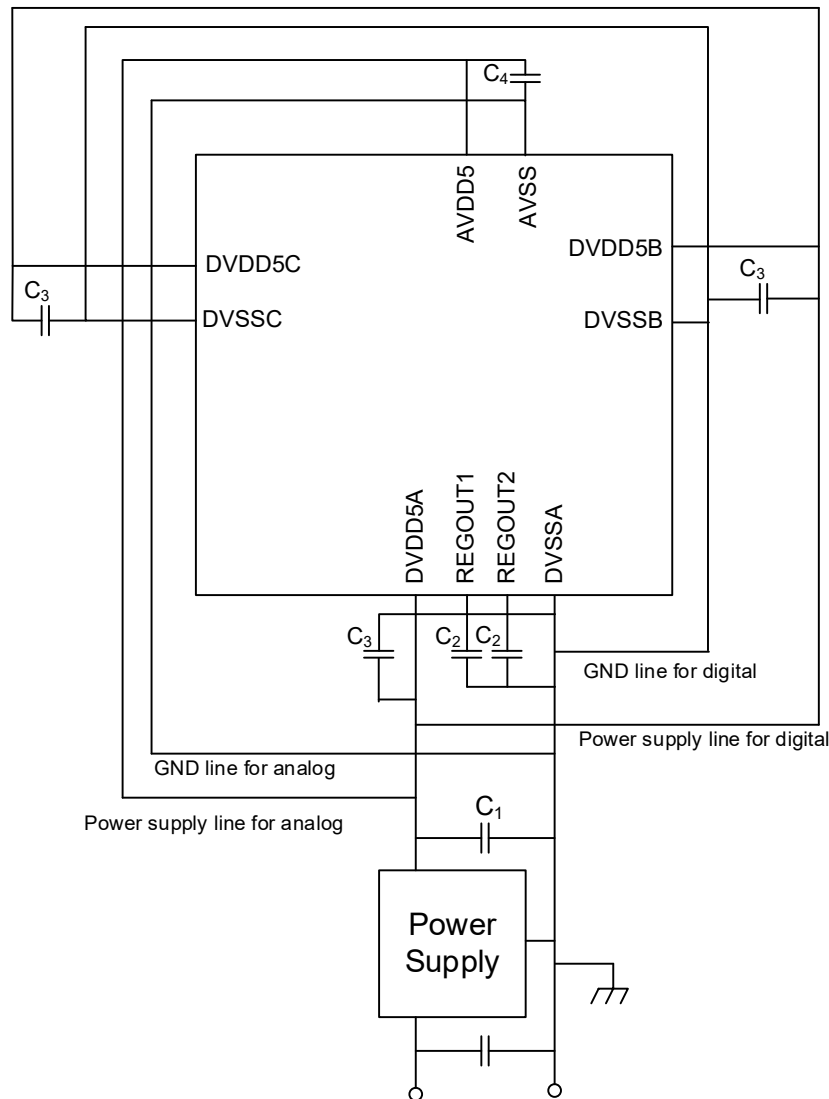
Note1: Apply same voltage to DVDD5A, DVDD5B, and DVDD5C except the case that the pins are not provided.

Note2: Apply same voltage to DVSSA, DVSSB, and DVSSC except the case that the pins are not provided.

Note3: For REGOUT1 and REGOUT2, do not cause a short circuit with DVDD5A, DVDD5B, or DVDD5C; or DVSSA, DVSSB, or DVSSC.

Note4: For the capacitor value, refer to the "7.13. Regulator".

## 4.1.5. Capacitors between Power Supply Pins



**Figure 4.1 Connection Diagram of Capacitors between Power Supply Pins**

- Note1: Insert a ceramic capacitor ( $C_1$ ) near the output pin of the power supply. The power gradient with  $C_1$  must be satisfied  $V_{PON}$  and  $V_{POFF}$  in "7.5. Characteristics of Internal Processing at RESET".
- Note2: Insert the bypass capacitor ( $C_3, C_4:0.01 \mu\text{F}$  to  $0.1 \mu\text{F}$ ) between the power supply and GND near each MCU power supply pin.
- Note3: Insert the power supply stabilizing ceramic capacitor ( $C_2$ ) of the same capacity into the capacitor connection pin for the internal regulator (REGOUT1, REGOUT2). The capacitor should be placed near DVSSA pin. Regarding value of capacitor, refer to "7.13. Regulator".
- Note4: In order to suppress noise mixing from the power supply for digital to the analog circuit, separate the power supply line for analog and the power supply line for digital near the power supply output pin.
- Note5: In order to suppress noise mixing from the peripheral circuit to the analog circuit, when inserting a filter circuit or pull-up/down resistor to the input/output pin of the analog power supply system, connect the components that make up these circuits to the power supply line for analog.
- Note6: In order to suppress high-frequency noise received from the loop circuit by the power supply line, the GND line, and the capacitor, do not separate the power supply line and the GND line from each other.

## 4.2. Functional Pins and Ports Assignment (in pin number order)

Following table shows the pin number for each product and the port assignment which were seen from the functional pin.

"-" means that it does not have a pin or there is no assignment of a function.

**Table 4.5 Signal Connection List (1/6)**

| Function      | Combination functional pin name | Port name | M4H4 (LQFP64) | M4H2 (LQFP48) | M4H1 (LQFP44) |
|---------------|---------------------------------|-----------|---------------|---------------|---------------|
| UART ch 0     | UT0RXD                          | PK0       | 63            | 48            | 43            |
|               |                                 | PK1       | 64            | 1             | 44            |
|               |                                 | PK2       | 1             | 2             | 1             |
|               |                                 | PK3       | 2             | 3             | 2             |
|               | UT0TXDA                         | PK1       | 64            | 1             | 44            |
|               |                                 | PK0       | 63            | 48            | 43            |
|               |                                 | PK3       | 2             | 3             | 2             |
| UART ch 1     | UT1RXD                          | PA1       | 18            | 13            | -             |
|               |                                 | PA0       | 19            | 14            |               |
|               |                                 | PB0       | 31            | 23            |               |
|               |                                 | PB1       | 32            | 24            |               |
|               | UT1TXDA                         | PA0       | 19            | 14            | -             |
|               |                                 | PA1       | 18            | 13            |               |
|               |                                 | PB1       | 32            | 24            |               |
|               |                                 | PB0       | 31            | 23            |               |
| UART ch 2     | UT2RXD                          | PG1       | 57            | 42            | 40            |
|               | UT2TXDA                         | PG0       | 56            | 41            | 39            |
| UART ch 3     | UT3RXD                          | PC1       | 34            | -             | -             |
|               |                                 | PC0       | 35            |               |               |
|               | UT3TXDA                         | PC0       | 35            |               |               |
|               |                                 | PC1       | 34            |               |               |
| I2C/EI2C ch 0 | I2C0SDA/<br>EI2C0SDA            | PB0       | 31            | 23            | 22            |
|               | I2C0SCL/<br>EI2C0SCL            | PB1       | 32            | 24            | 23            |
| TSPI ch 0     | TSPI0RXD                        | PK2       | 1             | 2             | 1             |
|               | TSPI0TXD                        | PK3       | 2             | 3             | 2             |
|               | TSPI0SCK                        | PK4       | 3             | 4             | 3             |
| TSPI ch 1     | TSPI1RXD                        | PA1       | 18            | -             | -             |
|               | TSPI1TXD                        | PA0       | 19            |               |               |
|               | TSPI1SCK                        | PA2       | 20            |               |               |
| TSPI ch 2     | TSPI2RXD                        | PG1       | 57            | 42            | 40            |
|               | TSPI2TXD                        | PG0       | 56            | 41            | 39            |
|               | TSPI2SCK                        | PG2       | 58            | 43            | 41            |
| TSPI ch 3     | TSPI3RXD                        | PC1       | 34            | -             | -             |
|               | TSPI3TXD                        | PC0       | 35            |               |               |
|               | TSPI3SCK                        | PC2       | 33            |               |               |

**Table 4.6 Signal Connection List (2/6)**

| Function  | Combination functional pin name | Port name | M4H4 (LQFP64) | M4H2 (LQFP48) | M4H1 (LQFP44) |
|-----------|---------------------------------|-----------|---------------|---------------|---------------|
| T32A ch 0 | T32A00INA0                      | PK1       | 64            | 1             | 44            |
|           | T32A00OUTA                      | PK0       | 63            | 48            | 43            |
|           | T32A00INC0                      | PK1       | 64            | 1             | 44            |
|           | T32A00OUTC                      | PK0       | 63            | 48            | 43            |
| T32A ch 1 | T32A01INA0                      | PA1       | 18            | 13            | -             |
|           | T32A01INA1                      | PA2       | 20            | -             | -             |
|           | T32A01OUTA                      | PA2       | 20            | -             | -             |
|           | T32A01INB0                      | PA0       | 19            | 14            | 13            |
|           | T32A01OUTB                      | PA0       | 19            | 14            | 13            |
|           | T32A01INC0                      | PA1       | 18            | 13            | -             |
|           | T32A01INC1                      | PA2       | 20            | -             | -             |
|           | T32A01OUTC                      | PA2       | 20            | -             | -             |
| T32A ch 2 | T32A02INA0                      | PG1       | 57            | 42            | 40            |
|           | T32A02INA1                      | PG2       | 58            | 43            | 41            |
|           | T32A02OUTA                      | PG0       | 56            | 41            | 39            |
|           | T32A02INC0                      | PG1       | 57            | 42            | 40            |
|           | T32A02INC1                      | PG2       | 58            | 43            | 41            |
|           | T32A02OUTC                      | PG0       | 56            | 41            | 39            |
| T32A ch 3 | T32A03INA0                      | PC1       | 34            | -             | -             |
|           | T32A03INA1                      | PC2       | 33            | -             | -             |
|           | T32A03OUTA                      | PC0       | 35            | 25            | 24            |
|           | T32A03INC0                      | PC1       | 34            | -             | -             |
|           | T32A03INC1                      | PC2       | 33            | -             | -             |
|           | T32A03OUTC                      | PC0       | 35            | 25            | 24            |
| T32A ch 4 | T32A04INA0                      | PF1       | 52            | -             | -             |
|           | T32A04INA1                      | PF2       | 51            | -             | -             |
|           | T32A04OUTA                      | PF0       | 55            | 40            | 38            |
|           | T32A04INC0                      | PF1       | 52            | -             | -             |
|           | T32A04INC1                      | PF2       | 51            | -             | -             |
|           | T32A04OUTC                      | PF0       | 55            | 40            | 38            |
| T32A ch 5 | T32A05INA0                      | PB1       | 32            | 24            | 23            |
|           | T32A05OUTA                      | PB0       | 31            | 23            | 22            |
|           | T32A05OUTB                      | PB1       | 32            | 24            | 23            |
|           | T32A05INC0                      | PB1       | 32            | 24            | 23            |
|           | T32A05OUTC                      | PB0       | 31            | 23            | 22            |

**Table 4.7 Signal Connection List (3/6)**

| Function                  | Combination functional pin name | Port name | M4H4 (LQFP64) | M4H2 (LQFP48) | M4H1 (LQFP44) |
|---------------------------|---------------------------------|-----------|---------------|---------------|---------------|
| 12-bit ADC unit A, unit B | AINA11                          | PD0       | 37            | 27            | 26            |
|                           | AINA12                          | PD1       | 38            | 28            | 27            |
|                           | AINA10                          | PD2       | 39            | 29            | 28            |
|                           | AINA09                          | PD3       | 40            | 30            | 29            |
|                           | AINA08                          | PD4       | 41            | 31            | 30            |
|                           | AINA07                          | PD5       | 42            | 32            | 31            |
|                           | AINA06                          | PD6       | 43            | 33            | 32            |
|                           | AINA05                          | PE0       | 44            | 34            | 33            |
|                           | AINA04                          | PE1       | 45            | 35            | 34            |
|                           | AINA03                          | PE2       | 46            | 36            | -             |
|                           | AINA02                          | PE3       | 47            | -             | -             |
|                           | AINA01                          | PE4       | 48            | -             | -             |
| INT                       | INT00a                          | PK0       | 63            | 48            | 43            |
|                           | INT00b                          | PF1       | 52            | -             | -             |
|                           | INT01a                          | PK1       | 64            | 1             | 44            |
|                           | INT01b                          | PF2       | 51            | -             | -             |
|                           | INT02a                          | PK2       | 1             | 2             | 1             |
|                           | INT02b                          | PB0       | 31            | 23            | 22            |
|                           | INT03a                          | PK3       | 2             | 3             | 2             |
|                           | INT03b                          | PB1       | 32            | 24            | 23            |
|                           | INT04                           | PG0       | 56            | 41            | 39            |
|                           | INT05                           | PG1       | 57            | 42            | 40            |
|                           | INT06                           | PK4       | 3             | 4             | 3             |
|                           | INT07a                          | PA0       | 19            | 14            | 13            |
|                           | INT07b                          | PC2       | 33            | -             | -             |
|                           | INT08                           | PC0       | 35            | 25            | 24            |
|                           | INT09                           | PA1       | 18            | 13            | -             |
| INT10                     | PC1                             | 34        | -             | -             |               |

**Table 4.8 Signal Connection List (4/6)**

| Function      | Combination functional pin name | Port name | M4H4 (LQFP64) | M4H2 (LQFP48) | M4H1 (LQFP44) |
|---------------|---------------------------------|-----------|---------------|---------------|---------------|
| A-PMD<br>ch 0 | EMG0                            | PJ6       | 22            | 15            | 14            |
|               |                                 | PD6       | 43            | 33            | 32            |
|               |                                 | PH2       | 13            | 8             | 8             |
|               | OVV0                            | PJ7       | 21            | -             | -             |
|               | U00                             | PJ0       | 28            | 21            | 20            |
|               | VO0                             | PJ2       | 26            | 19            | 18            |
|               | WO0                             | PJ4       | 24            | 17            | 16            |
|               | XO0                             | PJ1       | 27            | 20            | 19            |
|               | YO0                             | PJ3       | 25            | 18            | 17            |
|               | ZO0                             | PJ5       | 23            | 16            | 15            |
|               | PMD0DBG                         | PB0       | 31            | 23            | 22            |
|               |                                 | PG0       | 56            | 41            | 39            |
|               |                                 | PJ0       | 28            | 21            | 20            |

**Table 4.9 Signal Connection List (5/6)**

| Function | Combination functional pin name | Port name | M4H4 (LQFP64) | M4H2 (LQFP48) | M4H1 (LQFP44) |
|----------|---------------------------------|-----------|---------------|---------------|---------------|
| TRGSEL   | TRGIN0                          | PF0       | 55            | 40            | 38            |
|          | TRGIN1                          | PB1       | 32            | 24            | 23            |
|          | TRGIN2                          | PF2       | 51            | -             | -             |
| JTAG/SW  | TMS                             | PK2       | 1             | 2             | 1             |
|          | TCK                             | PK3       | 2             | 3             | 2             |
|          | TDO                             | PK1       | 64            | 1             | 44            |
|          | TDI                             | PK0       | 63            | 48            | 43            |
|          | TRST_N                          | PK4       | 3             | 4             | 3             |
|          | SWDIO                           | PK2       | 1             | 2             | 1             |
|          | SWCLK                           | PK3       | 2             | 3             | 2             |
|          | SWV                             | PK1       | 64            | 1             | 44            |
| TRACE    | TRACECLK                        | PL4       | 8             | -             | -             |
|          | TRACEDATA0                      | PL0       | 7             |               |               |
|          | TRACEDATA1                      | PL1       | 6             |               |               |
|          | TRACEDATA2                      | PL2       | 5             |               |               |
|          | TRACEDATA3                      | PL3       | 4             |               |               |
| NBDIF    | NBDSYNC                         | PK4       | 3             | -             | -             |
|          | NBDCLK                          | PL4       | 8             |               |               |
|          | NBDDATA0                        | PL0       | 7             |               |               |
|          | NBDDATA1                        | PL1       | 6             |               |               |
|          | NBDDATA2                        | PL2       | 5             |               |               |
|          | NBDDATA3                        | PL3       | 4             |               |               |

**Table 4.10 Signal Connection List (6/6)**

| Function          | Pin name | Port name | M4H4<br>(LQFP64) | M4H2<br>(LQFP48) | M4H1<br>(LQFP44) |
|-------------------|----------|-----------|------------------|------------------|------------------|
| Input/output port | PH3      |           | 12               | -                | 7                |
| Control pin       | X1       | PH0       | 15               | 10               | 10               |
|                   | X2       | PH1       | 16               | 11               | 11               |
|                   | EHCLKIN  | PH0       | 15               | 10               | 10               |
|                   | SCOUT    | PJ0       | 28               | 21               | 20               |
|                   | BOOT_N   | PJ6       | 22               | 15               | 14               |
|                   | RESET_N  |           | 17               | 12               | 12               |
|                   | MODE     |           | 62               | 47               | 42               |
| Power supply pin  | VREFH    |           | 49               | 37               | 35               |
|                   | AVDD5    |           | 50               | 38               | 36               |
|                   | AVSS     |           | 36               | 26               | 25               |
|                   | DVDD5A   |           | 9                | 5                | 4                |
|                   | DVDD5B   |           | 30               | -                | -                |
|                   | DVDD5C   |           | 53               | -                | -                |
|                   | DVSSA    |           | 14               | 9                | 9                |
|                   | DVSSB    |           | 29               | 22               | 21               |
|                   | DVSSC    |           | 54               | 39               | 37               |
|                   | REGOUT1  |           | 11               | 7                | 6                |
|                   | REGOUT2  |           | 10               | 6                | 5                |

### 4.3. Ports

The symbols of each table of the port have the following meanings.

- Input/Output: Input or/and output of port
  - Input: Input port
  - Output: Output port
  - I/O: Input/Output port
  
- PU/PD: Programmable pull-up or/and pull-down register
  - PU: Programmable pull-up resistor can be enabled.
  - PD: Programmable pull-down resistor can be enabled.
  
- OD: Programmable open-drain output
  - Yes: Supported
  - No: Not supported
  
- 5V\_T: 5V-tolerant input
  - Yes: Supported
  - N/A: Not available
  
- SMT/CMOS: Input gate
  - SMT: Schmitt trigger input
  - CMOS: CMOS input
  
- Under Reset: Port state under reset
  - Hi-Z: High impedance
  - PU: Pull-up resistor enabled
  - PD: Pull-down resistor enabled
  
- After Reset: Port state after reset
  - Hi-z: High impedance
  - PU: Pull-up resistor enabled
  - PD: Pull-down resistor enabled

## 4.3.1. Port Specification Table

**Table 4.11 Port Names and Specifications of Port A, B, C, D, E, F, G**

| Port name | Input/output | PU/PD | OD  | 5V_T | SMT/CMOS | Under reset | After reset |
|-----------|--------------|-------|-----|------|----------|-------------|-------------|
| PA0       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PA1       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PA2       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PB0       | Input/Output | PU/PD | YES | YES  | SMT      | Hi-Z        | Hi-Z        |
| PB1       | Input/Output | PU/PD | YES | YES  | SMT      | Hi-Z        | Hi-Z        |
| PC0       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PC1       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PC2       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PD0       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PD1       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PD2       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PD3       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PD4       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PD5       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PD6       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PE0       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PE1       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PE2       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PE3       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PE4       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PF0       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PF1       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PF2       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PG0       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PG1       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PG2       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PG3       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PG4       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |
| PG5       | Input/Output | PU/PD | YES | N/A  | SMT      | Hi-Z        | Hi-Z        |

**Table 4.12 Port Names and Specifications of Port H, J, K, L**

| Port name | Input/output | PU/PD            | OD  | 5V_T | SMT/CMOS | Under reset     | After reset   |
|-----------|--------------|------------------|-----|------|----------|-----------------|---------------|
| PH0       | Input        | PD               | N/A | N/A  | SMT      | Hi-Z            | Hi-Z          |
| PH1       | Input        | PD               | N/A | N/A  | SMT      | Hi-Z            | Hi-Z          |
| PH2       | Input/Output | PU/PD            | YES | N/A  | SMT      | Hi-Z            | Hi-Z          |
| PH3       | Input/Output | PU/PD            | YES | N/A  | SMT      | Hi-Z            | Hi-Z          |
| PJ0       | Input/Output | PU/PD            | YES | N/A  | SMT      | Hi-Z            | Hi-Z          |
| PJ1       | Input/Output | PU/PD            | YES | N/A  | SMT      | Hi-Z            | Hi-Z          |
| PJ2       | Input/Output | PU/PD            | YES | N/A  | SMT      | Hi-Z            | Hi-Z          |
| PJ3       | Input/Output | PU/PD            | YES | N/A  | SMT      | Hi-Z            | Hi-Z          |
| PJ4       | Input/Output | PU/PD            | YES | N/A  | SMT      | Hi-Z            | Hi-Z          |
| PJ5       | Input/Output | PU/PD            | YES | N/A  | SMT      | Hi-Z            | Hi-Z          |
| PJ6       | Input/Output | PU/PD<br>(Note1) | YES | N/A  | SMT      | PU              | Hi-Z          |
| PJ7       | Input/Output | PU/PD            | YES | N/A  | SMT      | Hi-Z            | Hi-Z          |
| PK0       | Input/Output | PU/PD            | YES | N/A  | SMT      | PU<br>(Note2)   | PU<br>(Note2) |
| PK1       | Input/Output | PU/PD            | YES | N/A  | SMT      | Hi-Z<br>(Note2) | Hi-Z<br>Note2 |
| PK2       | Input/Output | PU/PD            | YES | N/A  | SMT      | PU<br>(Note2)   | PU<br>(Note2) |
| PK3       | Input/Output | PU/PD            | YES | N/A  | SMT      | PD<br>(Note2)   | PD<br>(Note2) |
| PK4       | Input/Output | PU/PD            | YES | N/A  | SMT      | PU<br>(Note2)   | PU<br>(Note2) |
| PL0       | Input/Output | PU/PD            | YES | N/A  | SMT      | Hi-Z            | Hi-Z          |
| PL1       | Input/Output | PU/PD            | YES | N/A  | SMT      | Hi-Z            | Hi-Z          |
| PL2       | Input/Output | PU/PD            | YES | N/A  | SMT      | Hi-Z            | Hi-Z          |
| PL3       | Input/Output | PU/PD            | YES | N/A  | SMT      | Hi-Z            | Hi-Z          |
| PL4       | Input/Output | PU/PD            | YES | N/A  | SMT      | Hi-Z            | Hi-Z          |

Note1: PJ6 is combination with BOOT\_N. When RESET\_N pin is "Low" level, pull-up resistor of PJ6 is connected.

When RESET\_N pin is "High" level, PJ6 state is Hi-Z with internal reset.

Note2: It is assigned to a debugging pin in the state of the initial stage.

(PK0: TDI, PK1: TDO/SWV, PK2: TMS/SWDIO, PK3: TCK/SWCLK, PK4: TRST\_N)

After receiving the command from TOOL, PK1: TDO/SWV becomes output.

## 5. Functional Description and Operation Description

### 5.1. Reference Manuals

For more information of built-in functions on TPM4H Group(1), refer to the Reference Manuals below;

**Table 5.1 Reference Manuals for TPM4H Group(1)**

| Reference Manual                                  | IP Symbol     | Category   |
|---|---------------|------------|
| Input/Output Ports (TPM4H Group(1))               | PORT-M4H(1)   | System     |
| Exception (TPM4H Group(1))                        | EXCEPT-M4H(1) | System     |
| Clock Control and Operation Mode (TPM4H Group(1)) | CG-M4H(1)     | System     |
| Product Information (TPM4H Group(1))              | PINFO-M4H(1)  | System     |
| Flash Memory                                      | FLASH256U2-A  | Peripheral |
| Trimming Circuit                                  | TRM-B         | Peripheral |
| Oscillation Frequency Detector                    | OFD-A         | Peripheral |
| Voltage Detection Circuit                         | LVD-D         | Peripheral |
| Digital Noise Filter Circuit                      | DNF-A         | Peripheral |
| Debug Interface                                   | DEBUG-A       | Peripheral |
| Non-break debug Interface                         | NBDIF-A       | Peripheral |
| DMA Controller                                    | DMAC-B        | Peripheral |
| Asynchronous Serial Communication Circuit         | UART-C        | Peripheral |
| Serial Peripheral Interface                       | TSPI-E        | Peripheral |
| I <sup>2</sup> C Interface                        | I2C-B         | Peripheral |
| I <sup>2</sup> C Interface version A              | EI2C-A2       | Peripheral |
| 12-bit Analog to Digital Converter                | ADC-G2        | Peripheral |
| Advanced Programmable Motor Control Circuit       | A-PMD-A       | Peripheral |
| 32-bit Timer Event Counter                        | T32A-C        | Peripheral |
| Clock Selective Watchdog Timer                    | SIWDT-A       | Peripheral |
| CRC Calculation Circuit                           | CRC-A         | Peripheral |
| RAM Parity  | RAMP-B        | Peripheral |

## 5.2. Processor Core

The TPM4H Group(1) incorporates a high-performance 32-bit processor core (Arm Cortex-M4 processor with FPU).

For the operation of the processor core, refer to the Arm documentation set for "Cortex-M series processors". This section explains the product-specific information.

### 5.2.1. Core Information

The Cortex-M4 processor with FPU revision used in the TPM4H Group(1) is shown as below:

For details of the CPU core and the architecture, refer to the Arm documentation on Arm's website.

**Table 5.2 Core Revision**

| Group name     | Core revision |
|----------------|---------------|
| TPM4H Group(1) | r0p1          |

### 5.2.2. Configurable Options

In the Cortex-M4 processor with FPU, some blocks can be selected to implement. The following table shows the configurations of the TPM4H Group(1).

**Table 5.3 Configurable Options and Their Implementations**

| Configurable option            | Implementation                                     |
|--------------------------------|--|
| FWB                            | Literal comparator: 2<br>Instruction comparator: 6 |
| DWT                            | Comparator: 4                                      |
| ITM                            | Available  |
| MPU                            | Available  |
| ETM                            | Available  |
| AHB-AP                         | Available  |
| AHB trace macro cell interface | Not available                                      |
| TPIU                           | Available  |
| WIC                            | Not available                                      |
| Debug port                     | JTAG/Serial wire                                   |
| Bit band                       | Available  |
| Sequential control of AHB      | Not available                                      |

### 5.3. Clock Control and Operating Mode (CG)

The clock control and operating mode (CG) selects a clock gear ratio and the prescaler clock, or warm-up time of the oscillator.

There are NORMAL mode and low-power consumption mode as operating modes. Power consumption can be decreased by operating mode transition for use purposes.

The outline of the clock/mode control circuit is as follows:

- Internal high-speed oscillator (IHOSC1): 10MHz
- Selectable from the external high-speed oscillator (EHOSC) or internal high-speed oscillator (IHOSC1).
- Clock multiplication circuit (PLL):  
For system clock, capable of 120MHz output by changing the multiplication ratio according to fosc.
- Clock gear:  
The high-speed clock can be divided by 1, 2, 4, 8, or 16 and used as the system clock (fsys).
- Low-power consumption mode:  
IDLE mode: Only CPU is stopped. The operation of each peripheral circuit can be enabled or disabled.  
STOP1 mode: fsys is stopped.

### 5.4. Flash Memory (256KB)

The cord flash stores instruction code, and CPU reads instruction code and executes.

It has protection function which prohibits write or erase by the block unit and security function which prohibits the reading of the program code by the 3rd person.

## 5.5. Oscillator

- External high-speed oscillator (EHOSC): Pins of EHOSC are connected crystal resonator or ceramic resonator. Use as clock source for system clock (fsys).
- Internal high-speed oscillator 1 (IHOSC1): The oscillation frequency is 10MHz. Use as clock source for system clock (fsys).
- Internal high-speed oscillator 2 (IHOSC2): The oscillation frequency is 10MHz. Use as the reference clock of OFD and clock source of SIWDT.

**Table 5.4 Built-in Oscillator**

| Oscillator | M4H4 | M4H2 | M4H1 |
|------------|------|------|------|
| EHOSC      | ✓    | ✓    | ✓    |
| IHOSC1     | ✓    | ✓    | ✓    |
| IHOSC2     | ✓    | ✓    | ✓    |

Note: ✓: Available, -: N/A

## 5.6. Trimming Circuit (TRM)

The trimming circuit (TRM) can adjust oscillation frequency of the internal high-speed oscillator 1 (IHOSC1).

**Table 5.5 Built-in TRM**

|     | M4H4 | M4H2 | M4H1 |
|-----|------|------|------|
| TRM | ✓    | ✓    | ✓    |

Note: ✓: Available, -: N/A

## 5.7. Oscillation Frequency Detector (OFD)

The oscillation frequency detector (OFD) can detect an abnormal system clock. The external high-speed clock ( $f_{EHOSC}$ ) or high-speed clock ( $f_c$ ) can be selected as the target of detection.

The selected clock is measured by the internal high-speed oscillator 2 (IHOSC2) which is used as the reference clock of OFD. If the clock frequency of  $f_{EHOSC}$  or  $f_c$  is out of the specified range, a reset signal occurs.

The upper limit and lower limit of detection frequency ranges can be specified respectively.

**Table 5.6 Built-in OFD**

|     | M4H4 | M4H2 | M4H1 |
|-----|------|------|------|
| OFD | ✓    | ✓    | ✓    |

Note: ✓: Available, -: N/A

## 5.8. Voltage Detection Circuit (LVD)

The voltage detection circuit (LVD) detects whether a power-supply voltage is lower or higher than the preset voltage. When a lower or higher voltage than the preset voltage is detected, the LVD generates an interrupt request or internal reset signal.

Setting voltage can be selected from eight voltages. The LVD is set to enable from resetting when the power supply is turned on.

**Table 5.7 Built-in LVD**

|     | M4H4 | M4H2 | M4H1 |
|-----|------|------|------|
| LVD | ✓    | ✓    | ✓    |

Note: ✓: Available, -: N/A

## 5.9. Digital Noise Filter Circuit (DNF)

The digital noise filter circuit (DNF) can eliminate the noise of signal from an external interrupt input pin. The high and low noise from an external interrupt signal INTx is eliminated.

**Table 5.8 Number of External Interrupts (Number of Built-in DNF)**

|                               | M4H4 | M4H2 | M4H1 |
|-------------------------------|------|------|------|
| Number of external interrupts | 11   | 10   | 9    |

## 5.10. Debug Interface (DEBUG)

The serial wire debug ports (SWCLK and SWDIO) and the JTAG debug ports (TDI, TDO, TMS, TCK, and TRST\_N) use for the interface for connecting debug tool. These pins are connected with the debug tool and used for the program development. And also the trace clock (TRACECLK), trace outputs (TRACEDATA0 to 3) and the NBDIF (NBDSYNC, NBDCLK, and NBDDATA0 to 3) are used to reduce the debug process.

TMPM4H Group(1) products support the serial wire debug ports, JTAG debug ports, trace clock and trace outputs, and NBDIF.

**Table 5.9 Built-in Debug Interface**

| Pin names  | PORT | M4H4 | M4H2 | M4H1 |
|------------|------|------|------|------|
| TMS/SWDIO  | PK2  | ✓    | ✓    | ✓    |
| TCK/SWCLK  | PK3  | ✓    | ✓    | ✓    |
| TDO/SWV    | PK1  | ✓    | ✓    | ✓    |
| TDI        | PK0  | ✓    | ✓    | ✓    |
| TRST_N     | PK4  | ✓    | ✓    | ✓    |
| TRACECLK   | PL4  | ✓    | -    | -    |
| TRACEDATA0 | PL0  | ✓    | -    | -    |
| TRACEDATA1 | PL1  | ✓    | -    | -    |
| TRACEDATA2 | PL2  | ✓    | -    | -    |
| TRACEDATA3 | PL3  | ✓    | -    | -    |
| NBDSYNC    | PK4  | ✓    | -    | -    |
| NBDCLK     | PL4  | ✓    | -    | -    |
| NBDDATA0   | PL0  | ✓    | -    | -    |
| NBDDATA1   | PL1  | ✓    | -    | -    |
| NBDDATA2   | PL2  | ✓    | -    | -    |
| NBDDATA3   | PL3  | ✓    | -    | -    |

Note: ✓: Available, -: N/A

### 5.10.1. Non-break Debug Interface (NBDIF)

Connecting the debug tools which support Non-break Debug Interface (NBDIF) can provide RAM monitor, etc. Supporting the NBDIF varies depending on the product. Refer to "Table 5.9 Built-in Debug Interface".

## 5.11. DMA Controller (DMAC)

The DMA controller (DMAC) is the peripheral function to move the data between peripheral function and the memory, or between memories. These operations are performed separately from the CPU control; thus, the CPU load can be greatly reduced by using the DMA.

TMPM4H Group(1) products have one unit of DMAC. One DMAC has the DMA requests of the 32 channels.

**Table 5.10 Built-in DMAC**

| DMAC   | M4H4 | M4H2 | M4H1 |
|--------|------|------|------|
| Unit A | ✓    | ✓    | ✓    |

Note: ✓: Available, -: N/A

## 5.12. Asynchronous Serial Communication Circuit (UART)

The asynchronous serial communication circuit (UART) is asynchronous serial communication function. It can select the data length of 7, 8 or 9 bits, use or not use parity bit, and a STOP bit length of 1 or 2 bits. Moreover, selection of the MSB first/LSB first, data signal polarity can be performed and pin exchanged of UTxTXDA/UTxRXD can be performed by a port setting.

The FIFO buffer supports data communication on 9 bits × 8 stages at transmission; and on 9 bits × 8 stages at reception.

**Table 5.11 Built-in UART**

| UART      | M4H4 | M4H2 | M4H1 |
|-----------|------|------|------|
| Channel 0 | ✓    | ✓    | ✓    |
| Channel 1 | ✓    | ✓    | ✓    |
| Channel 2 | ✓    | ✓    | ✓    |
| Channel 3 | ✓    | -    | -    |

Note1: ✓: Available, -: N/A

Note2: External pins vary depending on the product. Refer to "2. Pin Assignment".

## 5.13. Serial Peripheral Interface (TSPI)

The serial peripheral interface (TSPI) on TPM4H Group(1) products supports only SIO mode which does not use a CS signal. It performs the serial communication with other device at high speed.

It can change the data length from 7 bits with a parity bit to 32 bits without a parity bit on a per bit basis

The TSPI has the reception and transmission 16-bit FIFO on 8 stages. The TSPI on TPM4H Group(1) products supports the controller device operation and target device operation.

The TSPI can use the frame mode (frame length: 8 to 32 bits) or sector mode (sector length: 2 to 4 sectors and frame length: 8 to 128 bits).

**Table 5.12 Built-in TSPI**

| TSPI      | M4H4 | M4H2 | M4H1 |
|-----------|------|------|------|
| Channel 0 | ✓    | ✓    | ✓    |
| Channel 1 | ✓    | -    | -    |
| Channel 2 | ✓    | ✓    | ✓    |
| Channel 3 | ✓    | -    | -    |

Note1: ✓: Available, -: N/A

Note2: External pins vary depending on the product. Please refer to section "2 Pin Assignment".

## 5.14. I<sup>2</sup>C Interface

The following table shows the list of built-in I<sup>2</sup>C interface (I2C/EI2C).

The I2C and EI2C must be used exclusively.

**Table 5.13 Built-in I2C/EI2C**

| I2C/EI2C  | M4H4 | M4H2 | M4H1 |
|-----------|------|------|------|
| Channel 0 | ✓    | ✓    | ✓    |

Note1: ✓: Available, -: N/A

Note2: External pins vary depending on the product. Please refer to "2. Pin Assignment".

### **5.14.1. I<sup>2</sup>C Interface (I2C)**

The I<sup>2</sup>C interface (I2C) is two-wire bidirectional serial communications between the controller and target devices. The I2C supports the multi-controller bus which two or more controller devices on the same bus in.

And also, it supports standard-mode (transfer speed: up to 100kHz), fast-mode (transfer speed: up to 400kHz). Its addressing mode supports 7-bit addressing.

### **5.14.2. I<sup>2</sup>C Interface Version A (EI2C)**

The I<sup>2</sup>C Interface version A (EI2C) is compatible with two-wire bidirectional serial communications of I<sup>2</sup>C interface between the controller and target devices. The EI2C supports the multi-controller bus which two or more controller devices on the same bus in.

And also, it supports standard-mode (transfer speed: up to 100kHz), fast-mode (transfer speed: up to 400kHz), and fast-mode Plus (transfer speed: up to 1MHz) . Its addressing mode supports 7-bit and 10-bit addressing.

### 5.15. 12-bit Analog to Digital Converter (ADC)

The 12-bit analog to digital converter (ADC) is a successive-approximation analog-to-digital converter. The combination of conversion result register and analog input can be programmed for each AD conversion start factor.

The AD conversion start factor is selected from a software or the peripheral functions (trigger output of A-PMD, timer/event counter output, port input, or trigger generation circuit).

The monitor function is available and it can generate an interrupt request when the compare conditions are matched.

The ADC incorporates a selector to connect VREFH/VREFL with reference power supply. Controlling by software can support self-diagnosis function.

**Table 5.14 Number of Analog Inputs**

|                                  | M4H4 | M4H2 | M4H1 |
|----------------------------------|------|------|------|
| Number of analog inputs (Unit A) | 12   | 10   | 9    |

Note: External pins vary depending on the product. Please refer to "2. Pin Assignment".

The trigger generation circuit (TRGGEN) is a function that can be used with the ADC.

The TRGGEN outputs a trigger signal to start the conversion.

For information on TRGGEN, refer to the section "12-bit Analog to Digital Converter (ADC)" in the reference manual "Product Information".

### 5.16. Advanced Programmable Motor Control Circuit (A-PMD)

The advanced programmable motor control circuit (A-PMD) controls the brushless DC motors easily. It incorporates the pulse modulation circuit and dead-time circuit, and easily generates waveforms for motor control by coordinating with the 3-phase complementary PWM and ADC.

It also provides the over-voltage detection input and abnormal detection input to support safety measures.

Furthermore, it can provide the 3-phase interleaved PFC control for power factor improvement.

**Table 5.15 Built-in A-PMD**

| A-PMD     | M4H4 | M4H2 | M4H1 |
|-----------|------|------|------|
| Channel 0 | ✓    | ✓    | ✓    |

Note1: ✓: Available, -: N/A

Note2: External pins vary depending on the product. Refer to section "2. Pin Assignment".

## 5.17. 32-bit Timer Event Counter (T32A)

The 32-bit timer event counter (T32A) is a timer event counter that can operate as a 32-bit timer or two 16-bit timers. The option to select whether T32A operates as a 32-bit timer or a 16-bit timer is available. When the T32A operates as 32-bit timer, the T32A operates as timer C incorporating a 32-bit counter. When the T32A operates as 16-bit timer, the T32A operates as timer A and B incorporating a 16-bit counter.

The T32A has various functions such as an interval timer, event counter, input capture, 2-phase pulse count, PPG output, synchronous start, and trigger start and stop.

**Table 5.16 Built-in T32A**

| T32A      | M4H4 | M4H2 | M4H1 |
|-----------|------|------|------|
| Channel 0 | ✓    | ✓    | ✓    |
| Channel 1 | ✓    | ✓    | ✓    |
| Channel 2 | ✓    | ✓    | ✓    |
| Channel 3 | ✓    | ✓    | ✓    |
| Channel 4 | ✓    | ✓    | ✓    |
| Channel 5 | ✓    | ✓    | ✓    |

Note1: ✓: Available, -: N/A

Note2: External pins vary depending on the product. Refer to section "2. Pin Assignment".

## 5.18. Clock Selective Watchdog Timer (SIWDT)

The clock selective watchdog timer (SIWDT) is a peripheral function that detects an overflow of the counter and generates an interrupt request or reset signal. This state occurs when a counter cannot be cleared within the preset detection time because the CPU executes mal function (a runaway) caused by a noise or others.

The count clock for the counter can be selected from three clocks: system clock (fsys) of 4 division, internal high-speed oscillation clock 1 (fIHOSC1), or internal high-speed oscillation clock 2 (fIHOSC2).

It also provides the count-clear window function that can clear the binary counter only for the specified period.

Moreover, change of a register can be prohibited by setting to protected mode until the MCU is reset. (the counter can be cleared in the protection mode.)

**Table 5.17 Built-in SIWDT**

|       | M4H4 | M4H2 | M4H1 |
|-------|------|------|------|
| SIWDT | ✓    | ✓    | ✓    |

Note: ✓: Available, -: N/A

## 5.19. CRC Calculation Circuit (CRC)

The TMPM4H Group(1) products incorporate the hardware calculation circuit for CRC32 and CRC16.

It can be used for detecting errors by processing a memory and communication data.

**Table 5.18 Built-in CRC**

|     | M4H4 | M4H2 | M4H1 |
|-----|------|------|------|
| CRC | ✓    | ✓    | ✓    |

Note: ✓: Available, -: N/A

## 5.20. RAM Parity (RAMP)

The RAM parity (RAMP) generates an even parity for one byte data at the timing of writing data to RAM and stores it to RAM at same time. The RAMP checks that the total number of 1s in the data and parity bit is even when the CPU read data in RAM. When parity errors is detected, the RAM parity interrupt occurs.

The error status and address which the error generated in can be monitored.

A parity error can be is detected in real time, since parity generating/checking is performed by the hardware.

**Table 5.19 Built-in RAMP**

|      | M4H4 | M4H2 | M4H1 |
|------|------|------|------|
| RAMP | ✓    | ✓    | ✓    |

Note: ✓: Available, -: N/A

## 5.21. Measures for Security Risk

### 5.21.1. Outline

TMPM4H Group(1) contains two measures for security risk to prevent unauthorized access. Table 5.20, Table 5.21 and Figure 5.1 show the assumed access paths and protection targets for each operation mode.

For more information, refer to the reference manual “Flash Memory”.

(1) Security Function

The security function prohibits communication with debugging tools. It also prohibits flash writers from reading and writing to flash memory.

**Table 5.20 Access Paths and Protection Targets (1)**

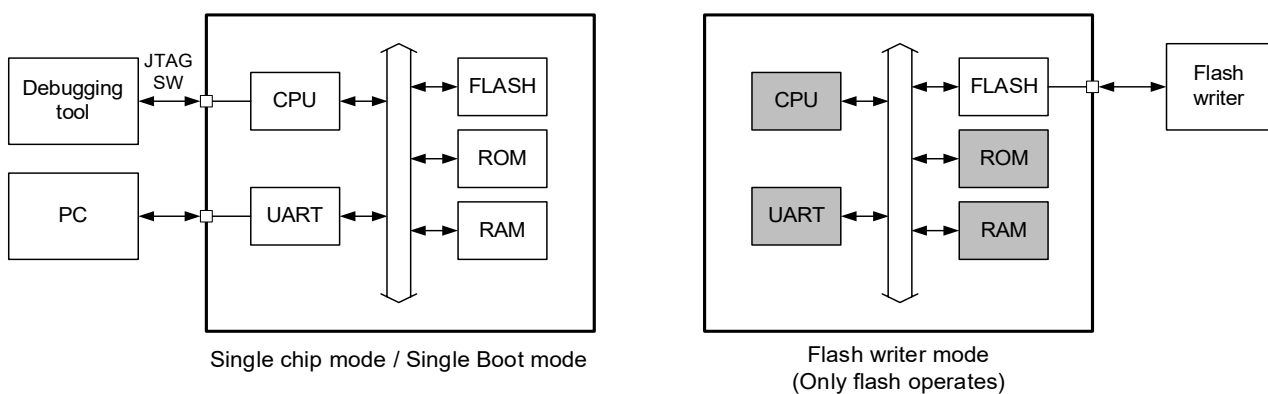
| Operation mode                       | Access path  | Protected object     |
|--------------------------------------|--------------|----------------------|
| Single chip mode<br>Single Boot mode | JTAG/SW      | CPU<br>FLASH/ROM/RAM |
| Flash writer mode                    | Flash writer | FLASH                |

(2) Password in RAM Transfer Command

Single boot mode is operated by sending a command via UART communication. The RAM transfer command is authenticated by the password.

**Table 5.21 Access Paths and Protection Targets (2)**

| Operation mode   | Access path | Protected object     |
|------------------|-------------|----------------------|
| Single Boot mode | UART        | CPU<br>FLASH/ROM/RAM |



**Figure 5.1 Measures for Security Risk**

Note) The security function does not prohibit Non-Break Debug Interface (NBDIF) communication. Prohibit it with *[NBDCR0]<NBDEN>*.  
(It’s applicable to the products with NBDIF.)

### 5.21.2. Disclaimer

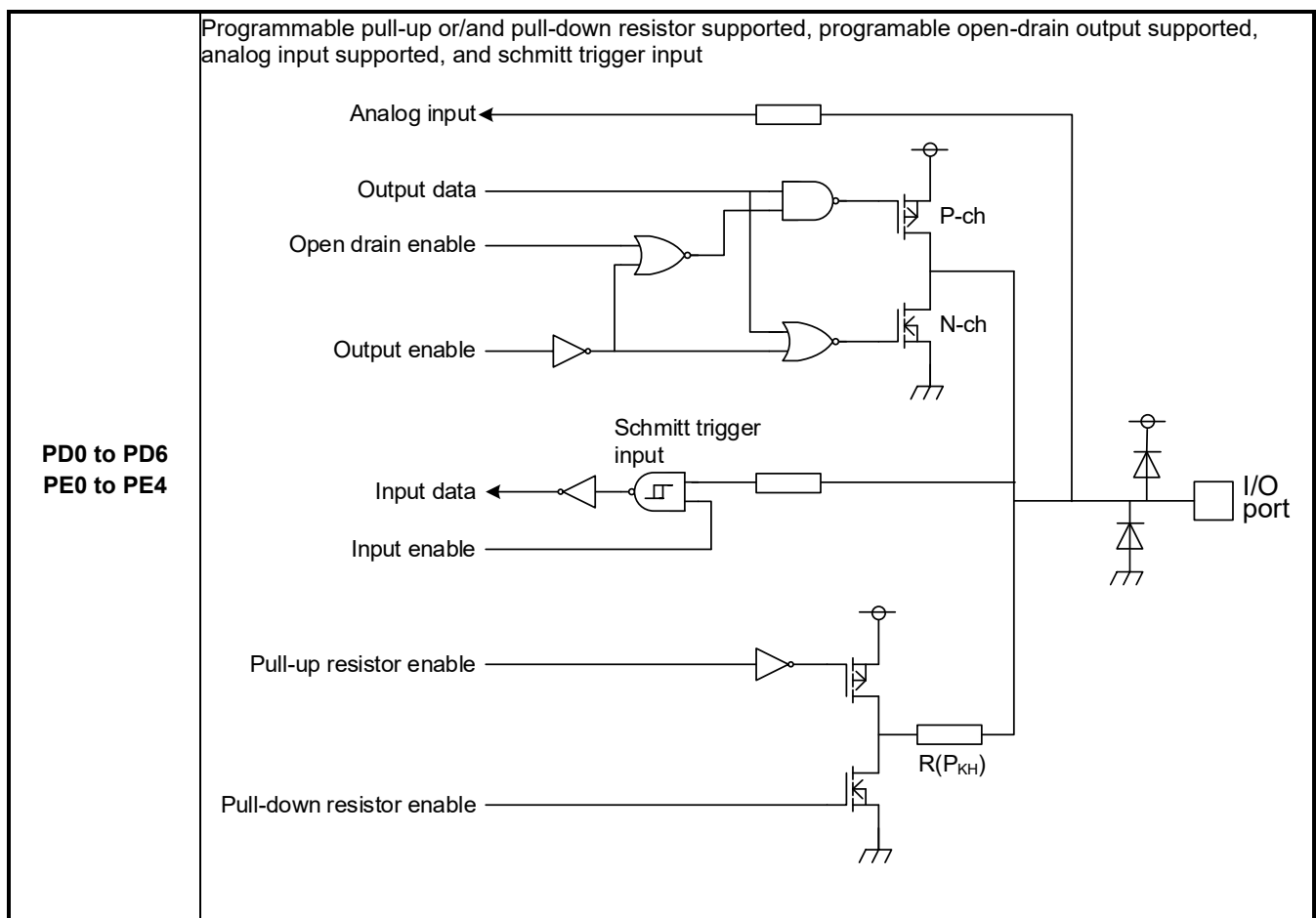
Refer to "RESTRICTIONS ON PRODUCT USE" at the end of this manual.

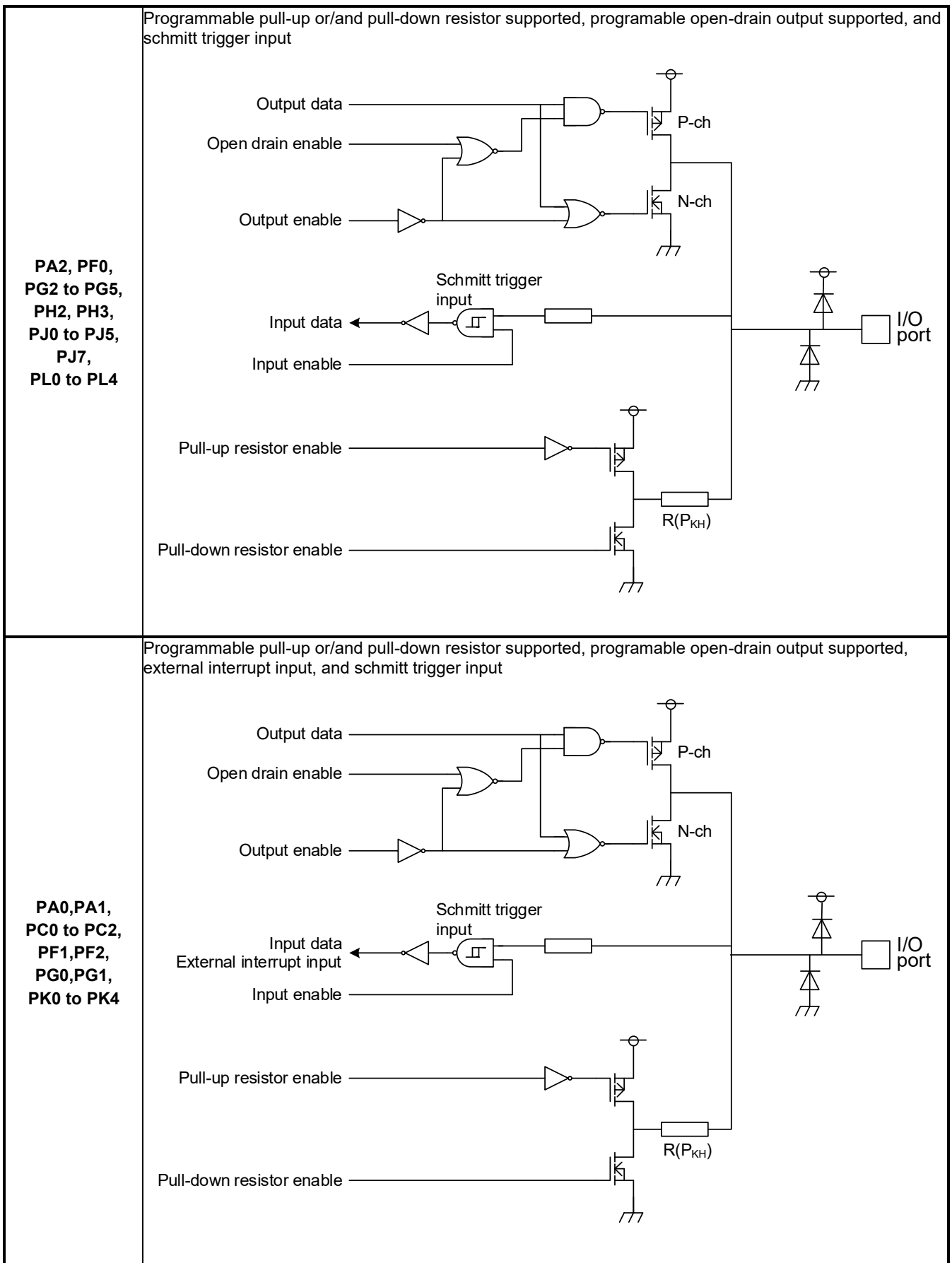
## 6. Equivalent Circuit

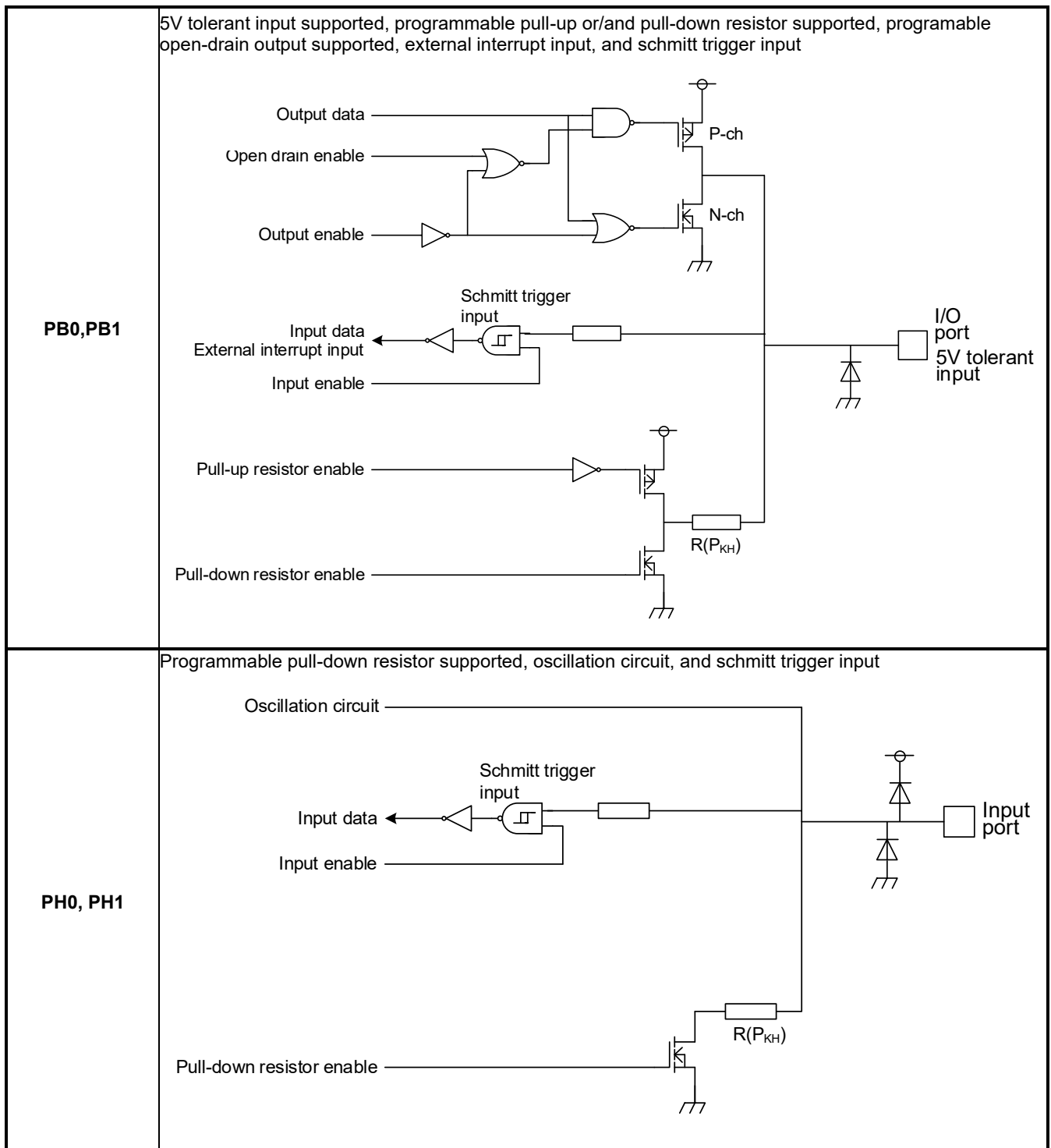
Basically, the gate symbols written are the same as those used for the standard CMOS logic IC “74HCXX” series. The input protection resistor ranges from several tens of  $\Omega$  to several hundred  $\Omega$ .

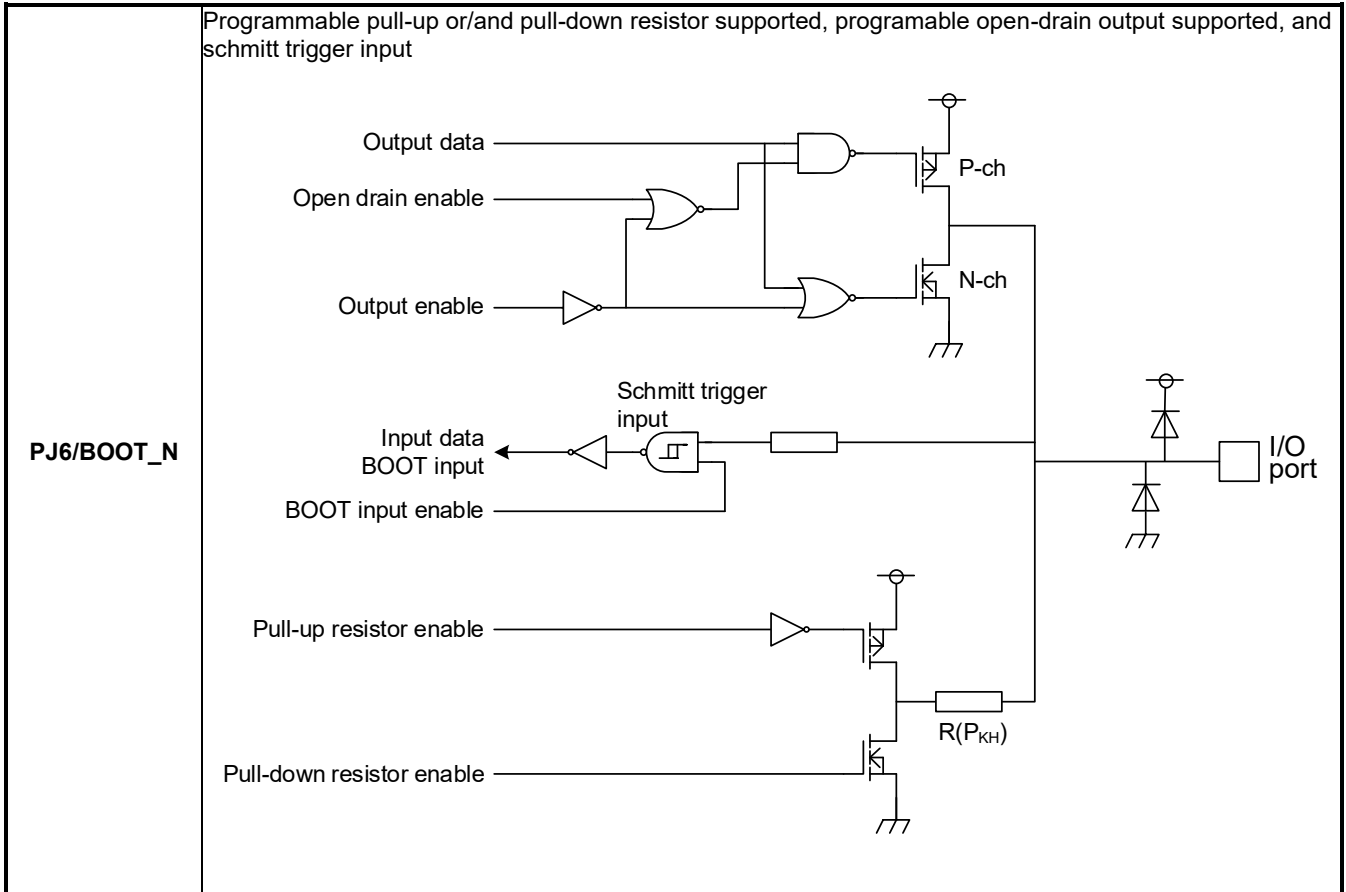
Note: The resistor without the symbol in the figure shows input protection resistor.

### 6.1. Port

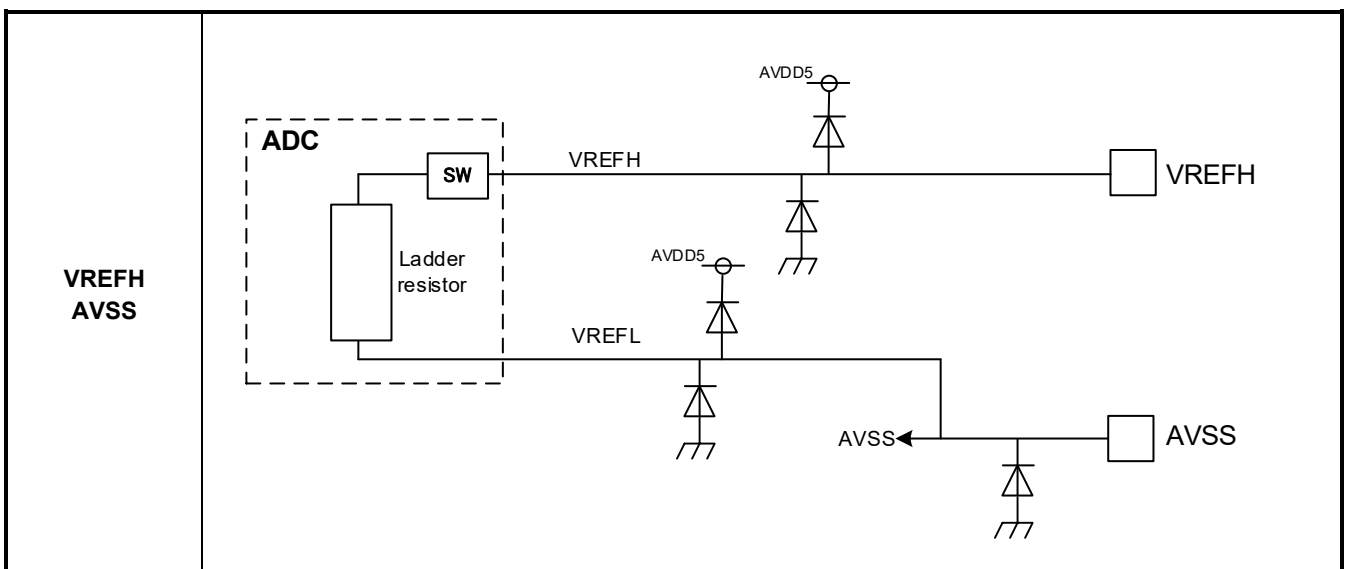






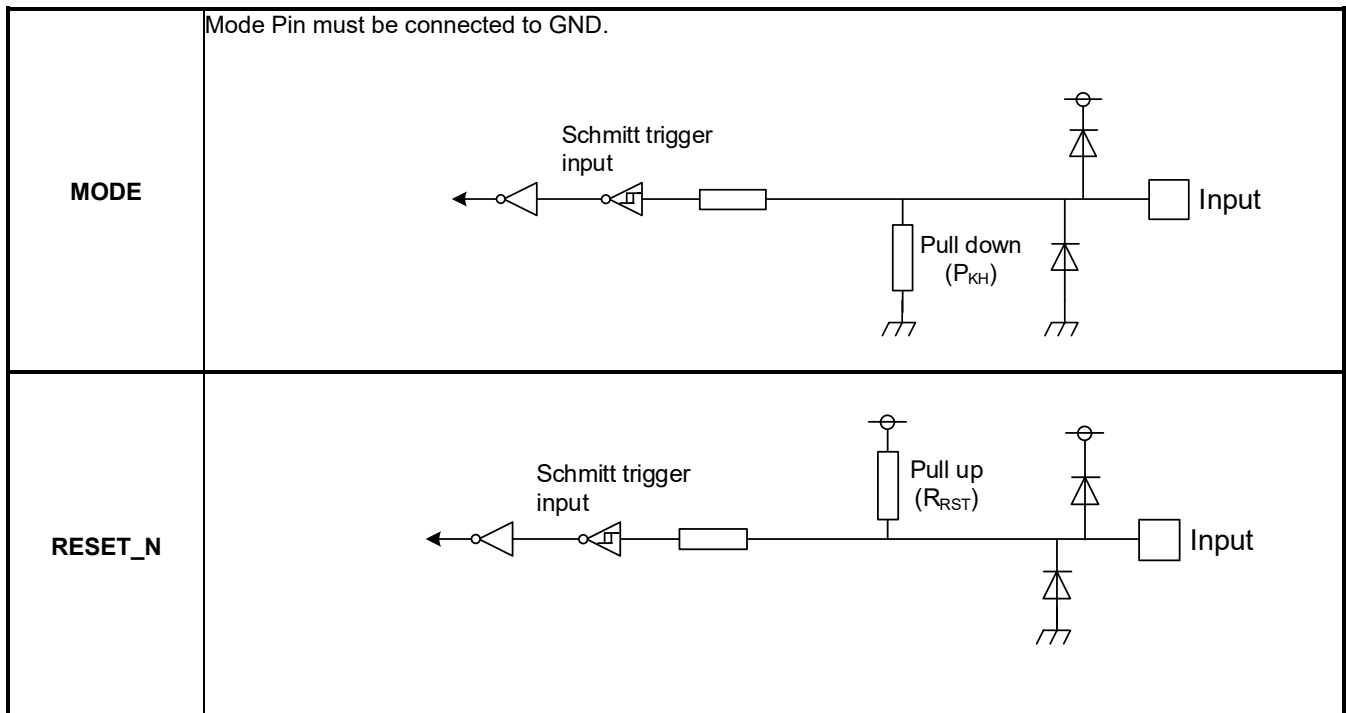


## 6.2. Power Supply Pin for Analog

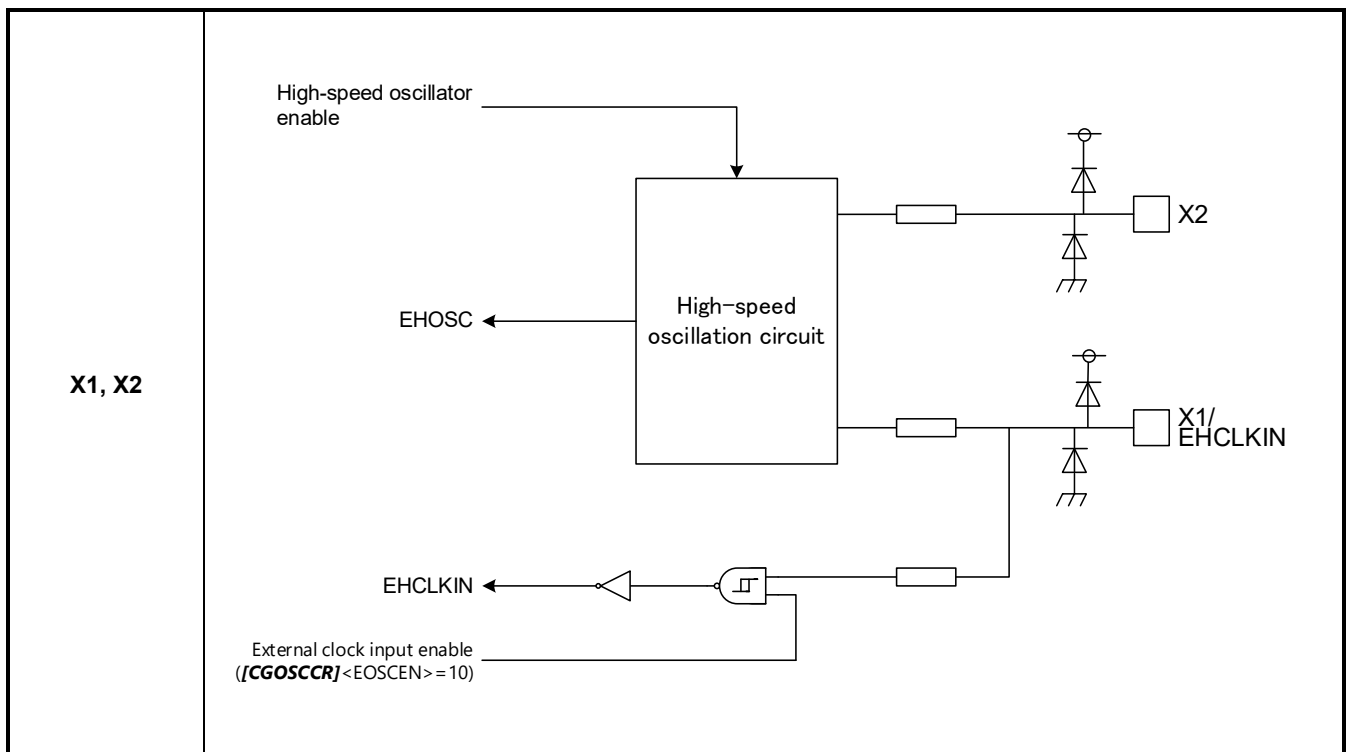


Note: SW: ON/OFF Switch Circuit

## 6.3. Control Pins



## 6.4. Clock Control Pins



## 7. Electrical Characteristics

### 7.1. Absolute Maximum Ratings

Table 7.1 Absolute Maximum Ratings

| Parameter                                     |  | Symbol                     | Rating  | Unit       |
|---|--|----------------------------|---|------------|
| Power supply voltage                          |  | DVDD5A<br>DVDD5B<br>DVDD5C | -0.3 to 6.0   | V          |
|   |  | AVDD5                      | -0.3 to 6.0   |            |
| Capacitor pin voltage for voltage maintenance |  | REGOUT1                    | -0.3 to 1.7   | V          |
|   |  | REGOUT2                    | -0.3 to 3.9   |            |
| Input voltage                                 | PA0 to PA2, PC0 to PC2,<br>PF0 to PF2, PG0 to PG5,<br>PH0 to PH3, PJ0 to PJ7,<br>PK0 to PK4, PL0 to PL4,<br>MODE, RESET_N                                  | $V_{IN1}$<br>$V_{IN2}$     | -0.3 to DVDD5+0.3 ( $\leq 6.0V$ ) (Note1)                 | V          |
|   | PD0 to PD6, PE0 to PE4   | $V_{IN3}$                  | -0.3 to AVDD5+0.3 ( $\leq 6.0V$ )                         |            |
|   | PB0, PB1   | $V_{IN4}$                  | -0.3 to 6.0   |            |
| Low level output current                      | Per pin<br>PA0 to PA2, PC0 to PC2,<br>PD0 to PD6, PE0 to PE4,<br>PF0 to PF2, PG0 to PG5,<br>PH2 to PH3, PJ0 to PJ7,<br>PK0 to PK4, PL0 to PL4              | $I_{OL}$                   | 5   | mA         |
|   | Per pin<br>PB0, PB1  | $I_{OL4}$                  | 25  |            |
|   | Total of all pins  | $\Sigma I_{OL}$            | 50  |            |
| High level output current                     | Per pin<br>PA0 to PA2, PC0 to PC2,<br>PD0 to PD6, PE0 to PE4,<br>PF0 to PF2, PG0 to PG5,<br>PH2 to PH3, PJ0 to PJ7,<br>PK0 to PK4, PL0 to PL4,<br>PB0, PB1 | $I_{OH}$                   | -5  | mA         |
|   | Total of all pins  | $\Sigma I_{OH}$            | -50   |            |
| Power consumption                             |  | PD                         | 500 ( $T_a = 85^\circ C$ )<br>250 ( $T_a = 105^\circ C$ ) | mW         |
| Soldering temperature                         |  | $T_{SOLDER}$               | 260   | $^\circ C$ |
| Storage temperature                           |  | $T_{STG}$                  | -55 to 125  | $^\circ C$ |
| Operating temperature                         |  | $T_{OPR}$                  | -40 to 105  | $^\circ C$ |

Note1: Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions. The equipment manufacturer should design so that no Absolute maximum rating value is exceeded with respect to current, voltage, power consumption, temperature, etc. Exposure to conditions beyond those listed above may cause permanent damage to the device or affect device reliability, which could increase potential risks of personal injury due to IC blow up and/or burning.

Note2: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

Note3: Apply the same voltage to DVDD5 and AVDD5 from power-on to power-off.

## 7.2. DC Electrical Characteristics (1/2)

DVDD5 = AVDD5 = 4.5 to 5.5V

DVSS = AVSS = 0V

Ta = -40 to 105°C

| Parameter                 | Symbol                               | Conditions  | Min        | Typ. | Max        | Unit |
|---------------------------|--------------------------------------|---|------------|------|------------|------|
| Power supply voltage      | VDD                                  | f <sub>osc</sub> = 6 to 24MHz<br>f <sub>sys</sub> = 1 to 120MHz | 4.5        | -    | 5.5        | V    |
| Low level Input voltage   | V <sub>IL1</sub><br>V <sub>IL2</sub> | -   | -0.3       | -    | DVDD5×0.25 | V    |
|                           | V <sub>IL3</sub>                     | -   |            |      | AVDD5×0.25 |      |
|                           | V <sub>IL4</sub>                     | -   |            |      | DVDD5×0.3  |      |
| High level Input voltage  | V <sub>IH1</sub><br>V <sub>IH2</sub> | -   | DVDD5×0.75 | -    | DVDD5+0.3  | V    |
|                           | V <sub>IH3</sub>                     | -   |            |      | AVDD5×0.75 |      |
|                           | V <sub>IH4</sub>                     | -   |            |      | DVDD5×0.7  |      |
| Low level output voltage  | V <sub>OL1</sub><br>V <sub>OL2</sub> | DVDD5 = 4.5V<br>I <sub>OL</sub> = 1.6mA                         | -          | -    | 0.4        | V    |
|                           | V <sub>OL3</sub>                     | AVDD5 = 4.5V<br>I <sub>OL</sub> = 1.6mA                         | -          | -    | 0.4        |      |
|                           | V <sub>OL4</sub>                     | DVDD5 = 4.5V<br>I <sub>OL</sub> = 8mA                           | -          | -    | 1.0        |      |
| High level output voltage | V <sub>OH1</sub><br>V <sub>OH2</sub> | DVDD5 = 4.5V<br>I <sub>OH</sub> = -1.6mA                        | DVDD5-0.4  | -    | -          | V    |
|                           | V <sub>OH3</sub>                     | AVDD5 = 4.5V<br>I <sub>OH</sub> = -1.6mA                        |            |      | AVDD5-0.4  |      |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDDA5 = 5.0V, unless otherwise noted.

Note3: Apply same voltage to DVDD5 and AVDD5.

DVDD5 = AVDD5 = 4.5 to 5.5V

DVSS = AVSS = 0V

Ta = -40 to 105°C

| Parameter                               |   | Symbol            | Conditions   | Min            | Typ.     | Max           | Unit |
|---|---|-------------------|--|----------------|----------|---------------|------|
| Input leak current                      |   | I <sub>LI</sub>   | 0.0V ≤ VIN ≤ DVDD5<br>0.0V ≤ VIN ≤ AVDD5           | -5             | ±0.05    | 5             | μA   |
| Output leak current                     |   | I <sub>LO</sub>   | 0.2 ≤ VIN ≤ DVDD5 - 0.2<br>0.2 ≤ VIN ≤ AVDD5 - 0.2 | -10            | ±0.05    | 10            |      |
| Schmitt trigger Input width             |   | V <sub>TH</sub>   | DVDD5 = AVDD5 = 5.0V                               | -              | 1.0      | -             | V    |
| Reset pull-up resistor                  |   | R <sub>RST</sub>  | -  | 25             | 50       | 100           | kΩ   |
| Programmable pull-up/pull-down resistor |   | P <sub>KH</sub>   | Pull-up<br>Pull-down                               | 25<br>25       | 50<br>50 | 100<br>100    |      |
| Pin capacity (except power supply pin)  |   | C <sub>IO</sub>   | fc = 1MHz  | -              | -        | 10            | pF   |
| Low level output current                | Per pin except PB0, PB1   | I <sub>OL</sub>   | DVDD5 = AVDD5 = 5.0V                               | -              | -        | 2<br>(Note4)  | mA   |
|   | Per pin PB0, PB1  | I <sub>OL4</sub>  | DVDD5 = 5.0V                                       | -              | -        | 12<br>(Note4) |      |
|   | Total of PH2, PH3, PA0 to PA2, PB0, PB1, PC0 to PC2, PJ0 to PJ7 | ΣI <sub>OL1</sub> | DVDD5 = 5.0V                                       | -              | -        | 35<br>(Note5) |      |
|   | Total of PF0 to PF2, PG0 to PG5, PK0 to PK4, PL0 to PL4         | ΣI <sub>OL2</sub> | DVDD5 = 5.0V                                       | -              | -        | 35<br>(Note5) |      |
|   | Total of PD0 to PD6, PE0 to PE4                                 | ΣI <sub>OL3</sub> | AVDD5 = 5.0V                                       | -              | -        | 20<br>(Note5) |      |
| High level output current               | Per pin   | I <sub>OH</sub>   | DVDD5 = AVDD5 = 5.0V                               | -2<br>(Note4)  | -        | -             | mA   |
|   | Total of PH2, PH3, PA0 to PA2, PB0, PB1, PC0 to PC2, PJ0 to PJ7 | ΣI <sub>OH1</sub> | DVDD5 = 5.0V                                       | -35<br>(Note5) | -        | -             |      |
|   | Total of PF0 to PF2, PG0 to PG5, PK0 to PK4, PL0 to PL4         | ΣI <sub>OH2</sub> | DVDD5 = 5.0V                                       | -35<br>(Note5) | -        | -             |      |
|   | Total of PD0 to PD6, PE0 to PE4                                 | ΣI <sub>OH3</sub> | AVDD5 = 5.0V                                       | -20<br>(Note5) | -        | -             |      |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDDA5 = 5.0V, unless otherwise noted.

Note3: Apply same voltage to DVDD5 and AVDD5.

Note4: The sum of the pin currents in each group should not exceed the total current of each group.

Note5: The sum of each group current should not exceed the absolute maximum rating.

DVDD5 = AVDD5 = 2.7 to 4.5V

DVSS = AVSS = 0V

Ta = -40 to 105°C

| Parameter                 |   | Symbol                               | Conditions  | Min        | Typ. | Max        | Unit |
|---------------------------|---|--------------------------------------|---|------------|------|------------|------|
| Power supply voltage      | DVDD5A, DVDD5B, DVDD5C, AVDD5   | VDD                                  | f <sub>osc</sub> = 6 to 24MHz<br>f <sub>sys</sub> = 1 to 120MHz | 2.7        | -    | 4.5        | V    |
| Low level Input voltage   | PA0 to PA2, PC0 to PC2, PF0 to PF2, PG0 to PG5, PH0 to PH3, PJ0 to PJ7, PK0 to PK4, PL0 to PL4, MODE, RESET_N | V <sub>IL1</sub><br>V <sub>IL2</sub> | -   | -0.3       | -    | DVDD5×0.25 | V    |
|                           | PD0 to PD6, PE0 to PE4  | V <sub>IL3</sub>                     | -   |            |      | AVDD5×0.25 |      |
|                           | PB0, PB1  | V <sub>IL4</sub>                     | -   |            |      | DVDD5×0.3  |      |
| High level Input voltage  | PA0 to PA2, PC0 to PC2, PF0 to PF2, PG0 to PG5, PH0 to PH3, PJ0 to PJ7, PK0 to PK4, PL0 to PL4, MODE, RESET_N | V <sub>IH1</sub><br>V <sub>IH2</sub> | -   | DVDD5×0.75 | -    | DVDD5+0.3  | V    |
|                           | PD0 to PD6, PE0 to PE4  | V <sub>IH3</sub>                     | -   | AVDD5×0.75 |      | AVDD5+0.3  |      |
|                           | PB0, PB1  | V <sub>IH4</sub>                     | -   | DVDD5×0.7  |      | 5.8        |      |
| Low level output voltage  | PA0 to PA2, PC0 to PC2, PF0 to PF2, PG0 to PG5, PH2, PH3, PJ0 to PJ7, PK0 to PK4, PL0 to PL4                  | V <sub>OL1</sub><br>V <sub>OL2</sub> | DVDD5 = 2.7V<br>I <sub>OL</sub> = 0.8mA                         | -          | -    | 0.4        | V    |
|                           | PD0 to PD6, PE0 to PE4  | V <sub>OL3</sub>                     | AVDD5 = 2.7V<br>I <sub>OL</sub> = 0.8mA                         | -          | -    | 0.4        |      |
|                           | PB0, PB1  | V <sub>OL4</sub>                     | DVDD5 = 2.7V<br>I <sub>OL</sub> = 4mA                           | -          | -    | 1.0        |      |
| High level output voltage | PA0 to PA2, PB0, PB1, PC0 to PC2, PF0 to PF2, PG0 to PG5, PH2, PH3, PJ0 to PJ7, PK0 to PK4, PL0 to PL4        | V <sub>OH1</sub><br>V <sub>OH2</sub> | DVDD5 = 2.7V<br>I <sub>OH</sub> = -0.8mA                        | DVDD5-0.4  | -    | -          | V    |
|                           | PD0 to PD6, PE0 to PE4  | V <sub>OH3</sub>                     | AVDD5 = 2.7V<br>I <sub>OH</sub> = -0.8mA                        | AVDD5-0.4  | -    | -          |      |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDDA5 = 3.0V, unless otherwise noted.

Note3: Apply same voltage to DVDD5 and AVDD5.

$$DVDD5 = AVDD5 = 2.7 \text{ to } 4.5V$$

$$DVSS = AVSS = 0V$$

$$T_a = -40 \text{ to } 105^\circ C$$

| Parameter                               | Symbol  | Conditions   | Min                    | Typ.           | Max | Unit          |    |
|---|---|--|------------------------|----------------|-----|---------------|----|
| Input leak current                      | $I_{LI}$  | $0.0V \leq V_{IN} \leq DVDD5$<br>$0.0V \leq V_{IN} \leq AVDD5$       | -5                     | $\pm 0.05$     | 5   | $\mu A$       |    |
| Output leak current                     | $I_{LO}$  | $0.2 \leq V_{IN} \leq DVDD5-0.2$<br>$0.2 \leq V_{IN} \leq AVDD5-0.2$ | -10                    | $\pm 0.05$     | 10  |               |    |
| Schmitt trigger Input width             | $V_{TH}$  | $DVDD5 = AVDD5 = 3.0V$   | -                      | 0.5            | -   | V             |    |
| Reset pull-up resistor                  | $R_{RST}$   | -  | 25                     | 100            | 200 | k $\Omega$    |    |
| Programmable pull-up/pull-down resistor | $P_{KH}$  | Pull-up  | 25                     | 100            | 200 |               |    |
|   |   | Pull-down  | 25                     | 100            | 200 |               |    |
| Pin capacity (except power supply pin)  | $C_{IO}$  | $f_c = 1MHz$   | -                      | -              | 10  | pF            |    |
| Low level output current                | Per pin except PB0, PB1   | $I_{OL}$   | $DVDD5 = AVDD5 = 3.0V$ | -              | -   | 1<br>(Note4)  | mA |
|   | Per pin PB0, PB1  | $I_{OL4}$  | $DVDD5 = 3.0V$         | -              | -   | 6<br>(Note4)  |    |
|   | Total of PJ2, PH3, PA0 to PA2, PB0, PB1, PC0 to PC2, PJ0 to PJ7 | $\Sigma I_{OL1}$   | $DVDD5 = 3.0V$         | -              | -   | 18<br>(Note5) |    |
|   | Total of PF0 to PF2, PG0 to PG5, PK0 to PK4, PL0 to PL4         | $\Sigma I_{OL2}$   | $DVDD5 = 3.0V$         | -              | -   | 18<br>(Note5) |    |
|   | Total of PD0 to PD6, PE0 to PE4                                 | $\Sigma I_{OL3}$   | $AVDD5 = 3.0V$         | -              | -   | 10<br>(Note5) |    |
| High level output current               | Per pin   | $I_{OH}$   | $DVDD5 = AVDD5 = 3.0V$ | -1<br>(Note4)  | -   | -             | mA |
|   | Total of PH2, PH3, PA0 to PA2, PB0, PB1, PC0 to PC2, PJ0 to PJ7 | $\Sigma I_{OH1}$   | $DVDD5 = 3.0V$         | -18<br>(Note5) | -   | -             |    |
|   | Total of PF0 to PF2, PG0 to PG5, PK0 to PK4, PL0 to PL4         | $\Sigma I_{OH2}$   | $DVDD5 = 3.0V$         | -18<br>(Note5) | -   | -             |    |
|   | Total of PD0 to PD6, PE0 to PE4                                 | $\Sigma I_{OH3}$   | $AVDD5 = 3.0V$         | -10<br>(Note5) | -   | -             |    |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Typ. value is in  $T_a = 25^\circ C$ ,  $DVDD5 = AVDDA5 = 3.0V$ , unless otherwise noted.

Note3: Apply same voltage to DVDD5 and AVDD5.

Note4: The sum of the pin currents in each group should not exceed the total current of each group.

Note5: The sum of each group current should not exceed the absolute maximum rating.

## 7.3. DC Electrical Characteristics (2/2)

### 7.3.1. Current Consumption

Ta = -40 to 105°C

| Parameter   | Symbol | Conditions                                       | Min | Typ. | Max  | Unit |
|-------------|--------|--|-----|------|------|------|
| NORMAL mode | IDD    | Refer to the Table 7.2 and Table 7.3 for detail. | -   | 25.0 | 35.0 | mA   |
| IDLE mode   |        |  | -   | 1.9  | 8.0  |      |
| STOP1 mode  |        |  | -   | 0.23 | 5.50 | mA   |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDDA5 = 5.0V, unless otherwise noted.

Note3: Apply same voltage to DVDD5 and AVDD5.

Note4: Input pins are fixed. Output pins are opened.

**Table 7.2 IDD Measurement Condition (Pin Setting and Oscillation Circuit)**

|   |   | NORMAL mode                                      | IDLE mode | STOP1 mode |
|---|---|--|-----------|------------|
| Pin setting                               | DVDD5 and AVDD5                           | 5.0V (Typ.), 5.5V (max)                          |           |            |
|   | X1 and X2 pins                            | External high-speed oscillator connected (10MHz) |           |            |
|   | Input pins                                | Fixed  |           |            |
|   | Output pins                               | Opened   |           |            |
| Operation condition (Oscillation circuit) | System clock (fsys)                       | 120MHz   |           | Stopped    |
|   | External high-speed oscillator (EHOSC)    | Oscillation                                      |           | Stopped    |
|   | Internal high-speed oscillator 1 (IHOSC1) | stopped  |           |            |
|   | PLL                                       | Operated   |           | Stopped    |

**Table 7.3 IDD Measurement Condition (CPU and Peripheral Function)**

| Peripheral function | Number of built-in peripherals | NORMAL mode  | IDLE mode | STOP1 mode |
|---------------------|--------------------------------|--|-----------|------------|
| CPU                 | 1                              | Operated<br>(DhystoneVer.2.1)                                    |           | Stopped    |
| DMAC                | 1                              | Operated<br>(Request from UART ch0 TX destination: RAM)          |           | Stopped    |
| ADC                 | 1                              | Operated<br>(Conversion time: 0.73 $\mu$ s, Repeated conversion) |           | Stopped    |
| RAMP                | 1                              | Operated   |           | Stopped    |
| T32A                | 6                              | All channels operated  |           | Stopped    |
| A-PMD               | 1                              | Operated   |           | Stopped    |
| SIWDT               | 1                              | Operated   |           | Stopped    |
| UART                | 4                              | 2channels operated, transmission (transfer speed: 5Mbps)         |           | Stopped    |
| I2C/EI2C            | 1                              |  | Stopped   |            |
| TSPI                | 4                              | 2channels operated, transmission (transfer speed 20MHz)          |           | Stopped    |
| CRC                 | 1                              |  | Stopped   |            |
| LVD                 | 1                              |  | Stopped   |            |
| OFD                 | 1                              |  | Stopped   |            |
| DEBUG               | 1                              |  | Stopped   |            |
| NBDIF               | 1                              |  | Stopped   |            |
| PORT                | -                              | Operated   |           | Stopped    |

## 7.3.2. Analog Current Consumption

Ta= -40 to 105°C

| Parameter  | Symbol            | Conditions   | Min | Typ. | Max  | Unit |
|--|-------------------|--|-----|------|------|------|
| Analog current consumption (Includes VREF current) | I <sub>AVDD</sub> | AVDD5=5.0V (Typ.), 5.5V (Max), AVSS=0V<br>ADC operated | -   | 10.2 | 17.0 | mA   |

## 7.4. Power Supply Voltage Fluctuation

DVSSA = DVSSB = DVSSC = AVSS = 0V  
Ta = -40 to 105°C

| Parameter                     | Symbol            | Conditions                  | Min | Typ. | Max | Unit  |
|-------------------------------|-------------------|-----------------------------|-----|------|-----|-------|
| Power gradient                | V <sub>PON</sub>  | Rising slope at power-on    | 0.3 | -    | 100 | mV/μs |
|                               | V <sub>POFF</sub> | Falling slope at power-off  | -   | -    | 10  |       |
| Power supply fluctuation rate | V <sub>fr</sub>   | 2.7V ≤ DVDD5 = AVDD5 ≤ 5.5V | -50 | -    | 50  |       |

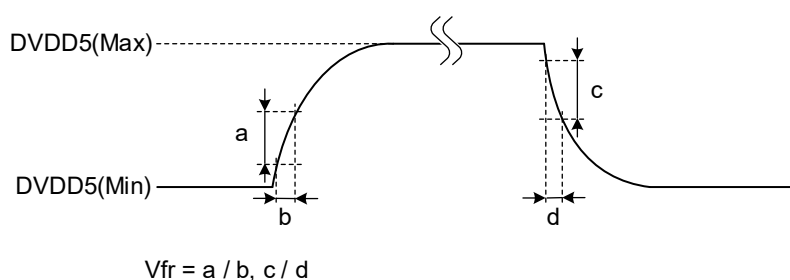


Figure 7.1 Power Supply Fluctuation Rate

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

## 7.5. Characteristics of Internal Processing at RESET

DVSSA = DVSSB = DVSSC = AVSS = 0V  
Ta = -40 to 105°C

| Parameter                              | Symbol             | Conditions  | Min | Typ. | Max  | Unit |
|--|--------------------|---|-----|------|------|------|
| Internal initialized time              | t <sub>IINIT</sub> | Power On  | -   | -    | 1.85 | ms   |
| Internal processing time for Reset     | t <sub>IRST</sub>  | -   | -   | -    | 1.09 |      |
| Waiting time till CPU operation (Note) | t <sub>CPUWT</sub> | Power-on<br>Reset operation by LVD in STOP1 mode<br>Reset operation by RESET_N pin in STOP1 mode  | 12  | -    | 15   | μs   |
|  |                    | Reset operation by LVD in NORMAL or IDLE mode<br>Reset operation by RESET_N pin in NORMAL or IDLE mode<br>Reset operation by SIWDT, OFD, LOCKUP, or SYSRESET in NORMAL or IDLE mode | 104 | -    | 108  |      |

Note: Except reset operation by SIWDT, OFD, LOCKUP, or SYSRESET, when reset factor repeats, t<sub>CPUWT</sub> (Waiting time till CPU running) starts measuring elapse time after releasing this factor.

## 7.6. Characteristics of Power-on Reset

DVSSA = DVSSB = DVSSC = AVSS = 0V  
 Ta = -40 to 105°C

| Parameter               | Symbol             | Conditions      | Min  | Typ. | Max  | Unit |
|-------------------------|--------------------|-----------------|------|------|------|------|
| Detection voltage       | V <sub>PREL</sub>  | Power increases | 2.22 | 2.33 | 2.44 | V    |
|                         | V <sub>PDET</sub>  | Power decreases | 2.17 | 2.28 | 2.39 |      |
| Detection pulse width 1 | T <sub>PDET1</sub> | -               | 200  | -    | -    | μs   |

## 7.7. Characteristics of PORF

DVSSA = DVSSB = DVSSC = AVSS = 0V  
 Ta = -40 to 105°C

| Parameter               | Symbol             | Conditions      | Min  | Typ. | Max  | Unit |
|-------------------------|--------------------|-----------------|------|------|------|------|
| Detection voltage       | V <sub>PORFL</sub> | Power increases | 2.57 | 2.64 | 2.71 | V    |
|                         | V <sub>PORFD</sub> | Power decreases | 2.52 | 2.59 | 2.66 |      |
| Detection pulse width 2 | T <sub>PDET2</sub> | -               | 200  | -    | -    | μs   |

## 7.8. Characteristics of Voltage Detection Circuit

DVDD5 = AVDD5 = 2.7 to 5.5V

DVSS = AVSS = 0V

Ta = -40 to 105°C

| Parameter                     | Symbol                  | Conditions         | Min        | Typ. | Max  | Unit |    |
|-------------------------------|-------------------------|--------------------|------------|------|------|------|----|
| Detection voltage             | V <sub>LVL0</sub>       | Power up           | 2.63       | 2.7  | 2.77 | V    |    |
|                               |                         | Power down         | 2.58       | 2.65 | 2.72 |      |    |
|                               | V <sub>LVL1</sub>       | Power up           | 2.68       | 2.75 | 2.82 | V    |    |
|                               |                         | Power down         | 2.63       | 2.7  | 2.77 |      |    |
|                               | V <sub>LVL2</sub>       | Power up           | 2.78       | 2.85 | 2.92 | V    |    |
|                               |                         | Power down         | 2.73       | 2.8  | 2.87 |      |    |
|                               | V <sub>LVL3</sub>       | Power up           | 2.88       | 2.95 | 3.02 | V    |    |
|                               |                         | Power down         | 2.83       | 2.9  | 2.97 |      |    |
|                               | V <sub>LVL4</sub>       | Power up           | 3.96       | 4.05 | 4.14 | V    |    |
|                               |                         | Power down         | 3.91       | 4.0  | 4.09 |      |    |
|                               | V <sub>LVL5</sub>       | Power up           | 4.16       | 4.25 | 4.34 | V    |    |
|                               |                         | Power down         | 4.11       | 4.2  | 4.29 |      |    |
|                               | V <sub>LVL6</sub>       | Power up           | 4.36       | 4.45 | 4.54 | V    |    |
|                               |                         | Power down         | 4.31       | 4.4  | 4.49 |      |    |
|                               | V <sub>LVL7</sub>       | Power up           | 4.56       | 4.65 | 4.74 | V    |    |
|                               |                         | Power down         | 4.51       | 4.6  | 4.69 |      |    |
|                               | Detection response time | t <sub>VDDT1</sub> | Power down | -    | -    | 100  | μs |
|                               | Release response time   | t <sub>VDDT2</sub> | Power up   | -    | -    | 100  |    |
| Setup time                    | t <sub>LV DEN</sub>     | -                  | -          | -    | 100  |      |    |
| Detection Minimum pulse width | t <sub>LV DPW</sub>     | -                  | 200        | -    | -    |      |    |

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

## 7.9. 12-bit AD Converter Characteristics

### 7.9.1. AD Converter Characteristics

DVDD5 = AVDD5 = 2.7 to 5.5V

DVSS = AVSS = 0V

Ta = -40 to 105°C

| Parameter  | Symbol            | Conditions  | Min             | Typ. | Max   | Unit    |
|--|-------------------|---|-----------------|------|-------|---------|
| Analog reference voltage (+)                                 | VREFH             | -   | 2.7             | -    | 5.5   | V       |
| Analog input voltage   | VAIN              | -   | AVSS<br>(VREFL) | -    | VREFH |         |
| Difference between analog power supply and reference voltage | $\Delta$ VREF     | VREFH $\leq$ AVDD5  | 0               | -    | 0.5   |         |
| Integral nonlinear error (INL)                               | -                 | 4.5V $\leq$ AVDD5 $\leq$ 5.5V<br>4.5V $\leq$ VREFH $\leq$ 5.5V<br>AVSS = VREFL = 0V<br>AIN load resistor = 600 $\Omega$<br>AIN load capacity $\geq$ 0.1 $\mu$ F | -5              | -    | 5     | LSB     |
| Differential nonlinear error (DNL)                           |                   |   | -1              | -    | 4     |         |
| Zero-scale error   |                   |   | -5              | -    | 5     |         |
| Full-scale error   |                   |   | -4.5            | -    | 4     |         |
| Total errors   |                   |   | -8              | -    | 8     |         |
| Integral nonlinear error (INL)                               | -                 | 2.7V $\leq$ AVDD5 < 4.5V<br>2.7V $\leq$ VREFH < 4.5V<br>AVSS = VREFL = 0V<br>AIN load resistor = 600 $\Omega$<br>AIN load capacity $\geq$ 0.1 $\mu$ F           | -5              | -    | 5     | LSB     |
| Differential nonlinear error (DNL)                           |                   |   | -1              | -    | 4     |         |
| Zero-scale error   |                   |   | -5              | -    | 3     |         |
| Full-scale error   |                   |   | -4.5            | -    | 4     |         |
| Total errors   |                   |   | -7              | -    | 6     |         |
| SCLK frequency   | f <sub>SCLK</sub> | 4.5V $\leq$ AVDD5 $\leq$ 5.5V   | 4               | -    | 30    | MHz     |
|  |                   | 2.7V $\leq$ AVDD5 < 4.5V  | 4               | -    | 24    |         |
| Sampling time  | t <sub>smpl</sub> | 4.5V $\leq$ AVDD5 $\leq$ 5.5V   | 0.2             | -    | -     | $\mu$ s |
|  |                   | 2.7V $\leq$ AVDD5 < 4.5V  | 0.33            | -    | -     |         |
| Conversion time  | t <sub>conv</sub> | 4.5V $\leq$ AVDD5 $\leq$ 5.5V   | 0.73            | -    | -     | $\mu$ s |
|  |                   | 2.7V $\leq$ AVDD5 < 4.5V  | 1               | -    | -     |         |
| Stable time  | t <sub>sta</sub>  | After [ADAMOD0]<DACON> =1 is set.   | 3               | -    | -     |         |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDDA5 = 5.0V, unless otherwise noted.

Note3: 1LSB = (VREFH - AVSS (VREFL)) / 4096 [V]

Note4: The ADC characteristics in the above table shows when only ADC operates.

### 7.9.2. Reference Power Supply

DVDD5 = AVDD5 = 2.7 to 5.5V

DVSS = AVSS = 0V

Ta = -40 to 105°C

| Parameter              | Conditions  | Min  | Typ. | Max  | Unit |
|------------------------|-------------|------|------|------|------|
| Reference power supply | ch18 select | 0.99 | -    | 1.21 | V    |

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

## 7.10. AC Electrical Characteristics

The values shown in the "AC Electrical Characteristics" of this chapter do not include clock errors. In practice, the AC characteristics can be affected by both errors (a) and (b).

- (a) Oscillation frequency error of the clock used as fosc
- (b) PLL error (maximum  $\pm 3\%$ )

### 7.10.1. Serial Peripheral Interface (TSPI)

#### 7.10.1.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5 V
- Ta = -40 to 105°C
- Output level: High =  $0.5 \times DVDD5$ , Low =  $0.5 \times DVDD5$
- Input level: High =  $0.5 \times DVDD5$ , Low =  $0.5 \times DVDD5$
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

## 7.10.1.2. AC Electrical Characteristics

"T" indicates an operation clock cycle of the TSPI. This operation clock has the same cycle of the system clock (fsys). This cycle depends on the clock gear setting.

The <RXDLY> is the setting value of  $[TSPIxCR2]/<RXDLY[2:0]>$  plus 1.

- (1) SIO mode controller

DVDD5 = AVDD5 = 4.5 to 5.5V

| Parameter   | Symbol             | Min                         | Max | Unit |
|---|--------------------|-----------------------------|-----|------|
| TSPIxSCK output frequency                             | f <sub>CYC</sub>   | -                           | 20  | MHz  |
| TSPIxSCK output cycle                                 | t <sub>CYC</sub>   | 50                          | -   | ns   |
| TSPIxSCK low level output pulse width                 | t <sub>WL</sub>    | (t <sub>CYC</sub> / 2) - 13 | -   |      |
| TSPIxSCK high level output pulse width                | t <sub>WH</sub>    | (t <sub>CYC</sub> / 2) - 13 | -   |      |
| TSPIxRXD input<br>← TSPIxSCK rising/falling time      | t <sub>DSU</sub>   | 35-<RXDLY>×T                | -   |      |
| TSPIxSCK rising/falling time<br>→ TSPIxRXD hold time  | t <sub>DHD</sub>   | <RXDLY>×T-5                 | -   |      |
| TSPIxSCK rising/falling time<br>→ TSPIxTXD hold time  | t <sub>ODLY1</sub> | -18                         | -   |      |
| TSPIxSCK rising/falling time<br>→ TSPIxTXD delay time | t <sub>ODLY2</sub> | -                           | 16  |      |

DVDD5 = AVDD5 = 2.7 to 4.5V

| Parameter   | Symbol             | Min                         | Max | Unit |
|---|--------------------|-----------------------------|-----|------|
| TSPIxSCK output frequency                             | f <sub>CYC</sub>   | -                           | 20  | MHz  |
| TSPIxSCK output cycle                                 | t <sub>CYC</sub>   | 50                          | -   | ns   |
| TSPIxSCK low level output pulse width                 | t <sub>WL</sub>    | (t <sub>CYC</sub> / 2) - 16 | -   |      |
| TSPIxSCK high level output pulse width                | t <sub>WH</sub>    | (t <sub>CYC</sub> / 2) - 16 | -   |      |
| TSPIxRXD input<br>← TSPIxSCK rising/falling time      | t <sub>DSU</sub>   | 45-<RXDLY>×T                | -   |      |
| TSPIxSCK rising/falling time<br>→ TSPIxRXD hold time  | t <sub>DHD</sub>   | <RXDLY>×T-5                 | -   |      |
| TSPIxSCK rising/falling time<br>→ TSPIxTXD hold time  | t <sub>ODLY1</sub> | -18                         | -   |      |
| TSPIxSCK rising/falling time<br>→ TSPIxTXD delay time | t <sub>ODLY2</sub> | -                           | 16  |      |

(2) SIO mode target

DVDD5 = AVDD5 = 4.5 to 5.5V

| Parameter   | Symbol             | Min | Max | Unit |
|---|--------------------|-----|-----|------|
| TSPIxSCK Input frequency                              | f <sub>CYC</sub>   | -   | 10  | MHz  |
| TSPIxSCK Input cycle                                  | t <sub>CYC</sub>   | 100 | -   | ns   |
| TSPIxSCK low level Input pulse width                  | t <sub>WL</sub>    | 37  | -   |      |
| TSPIxSCK high level Input pulse width                 | t <sub>WH</sub>    | 37  | -   |      |
| TSPIxRXD Input<br>← TSPIxSCK rising/falling time      | t <sub>DSU</sub>   | 7   | -   |      |
| TSPIxSCK rising/falling edge<br>→ TSPIxRXD hold time  | t <sub>DHD</sub>   | 10  | -   |      |
| TSPIxSCK rising/falling edge<br>→ TSPIxTXD hold time  | t <sub>ODLY1</sub> | 0   | -   |      |
| TSPIxSCK rising/falling edge<br>→ TSPIxTXD delay time | t <sub>ODLY2</sub> | -   | 36  |      |

DVDD5 = AVDD5 = 2.7 to 4.5V

| Parameter   | Symbol             | Min | Max | Unit |
|---|--------------------|-----|-----|------|
| TSPIxSCK Input frequency                              | f <sub>CYC</sub>   | -   | 10  | MHz  |
| TSPIxSCK Input cycle                                  | t <sub>CYC</sub>   | 100 | -   | ns   |
| TSPIxSCK low level Input pulse width                  | t <sub>WL</sub>    | 37  | -   |      |
| TSPIxSCK high level Input pulse width                 | t <sub>WH</sub>    | 37  | -   |      |
| TSPIxRXD Input<br>← TSPIxSCK rising/falling time      | t <sub>DSU</sub>   | 7   | -   |      |
| TSPIxSCK rising/falling edge<br>→ TSPIxRXD hold time  | t <sub>DHD</sub>   | 10  | -   |      |
| TSPIxSCK rising/falling edge<br>→ TSPIxTXD hold time  | t <sub>ODLY1</sub> | 0   | -   |      |
| TSPIxSCK rising/falling edge<br>→ TSPIxTXD delay time | t <sub>ODLY2</sub> | -   | 55  |      |

(1) 1st clock edge sampling (Controller)

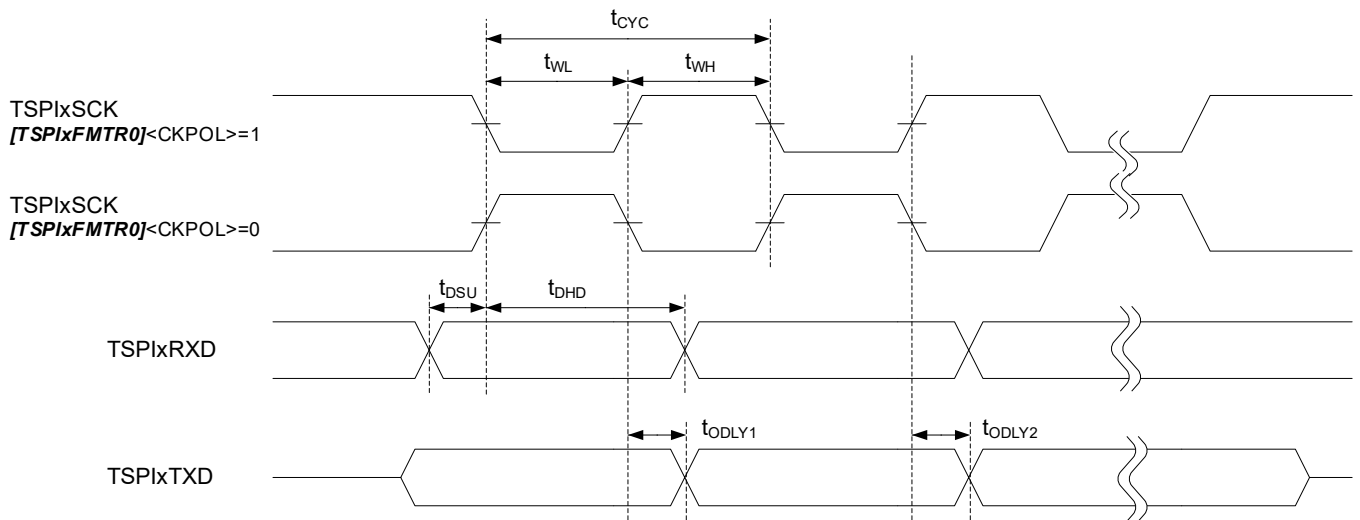


Figure 7.2 1st Clock Edge Sampling (Controller)

(2) 2nd clock edge sampling (Controller)

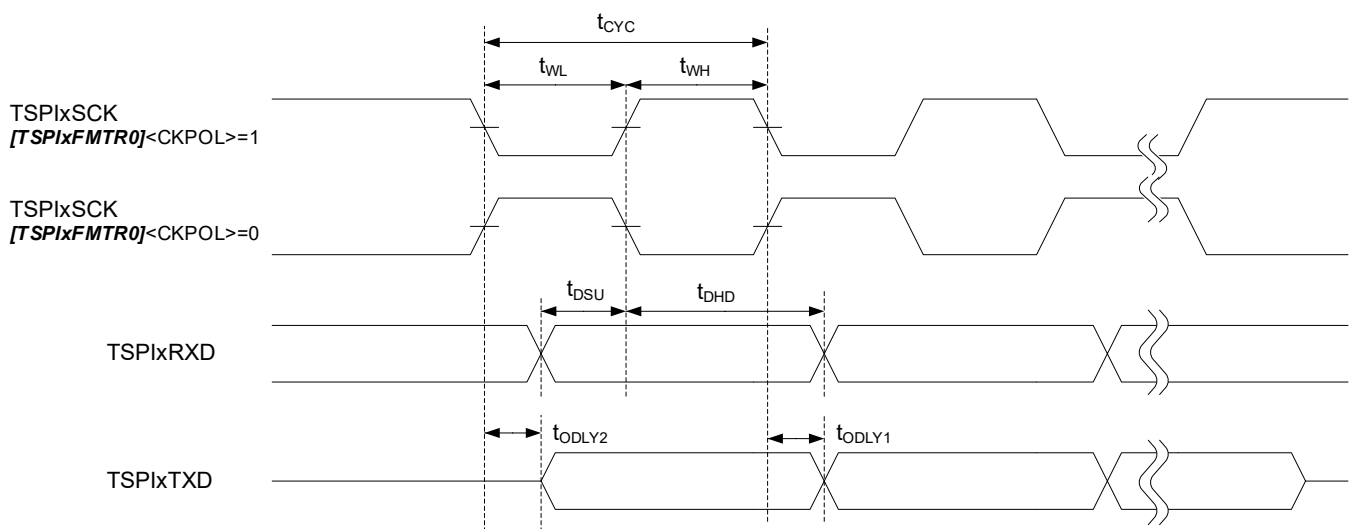


Figure 7.3 2nd Clock Edge Sampling (Controller)

(3) 1st clock edge sampling (Target)

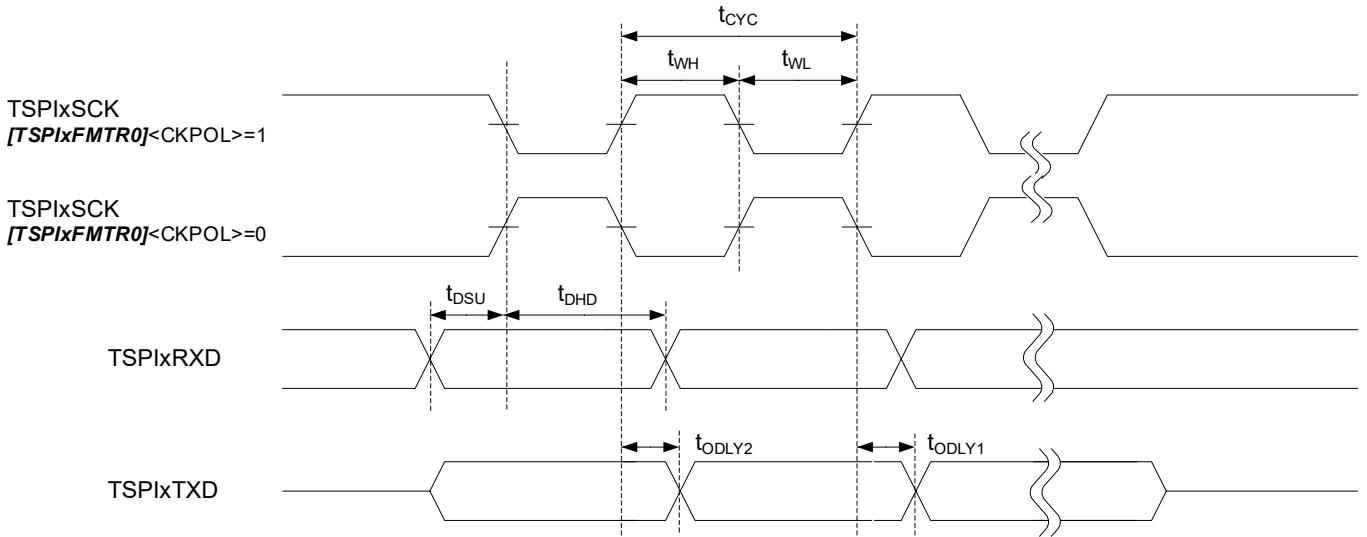


Figure 7.4 1st Clock Edge Sampling (Target)

(4) 2nd clock edge sampling (Target)

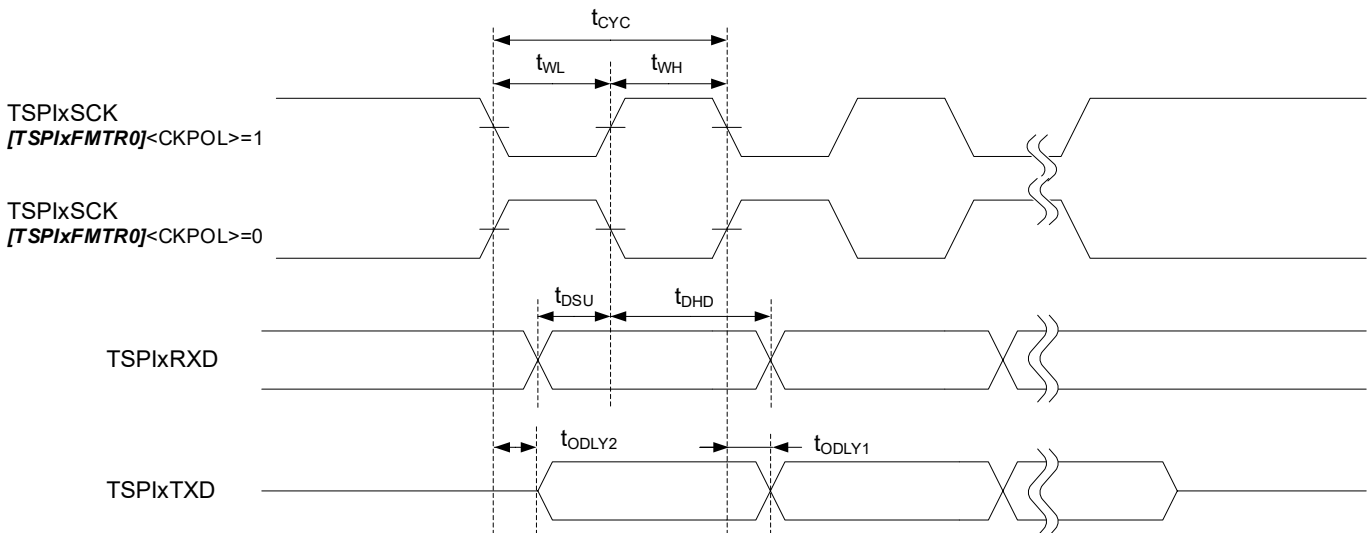


Figure 7.5 2nd Clock Edge Sampling (Target)

## 7.10.2. I<sup>2</sup>C Interface (I2C)

### 7.10.2.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5 V
- Ta = -40 to 105°C
- Output level: Low = 0.4V
- Input level: High = 0.7 × DVDD5, Low = 0.3 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

### 7.10.2.2. AC Electrical Characteristics

| Parameter  | Symbol              | Standard mode       |             | Fast mode |             | Unit |   |
|--|---------------------|---------------------|-------------|-----------|-------------|------|---|
|  |                     | Min                 | Max         | Min       | Max         |      |   |
| SCL clock frequency  | f <sub>SCL</sub>    | 0                   | 100         | 0         | 400         | kHz  |   |
| Start condition hold time  | t <sub>HD;STA</sub> | 4.0                 | -           | 0.6       | -           |      |   |
| SCL clock Low width (Input) (Note1)                              | t <sub>LOW</sub>    | 4.7                 | -           | 1.3       | -           | μs   |   |
| SCL clock High width (Input) (Note1)                             | t <sub>HIGH</sub>   | 4.0                 | -           | 0.6       | -           |      |   |
| Re-start condition setup time                                    | <SREN>=0            | t <sub>SU;STA</sub> | 4.7 (Note3) | -         | 0.6 (Note3) |      | - |
|  | <SREN>=1            | t <sub>SU;STA</sub> | 4.7 (Note3) | -         | 0.6         |      | - |
| Data hold time (Input) (Note2)                                   | t <sub>HD;DAT</sub> | 0                   | -           | 0         | -           | ns   |   |
| Data setup time  | t <sub>SU;DAT</sub> | 250                 | -           | 100       | -           |      |   |
| Stop condition setup time  | t <sub>SU;STO</sub> | 4.0                 | -           | 0.6       | -           | μs   |   |
| Bus free time between stop condition and start condition (Note3) | t <sub>BUF</sub>    | 4.7                 | -           | 1.3       | -           |      |   |

Note1: On I<sup>2</sup>C bus standard, the maximum speed of standard mode/fast mode is 100kHz/400 kHz, respectively. For the frequency setting of the internal SCL clock, refer to the calculation formula in chapter 3.3.2 of "I2C Interface" in reference manual .

Note2: On I<sup>2</sup>C bus standard, it is described that a data internal hold time should be set at least 300 ns to avoid unstable condition on the falling of the SCL when the SDA is input; however, this precaution is not supported in this MCU. Also, the edge slope control function for the SCL is not available. Therefore, when the customer designs the MCU, make sure to follow the data hold time (input) in the table above. Note that t<sub>r</sub>/t<sub>f</sub> on the SCL/SDA should be included in the data hold time.

Note3: To keep the time by software.

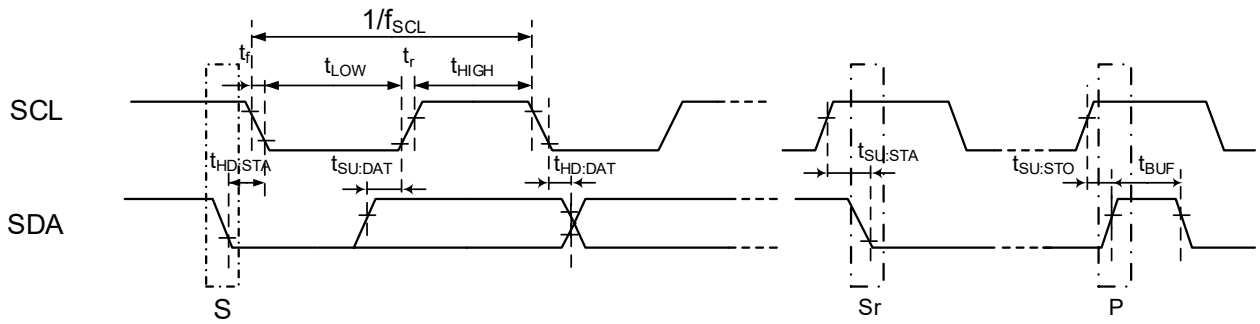


Figure 7.6 AC Timing of I2C

## 7.10.3. I<sup>2</sup>C Interface Version A (EI2C)

### 7.10.3.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5= 2.7 to 5.5 V
- Ta = -40 to 105°C
- Output level: Low = 0.4V
- Input level: High = 0.7 × DVDD5, Low = 0.3 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

### 7.10.3.2. AC Electrical Characteristics

| Parameter  | Symbol              | Standard mode |     | Fast mode |     | Fast mode plus |      | Unit |
|--|---------------------|---------------|-----|-----------|-----|----------------|------|------|
|  |                     | Min           | Max | Min       | Max | Min            | Max  |      |
| SCL clock frequency  | f <sub>SCL</sub>    | 0             | 100 | 0         | 400 | 0              | 1000 | kHz  |
| Start condition hold time  | t <sub>HD;STA</sub> | 4.0           | -   | 0.6       | -   | 0.26           | -    | μs   |
| SCL clock Low width (Input) (Note1)                              | t <sub>LOW</sub>    | 4.7           | -   | 1.3       | -   | 0.5            | -    |      |
| SCL clock High width (Input) (Note1)                             | t <sub>HIGH</sub>   | 4.0           | -   | 0.6       | -   | 0.26           | -    |      |
| Re-start condition setup time                                    | t <sub>SU;STA</sub> | 4.7           | -   | 0.6       | -   | 0.26           | -    |      |
| Data hold time (Input) (Note2)                                   | t <sub>HD;DAT</sub> | 0             | -   | 0         | -   | 0              | -    |      |
| Data setup time  | t <sub>SU;DAT</sub> | 250           | -   | 100       | -   | 50             | -    | ns   |
| Stop condition setup time  | t <sub>SU;STO</sub> | 4.0           | -   | 0.6       | -   | 0.26           | -    | μs   |
| Bus free time between stop condition and start condition (Note3) | t <sub>BUF</sub>    | 4.7           | -   | 1.3       | -   | 0.5            | -    |      |

Note1: On I<sup>2</sup>C bus standard, the maximum speed of standard mode/fast mode/fast mode plus is 100kHz/400 kHz/1000kHz, respectively. For the frequency setting of the internal SCL clock, refer to the calculation formula in chapter 3.3.1 of "I<sup>2</sup>C Interface Version A" in reference manual.

Note2: On I<sup>2</sup>C bus standard, it is described that a data internal hold time should be set at least 300 ns to avoid unstable condition on the falling of the SCL when the SDA is input; however, this precaution is not supported in this MCU. Also, the edge slope control function for the SCL is not available. Therefore, when the customer designs the MCU, make sure to follow the data hold time (input) in the table above. Note that t<sub>r</sub>/t<sub>f</sub> on the SCL/SDA should be included in the data hold time.

Note3: To keep the time by software.

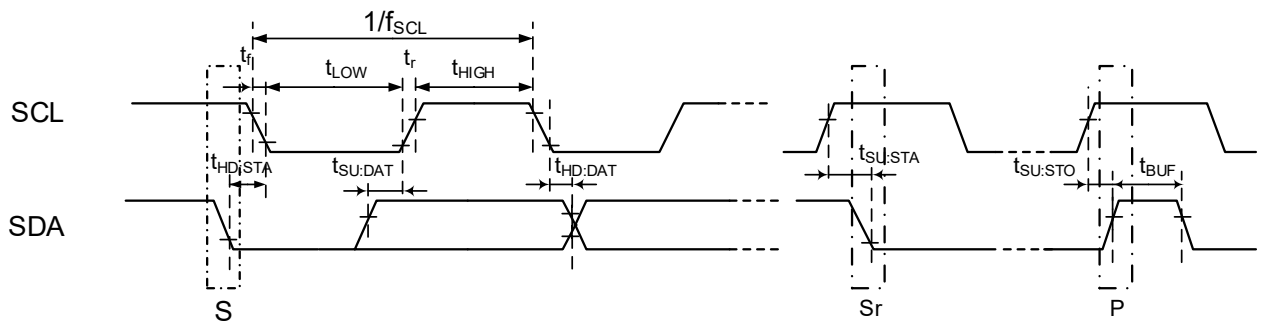


Figure 7.7 AC timing of I2C

## 7.10.4. 32-bit Timer Event Counter (T32A)

This section describes AC characteristics of T32AxINA0/A1, T32AxINB0/B1, and T32AxINC0/C1.

### 7.10.4.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5 V
- Ta = -40 to 105°C
- Input level: High = 0.5 × DVDD5, Low = 0.5 × DVDD5

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

### 7.10.4.2. AC Electrical Characteristics

"T" in the table below indicates the operation clock cycle of the T32A. The operation clock of the T32A is the same cycle as the  $\Phi T0$  clock. This cycle is depending on the prescaler clock setting.

(1) Operation other than the pulse count

| Parameter              | Symbol            | Min     | Max | Unit |
|------------------------|-------------------|---------|-----|------|
| Low level pulse width  | t <sub>VCKL</sub> | 2T + 20 | -   | ns   |
| High level pulse width | t <sub>VCKH</sub> | 2T + 20 | -   |      |

(2) Operation at the pulse count

| Parameter              | Symbol            | Min             | Max | Unit |
|------------------------|-------------------|-----------------|-----|------|
| Pulse cycle            | t <sub>DCYC</sub> | 1000            | -   | ns   |
| Low level pulse width  | t <sub>PWL</sub>  | 500             | -   |      |
| High level pulse width | t <sub>PWH</sub>  | 500             | -   |      |
| Input setup            | t <sub>ABS</sub>  | (NF+1) × T + 20 | -   |      |
| Input hold             | t <sub>ABH</sub>  | (NF+1) × T + 20 | -   |      |

The value of NF in above table depends on the  $[T32AxPLSCR]<NF[1:0]>$  setting as follows.

| $[T32AxPLSCR]<NF[1:0]>$ | NF Value of Formula |
|-------------------------|---------------------|
| 00                      | 0                   |
| 01                      | 2                   |
| 10                      | 4                   |
| 11                      | 8                   |

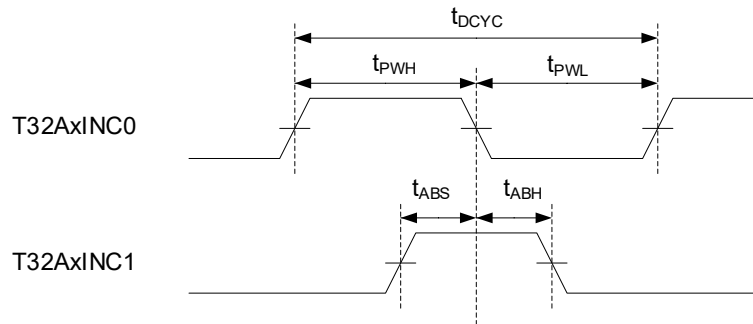


Figure 7.8 Count Pulse Input

## 7.10.5. External Interrupt

### 7.10.5.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5 V
- Ta = -40 to 105°C
- Input level: High =  $0.5 \times DVDD5$ , Low =  $0.5 \times DVDD5$

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

### 7.10.5.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

(1) NORMAL and IDLE mode

| Parameter              | Symbol       | Min     | Max | Unit |
|------------------------|--------------|---------|-----|------|
| Low level pulse width  | $t_{INTAL1}$ | T + 100 | -   | ns   |
| High level pulse width | $t_{INTAH1}$ | T + 100 | -   |      |

(2) STOP1 mode

| Parameter              | Symbol       | Min | Max | Unit |
|------------------------|--------------|-----|-----|------|
| Low level pulse width  | $t_{INTCL2}$ | 125 | -   | ns   |
| High level pulse width | $t_{INTCH2}$ | 125 | -   |      |

## 7.10.6. Trigger Selection Circuit (TRGSEL)

### 7.10.6.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5V
- Ta = -40 to 105°C
- Input level: High =  $0.5 \times DVDD5$ , Low =  $0.5 \times DVDD5$

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

### 7.10.6.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

| Parameter              | Symbol           | Min     | Max | Unit |
|------------------------|------------------|---------|-----|------|
| Low level pulse width  | t <sub>ADL</sub> | 2T + 20 | -   | ns   |
| High level pulse width | t <sub>ADH</sub> | 2T + 20 | -   |      |

## 7.10.7. Debug Communication

### 7.10.7.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5V
- Ta = -40 to 105°C
- Output level: High = 0.5 × DVDD5, Low = 0.5 × DVDD5
- Input level: High = 0.5 × DVDD5, Low = 0.5 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

### 7.10.7.2. SWD Interface

DVDD5 = AVDD5 = 4.5 to 5.5V

| Parameter  | Symbol           | Min | Max | Unit |
|--|------------------|-----|-----|------|
| CLK cycle  | t <sub>dck</sub> | 100 | -   | ns   |
| Output data hold from on the rising edge of CLK  | t <sub>d1</sub>  | 4   | -   |      |
| Output data valid from on the rising edge of CLK | t <sub>d2</sub>  | -   | 31  |      |
| Rising edge of CLK from input data valid         | t <sub>ds</sub>  | 20  | -   |      |
| Input data hold from on the rising edge of CLK   | t <sub>dh</sub>  | 15  | -   |      |

DVDD5 = AVDD5 = 2.7 to 4.5V

| Parameter  | Symbol           | Min | Max | Unit |
|--|------------------|-----|-----|------|
| CLK cycle  | t <sub>dck</sub> | 100 | -   | ns   |
| Output data hold from on the rising edge of CLK  | t <sub>d1</sub>  | 4   | -   |      |
| Output data valid from on the rising edge of CLK | t <sub>d2</sub>  | -   | 45  |      |
| Rising edge of CLK from input data valid         | t <sub>ds</sub>  | 20  | -   |      |
| Input data hold from on the rising edge of CLK   | t <sub>dh</sub>  | 15  | -   |      |

### 7.10.7.3. JTAG Interface

DVDD5 = AVDD5 = 4.5 to 5.5V

| Parameter   | Symbol    | Min  | Max | Unit |
|---|-----------|------|-----|------|
| CLK cycle   | $t_{dck}$ | 83.3 | -   | ns   |
| Output data hold from on the falling edge of CLK  | $t_{d3}$  | 4    | -   |      |
| Output data valid from on the falling edge of CLK | $t_{d4}$  | -    | 33  |      |
| Rising edge of CLK from input data valid          | $t_{ds}$  | 20   | -   |      |
| Input data hold from on the rising edge of CLK    | $t_{dh}$  | 15   | -   |      |

DVDD5 = AVDD5 = 2.7 to 4.5V

| Parameter   | Symbol    | Min  | Max | Unit |
|---|-----------|------|-----|------|
| CLK cycle   | $t_{dck}$ | 83.3 | -   | ns   |
| Output data hold from on the falling edge of CLK  | $t_{d3}$  | 4    | -   |      |
| Output data valid from on the falling edge of CLK | $t_{d4}$  | -    | 45  |      |
| Rising edge of CLK from input data valid          | $t_{ds}$  | 20   | -   |      |
| Input data hold from on the rising edge of CLK    | $t_{dh}$  | 15   | -   |      |

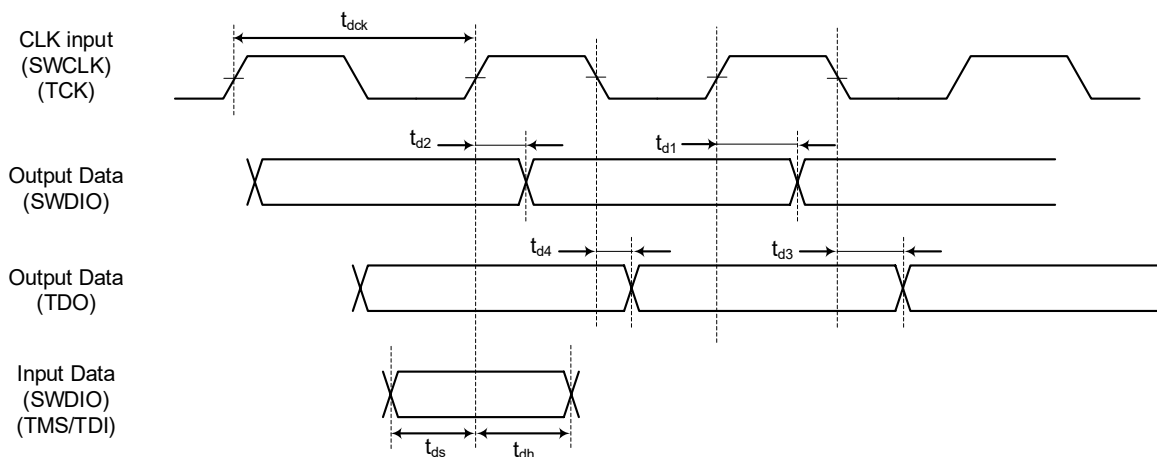


Figure 7.9 JTAG/SWD Signal Waveform

## 7.10.7.4. ETM Interface

DVDD5 = AVDD5 = 4.5 to 5.5V

| Parameter  | Symbol       | Min  | Max | Unit |
|--|--------------|------|-----|------|
| TRACECLK cycle                                       | $t_{clk}$    | 33.3 | -   | ns   |
| Data valid from rising on TRACECLK                   | $t_{setupr}$ | 2    | -   |      |
| TRACEDATA hold from on the rising edge of TRACECLK   | $t_{holdr}$  | 1    | -   |      |
| TRACEDATA valid from on the falling edge of TRACECLK | $t_{setupf}$ | 2    | -   |      |
| TRACEDATA hold from on the falling edge of TRACECLK  | $t_{holdf}$  | 1    | -   |      |

DVDD5 = AVDD5 = 2.7 to 4.5V

| Parameter  | Symbol       | Min  | Max | Unit |
|--|--------------|------|-----|------|
| TRACECLK cycle                                       | $t_{clk}$    | 33.3 | -   | ns   |
| Data valid from rising on TRACECLK                   | $t_{setupr}$ | 2    | -   |      |
| TRACEDATA hold from on the rising edge of TRACECLK   | $t_{holdr}$  | 1    | -   |      |
| TRACEDATA valid from on the falling edge of TRACECLK | $t_{setupf}$ | 2    | -   |      |
| TRACEDATA hold from on the falling edge of TRACECLK  | $t_{holdf}$  | 1    | -   |      |

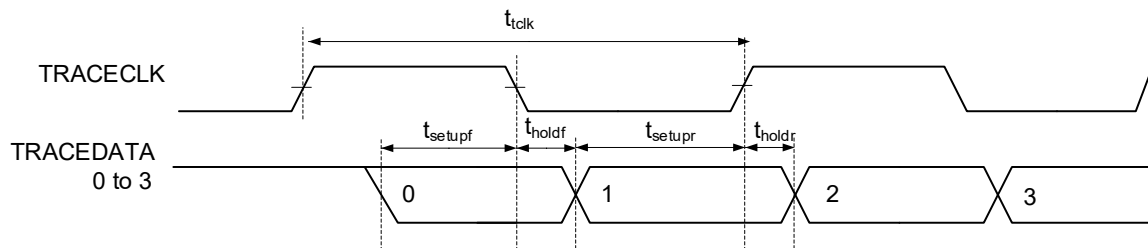


Figure 7.10 Trace Signal Waveform

## 7.10.8. NBD Interface

### 7.10.8.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5V
- Ta = -40 to 105°C
- Output level: High = 0.5 × DVDD5, Low = 0.5 × DVDD5
- Input level: High = 0.5 × DVDD5, Low = 0.5 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

### 7.10.8.2. AC Electrical Characteristics

| Parameter                    | Symbol      | Min | Max              | Unit |
|------------------------------|-------------|-----|------------------|------|
| NBDCLK cycle                 | $t_{NDCYC}$ | 80  | -                | ns   |
| NBDCLK low level pulse width | $t_{NDL}$   | 35  | -                |      |
| NBDDATA output delay time    | $t_{NDD}$   | -   | $t_{NDCYC} - 20$ |      |
| NBDDATA output hold time     | $t_{NDHD}$  | 5   | -                |      |
| NBDDATA setup time           | $t_{NDS}$   | 20  | -                |      |
| NBDDATA hold time            | $t_{NDH}$   | 5   | -                |      |
| NBDSYNC setup time           | $t_{NDSYS}$ | 20  | -                |      |
| NBDSYNC output hold time     | $t_{NDSYH}$ | 5   | -                |      |

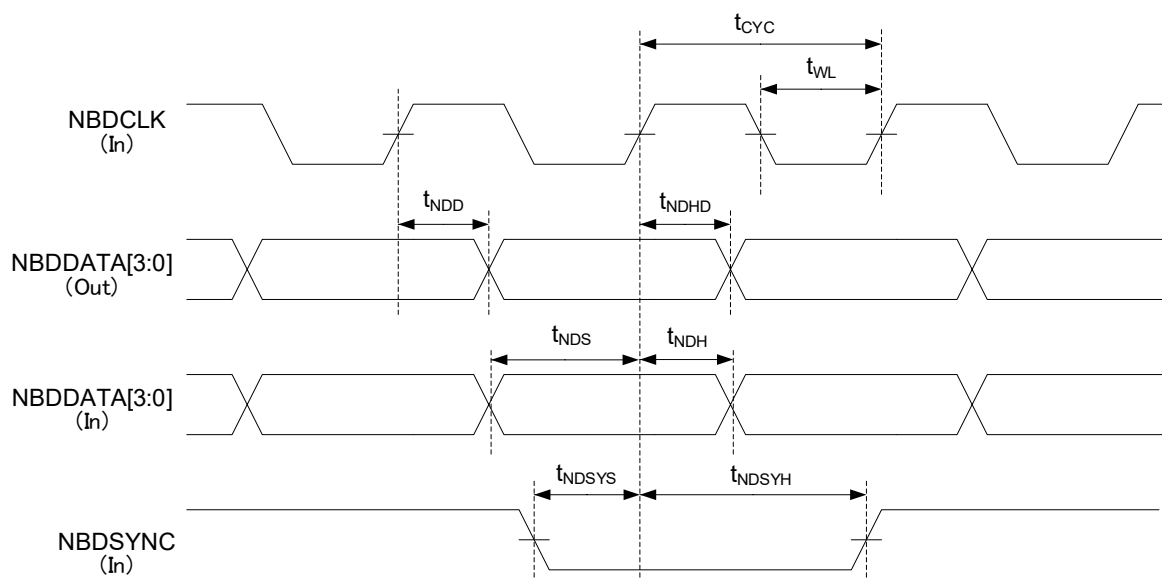


Figure 7.11 AC Timing of NBDIF

## 7.10.9. SCOUT Pin

### 7.10.9.1. AC Measurement Conditions

The AC characteristics are the result of the measurement conditions below:

- DVDD5 = AVDD5= 2.7 to 5.5V
- Ta = -40 to 105°C
- Output level: High =  $0.5 \times DVDD5$ , Low =  $0.5 \times DVDD5$
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

### 7.10.9.2. AC Electrical Characteristics

"T" in the table indicates the cycle of the SCOUT output waveform.

DVDD5 = AVDD5 = 4.5 to 5.5V

| Parameter              | Symbol           | Min                 | Max | Unit |
|------------------------|------------------|---------------------|-----|------|
| Low level pulse width  | t <sub>sCL</sub> | $0.5 \times T - 10$ | -   | ns   |
| High level pulse width | t <sub>sCH</sub> | $0.5 \times T - 10$ | -   |      |

DVDD5 = AVDD5 = 2.7 to 4.5V

| Parameter              | Symbol           | Min                 | Max | Unit |
|------------------------|------------------|---------------------|-----|------|
| Low level pulse width  | t <sub>sCL</sub> | $0.5 \times T - 12$ | -   | ns   |
| High level pulse width | t <sub>sCH</sub> | $0.5 \times T - 12$ | -   |      |

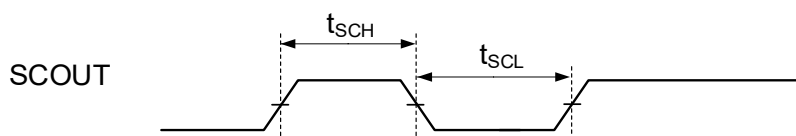


Figure 7.12 SCOUT Waveform Output

## 7.10.10. External Clock Input

### 7.10.10.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5V
- Ta = -40 to 105°C
- Input level: High =  $0.75 \times DVDD5$ , Low =  $0.25 \times DVDD5$

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

### 7.10.10.2. AC Electrical Characteristics

| Parameter                         | Symbol        | Min | Typ. | Max | Unit |
|-----------------------------------|---------------|-----|------|-----|------|
| Clock frequency ( $1/t_{echin}$ ) | $f_{EHCLKIN}$ | 6   | -    | 24  | MHz  |
| Clock duty                        | -             | 45  | -    | 55  | %    |
| Clock rising time                 | $t_r$         | -   | -    | 10  | ns   |
| Clock falling time                | $t_f$         | -   | -    | 10  | ns   |

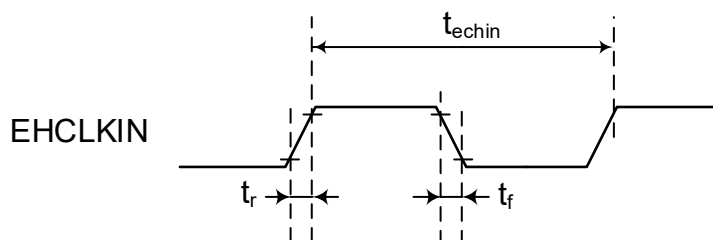


Figure 7.13 External Clock Input Waveform

## 7.11. Noise Filter (Analog) Characteristics

DVDD5 = AVDD5 = 2.7 to 5.5V  
 Ta = -40 to 105°C

| Parameter          | Condition | Min | Typ. | Max | Unit |
|--------------------|-----------|-----|------|-----|------|
| Noise cancel width | -         | 15  | 30   | 60  | ns   |

## 7.12. Flash Memory Characteristics

### 7.12.1. Code Flash

DVDD5 = AVDD5 = 2.7 to 5.5V  
 Ta = -40 to 105°C

| Parameter           | Condition                   | Min  | Typ. | Max     | Unit   |
|---------------------|-----------------------------|------|------|---------|--------|
| Rewrite frequencies | -                           | -    | -    | 100,000 | cycles |
| Programming time    | Programming time for a word | -    | 22.6 | -       | μs     |
| Erase time          | Page erase time             | 2.1  | -    | 8.4     | ms     |
|                     | Block erase time            | 16.8 | -    | 67.1    |        |
|                     | Area erase time (Note2)     | -    | 9.1  | -       |        |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: In case that flash memory has no block with effective protection.

### 7.12.2. Chip Erase

DVDD5 = AVDD5 = 2.7 to 5.5V  
 Ta = -40 to 105°C

| Parameter       | Condition  | Min  | Typ. | Max  | Unit |
|-----------------|--|------|------|------|------|
| Chip erase time | Erasing of code flash, protect bits (Code), and security bit | 13.3 | -    | 25.9 | ms   |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Chip erase time when flash memory has no block with effective protection.

## 7.13. Regulator Characteristics

DVDD5 = AVDD5 = 2.7 to 5.5V  
 Ta = -40 to 105°C

| Parameter                        | Condition | Min | Typ. | Max  | Unit |
|----------------------------------|-----------|-----|------|------|------|
| Capacitance of REGOUT2 capacitor | -         | 0.8 | 4.7  | 5.64 | μF   |
| Capacitance of REGOUT1 capacitor |           | 0.8 | 4.7  | 5.64 |      |

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

## 7.14. Oscillation Circuit Characteristics

### 7.14.1. Internal Oscillator

DVDD5 = AVDD5 = 2.7 to 5.5V

Ta = -40 to 105°C

| Parameter                                      | Symbol              | Condition | Min | Typ. | Max  | Unit |
|--|---------------------|-----------|-----|------|------|------|
| Internal Oscillator 1<br>Oscillation frequency | f <sub>IHOSC1</sub> | -         | 9.9 | 10   | 10.1 | MHz  |

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

DVDD5 = AVDD5 = 2.7 to 5.5V

Ta = -40 to 105°C

| Parameter                                      | Symbol              | Condition | Min | Typ. | Max | Unit |
|--|---------------------|-----------|-----|------|-----|------|
| Internal Oscillator 2<br>Oscillation frequency | f <sub>IHOSC2</sub> | -         | 9   | 10   | 11  | MHz  |

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

### 7.14.2. External Oscillator

DVDD5 = AVDD5 = 2.7 to 5.5V

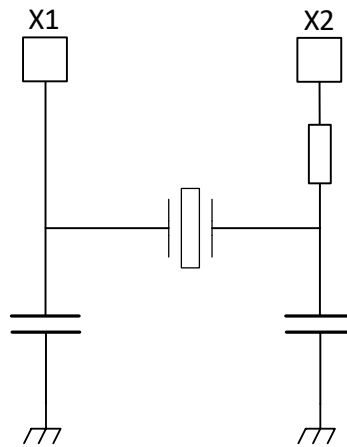
Ta = -40 to 105°C

| Parameter             | Symbol             | Condition | Min | Typ. | Max | Unit |
|-----------------------|--------------------|-----------|-----|------|-----|------|
| Oscillation frequency | f <sub>EHOSC</sub> | -         | 6   | -    | 24  | MHz  |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Please contact the oscillator vendor, regarding the matching data of the device and the oscillator.

### 7.14.3. Oscillation Circuit



**Figure 7.14 Example of Oscillation Circuit**

To obtain a stable oscillation, load capacity and the position of the oscillator must be configured properly. Since these factors are strongly affected by substrate patterns, please evaluate oscillation stability using the substrate you use.

This product has been evaluated by the oscillator vendor below. Please refer this information when selecting external parts.

### 7.14.4. Ceramic Oscillator

This product has been evaluated by the ceramic oscillator by Murata Manufacturing Co., Ltd.

Please refer to the company's website for details.

### 7.14.5. Crystal Oscillator

This product has been evaluated by the crystal unit by KYOCERA Corporation.

Please refer to the company's website for details.

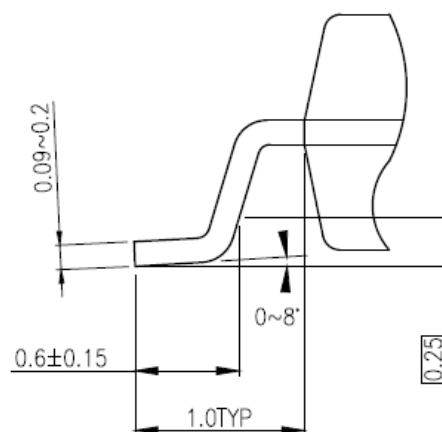
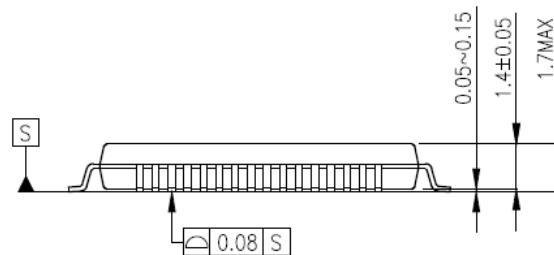
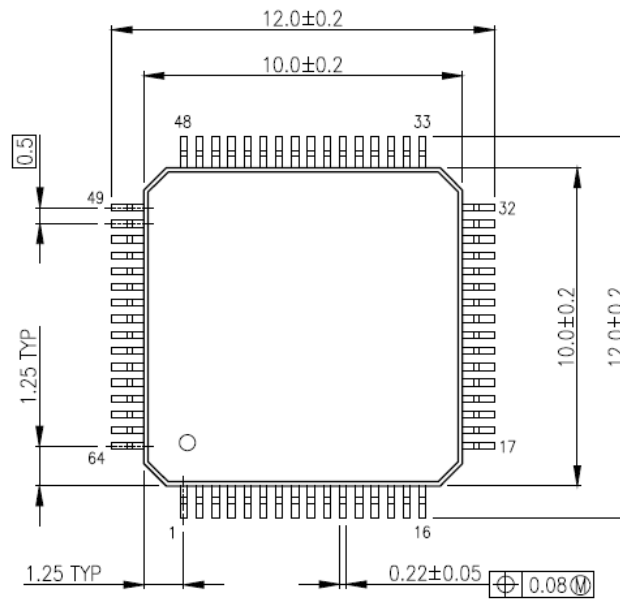
### 7.14.6. Precautions for Designing Printed Circuit Board

Be sure to design printed circuit board patterns that connect a crystal unit with other oscillation elements so that the length of such patterns become shortest possible to prevent deterioration of characteristics due to stray capacitances and wiring inductance. For multi-layer circuit boards, it is important not to wire the ground and other signal patterns right beneath the oscillation circuit. For more information, please refer to the URL of the oscillator vendor.

## 8. Package Dimensions

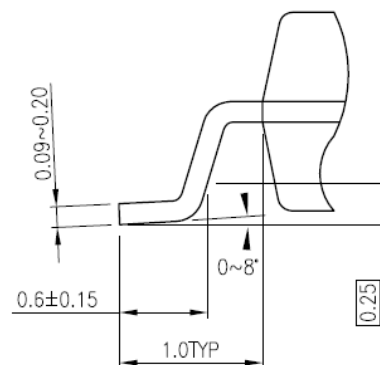
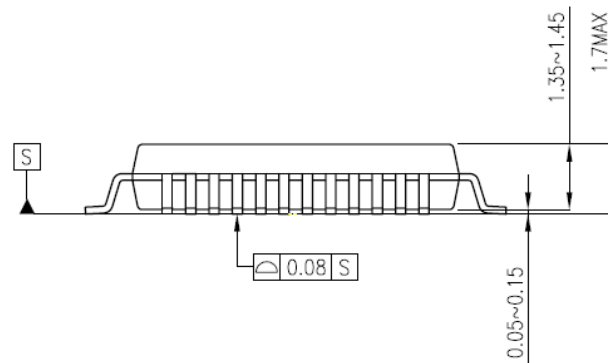
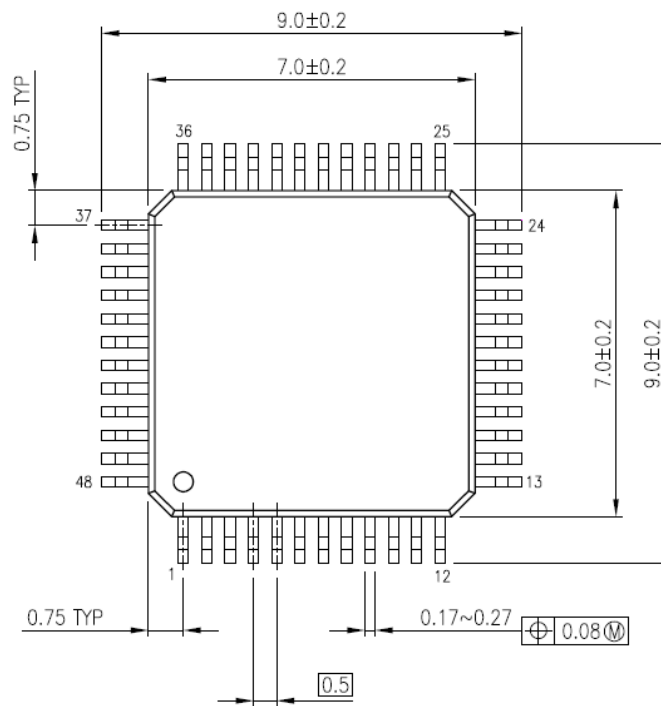
### 8.1. P-LQFP64-1010-0.50-003

Unit: mm



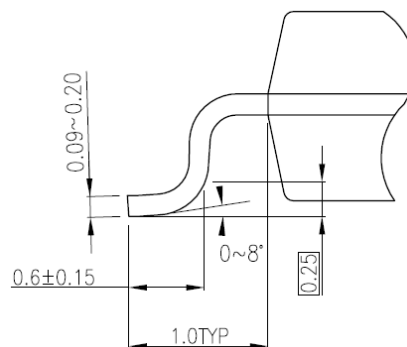
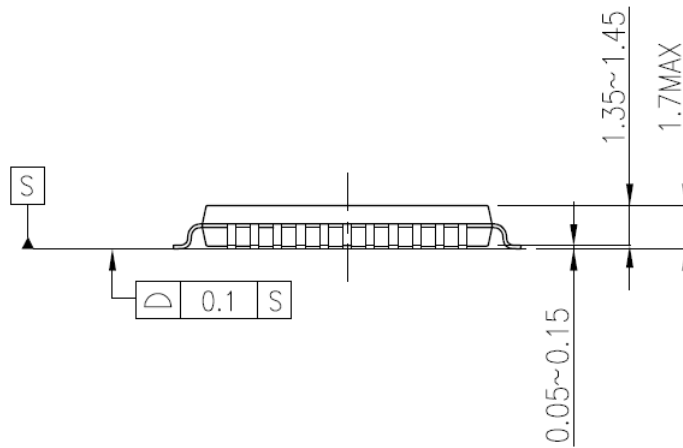
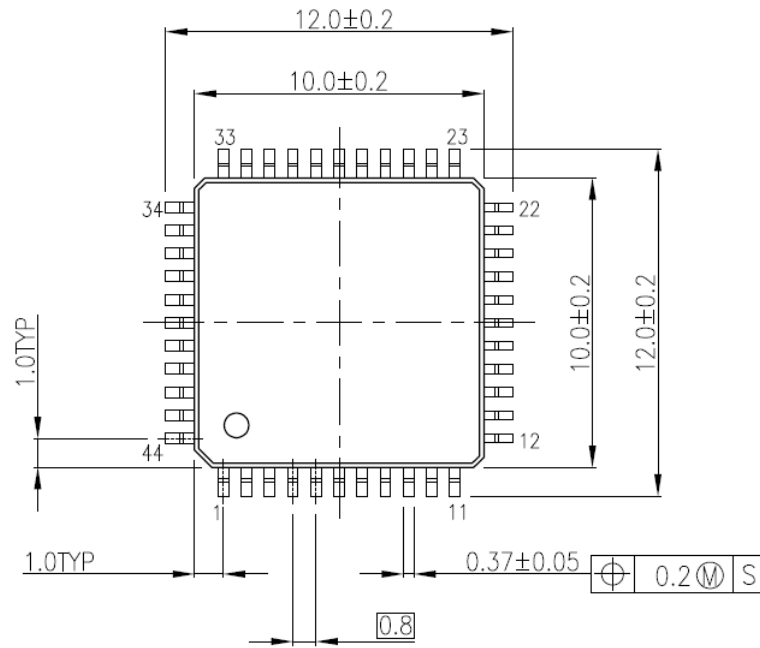
## 8.2. P-LQFP48-0707-0.50-002

Unit: mm



## 8.3. P-LQFP44-1010-0.80-003

Unit: mm



## 9. Precautions

This Page explains general precautions on the use of our MCUs.

Note that if there is a difference between the general precautions and the description in the body of the document, the description in the body of the document has higher priority.

(1) The MCUs' operation at power on

At power on, internal state of the MCUs is unstable. Therefore, state of the pins is undefined until reset operation is completed.

When a reset is performed by an external reset pin, pins of the MCUs that use the reset pin are undefined until reset operation by the external pin is completed.

Also, when a reset is performed by the internal power on reset, pins of the MCUs that use the internal power on reset are undefined until power supply voltage reaches the voltage at which power on reset is valid.

(2) Unused pins

Unused input/output ports of the MCUs are prohibited to use. The pins are high impedance.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

(3) Clock oscillation stability

A reset state must be released after the clock oscillation becomes stable. If the clock is changed to another clock while the program is in progress, wait until the clock is stable.

## 10. Revision History

**Table 10.1 Revision History**

| Revision | Date       | Description     |
|----------|------------|-----------------|
| 1.0      | 2026-04-24 | - First release |

## Appendix

### List of All Pins

Combination Function A and B: These are the functions which are assigned without setting port function registers.

Combination Function 1 to 8: These are the functions which are assigned with setting port function registers.

| M4H4<br>LQFP64 | M4H2<br>LQFP48 | M4H1<br>LQFP44 | Pin name | Combination<br>function A | Combination<br>function B | Combination<br>function 1 | Combination<br>function 2 | Combination<br>function 3 | Combination<br>function 4 | Combination<br>function 5 | Combination<br>function 6 | Combination<br>function 7 | Combination<br>function 8 | Input/<br>output | PU/PD | SV_T | SMT/<br>CMOS | Under<br>reset | After<br>reset |
|----------------|----------------|----------------|----------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|------------------|-------|------|--------------|----------------|----------------|
| 1              | 2              | 1              | PK2      |                           | INT02a                    | UT0RXD                    | UT0TXDA                   | TSPI0RXD                  |                           |                           |                           | TMS/SWDIO                 |                           | I/O              | PU/PD | N/A  | SMT          | PU<br>(Note1)  | PU<br>(Note1)  |
| 2              | 3              | 2              | PK3      |                           | INT03a                    | UT0TXDA                   | UT0RXD                    | TSPI0TXD                  |                           |                           |                           | TCK/SWCLK                 |                           | I/O              | PU/PD | N/A  | SMT          | PD<br>(Note1)  | PD<br>(Note1)  |
| 3              | 4              | 3              | PK4      |                           | INT06                     |                           |                           | TSPI0SCK                  |                           |                           | NBDSYNC                   | TRST_N                    |                           | I/O              | PU/PD | N/A  | SMT          | PU<br>(Note1)  | PU<br>(Note1)  |
| 4              | -              | -              | PL3      |                           |                           |                           |                           |                           |                           |                           | NBDDATA3                  | TRACEDATA3                |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 5              | -              | -              | PL2      |                           |                           |                           |                           |                           |                           |                           | NBDDATA2                  | TRACEDATA2                |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 6              | -              | -              | PL1      |                           |                           |                           |                           |                           |                           |                           | NBDDATA1                  | TRACEDATA1                |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 7              | -              | -              | PL0      |                           |                           |                           |                           |                           |                           |                           | NBDDATA0                  | TRACEDATA0                |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 8              | -              | -              | PL4      |                           |                           |                           |                           |                           |                           |                           | NBDCLK                    | TRACECLK                  |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 9              | 5              | 4              | DVDD5A   |                           |                           |                           |                           |                           |                           |                           |                           |                           |                           | -                | -     | -    | -            | -              | -              |
| 10             | 6              | 5              | REGOUT2  |                           |                           |                           |                           |                           |                           |                           |                           |                           |                           | -                | -     | -    | -            | -              | -              |
| 11             | 7              | 6              | REGOUT1  |                           |                           |                           |                           |                           |                           |                           |                           |                           |                           | -                | -     | -    | -            | -              | -              |
| 12             | -              | 7              | PH3      |                           |                           |                           |                           |                           |                           |                           |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 13             | 8              | 8              | PH2      |                           |                           |                           |                           |                           |                           | EMG0                      |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 14             | 9              | 9              | DVSSA    |                           |                           |                           |                           |                           |                           |                           |                           |                           |                           | -                | -     | -    | -            | -              | -              |
| 15             | 10             | 10             | PH0      | X1                        | EHCLKIN                   |                           |                           |                           |                           |                           |                           |                           |                           | Input            | PD    | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 16             | 11             | 11             | PH1      | X2                        |                           |                           |                           |                           |                           |                           |                           |                           |                           | Input            | PD    | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 17             | 12             | 12             | RESET_N  |                           |                           |                           |                           |                           |                           |                           |                           |                           |                           | -                | PU    | -    | SMT          | -              | -              |
| 18             | 13             | -              | PA1      |                           | INT09                     | UT1RXD                    | UT1TXDA                   | TSPI1RXD                  | T32A01INA0                | T32A01INC0                |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 19             | 14             | 13             | PA0      |                           | INT07a                    | UT1TXDA                   | UT1RXD                    | TSPI1TXD                  | T32A01INB0                | T32A01OUTB                |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 20             | -              | -              | PA2      |                           |                           |                           |                           | TSPI1SCK                  | T32A01INA1                | T32A01INC1                | T32A01OUTA                | T32A01OUTC                |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 21             | -              | -              | PJ7      |                           |                           |                           |                           |                           |                           | OVV0                      |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 22             | 15             | 14             | PJ6      | BOOT_N                    |                           |                           |                           |                           |                           | EMG0                      |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 23             | 16             | 15             | PJ5      |                           |                           |                           |                           |                           |                           | ZO0                       |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 24             | 17             | 16             | PJ4      |                           |                           |                           |                           |                           |                           | WO0                       |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 25             | 18             | 17             | PJ3      |                           |                           |                           |                           |                           |                           | YO0                       |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 26             | 19             | 18             | PJ2      |                           |                           |                           |                           |                           |                           | VO0                       |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 27             | 20             | 19             | PJ1      |                           |                           |                           |                           |                           |                           | XO0                       |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 28             | 21             | 20             | PJ0      |                           |                           |                           |                           |                           |                           | UO0                       | SCOUT                     | PMD0DBG                   |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 29             | 22             | 21             | DVSSB    |                           |                           |                           |                           |                           |                           |                           |                           |                           |                           | -                | -     | -    | -            | -              | -              |
| 30             | -              | -              | DVDD5B   |                           |                           |                           |                           |                           |                           |                           |                           |                           |                           | -                | -     | -    | -            | -              | -              |
| 31             | 23             | 22             | PB0      |                           | INT02b                    |                           | UT1TXDA                   | I2C0SDA/<br>EI2C0SDA      | T32A05OUTA                | T32A05OUTC                |                           | PMD0DBG                   | UT1RXD                    | I/O              | PU/PD | YES  | SMT          | Hi-Z           | Hi-Z           |
| 32             | 24             | 23             | PB1      |                           | INT03b                    | T32A05OUTB                | UT1RXD                    | I2C0SCL/<br>EI2C0SCL      | T32A05INA0                | T32A05INC0                | TRGIN1                    |                           | UT1TXDA                   | I/O              | PU/PD | YES  | SMT          | Hi-Z           | Hi-Z           |
| 33             | -              | -              | PC2      |                           | INT07b                    |                           |                           | TSPI3SCK                  | T32A03INA1                | T32A03INC1                |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 34             | -              | -              | PC1      |                           | INT10                     | UT3RXD                    | UT3TXDA                   | TSPI3RXD                  | T32A03INA0                | T32A03INC0                |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 35             | 25             | 24             | PC0      |                           | INT08                     | UT3TXDA                   | UT3RXD                    | TSPI3TXD                  | T32A03OUTA                | T32A03OUTC                |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 36             | 26             | 25             | AVSS     |                           |                           |                           |                           |                           |                           |                           |                           |                           |                           | -                | -     | -    | -            | -              | -              |
| 37             | 27             | 26             | PD0      | AINA11                    |                           |                           |                           |                           |                           |                           |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 38             | 28             | 27             | PD1      | AINA12                    |                           |                           |                           |                           |                           |                           |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 39             | 29             | 28             | PD2      | AINA10                    |                           |                           |                           |                           |                           |                           |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 40             | 30             | 29             | PD3      | AINA09                    |                           |                           |                           |                           |                           |                           |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 41             | 31             | 30             | PD4      | AINA08                    |                           |                           |                           |                           |                           |                           |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 42             | 32             | 31             | PD5      | AINA07                    |                           |                           |                           |                           |                           |                           |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 43             | 33             | 32             | PD6      | AINA06                    |                           |                           |                           |                           |                           | EMG0                      |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 44             | 34             | 33             | PE0      | AINA05                    |                           |                           |                           |                           |                           |                           |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 45             | 35             | 34             | PE1      | AINA04                    |                           |                           |                           |                           |                           |                           |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 46             | 36             | -              | PE2      | AINA03                    |                           |                           |                           |                           |                           |                           |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |

| M4H4<br>LQFP64 | M4H2<br>LQFP48 | M4H1<br>LQFP44 | Pin name | Combination<br>function A | Combination<br>function B | Combination<br>function 1 | Combination<br>function 2 | Combination<br>function 3 | Combination<br>function 4 | Combination<br>function 5 | Combination<br>function 6 | Combination<br>function 7 | Combination<br>function 8 | Input/<br>output | PU/PD | SV_T | SMT/<br>CMOS | Under<br>reset | After<br>reset |
|----------------|----------------|----------------|----------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|------------------|-------|------|--------------|----------------|----------------|
| 47             | -              | -              | PE3      | AINA02                    |                           |                           |                           |                           |                           |                           |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 48             | -              | -              | PE4      | AINA01                    |                           |                           |                           |                           |                           |                           |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 49             | 37             | 35             | VREFH    |                           |                           |                           |                           |                           |                           |                           |                           |                           |                           | -                | -     | -    | -            | -              | -              |
| 50             | 38             | 36             | AVDD5    |                           |                           |                           |                           |                           |                           |                           |                           |                           |                           | -                | -     | -    | -            | -              | -              |
| 51             | -              | -              | PF2      |                           | INT01b                    |                           |                           |                           | T32A04INA1                | T32A04INC1                | TRGIN2                    |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 52             | -              | -              | PF1      |                           | INT00b                    |                           |                           |                           | T32A04INA0                | T32A04INC0                |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 53             | -              | -              | DVDD5C   |                           |                           |                           |                           |                           |                           |                           |                           |                           |                           | -                | -     | -    | -            | -              | -              |
| 54             | 39             | 37             | DVSSC    |                           |                           |                           |                           |                           |                           |                           |                           |                           |                           | -                | -     | -    | -            | -              | -              |
| 55             | 40             | 38             | PF0      |                           |                           |                           |                           |                           | T32A04OUTA                | T32A04OUTC                | TRGIN0                    |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 56             | 41             | 39             | PG0      |                           | INT04                     | UT2TXDA                   | TSPI2TXD                  | T32A02OUTA                | T32A02OUTC                |                           |                           | PMD0DBG                   |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 57             | 42             | 40             | PG1      |                           | INT05                     | UT2RXD                    | TSPI2RXD                  | T32A02INA0                | T32A02INC0                |                           |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 58             | 43             | 41             | PG2      |                           |                           |                           | TSPI2SCK                  | T32A02INA1                | T32A02INC1                |                           |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 59             | 44             | -              | PG3      |                           |                           |                           |                           |                           |                           |                           |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 60             | 45             | -              | PG4      |                           |                           |                           |                           |                           |                           |                           |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 61             | 46             | -              | PG5      |                           |                           |                           |                           |                           |                           |                           |                           |                           |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |
| 62             | 47             | 42             | MODE     |                           |                           |                           |                           |                           |                           |                           |                           |                           |                           | -                | PD    | -    | SMT          | -              | -              |
| 63             | 48             | 43             | PK0      |                           | INT00a                    | UT0RXD                    | UT0TXDA                   |                           | T32A00OUTA                | T32A00OUTC                |                           | TDI                       |                           | I/O              | PU/PD | N/A  | SMT          | PU<br>(Note1)  | PU<br>(Note1)  |
| 64             | 1              | 44             | PK1      |                           | INT01a                    | UT0TXDA                   | UT0RXD                    |                           | T32A00INA0                | T32A00INC0                |                           | TDO/SWV                   |                           | I/O              | PU/PD | N/A  | SMT          | Hi-Z           | Hi-Z           |

Note1: In the initial state, the built-in pull-up and pull-down resistors are enabled.

Note2: TRACE and NBDIF are not available in M4H2 and M4H1.

Note3: UART ch3 is not in M4H2 and M4H1.

Note4: TSPI ch1 and 3 are not in M4H2 and M4H1.

Note5: INT00b, INT01b, INT07b and INT10 are not available in M4H2 and M4H1.  
INT09 is not in M4H1.

## Part Naming Conventions

# TMP M4 H 4 F Y x UG

The identification of Toshiba microcontrollers

Core

| Symbol | Description            |
|--------|------------------------|
| M4     | Arm Cortex-M4 with FPU |
| M3     | Arm Cortex-M3          |
| M0     | Arm Cortex-M0          |

Revision

Package

| Symbol           | Description  |
|------------------|--|
| QG               | Plastic shrink quad outline non-leaded package, dry-packed |
| UG, DUG, FG, DFG | Plastic quad flat package, dry-packed                      |
| MG, DMG          | Plastic small outline package, dry-packed                  |
| XBG              | Plastic ball grid array, dry-packed                        |

Product group

| Family       | Symbol | Main application   |
|--------------|--------|--|
| TXZ/<br>TXZ+ | H      | For general-purpose/consumer electronics equipment                                       |
|              | K      | For control of motors/inverter control/industrial equipment (Analog combo)               |
|              | M      | For control of motors/inverter control/industrial equipment (Analog combo), CAN built-in |
|              | G      | For OA/digital equipment/industrial equipment  |
|              | N      | For industrial network/IoT information management device/Ethernet, USB, and CAN built-in |
|              | E      | For precision instrument   |
|              | L      | For control of one motor/inverter control/industrial equipment                           |
|              | V      | For general-purpose/consumer electronics equipment                                       |

ROM Size

| Symbol | Size [KB] |
|--------|-----------|
| M      | 32        |
| P      | 48        |
| S      | 64        |
| U      | 96        |
| W      | 128       |
| Y      | 256       |
| Z      | 384       |
| D      | 512       |
| E      | 768       |
| 10     | 1024      |
| 15     | 1536      |
| 20     | 2048      |

Pin count

| Symbol | Pin count | Symbol          | Pin count |   |                 |
|--------|-----------|-----------------|-----------|---|-----------------|
| 0      | G         | 32 pins or less | 7         | P | 101 to 128 pins |
| 1      | H         | 33 to 44 pins   | 8         | Q | 129 to 144 pins |
| 2      | J         | 45 to 48 pins   | 9         | R | 145 to 176 pins |
| 3      | K         | 49 to 52 pins   | A         | S | 177 to 200 pins |
| 4      | L         | 53 to 64 pins   | B         | T | 201 to 224 pins |
| 5      | M         | 65 to 80 pins   | C         | U | 225 to 250 pins |
| 6      | N         | 81 to 100 pins  | D         | V | 251 to 300 pins |

ROM type

| Symbol | Type  |
|--------|-------|
| F      | Flash |

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