

**32-bit RISC Microcontroller**

**TXZ+ Family  
TMPM4H Group (1)**

**Reference Manual  
Clock Control and Operating Mode  
(CG-M4H(1))**

**Revision 1.0**

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**Toshiba Electronic Devices & Storage Corporation**

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## Preface

### Related Documents

Document name
Arm® Cortex®-M4 Processor Technical Reference Manual
Exception
Oscillation Frequency Detector
Voltage Detection Circuit
Clock Selective Watchdog Timer
Flash Memory
Datasheet

## Conventions

- Numeric formats follow the rules as shown below:  
Hexadecimal: 0xABC  
Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.  
Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "\_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].  
Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by [ ] defines the register.  
Example: [ABCD]
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.  
Example: [XYZ1], [XYZ2], [XYZ3] → [XYZn]
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...  
Example: [ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]
- In case of channel, "x" means 0, 1, and 2, ...  
Example: [T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]
- The bit range of a register is written like as [m: n].  
Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.  
Example: [ABCD]<EFG> = 0x01 (hexadecimal), [XYZn]<VW> = 1 (binary)
- Word and byte represent the following bit length.  
Byte: 8 bits  
Half word: 16 bits  
Word: 32 bits  
Double word: 64 bits
- Properties of each bit in a register are expressed as follows:  
R: Read only  
W: Write only  
R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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## Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-PMD	Advanced Programmable Motor Control Circuit
CG	Clock Control and Operating Mode
CRC	Cyclic Redundancy Check
D-Bus	DCode Memory Interface
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
EHOSC	External High-speed Oscillator
EI2C	I <sup>2</sup> C Interface Version A
fsys	Frequency of SYSTEM Clock
IA(INTIF)	Interrupt Control Register A
IB(INTIF)	Interrupt Control Register B
I-Bus	ICode Memory Interface
IHOSC	Internal High-speed Oscillator
IMN	Interrupt Monitor
INT	Interrupt
I2C	Inter-Integrated Circuit
LVD	Voltage Detection Circuit
NBDIF	Non-break Debug Interface
NMI	Non-maskable Interrupt
OFD	Oscillation Frequency Detector
POR	Power-on Reset Circuit
PORF	Power-on Reset Circuit for FLASH and Debug
RAMP	RAM Parity
RLM	Low-speed Oscillation/Power Supply Control/Reset
S-Bus	System Interface
SIWDT	Clock Selective Watchdog Timer
TRGSEL	Trigger Selection Circuit
TRM	Trimming Circuit
TSPI	Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Asynchronous Serial Communication Circuit

# 1. Clock Control and Operating Mode

## 1.1. Outlines

The clock/mode control block can select a clock gear and prescaler clock and set the warming up of oscillator and so on.

Furthermore, this product has NORMAL mode and a low-power consumption mode as the operating mode in order to reduce power consumption by operating mode transition depending on the situation.

Functions related to a clock are as follows.

- System clock control
- Prescaler clock control

## 1.2. Clock Control

### 1.2.1. Clock Types

A list of clocks is shown below.

EHCLKIN:	The high-speed clock input from the external
fosc:	A clock generated in the internal oscillation circuit or input from the X1 and X2 pins after being selected by <i>/CGOSCCR/</i> <OSCSEL>
f <sub>PLL</sub> :	A clock multiplied with PLL0
fc:	A clock selected by <i>/CGPLL0SEL/</i> <PLL0SEL> (High-speed clock)
fsys:	A system clock selected by <i>/CGSYSCR/</i> <GEAR[2:0]>
ΦT0:	A clock selected by <i>/CGSYSCR/</i> <PRCK[3:0]> (Prescaler clock)
f <sub>IHOSC1</sub> :	A clock generated with the internal high-speed oscillator 1
f <sub>IHOSC2</sub> :	A clock generated with the internal high-speed oscillator 2
ADCLK:	A conversion clock for the ADC
TRCLKIN:	A clock for tracing facilities of a debug circuit (Trace or SWV)

### 1.2.2. Initial State of Clock Setting by Reset

Each clock setting is initialized to the following states by reset.

External high-speed oscillator:	Stop
Internal high-speed oscillator 1:	Oscillation
Internal high-speed oscillator 2:	Stop
PLL (multiplying circuit):	Stop
Gear clock:	fc (no frequency dividing)



## 1.2.4. Warming-up Function

A warming-up function starts the warming-up timer for high-speed oscillation automatically to secure the oscillation stable time when the STOP1 mode is released.

It is also available as a count-up timer which uses the warming-up timer for high-speed oscillation to secure the stability of an external oscillator or an internal oscillator.

This chapter explains the setting method to the register for warming-up timers, and the case where it is used as a count-up timer. The detailed explanation for STOP1 mode release, refer to "1.3.3.2. Warming-up when Releasing Low-power Consumption Mode".

### 1.2.4.1. Warming-up Timer for High-speed Oscillation

A 16-bit up timer is built-in as a warming-up timer for a high-speed oscillation. Also, before changing to the STOP1 mode, the setting value to a 16-bit up timer is calculated with the following formula and the lower 4bits of calculated value are rounded down. And set  $[CGWUPHCR]<WUPT[15:4]>$  to the upper 12 bits of it.

<Formula>

(For external high-speed oscillation)

$$\begin{aligned} &\text{Warming-up timer setting value (16 bits)} \\ &= (\text{warming-up time (s)} / \text{clock period (s)}) - 16 \end{aligned}$$

(Example) When 5 ms of warming-up time is set up with 10 MHz oscillator (100ns of clock period)

$$\begin{aligned} \text{Warming-up timer setting value (16 bits)} &= (5\text{ms} / 100\text{ns}) - 16 \\ &= 50000 - 16 \\ &= 49984 \\ &= 0xC340 \end{aligned}$$

Since upper 12 bits are used, set the register as follows.

$$[CGWUPHCR]<WUPT[15:4]> = 0xC34$$

(For internal high-speed oscillator 1)

$$\begin{aligned} &\text{Warming-up timer setting value (16 bits)} \\ &= (\text{warming-up time (s)} - 63.3(\mu\text{s})) / \text{clock period (s)} - 41 \end{aligned}$$

(Example) When 163.4 μs of warming-up time is set up with 10 MHz oscillator (100 ns of clock periods)

$$\begin{aligned} \text{Warming-up timer setting value (16 bits)} &= ((163.4\mu\text{s} - 63.3\mu\text{s}) / 100\text{ns}) - 41 \\ &= (100.1\mu\text{s} / 100\text{ns}) - 41 \\ &= 960 \\ &= 0x03C0 \end{aligned}$$

Since upper 12 bits are used, set the register as follows.

$$[CGWUPHCR]<WUPT[15:4]> = 0x03C$$

The setting range is  $0x03C \leq <WUPT[15:4]> \leq 0xFFFF$ , warming-up time is set from 163.4 μs to 6.6194 ms.

### 1.2.4.2. Directions for Use of Warming-up Timer

The directions for use of a warming-up timer are explained.

- (1) Selection of a clock  
The warming-up timer is used for a high-speed oscillation, the clock classification (internal oscillation or external oscillation) counted with a warming-up timer is selected by *[CGWUPHCR]*<WUCLK>.
- (2) Calculation of warming-up timer setting value  
Setting value for a high-speed oscillation to the warming-up time can be set any value. Calculate from the suitable formula for each oscillation and set it.
- (3) Start of warming up, and confirm completion  
When software (Instruction) performs the start of warming up, start warming-up timer by setting *[CGWUPHCR]*<WUON> to "1". When it performs the confirmation of completion of warm up, check *[CGWUPHCR]*<WUEF> that becomes from "1" to "0". "1" shows that warming up is on-going and "0" shows that it is completed. After the warming up is completed, a timer is reset and returns to an initial state. A warming-up timer is not stopped even if "0" is written to *[CGWUPHCR]*<WUON> during a warming-up counter is counting. Writing "0" has no meaning.

Note: Since a warming-up timer is operating with the oscillating clock, a warming-up time includes an error, when oscillation frequency has fluctuation. Therefore, it serves an approximate time.

### 1.2.5. Clock Multiplying Circuit (PLL) for fsys

The clock multiplying circuit for fsys outputs the  $f_{PLL}$  clock (up to 120MHz) multiplied by the optimum condition for the frequency (6MHz to 24MHz) of the fosc.

It is possible to make the frequency of an oscillator low and to make the frequency of an internal clock high by this circuit.

#### 1.2.5.1. PLL Setting after Reset Release

The PLL is disabled after reset release.

In order to use the PLL, set *[CGPLL0SEL]*<PLL0SET[23:0]> to a multiplication value while *[CGPLL0SEL]*<PLL0ON> is "0". Then wait until approximately 100  $\mu$ s as a PLL initialization time. And set <PLL0ON> to "1" to start PLL operation. Then, the  $f_{PLL}$  clock which is multiplied fosc can be used by setting *[CGPLL0SEL]*<PLL0SEL> to "1" after waiting for approximately 400  $\mu$ s as a lock up time.

Notethat a stable time for the PLL operation is required. This time is made by a warming-up timer, etc.

## 1.2.5.2. Formula and Example of Setting Value for PLL Multiplication Value

The details of the items of *[CGPLL0SEL]<PLL0SET[23:0]>* which set up a PLL multiplication value are shown below.

**Table 1.1 Details of Setting Value to *[CGPLL0SEL]<PLL0SET[23:0]>***

The items of PLL0SET	Function	
[23:17]	Correction value setting	The quotient of fosc / 450000 (integer). Refer to Table 1.2.
[16:14]	fosc frequency range setting	000: 6 ≤ fosc ≤ 7      100: 12 < fosc ≤ 15 001: 7 < fosc ≤ 8      101: 15 < fosc ≤ 19 010: 8 < fosc ≤ 10     110: 19 < fosc ≤ 24 011: 10 < fosc ≤ 12    111: Reserved (Unit: MHz)
[13:12]	Dividing setting	00: Reserved 01: 1 / 2 (Divided by 2) 10: 1 / 4 (Divided by 4) 11: 1 / 8 (Divided by 8)
[11:8]	Fraction part of multiplication value	0000: 0.0000      1000: 0.5000 0001: 0.0625      1001: 0.5625 0010: 0.1250      1010: 0.6250 0011: 0.1875      1011: 0.6875 0100: 0.2500      1100: 0.7500 0101: 0.3125      1101: 0.8125 0110: 0.3750      1110: 0.8750 0111: 0.4375      1111: 0.9375
[7:0]	Integer part of multiplication value	0x00: 0 0x01: 1 0x02: 2 : 0xFD: 253 0xFE: 254 0xFF: 255

Note: A multiplication value is the total of *<PLL0SET[7:0]>* (integer part) and *<PLL0SET[11:8]>* (fraction part).

f<sub>PLL</sub> is calculated by the following formula.

$$f_{PLL} = f_{osc} \times [CGPLL0SEL]<PLL0SET[7:0]> + [CGPLL0SEL]<PLL0SET[11:8]> \times [CGPLL0SEL]<PLL0SET[13:12]>$$

Note1: The absolute value of frequency accuracy is not guaranteed.

Note2: There is no linearity in the frequency by the fraction part of multiplication value setup.

Note3: f<sub>PLL</sub> ≤ Maximum operating frequency

**Table 1.2 PLL Correction Value (Example)**

fosc (MHz)	<PLL0SET[23:17]> (Decimal, integral value)
6.00	14
8.00	18
10.00	23
12.00	27
24.00	54

The PLL correction value can be calculated by following formula.

When fosc is 6.0 MHz, the correction value is  $6 / 0.45 = 13.33 \rightarrow 14$  ; A fraction part is rounded up.

The major examples of a setting value to *[CGPLL0SEL]*<PLL0SET[23:0]> are shown below.

The target clock frequency ( $f_{PLL}$ ) is generated from input frequency (fosc). The fosc is multiplied and divided by PLL.

A dividing value is chosen from 2, 4, and 8.

Moreover, the multiplied frequency must be within the following ranges.

$$200 \text{ MHz} \leq \text{fosc} \times \text{Multiplication value} \leq 400 \text{ MHz}$$

**Table 1.3 Example of <PLL0SET[23:0]> Setting Value**

fosc (MHz)	Multiplication value	Dividing value	$f_{PLL}$ (MHz)	<PLL0SET[23:0]>
6.00	40.0000	2	120.00	0x1C1028
8.00	30.0000	2	120.00	0x24501E
10.00	24.0000	2	120.00	0x2E9018
12.00	20.0000	2	120.00	0x36D014
24.00	10.0000	2	120.00	0x6D900A
6.00	53.3125	4	79.97	0x1C2535
8.00	40.0000	4	80.00	0x246028
10.00	32.0000	4	80.00	0x2EA020
12.00	26.6250	4	79.88	0x36EA1A
24.00	13.3125	4	79.88	0x6DA50D

### 1.2.5.3. Change of PLL Multiplication Value Under Operating

It changes to a setup which sets "0" to *[CGPLL0SEL]*<PLL0SEL> first, and does not use a PLL multiplication clock during PLL multiplication clock operation when changing a multiplication value. And *[CGPLL0SEL]*<PLL0ST>=0 is read, after checking having changed to a setup which does not use a multiplication clock, *[CGPLL0SEL]*<PLL0ON> is set to "0", and PLL is stopped.

Then, the multiplication value of *[CGPLL0SEL]*<PLL0SET> is changed, as reset time of PLL, after about 100 $\mu$ s progress, *[CGPLL0SEL]*<PLL0ON> is set as "1", and operation of PLL is started.

Then, *[CGPLL0SEL]*<PLL0SEL> is set as "1" after lock up time and about 400 $\mu$ s progress.

Finally, *[CGPLL0SEL]*<PLL0ST> is read and it checks having changed.

## 1.2.5.4. Procedures of Switching Starting and Stopping PLL Operation

- (1) fc setting (PLL operation stopped → PLL operation started)

The example of switching procedure from the state of PLL operation stopped to the state of PLL operation started is as follows for the fc.

<< State before switching >>	
<b>[CGPLL0SEL]&lt;PLL0ON&gt; = 0</b>	The PLL operation for fsys is stopped.
<b>[CGPLL0SEL]&lt;PLL0SEL&gt; = 0</b>	The fosc is selected as the clock for fsys (PLL is unused.).
<b>[CGPLL0SEL]&lt;PLL0ST&gt; = 0</b>	The status of the clock selection for fsys indicates that the fosc is selected (PLL is unused.).

<< Example of switching procedure >>		
1	<b>[CGPLL0SEL]&lt;PLL0SET[23:0]&gt; = 0xX</b>	Set PLL multiplication value (0xX).
2	Wait 100 μs or more.	Wait for an initialization time after a PLL multiplication value is set.
3	<b>[CGPLL0SEL]&lt;PLL0ON&gt; = 1</b>	Start the PLL operation for fsys.
4	Wait 400 μs or more.	Wait for the PLL output clock stable.
5	<b>[CGPLL0SEL]&lt;PLL0SEL&gt; = 1</b>	Select the f <sub>PLL</sub> as the clock for fsys.
6	<b>[CGPLL0SEL]&lt;PLL0ST&gt; is read.</b>	Wait until the status of the clock selection for fsys becomes that the f <sub>PLL</sub> is selected (PLL is used.). ( <b>[CGPLL0SEL]&lt;PLL0ST&gt; = 1</b> ).

Note: Procedure 1 to 4 are not required when the state before switching is **[CGPLL0SEL]<PLL0ON> = 1**.  
 When switching from the state of PLL operation stopped to the state of PLL operation started while the PLL output clock is stable, only procedure 5 and 6bit are required.

- (2) fc setting (PLL operation oscillated → PLL operation stopped)

The example of switching procedure from the state of PLL oscillated to the state of PLL operation stopped is as follows for the fc.

<< State before switching >>	
<b>[CGPLL0SEL]&lt;PLL0ON&gt; = 1</b>	The PLL operation for fsys is oscillated.
<b>[CGPLL0SEL]&lt;PLL0SEL&gt; = 1</b>	The f <sub>PLL</sub> is selected as the clock for fsys (PLL is used.).
<b>[CGPLL0SEL]&lt;PLL0ST&gt; = 1</b>	The status of the clock selection for fsys indicates that the f <sub>PLL</sub> is selected (PLL is used.).

<< Example of switching sequence >>		
1	<b>[CGPLL0SEL]&lt;PLL0SEL&gt; = 0</b>	Selects the fosc as the clock for fsys.
2	<b>[CGPLL0SEL]&lt;PLL0ST&gt; is read.</b>	Wait until the status of the clock selection for fsys becomes that the fosc is selected (PLL is unused.). ( <b>[CGPLL0SEL]&lt;PLL0ST&gt; = 0</b> ).
3	<b>[CGPLL0SEL]&lt;PLL0ON&gt; = 0</b>	Stop the PLL operation for fsys.

## 1.2.6. System Clock

An internal high speed oscillation clock and external high speed oscillation clock (connected oscillator or clock input) can be used as a source of system clock.

Dividing is possible for a system clock at  $[CGSYSCR]<GEAR[2:0]>$  (clock gear). Although a setup can be changed during operation, after register writing before a clock actually changes, a maximum of 16-clock time is required of  $f_c$ . Check completion of a clock change by  $[CGSYSCR]<GEARST[2:0]>$ .

Note: Do not change a clock gear during operation of peripheral functions, such as a timer counter.

It is the following about the example of operation frequency by the clock gear ratio (1/1 to 1/16) to the frequency  $f_c$  set up with oscillation frequency, a PLL multiplication value, etc.

**Table 1.4 Example of Operating Frequency (Unit: MHz)**

External high-speed oscillation (MHz)	External high-speed clock input (MHz)	Internal high-speed oscillation 1 (MHz)	PLL multiplication value (after dividing)	Maximum frequency (MHz)	System clock frequency divided by clock gear (MHz) with PLL					System clock frequency divided by clock gear (MHz) without PLL				
					1/1	1/2	1/4	1/8	1/16	1/1	1/2	1/4	1/8	1/16
6	6	-	20	120	120	60	30	15	7.5	6	3	1.5	-	-
8	8	-	15	120	120	60	30	15	7.5	8	4	2	1	-
10	10	10	12	120	120	60	30	15	7.5	10	5	2.5	1.25	-
12	12	-	10	120	120	60	30	15	7.5	12	6	3	1.5	-
24	24	-	5	120	120	60	30	15	7.5	24	12	6	3	1.5
6	6	-	13.329	79.97	79.97	39.99	20	10	5	6	3	1.5	-	-
8	8	-	10	80	80	40	20	10	5	8	4	2	1	-
10	10	10	8	80	80	40	20	10	5	10	5	2.5	1.25	-
12	12	-	6.657	79.88	79.88	39.95	19.98	9.99	4.99	12	6	3	1.5	-
24	24	-	3.328	79.88	79.88	39.95	19.98	9.99	4.99	24	12	6	3	1.5

## 1.2.6.1. Procedure of Switching Oscillator for System Clock

### (1) fosc setting (Internal oscillator → External oscillator)

The example of switching procedure from the internal high-speed oscillator 1 (IHOSC1) to the external high-speed oscillator (EHOSC) is shown below.

<< State before switching >>	
<b>[CGOSCCR]&lt;IHOSC1EN&gt; = 1</b>	The internal high-speed oscillator 1 is oscillating.
<b>[CGOSCCR]&lt;OSCSEL&gt; = 0</b>	The internal high-speed oscillator 1 (IHOSC1) is selected as oscillator for fosc.
<b>[CGOSCCR]&lt;OSCF&gt; = 0</b>	The oscillator selection status for fosc indicates that IHOSC1 is selected.
An oscillator is connected to X1/X2 pin. (Note)	-

Note: Do not connect any devices except a oscillator.

<< Example of switching procedure >>		
1	<b>[PHPDN]&lt;bit[1:0]&gt; = 00</b> <b>[PHIE]&lt;bit[1:0]&gt; = 00</b>	Disable the pull-down resistors of X1 and X2 pins. Disable input control of X1 and X2 pins.
2	<b>[CGOSCCR]&lt;EOSCEN[1:0]&gt; = 01</b>	Use the external high-speed oscillator (EHOSC) as the external high-speed oscillator connection pins.
3	<b>[CGWUPHCR]&lt;WUCLK&gt; = 1</b> <b>[CGWUPHCR]&lt;WUPT[15:4]&gt; =</b> arbitrary value	Use the clock of external high-speed oscillator (EHOSC) as the source clock of warming-up timer. Set the arbitrary value as oscillator stable time to warming-up timer.
4	<b>[CGWUPHCR]&lt;WUON&gt; = 1</b>	Start the warming-up timer.
5	<b>[CGWUPHCR]&lt;WUEF&gt; is read.</b>	Wait until warming-up operation is completed ( <b>[CGWUPHCR]&lt;WUEF&gt; = 0</b> )
6	<b>[CGOSCCR]&lt;OSCSEL&gt; = 1</b>	Select the external high-speed oscillator (EHOSC) as oscillator for fosc.
7	<b>[CGOSCCR]&lt;OSCF&gt; is read.</b>	Wait until the status of the oscillator selection for fosc becomes that the external high-speed oscillator (EHOSC) is selected. ( <b>[CGOSCCR]&lt;OSCF&gt; = 1</b> )
8	<b>[CGOSCCR]&lt;IHOSC1EN&gt; = 0</b>	Stop the internal high-speed oscillator 1.

### (2) fosc setting (Internal oscillator → External clock input)

The example of switching procedure from the internal high-speed oscillator 1 (IHOSC1) to the external clock input (EHCLKIN) is shown below.

<< State before switching >>	
<b>[CGOSCCR]&lt;IHOSC1EN&gt; = 1</b>	The internal high-speed oscillator 1 is oscillating.
<b>[CGOSCCR]&lt;OSCSEL&gt; = 0</b>	The internal high-speed oscillator 1 (IHOSC1) is selected as oscillator for fosc.
<b>[CGOSCCR]&lt;OSCF&gt; = 0</b>	The oscillator selection status for fosc indicates that the internal high-speed oscillator 1 (IHOSC1) is selected.
Input clock to EHCLKIN	Voltage level of clock must be within the proper voltage range.

<< Example of switching procedure >>		
1	<b>[PHPDN]&lt;bit[0]&gt; = 0</b> <b>[PHIE]&lt;bit[0]&gt; = 0/1</b>	Disable the pull-down resistors of X1/EHCLKIN pin. The input control of X1/EHCLKIN pin is arbitrary.
2	<b>[CGOSCCR]&lt;EOSCEN[1:0]&gt; = 10</b>	Use the external high-speed oscillator (EHOSC) as the external clock input pin (EHCLKIN).
3	<b>[CGOSCCR]&lt;OSCSEL&gt; = 1</b>	Select the external high-speed oscillator (EHOSC) as oscillator for fosc.
4	<b>[CGOSCCR]&lt;OSCF&gt; is read.</b>	Wait until the status of the oscillator selection for fosc becomes that the external high-speed oscillator (EHOSC) is selected. ( <b>[CGOSCCR]&lt;OSCF&gt; = 1</b> )
5	<b>[CGOSCCR]&lt;IHOSC1EN&gt; = 0</b>	Stop the internal high-speed oscillator 1.

(3) fosc setting (External oscillator or external clock input → Internal oscillator)

The example of switching procedure from the external high-speed oscillator (EHOSC) or external clock input (EHCLKIN) to the external clock input (EHCLKIN) is shown below.

<< State before switching >>	
<b>[CGOSCCR]&lt;EOSCEN[1:0]&gt; = 01 or 10</b>	The external high-speed oscillator (EHOSC) is used as the external high-speed oscillator (HOSC) or external clock input pin (EHCLKIN).
<b>[CGOSCCR]&lt;OSCSEL&gt; = 1</b>	The external high-speed oscillator (EHOSC) is selected as oscillator for fosc.
<b>[CGOSCCR]&lt;OSCF&gt; = 1</b>	The oscillator selection status for fosc indicates that the external high-speed oscillator (EHOSC) is selected.

<< Example of switching procedure >>		
1	<b>[CGWUPHCR]&lt;WUCLK&gt; = 0</b>	Use the clock of internal high-speed oscillator (IHOSC1) as the source clock of warming-up timer.
2	<b>[CGWUPHCR]&lt;WUPT[15:4]&gt; = 0x03C</b>	Set the value as oscillator stable time (163.4μs (= 0x03C) or more) to warming-up timer.
3	<b>[CGOSCCR]&lt;IHOSC1EN&gt; = 1</b>	Start the internal high-speed oscillator 1 (IHOSC1).
4	<b>[CGWUPHCR]&lt;WUON&gt; = 1</b>	Start the warming-up timer.
5	<b>[CGWUPHCR]&lt;WUEF&gt;</b> is read.	Wait until the warming-up operation is completed. ( <b>[CGWUPHCR]&lt;WUEF&gt; = 0</b> )
6	<b>[CGOSCCR]&lt;OSCSEL&gt; = 0</b>	Select the internal high-speed oscillator 1 (IHOSC1) as oscillator for fosc.
7	<b>[CGOSCCR]&lt;OSCF&gt;</b> is read.	Wait until the status of the oscillator selection for fosc becomes that the internal high-speed oscillator 1 (IHOSC1) is selected. ( <b>[CGOSCCR]&lt;OSCF&gt; = 0</b> )
8	<b>[CGOSCCR]&lt;EOSCEN[1:0]&gt; = 00</b>	Use the external high-speed oscillator (EHOSC) as no oscillator.

## 1.2.7. Clock Supply Setting Function

TPM4H Group (1) has the clock supply supply/stop function for the peripheral circuits. To reduce the power consumption, it can stop supplying the clock to the peripheral functions that are not used.

Except some peripheral functions, clocks of the peripheral functions are not supplied after releasing reset.

In order to supply the clock of the peripheral function to be used, set the corresponding bit of *[CGFSYSENA]*, *[CGFSYSENB]*, *[CGFCEN]* and *[CGSPCLKEN]* to "1".

For details, refer to "1.4 Explanation of Register".

## 1.2.8. Clock Output Function

TPM4H Group (1) has the clock output function to the pin. The high-speed oscillation clock "fosc", high-speed clock "fc", system clock "fsys" can be output from the SCOUT pin.

For details, refer to "1.4.2.5. *[CGSCOCR]* (SCOUT Output Control Register)".

The below table shows the use propriety state of SCOUT pin in each operating mode.

**Table 1.5 List of Use Propriety in Each Operating Mode**

SCOUT selection	Operating mode	
	NORMAL/IDLE	STOP1
fosc	✓	-
fc	✓	-
fsys	✓	-

Note: ✓: available, -: not available

## 1.2.9. Prescaler Clock

Each peripheral function has a prescaler circuit to divide the  $\Phi T0$  clock. The  $\Phi T0$  clock which is input into the prescaler circuit can be divided by the divide rate specified by the *[CGSYSCR]<PRCK[3:0]>*.

For  $\Phi T0$  after releasing reset, fc is selected.

After writing register, the time of up to 512 fc clocks is required before a clock actually changes.

To confirm the completion of the clock change, check the status of *[CGSYSCR]<PRCKST[3:0]>*.

Note: Do not change a prescaler clock during operation of peripheral functions, such as a timer counter.

## 1.3. Operating Mode

TMPM4H Group (1) has NORMAL mode and low-power consumption modes (IDLE and STOP1 modes) as the operating mode. The power consumption can be reduced by changing operating mode according to directions for use.

### 1.3.1. Details of Operating Mode

#### 1.3.1.1. Feature in Each Operating Mode

The feature in NORMAL and low-power consumption modes are as follows.

- NORMAL mode

The CPU core and peripheral functions operate in the NORMAL mode. After releasing reset, TMPM4H Group (1) operates in NORMAL mode.

- Low-power consumption mode

The feature in low-power consumption modes is as follows.

- IDLE mode

The CPU stops in the IDLE mode.

The peripheral functions should perform operating or stopping by the register of each peripheral function, such as the clock supply setting function, etc.

Note: Note that the CPU cannot clear the watchdog timer in IDLE mode.

- STOP1 mode

All built-in circuits including the internal oscillators stop.

If the STOP1 mode is released, the internal high-speed oscillator 1 (IHOSC1) starts oscillation, and TMPM4H Group (1) returns to the NORMAL mode.

Disable the interrupts which are not used for STOP1 release before transition to the STOP1 mode.

### 1.3.1.2. Transition to and Return from Low-power Consumption Mode

In order to transit to each low-power consumption mode, the IDLE or STOP1 mode is selected by the standby control register *[CGSTBYCR]<STBY[1:0]>*, and a WFI (Wait For Interrupt) command is executed. When the transition to the low-power consumption mode has been performed by WFI instruction, the returning from the low-power consumption mode can be performed by the reset or the interrupt generation. To return by interrupt, the preparation for releasing the low-power consumption mode is required beforehand. Refer to "Interrupts" chapter of the Reference Manual "Exception" for details.

Note1: TPM4H Group (1) does not support a return by events; therefore, do not perform a transition to low-power consumption mode by WFE (Wait For Event).

Note2: TPM4H Group (1) does not support low-power consumption mode by SLEEPDEEP of the Cortex-M4 (with FPU) processor core. Do not use the <SLEEPDEEP> bit of the system control register.

### 1.3.1.3. Selection of Low-power Consumption Mode

The low-power consumption mode is selected by *[CGSTBYCR]<STBY[1:0]>*.

Following table shows the mode selected by <STBY[1:0]>.

**Table 1.6 Low-power Consumption Mode Selection**

Mode	<i>[CGSTBYCR]&lt;STBY[1:0]&gt;</i>
IDLE	00
STOP1	01

Note: Do not use the settings other than the above.

### 1.3.1.4. Peripheral Function State in Low-power Consumption Mode

The following Table 1.7 shows the operating status of the peripheral functions (block) in each operating mode. In addition, after releasing reset, the clock supply status of the peripheral functions except some peripheral functions is not supplied.

If needed, set *[CGFSYSENA]*, *[CGFSYSENB]*, *[CGFCEN]*, and *[CGSPCLKEN]* to enable clock supply.

**Table 1.7 Operating Status of Peripheral Functions in Each Low-power Consumption Mode**

Peripheral function		NORMAL mode	IDLE mode	STOP1 mode
Processor core (Including debug circuit)		✓	-	-
DMAC		✓	✓	-
I/O port	Pin status	✓	✓	✓
	Register	✓	✓	-
ADC		✓	✓	-
UART		✓	✓	-
I2C		✓	✓	-
EI2C		✓	✓	-
TSPI		✓	✓	-
A-PMD		✓	✓	-
T32A		✓	✓	-
TRGSEL		✓	✓	-
CRC		✓	✓	-
SIWDT		✓	✓ (Note1)	-
LVD		✓	✓	✓
OFD		✓	✓	-
TRM		✓	Unavailable	-
CG		✓	✓	✓
PLL		✓	✓	-
RAMP		✓	✓	-
External high-speed oscillator (EHOSC)		✓	✓	-
Internal high-speed oscillator 1 (IHOSC1)		✓	✓	-
Internal high-speed oscillator 2 (IHOSC2)		✓	✓	-
Code Flash memory		Access Possible	Access Possible (Note2)	Data hold
RAM				

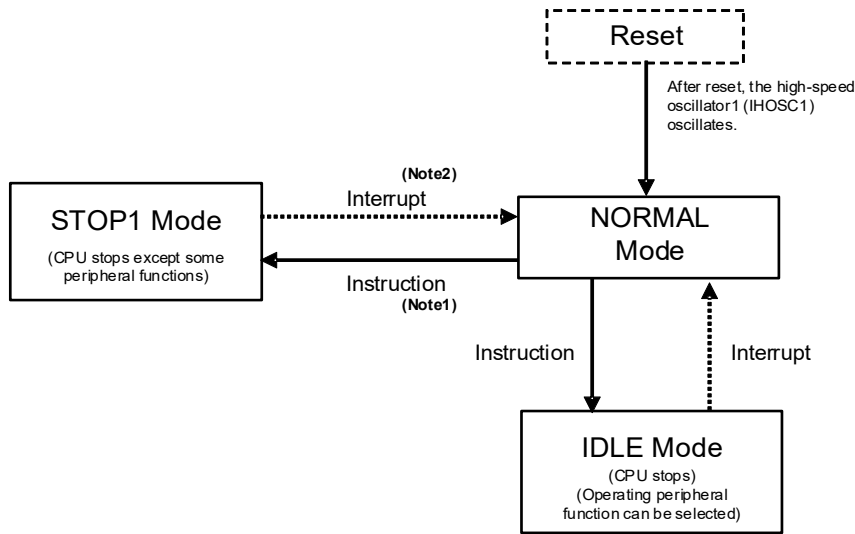
✓: Operation is possible.

-: If it transits to the target operating mode, the clock to peripheral function stops automatically.

Note1: Protect A mode only. In other cases, stop SIWDT before transiting to IDLE mode.

Note2: Data is held when the peripheral functions which are access (read or write) to code Flash or RAM (such as DMA, etc.) except CPU are not connected on the bus matrix.

## 1.3.2. Mode State Transition



**Figure 1.2 Mode State Transition**

Note1: Warming-up is required at returning. A warming-up time must be set in the previous operating mode (NORMAL mode) before entering to the STOP1 mode.

Note2: When TMPM4H Group (1) returns from the STOP1 mode, it branches to the service routine of interrupt source.

### 1.3.2.1. IDLE Mode Transition Flow

Perform the following procedure when transiting to the IDLE mode.

Because the IDLE mode is released by the interrupt, set the interrupt source setting before transiting to the IDLE mode. For the interrupts that can be used to release the IDLE mode, refer to "1.3.3.1. Release Sources of Low-power Consumption Mode". Disable interrupts which do not use for releasing the IDLE mode and ones which cannot be used.

Transition flow (from NORMAL mode)		
1	$[SIWDxEN] <WDTE> = 0$	Disable SIWDT.
2	$[SIWDxCR] <WDCR[7:0]> = 0xB1$	Disable SIWDT.
3	$[FCSR0] <RDYBSY>$ is read.	Wait until the Flash memory is in automatic operation completion state (= 1).
4	$[CGSTBYCR] <STBY[1:0]> = 00$	Low-power consumption mode selection is set to IDLE mode.
5	$[CGSTBYCR] <STBY[1:0]>$ is read.	Check that the value written in step 4 can be read.
6	WFI command execution	Transit to IDLE mode.

Note: When using the protect A mode of SIWDT, step 1 and 2 are not required.

## 1.3.2.2. STOP1 Mode Transition Flow

Perform the following procedure when transiting to STOP1 mode.

Because the STOP1 mode is released by an interrupt, set the interrupt source setting before transiting to STOP1 mode. For the interrupts that can be used to release the STOP1 mode, refer to "1.3.3.1. Release Sources of Low-power Consumption Mode". Disable interrupts which do not use for releasing the STOP1 mode and ones which cannot be used.

Transition flow (from NORMAL mode)		
1	<b>[SIWDxEN]</b> <WDTE> = 0	Disable SIWDT.
2	<b>[SIWDxCR]</b> <WDCR[7:0]> = 0xB1	Disable SIWDT.
3	<b>[FCSR0]</b> <RDYBSY> is read.	Wait until the Flash memory is in automatic operation completion state (= 1).
4	<b>[CGWUPHCR]</b> <WUEF> is read.	Wait until the warming-up operation is completed. ( <b>[CGWUPHCR]</b> <WUEF> = 0)
5	<b>[CGWUPHCR]</b> <WUCLK> = 0	Use the clock of internal high-speed oscillator (IHOSC1) as the source clock of warming-up timer.
	<b>[CGWUPHCR]</b> <WUPT[15:4]> = 0x03C	Set the value as oscillator stable time (163.4μs(=0x03C) or more) to warming-up timer.
6	<b>[CGSTBYCR]</b> <STBY[1:0]> = 01	Low-power consumption mode selection is set to STOP1 mode.
7	<b>[CGPLL0SEL]</b> <PLL0SEL> = 0	Selects the fosc as the clock for fsys.
8	<b>[CGPLL0SEL]</b> <PLL0ST> is read.	Wait until the status of the clock selection for fsys becomes that the fosc is selected ("PLL is unused"). ( <b>[CGPLL0SEL]</b> <PLL0ST> = 0)
9	<b>[CGPLL0SEL]</b> <PLL0ON> = 0	Stop the PLL operation for fsys.
10	<b>[CGOSCCR]</b> <IHOSC1EN> = 1	Start the internal high-speed oscillator 1 (IHOSC1).
11	<b>[CGWUPHCR]</b> <WUON> = 1	Start the warming-up timer.
12	<b>[CGWUPHCR]</b> <WUEF> is read.	Wait until the warming-up operation is completed. ( <b>[CGWUPHCR]</b> <WUEF> = 0)
13	<b>[CGOSCCR]</b> <OSCSEL> = 0	Select the internal high-speed oscillator 1 (IHOSC1) as oscillator for fosc.
14	<b>[CGOSCCR]</b> <OSCF> is read.	Wait until the status of the oscillator selection for fosc becomes that IHOSC1 is selected. ( <b>[CGOSCCR]</b> <OSCF> = 0)
15	<b>[CGOSCCR]</b> <EOSCEN[1:0]> = 00	Use the external high-speed oscillator (EHOSC) as no oscillator.
16	<b>[CGOSCCR]</b> <IHOSC2EN> = 0	Stop the internal high-speed oscillator 2 (IHOSC2).
17	<b>[CGOSCCR]</b> <EOSCEN[1:0]> is read.	Check that the value written in step 15 can be read. ( <b>[CGOSCCR]</b> <EOSCEN[1:0]> = 00)
18	<b>[CGOSCCR]</b> <IHOSC2F> is read.	Wait until the stability flag of internal oscillation for the internal high-speed oscillator (IHOSC2) becomes "0".
19	WFI command execution	Transit to STOP1 mode.

## 1.3.3. Return from Low-power Consumption Mode

### 1.3.3.1. Release Sources of Low-power Consumption Mode

The interrupt, Non-maskable interrupt, and reset can perform return from a low-power consumption mode. The source which can be used to release the low-power consumption mode is depending on the low-power consumption mode.

For details, the following table is shown.

**Table 1.8 List of Release Sources**

Low-power consumption mode		IDLE mode	STOP1 mode	
Release sources	Interrupt	INT00 to INT10 (Note1)	✓	✓
		INTEMGx, INTOVVx, INTPWMx	✓	-
		INTADxPDA, INTADxPDB	✓	-
		INTADxCP0, INTADxCP1, INTADxTRG	✓	-
		INTADxSGL, INTADxCNT	✓	-
		INTSCxRX, INTSCxTX, INTSCxERR	✓	-
		INTI2CxNST, INTI2CxATX, INTI2CxBRX, INTI2CxNA	✓	-
		INTT32AxAC, INTT32AxACAP0, INTT32AxACAP1, INTT32AxB, INTT32AxBCAP0, INTT32BxBCAP1	✓	-
		INTDMAATC, INTDMAAERR	✓	-
		INTPARI	✓	-
	INTFLCRDY	✓	-	
	SysTick interrupt	✓	-	
	Non-maskable interrupt (INTWDT0)	✓ (Note2)	-	
	Non-maskable interrupt (INTLVD)	✓	✓	
	Reset (SIWDT)	✓ (Note2)	-	
Reset (LVD)	✓	✓		
Reset (OFD)	✓	-		
Reset (RESET_N pin)	✓	✓		

✓: After release the low-power consumption mode, the interrupt procedure will start.

-: It cannot be used for release the low-power consumption mode.

Note1: The interrupt detection level of INT00 to INT10 (External Interrupt 00 to 10) can be selected from falling edge, rising edge or level. For details, refer to the Reference Manual "Exception".

Note2: Protected A mode only. In other cases, stop SIWDT before transition to IDLE mode.

- Released by an interrupt request

When the interrupt request releases the low-power consumption mode, it is necessary to prepare so that interrupt request may be detected by the CPU. It is necessary that the interrupt request used for releasing STOP1 may be detected by the CPU and INTIF.

- Released by Non-maskable interrupt (NMI)

The SIWDT interrupt (INTWDT0, Protect A mode only) and the LVD interrupt (INTLVD) for the NMI sources can perform release from the low-power consumption mode.

- Released by reset

The reset can perform release from all the low-power consumption modes.

When released by reset, TPM4H Group (1) operates in the NORMAL mode and its registers will be initialized after releasing reset. For details, refer to "3.2.6.1. Reset Factors and Initialized Range".

- Released by SysTick interrupt

SysTick interrupt can be used only in the IDLE mode.

Refer to "Interrupt" chapter of the Reference Manual "Exception" for details of interrupt.

### 1.3.3.2. Warming-up when Releasing Low-power Consumption Mode

Warming up may be required for the stability of an internal oscillator when the operating mode transits.

When the transition from STOP1 mode to NORMAL mode is performed, the internal oscillation is selected as the source clock of the warming-up timer automatically and the warming-up timer is started. A system clock is output after warming-up time is elapsed.

For this reason, before executing the command which the operating mode transits to the STOP1 mode by, set warming-up time to  $[CGWUPHCR] \langle WUPT[15:4] \rangle$ . For the setting value, refer to "1.2.4.1. Warming-up Timer for High-speed Oscillation".

The following table shows the necessity of a warming-up setting at the time of each operating mode transition.

**Table 1.9 Warming-up Time Setting**

Operating mode transition	Warming-up setting
NORMAL → IDLE	Not required
NORMAL → STOP1	Not required
IDLE → NORMAL	Not required
STOP1 → NORMAL	Required

### 1.3.4. Clock Operation when Operating Mode Transition

The clock operation is shown below when operating mode transition.

#### 1.3.4.1. NORMAL Mode → IDLE Mode → NORMAL Mode Transition

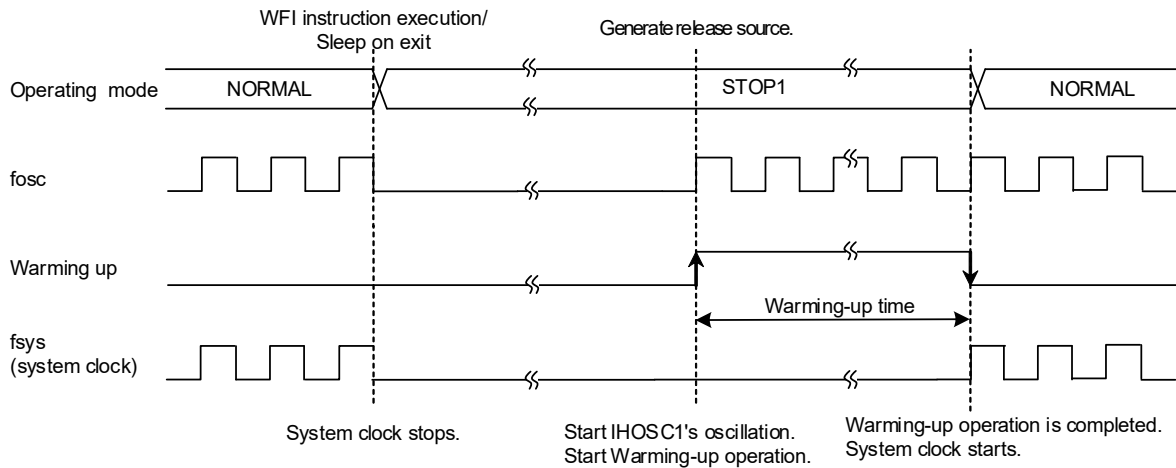
The CPU stops in the IDLE mode. The clock supply to peripheral functions keeps a setting state. Enable or disable the peripheral by the register of each peripheral function and/or a clock supply setting function, etc. if needed. The warming-up operation is not performed when the operating mode transits from IDLE mode to NORMAL mode.

After the instruction (WFI) execution which make the operating mode to IDLE mode, a program counter points to the next instruction. Then, the CPU stops. By a source released from the IDLE mode, the CPU is started again. If the interrupt is enabled, the next instruction of transition instruction (WFI) is done, after the interrupt processing by the released source is completed.

#### 1.3.4.2. NORMAL → STOP1 → NORMAL Mode Transition

When the operating mode transits from the STOP1 mode to NORMAL mode, warming up is started automatically. Set  $[CGWUPHCRJ] < WUPT[15:4] >$  to warming-up time (163.4μs or more) before transiting to the STOP1 mode.

Note: When the reset by the RESET\_N pin or LVD is the release source from the STOP1 mode, warming-up time is the same as time of warm reset "Internal processing time" and "CPU operation wait time". For details, refer to "3.2.2.1. Warm Reset by RESET\_N Pin" and "3.2.2.2. Warm Reset by LVD".



**Figure 1.3 NORMAL Mode → STOP1 Mode → NORMAL Mode Transition**

## 1.4. Explanation of Register

### 1.4.1. Register List

The registers related to CG and its addresses are shown below.

Peripheral function		Channel/Unit	Base address
Clock Control and Operating Mode	CG	-	0x400F3000

Register name		Address (Base+)
CG Write Protection Register	<b>[CGPROTECT]</b>	0x0000
Oscillation Control Register	<b>[CGOSCCR]</b>	0x0004
System Clock Control Register	<b>[CGSYSCR]</b>	0x0008
Standby Control Register	<b>[CGSTBYCR]</b>	0x000C
SCOUT Output Control Register	<b>[CGSCOCR]</b>	0x0010
PLL Selection Register for fsys	<b>[CGPLLOSEL]</b>	0x0020
High-speed Oscillation Warming-up Register	<b>[CGWUPHCR]</b>	0x0030
Supply Stop Register A for fsys	<b>[CGFSYSENA]</b>	0x0050
Supply Stop Register B for fsys	<b>[CGFSYSENB]</b>	0x0054
Supply Stop Register for fc	<b>[CGFCEN]</b>	0x0058
Clock Supply Stop Register for ADC and Debug Circuit	<b>[CGSPCLKEN]</b>	0x005C

## 1.4.2. Detail of Register

### 1.4.2.1. [CGPROTECT] (CG Write Protection Register)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0".
7:0	PROTECT[7:0]	0xC1	R/W	Control write-protection for the CG register (all registers included except this register) 0xC1: CG Registers are write-enabled. Other than 0xC1: Sets write protection (Protect enable)

### 1.4.2.2. [CGOSCCR] (Oscillation Control Register)

Bit	Bit symbol	After reset	Type	Function
31:20	-	0	R	Read as "0".
19	IHOSC2F	0	R	Stability flag of internal oscillation for internal high-speed oscillator 2 (IHOSC2) 0: Stopping or being in warming up 1: Stable oscillation
18:17	-	0	R	Read as "0".
16	IHOSC1F	1	R	Stability flag of internal oscillation for internal high-speed oscillator 1 (IHOSC1) (Note4) 0: Stopping or being in warming up 1: Stable oscillation
15:13	-	0	R	Read as "0".
12	-	0	R/W	Write as "0".
11:10	-	0	R	Read as "0".
9	OSCF	0	R	High-speed oscillator for fosc selection status. 0: Internal high-speed oscillator 1 (IHOSC1) 1: External high-speed oscillator (EHOSC)
8	OSCSEL	0	R/W	Selection high-speed oscillation for fosc. (Note1) 0: Internal high-speed oscillator 1 (IHOSC1) 1: External high-speed oscillator (EHOSC)
7:4	-	0	R	Read as "0".
3	IHOSC2EN	0	R/W	Internal high-speed oscillator 2 (IHOSC2) control (Note2) 0: Stop 1: Oscillation
2:1	EOSCEN[1:0]	00	R/W	Selection operation of external high-speed oscillator (EHOSC) (Note3) 00: External high-speed oscillator is not used 01: Use as external high-speed oscillator (EHOSC) 10: Use as external clock input (EHCLKIN) 11: Reserved
0	IHOSC1EN	1	R/W	Internal high-speed oscillator 1 (IHOSC1) control 0: Stop 1: Oscillation

Note1: When the setting is modified, confirm that the written value can be read from [CGOSCCR]<OSCF> before executing the next operation.

Note2: Setting cannot be changed, when [SIWDXOSCCR]<OSCPRO> is "1" (Write protection of SIWDT is enabled).

Note3: When the external high-speed oscillator (EHOSC) is used as the oscillator connection pin, set these bits to "01" (use as external high-speed oscillator.).

Note4: To wait stabilizing oscillation of the internal high-speed oscillator 1 (IHOSC1), use a warming-up timer and confirm [CGWUPHCR]<WUEF> instead of <IHOSC1F>.

### 1.4.2.3. [CGSYSCR] (System Clock Control Register)

Bit	Bit symbol	After reset	Type	Functions
31:28	-	0	R	Read as "0".
27:24	PRCKST[3:0]	0000	R	Prescaler clock ( $\Phi T0$ ) selection status 0000: fc    0100: fc/16    1000: fc/256 0001: fc/2    0101: fc/32    1001: fc/512 0010: fc/4    0110: fc/64    1010 to 1111: Reserved 0011: fc/8    0111: fc/128
23:19	-	0	R	Read as "0".
18:16	GEARST[2:0]	000	R	Selection status of the gear ratio of the system clock (fsys). 000: fc    100: fc/16 001: fc/2    101 to 111: Reserved 010: fc/4 011: fc/8
15:12	-	0	R	Read as "0".
11:8	PRCK[3:0]	0000	R/W	Select prescaler clock ( $\Phi T0$ ). 0000: fc    0100: fc/16    1000: fc/256 0001: fc/2    0101: fc/32    1001: fc/512 0010: fc/4    0110: fc/64    1010 to 1111: Reserved 0011: fc/8    0111: fc/128 Selects a prescaler clock for the peripheral functions.
7:3	-	0	R	Read as "0".
2:0	GEAR[2:0]	000	R/W	Select gear ratio of the system clock (fsys). 000: fc    100: fc/16 001: fc/2    101 to 111: Reserved 010: fc/4 011: fc/8

## 1.4.2.4. [CGSTBYCR] (Standby Control Register)

Bit	Bit symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1:0	STBY[1:0]	00	R/W	Select a low-power consumption mode. 00: IDLE mode 01: STOP1 mode 10: Reserved 11: Reserved

## 1.4.2.5. [CGSCOCR] (SCOUT Output Control Register)

Bit	Bit symbol	After reset	Type	Functions
31:7	-	0	R	Read as "0".
6:4	SCODIV[2:0]	000	R/W	SCOUT division ratio selection (Note) 000: No dividing 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101 to 111: Reserved
3:1	SCOSEL[2:0]	000	R/W	SCOUT base clock selection (Note) 000: fosc 001: fc 010: Reserved 011: fsys 100 to 111: Reserved
0	SCOEN	0	R/W	SCOUT output enable control 0: Disabled 1: Enabled

Note: When "011: fsys" for SCOUT is selected by <SCOSEL[2:0]>, "000: No dividing" by <SCODIV[2:0]> cannot be selected.

### 1.4.2.6. [CGPLL0SEL] (PLL Selection Register for fsys)

Bit	Bit symbol	After reset	Type	Function
31:8	PLL0SET[23:0]	0x000000	R/W	PLL0 multiplication setting About a multiplication setting, refer to "1.2.5.2. Formula and Example of Setting Value for PLL Multiplication Value".
7:3	-	0	R	Read as "0".
2	PLL0ST	0	R	PLL for fsys selection status 0: fosc 1: f <sub>PLL</sub>
1	PLL0SEL	0	R/W	Clock selection for fsys 0: fosc 1: f <sub>PLL</sub>
0	PLL0ON	0	R/W	PLL operation for fsys 0: Stopped 1: Operated

### 1.4.2.7. [CGWUPHCR] (High-speed Oscillation Warming-up Register)

Bit	Bit symbol	After reset	Type	Function
31:20	WUPT[15:4]	0x800	R/W	Set the upper 12 bits of the 16 bits of calculation value of the warming-up timer. About setting of a warming-up timer, refer to "1.2.4.1. Warming-up Timer for High-speed Oscillation".
19:16	WUPT[3:0]	0000	R	Set the lower 4 bits of the 16 bits of calculation value of the warming-up timer. It is fixed to "0000".
15:9	-	0	R	Read as "0".
8	WUCLK	0	R/W	Warming-up source clock selection (Note1) 0: Clock of internal high-speed oscillator 1 (IHOSC1) 1: Clock of external high-speed oscillator (EHOSC)
7:2	-	0	R	Read as "0".
1	WUEF	0	R	Status of the warming-up timer (Note2) 0: The end of warming-up operation 1: In warming-up operation
0	WUON	0	W	Control the warming-up timer. 0: Don't care 1: Warming-up operation start

Note1: Use the clock of internal high-speed oscillator 1 for warming up when the operating mode transits from STOP1 mode. Do not use the clock of external high-speed oscillator.

Note2: Do not modify the registers during the warming up (<WUEF> = 1). Set the registers when <WUEF> is "0".

## 1.4.2.8. [CGFSYSENA] (Supply Stop Register A for fsys)

Bit	Bit symbol	After reset	Type	Functions
31	IPENA31	0	R	Read as "0".
30	IPENA30	0	R/W	Enables the clock of T32A ch5 0: Clock stop 1: Clock supply
29	IPENA29	0	R/W	Enables the clock of T32A ch4 0: Clock stop 1: Clock supply
28	IPENA28	0	R/W	Enables the clock of T32A ch3 0: Clock stop 1: Clock supply
27	IPENA27	0	R/W	Enables the clock of T32A ch2 0: Clock stop 1: Clock supply
26	IPENA26	0	R/W	Enables the clock of T32A ch1 0: Clock stop 1: Clock supply
25	IPENA25	0	R/W	Enables the clock of T32A ch0 0: Clock stop 1: Clock supply
24	IPENA24	0	R/W	Enables the clock of I2C ch0 (Note3) 0: Clock stop 1: Clock supply
23	IPENA23	0	R/W	Enables the clock of UART ch3 0: Clock stop 1: Clock supply
22	IPENA22	0	R/W	Enables the clock of UART ch2 0: Clock stop 1: Clock supply
21	IPENA21	0	R/W	Enables the clock of UART ch1 0: Clock stop 1: Clock supply
20	IPENA20	0	R/W	Enables the clock of UART ch0 0: Clock stop 1: Clock supply
19	IPENA19	0	R/W	Enables the clock of TSPI ch3 0: Clock stop 1: Clock supply
18	IPENA18	0	R/W	Enables the clock of TSPI ch2 0: Clock stop 1: Clock supply
17	IPENA17	0	R/W	Enables the clock of TSPI ch1 0: Clock stop 1: Clock supply
16	IPENA16	0	R/W	Enables the clock of TSPI ch0 0: Clock stop 1: Clock supply
15	IPENA15	0	R	Read as "0".
14	IPENA14	0	R	
13	IPENA13	0	R	
12	IPENA12	0	R	
11	IPENA11	0	R	
10	IPENA10	0	R/W	Enables the clock of PORT L 0: Clock stop 1: Clock supply
9	IPENA09	0	R/W	Enables the clock of PORT K 0: Clock stop 1: Clock supply
8	IPENA08	0	R/W	Enables the clock of PORT J 0: Clock stop 1: Clock supply

Bit	Bit symbol	After reset	Type	Functions
7	IPENA07	0	R/W	Enables the clock of PORT H 0: Clock stop 1: Clock supply
6	IPENA06	0	R/W	Enables the clock of PORT G 0: Clock stop 1: Clock supply
5	IPENA05	0	R/W	Enables the clock of PORT F 0: Clock stop 1: Clock supply
4	IPENA04	0	R/W	Enables the clock of PORT E 0: Clock stop 1: Clock supply
3	IPENA03	0	R/W	Enables the clock of PORT D 0: Clock stop 1: Clock supply
2	IPENA02	0	R/W	Enables the clock of PORT C 0: Clock stop 1: Clock supply
1	IPENA01	0	R/W	Enables the clock of PORT B 0: Clock stop 1: Clock supply
0	IPENA00	0	R/W	Enables the clock of PORT A 0: Clock stop 1: Clock supply

Note1: Even if the initial value of the register is set to clock stop, the clock is supplied during the reset.

Note2: Write "0" for bit of peripheral function that does not exist in TMPM4H2 and TMPM4H1. For details, refer to "1.5. Information for Each Product".

Note3: The I2C and EI2C must be used exclusively.

## 1.4.2.9. [CGFSYSENB] (Supply Stop Register B for fsys)

Bit	Bit symbol	After reset	Type	Functions
31	IPENB31	1	R/W	Enables the clock of SIWDT 0: Clock stop 1: Clock supply
30	IPENB30	1	R/W	Enables the clock of NBDIF 0: Clock stop 1: Clock supply
29	IPENB29	0	R	Read as "0".
28	IPENB28	1	R/W	Write as "1".
27	IPENB27	0	R	Read as "0".
26	IPENB26	0	R	
25	IPENB25	0	R	
24	IPENB24	0	R/W	
23	IPENB23	0	R	Read as "0".
22	IPENB22	0	R	
21	IPENB21	0	R	
20	IPENB20	0	R	
19	IPENB19	0	R	
18	IPENB18	0	R	
17	IPENB17	0	R	Read as "0".
16	IPENB16	0	R/W	
15	IPENB15	0	R/W	Enables the clock of TRGSEL 0: Clock stop 1: Clock supply
14	IPENB14	0	R/W	Enables the clock of TRM 0: Clock stop 1: Clock supply
13	IPENB13	0	R/W	Enables the clock of OFD 0: Clock stop 1: Clock supply
12	IPENB12	0	R/W	Enables the clock of CRC 0: Clock stop 1: Clock supply
11	IPENB11	0	R/W	Enables the clock of RAMP 0: Clock stop 1: Clock supply
10	IPENB10	0	R	Read as "0".
9	IPENB09	0	R/W	Write as "0".
8	IPENB08	0	R/W	Enables the clock of A-PMD ch0 0: Clock stop 1: Clock supply
7	IPENB07	0	R/W	Write as "0".
6	IPENB06	0	R/W	
5	IPENB05	0	R	Read as "0".
4	IPENB04	0	R	
3	IPENB03	0	R/W	Write as "0".
2	IPENB02	0	R/W	
1	IPENB01	0	R/W	
0	IPENB00	0	R/W	Enables the clock of ADC unit A 0: Clock stop 1: Clock supply

Note1: Even if the initial value of the register is set to clock stop, the clock is supplied during the reset.

Note2: Write "0" for bit of peripheral function that does not exist in TPM4H2 and TPM4H1. For details, refer to "1.5. Information for Each Product".

Note3: The I2C and EI2C must be used exclusively.

### 1.4.2.10. [CGFCEN] (Supply Stop Register for fc)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0".
7	DNFCKEN	0	R/W	Enables the clock of DNF 0: Clock stop 1: Clock supply
6:0	-	0	R	Read as "0".

Note: Even if the initial value of the register is set to clock stop, the clock is supplied during the reset.

### 1.4.2.11. [CGSPCLKEN] (Clock Supply Stop Register for ADC and Debug Circuit)

Bit	Bit symbol	After reset	Type	Function
31:18	-	0	R	Read as "0".
17	-	0	R/W	Write as "0".
16	ADCKEN0	0	R/W	Enable the clock for ADC unit A (Note2) 0: Clock stop 1: Clock supply
15:1	-	0	R	Read as "0".
0	TRCKEN	0	R/W	Enable the Clock for the Trace function of Debug circuit (Trace or SWV). 0: Clock stop 1: Clock supply

Note1: Even if the initial value of the register is set to clock stop, the clock is supplied during the reset.

Note2: When setting this bit to "0" (clock stop), make sure that AD conversion is stopped.

## 1.5. Information for Each Product

The information about *[CGFSYSENA]* and *[CGFSYSENB]* which are different according to each product is shown below.

### 1.5.1. *[CGFSYSENA]*

**Table 1.10 *[CGFSYSENA]* Corresponding to Each Product**

Bit	Bit symbol	Destination	Channel No./ unit name/ port name	M4H4	M4H2	M4H1
31	IPENA31	-	-	-	-	-
30	IPENA30	T32A	5	✓	✓	✓
29	IPENA29		4	✓	✓	✓
28	IPENA28		3	✓	✓	✓
27	IPENA27		2	✓	✓	✓
26	IPENA26		1	✓	✓	✓
25	IPENA25		0	✓	✓	✓
24	IPENA24		I2C	0	✓	✓
23	IPENA23	UART	3	✓	-	-
22	IPENA22		2	✓	✓	✓
21	IPENA21		1	✓	✓	✓
20	IPENA20		0	✓	✓	✓
19	IPENA19	TSPI	3	✓	-	-
18	IPENA18		2	✓	✓	✓
17	IPENA17		1	✓	-	-
16	IPENA16		0	✓	✓	✓
15	IPENA15	-	-	-	-	-
14	IPENA14	-	-	-	-	-
13	IPENA13	-	-	-	-	-
12	IPENA12	-	-	-	-	-
11	IPENA11	-	-	-	-	-
10	IPENA10	PORT	L	✓	✓	-
9	IPENA09		K	✓	✓	✓
8	IPENA08		J	✓	✓	✓
7	IPENA07		H	✓	✓	✓
6	IPENA06		G	✓	✓	✓
5	IPENA05		F	✓	✓	✓
4	IPENA04		E	✓	✓	✓
3	IPENA03		D	✓	✓	✓
2	IPENA02		C	✓	✓	✓
1	IPENA01		B	✓	✓	✓
0	IPENA00		A	✓	✓	✓

Note: ✓: Available, -: N/A

## 1.5.2. [CGFSYSENB]

**Table 1.11 [CGFSYSENB] Corresponding to Each Product**

Bit	Bit symbol	Destination	Channel No./ unit name/ port name	M4H4	M4H2	M4H1
31	IPENB31	SIWDT	0	✓	✓	✓
30	IPENB30	NBDIF	-	✓	-	-
29	IPENB29	-	-	-	-	-
28	IPENB28	- (Note2)	-	-	-	-
27	IPENB27	-	-	-	-	-
26	IPENB26	-	-	-	-	-
25	IPENB25	-	-	-	-	-
24	IPENB24	EI2C	0	✓	✓	✓
23	IPENB23	-	-	-	-	-
22	IPENB22	-	-	-	-	-
21	IPENB21	-	-	-	-	-
20	IPENB20	-	-	-	-	-
19	IPENB19	-	-	-	-	-
18	IPENB18	-	-	-	-	-
17	IPENB17	-	-	-	-	-
16	IPENB16	DMAC	A	✓	✓	✓
15	IPENB15	TRGSEL	-	✓	✓	✓
14	IPENB14	TRM	-	✓	✓	✓
13	IPENB13	OFD	-	✓	✓	✓
12	IPENB12	CRC	-	✓	✓	✓
11	IPENB11	RAMP	-	✓	✓	✓
10	IPENB10	-	-	-	-	-
9	IPENB09	- (Note3)	-	-	-	-
8	IPENB08	A-PMD	0	✓	✓	✓
7	IPENB07	- (Note3)	-	-	-	-
6	IPENB06	- (Note3)	-	-	-	-
5	IPENB05	-	-	-	-	-
4	IPENB04	-	-	-	-	-
3	IPENB03	- (Note3)	-	-	-	-
2	IPENB02	- (Note3)	-	-	-	-
1	IPENB01	- (Note3)	-	-	-	-
0	IPENB00	ADC	A	✓	✓	✓

Note1: ✓: Available, -: N/A

Note2: Write as "1".

Note3: Write as "0".

## 2. Memory Map

### 2.1. Outlines

The memory maps for TMPM4H Group (1) are based on the Cortex-M4 (with FPU) processor core memory map. The built-in ROM, built-in RAM and special function registers (SFR) of TMPM4H Group (1) are mapped to the Code, SRAM and peripheral regions of the Cortex-M4 (with FPU) respectively. The special function register (SFR) means the control registers of all input/output ports and peripheral functions.

The CPU register region is the processor core's internal register region.

For more information on each region, refer to the "Arm Cortex-M4 Processor Technical Reference Manual".

Note that access to regions indicated as "Fault" causes a bus fault if bus faults are enabled, or causes a hard fault if bus faults are disabled. Also, do not access the vendor-specific region (Vender-Specific).

## 2.1.1. TPM4HxFYB

- Code Flash : 256KB
- RAM : 18KB
- Products : TPM4H4FYBUG, TPM4H2FYBDUG, TPM4H1FYBUG

0xFFFFFFFF	Vendor-Specific	System level	0xFFFFFFFF	Vendor-Specific
0xE0100000			0xE0100000	
	CPU Register Region			CPU Register Region
0xE0000000			0xE0000000	
	Fault	Peripheral		Fault
0x5E040000			0x5E040000	
0x5E000000	Code Flash (Mirror 256KB)		0x5E000000	Code Flash (Mirror 256KB)
0x5DFF0000	Flash (SFR)		0x5DFF0000	Flash (SFR)
0x44000000	Fault		0x44000000	Fault
	Bit Band Alias (SFR)			Bit Band Alias (SFR)
0x42000000			0x42000000	
0x40100000	Fault		0x40100000	Fault
0x4003E000	SFR		0x4003E000	SFR
0x40000000	Fault		0x40000000	Fault
0x3F7F9800		0x3F7F9800		
0x3F7F8000	BOOT ROM	0x3F7F8000	BOOT ROM (Mirror 6KB)	
	Fault		Fault	
0x24000000		0x24000000		
	Bit Band Alias (RAM/Backup RAM)	SRAM		Bit Band Alias (RAM/Backup RAM)
0x22000000			0x22000000	
0x20004800	Fault		0x20004800	Fault
0x20002000	RAM2 (10KB)		0x20002000	RAM2 (10KB)
0x20010000	RAM1 (4KB)		0x20010000	RAM1 (4KB)
0x20000000	RAM0 (4KB)		0x20000000	RAM0 (4KB)
	Fault			Fault
0x00040000			0x00001800	
0x00000000	Code Flash (256KB)		0x00000000	BOOT ROM (6KB)

Single chip mode
Single BOOT mode

**Figure 2.1 TPM4HxFYB**

## 2.2. Bus Matrix

TMPM4H Group (1) contains three bus managers such as a CPU core, DMA controller and NBDIF.

Bus managers connect to subordinate ports (S0 to S4) of Bus Matrix. In the bus matrix, manager ports (M0 to M12) connect to peripheral functions via connections described as (○) or (●) in the following figure. (●) shows a connection to a mirror area.

While multiple subordinates are connected to the same bus manager line in the Bus Matrix, if multiple subordinate accesses are generated at the same time, a priority is given to access from a manager with the smallest subordinate number.

## 2.2.1. Configuration

### 2.2.1.1. Single Chip Mode

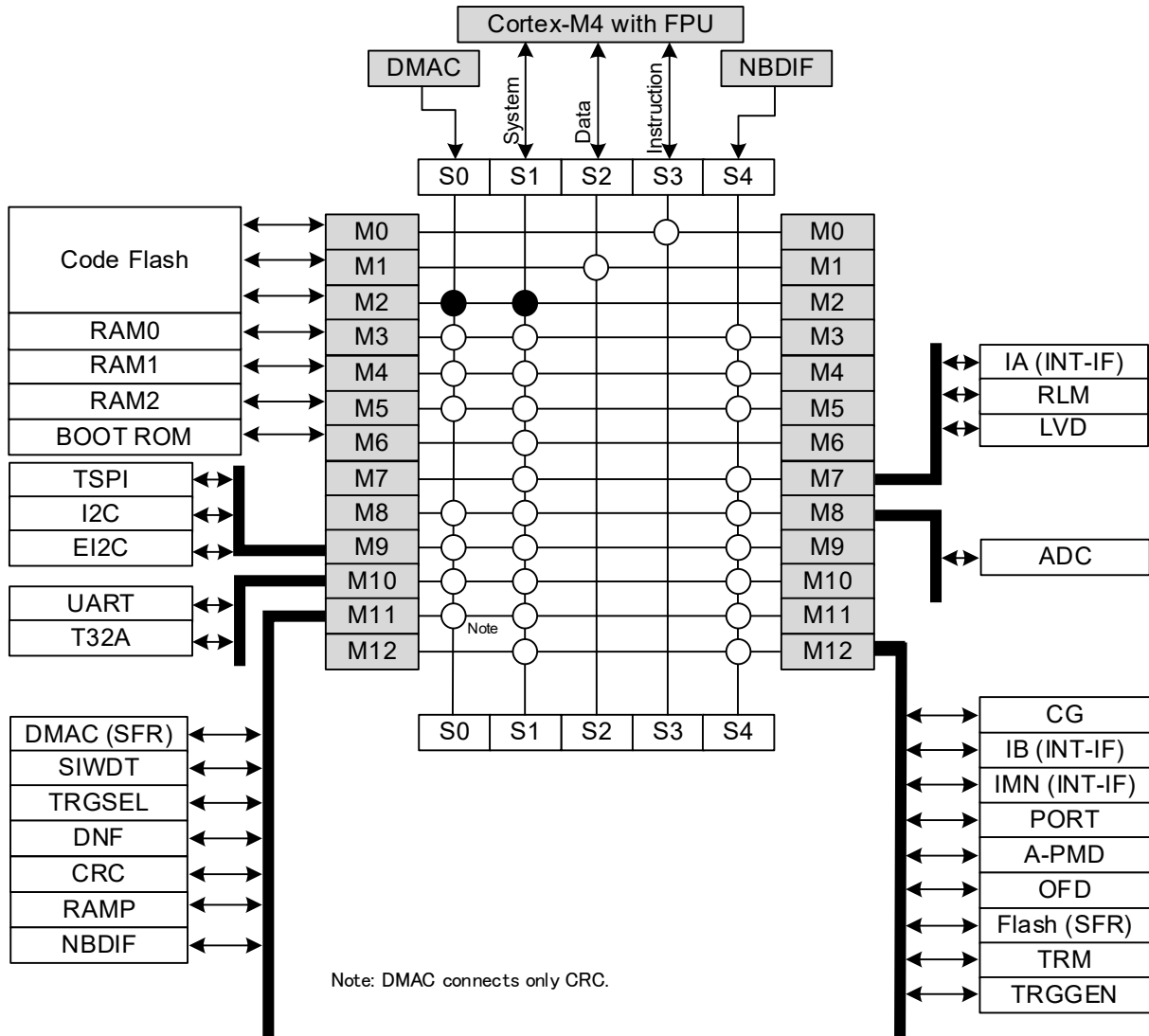


Figure 2.2 Single Chip Mode

## 2.2.1.2. Single Boot Mode

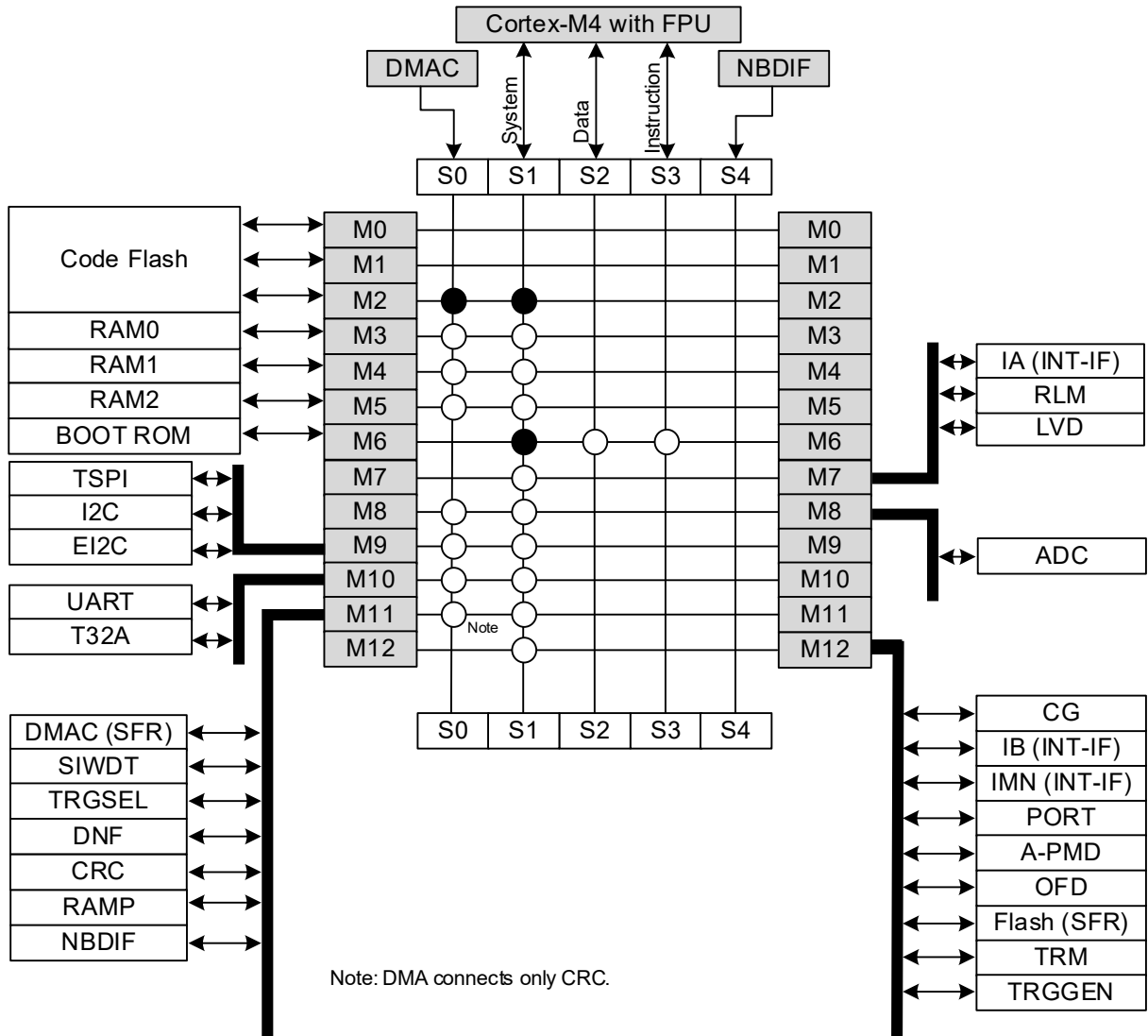


Figure 2.3 Single Boot Mode

## 2.2.2. Connection Table

### 2.2.2.1. Connection of Memory, etc.

- Single Chip Mode

**Table 2.1 Single Chip Mode**

Start address	Subordinate		Manager				
			DMAC	Core S-Bus	Core D-Bus	Core I-Bus	NBDIF
			S0	S1	S2	S3	S4
0x00000000	Code Flash	M0	Fault	-	Fault	✓	Fault
		M1	Fault	-	✓	Fault	Fault
0x00040000	Fault	-	Fault	-	Fault	Fault	Fault
0x20000000	RAM0	M3	✓	✓	-	-	✓
0x20001000	RAM1	M4	✓	✓	-	-	✓
0x20002000	RAM2	M5	✓	✓	-	-	✓
0x20004800	Fault	-	Fault	Fault	-	-	Fault
0x22000000	Bit band alias	-	Fault	✓	-	-	Fault
0x24000000	Fault	-	Fault	Fault	-	-	Fault
0x3F7F8000	BOOT ROM (Mirror)	M6	Fault	✓	-	-	Fault
0x3F7F9800	Fault	-	Fault	Fault	-	-	Fault
Refer to "Table 2.3 Connection of Peripheral Function" for these addresses.							
0x5E000000	Code Flash (Mirror)	M2	✓	✓	-	-	Fault

✓: Accessible, -: not accessible, Fault: Fault occurs

- Single Boot Mode

**Table 2.2 Single Boot Mode**

Start address	Subordinate		Manager				
			DMAC	Core S-Bus	Core D-Bus	Core I-Bus	NBDIF
			S0	S1	S2	S3	S4
0x00000000	BOOT ROM	M6	Fault	-	✓	✓	Fault
0x00001800	Fault	-	Fault	-	Fault	Fault	Fault
0x20000000	RAM0	M3	✓	✓	-	-	✓
0x20001000	RAM1	M4	✓	✓	-	-	✓
0x20002000	RAM2	M5	✓	✓	-	-	✓
0x20004800	Fault	-	Fault	Fault	-	-	Fault
0x22000000	Bit band alias	-	Fault	✓	-	-	Fault
0x24000000	Fault	-	Fault	Fault	-	-	Fault
0x3F7F8000	BOOT ROM (Mirror)	M6	Fault	✓	-	-	Fault
0x3F7F9800	Fault	-	Fault	Fault	-	-	Fault
Refer to "Table 2.3 Connection of Peripheral Function" for these addresses.							
0x5E000000	Code Flash (Mirror)	M2	✓	✓	-	-	Fault

✓: Accessible, -: not accessible, Fault: Fault occurs

## 2.2.2.2. Connection of Peripheral Functions

**Table 2.3 Connection of Peripheral Functions**

Start address	Subordinate		Manager				
			DMAC	Core S-Bus	Core D-Bus	Core I-Bus	NBDIF
			S0	S1	S2	S3	S4
0x40000000	Fault	-	Fault	Fault	-	-	Fault
0x4003E000	IA (INTIF)	M7	Fault	✓	-	-	✓
0x4003E400	RLM		Fault	✓	-	-	✓
0x4003EC00	LVD		Fault	✓	-	-	✓
0x4004C000	DMAC (SFR)	M11	Fault	✓	-	-	✓
0x40098000	TSPI (ch0 to 3)	M9	✓	✓	-	-	✓
0x400A0000	I2C (ch0)		✓	✓	-	-	✓
0x400A5000	EI2C (ch0)		✓	✓	-	-	✓
0x400B8800	ADC (unit A)	M8	✓	✓	-	-	✓
0x400BA000	T32A (ch0 to 5)	M10	✓	✓	-	-	✓
0x400BB000	UART (ch0 to 3)		✓	✓	-	-	✓
0x400BB400	SIWDT	M11	Fault	✓	-	-	✓
0x400BB600	DNF		Fault	✓	-	-	✓
0x400BB800	TRGSEL		Fault	✓	-	-	✓
0x400BBA00	NBDIF		Fault	✓	-	-	✓
0x400BBB00	RAMP		Fault	✓	-	-	✓
0x400BBC00	CRC		✓	✓	-	-	✓
0x400C0000	PORT	M12	Fault	✓	-	-	✓
0x400F1000	OFD		Fault	✓	-	-	✓
0x400F3000	CG		Fault	✓	-	-	✓
0x400F3200	TRM		Fault	✓	-	-	✓
0x400F4E00	IB (INTIF)		Fault	✓	-	-	✓
0x400F4F00	IMN		Fault	✓	-	-	✓
0x400F6000	A-PMD (ch0)		Fault	✓	-	-	✓
0x400FF000	TRGGEN		Fault	✓	-	-	✓
0x40100000	Fault	-	Fault	Fault	-	-	Fault
0x42000000	Bit Band Alias	-	Fault	✓	-	-	Fault
0x44000000	Fault	-	Fault	Fault	-	-	Fault
0x5DFF0000	Flash (SFR)	M12	Fault	✓	-	-	✓
0x5E040000	Fault	-	Fault	Fault	-	-	Fault

✓: Accessible, -: not accessible, Fault: Fault occurs

## 3. Reset and Power Supply Control

### 3.1. Outlines

Function classification	Function	Operation description
Cold reset (Reset with turning on a power supply)	Power-on reset	Reset which occurs at the time of a power supply turning on or turning off
	LVD reset	Reset which occurs when the voltage of power supply is the setting voltage or less
	Reset pin	Reset by a RESET_N pin
	PORF reset	Reset which occurs at the time of a power supply turning on or turning off PORF reset resets Flash memory and debug circuits with priority.
Warm reset (Reset without turning on a power supply)	Internal reset	Reset by SIWDT, OFD, LVD, LOCKUP, and <SYSRESETREQ>
	Reset pin	Reset by a RESET_N pin
Single boot mode starting	Reset pin	After reset is released, TPM4H Group (1) starts from the built-in BOOT ROM.

### 3.2. Description of Function and Operation

This chapter describes that the power supply turns on and turns off, and items related with the reset.

Note: Refer to "Electrical Characteristics" of a datasheet for the time and voltage of description of the symbol in a figure.

#### 3.2.1. Cold Reset

When a power supply is turned on, the stabilization time for the built-in regulator, the built-in Flash memory, and the built-in high-speed oscillator is necessary. The TXZ+ family automatically inserts a wait time for the stabilization of these circuits.

When a power supply is turned on, make sure that the slope of the power supply voltage rises to the right. If the power supply voltage drops and rises near the voltage level of POR and PORF detection voltage, it may not operate normally even if the power supply voltage rises to the guaranteed operating range thereafter.

### 3.2.1.1. Reset by Power-on Reset Circuit (without Using RESET\_N pin)

After a supply voltage exceeds the release voltage of a power-on reset circuit (POR), the internal reset is released after "Internal initialization time" is elapsed. Increase a supply voltage to an operating voltage range before "Internal initialization time" is elapsed. The CPU operates after the internal reset is released.

After a supply voltage exceeds the release voltage of a power-on reset circuit (POR), LVD continuously keeps outputting reset signal until the supply voltage exceeds the LVD release voltage. And the internal reset has priority during the time of "Internal initialization time". When rising time of a supply voltage beyond "Internal initialization time", refer to "3.2.1.3. Continuation of Reset by LVD".

For example, if the operating voltage of a user's set is 2.7V or more, after the reset by power-on reset circuit is released, increase a supply voltage to 2.7V before "Internal initialization time" is elapsed. And if the operating voltage of a user's set is 4.5V or more, after the reset by power-on reset circuit is released, increase a supply voltage to 4.5V before "Internal initialization time" is elapsed.

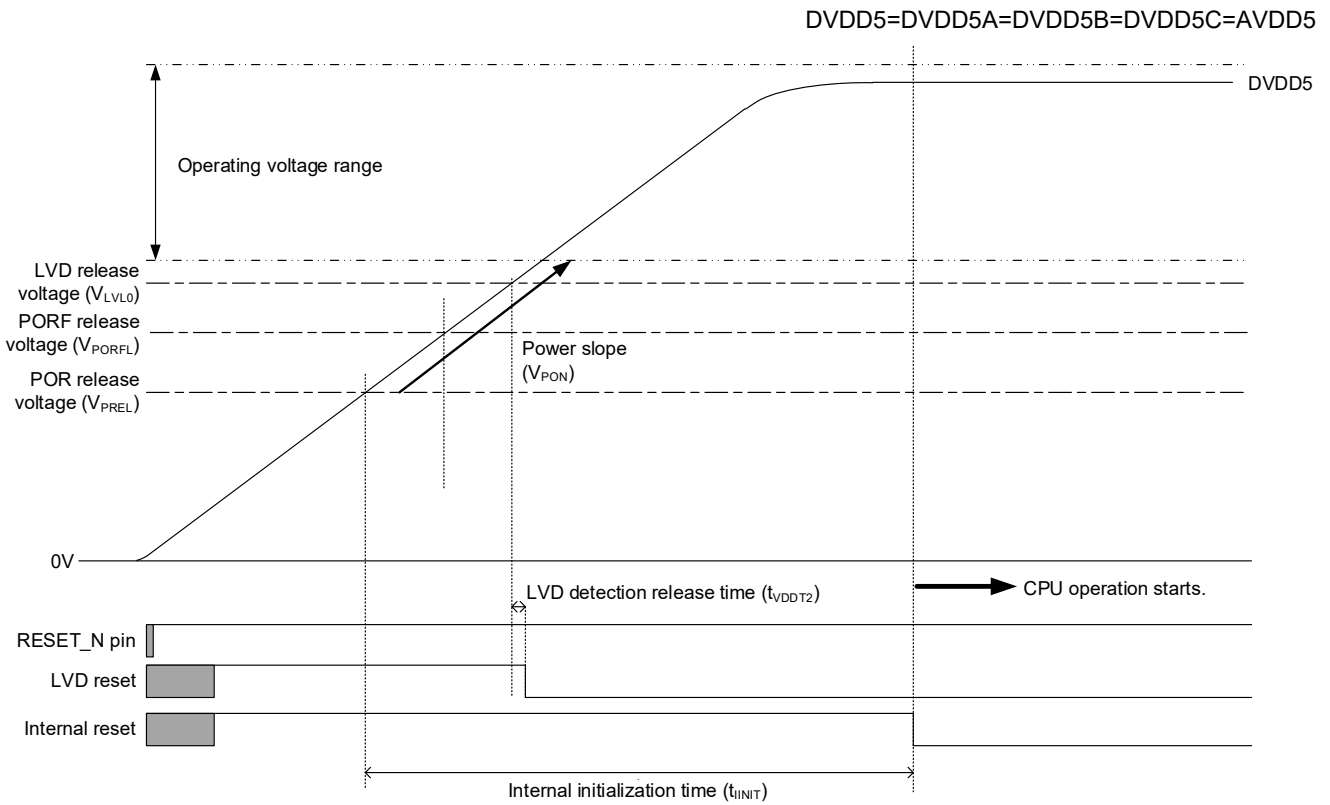


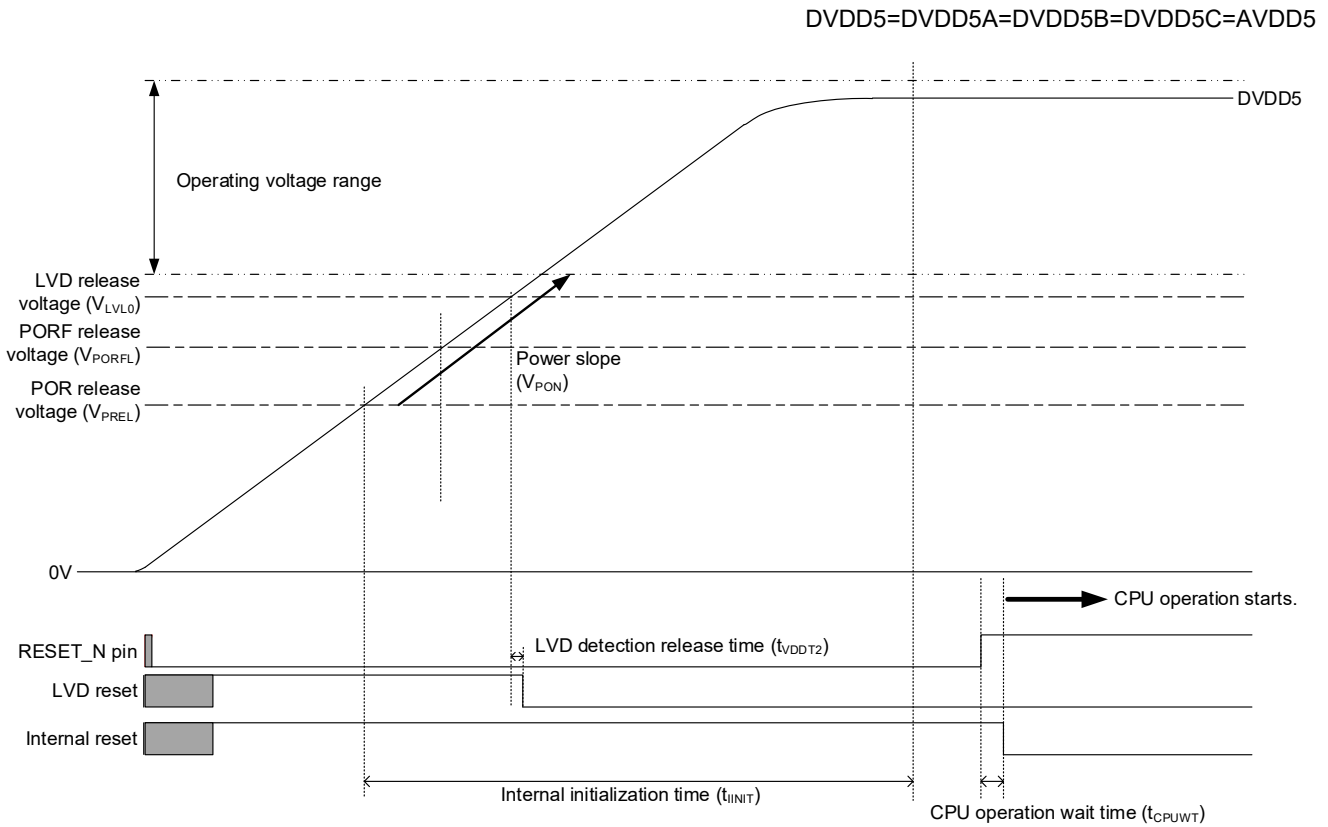
Figure 3.1 Reset by Power-on Reset Circuit

Note: When only power-on reset circuit without RESET\_N pin is used, "High" or opened level should be input to the RESET\_N pin.

**3.2.1.2. Reset by RESET\_N Pin**

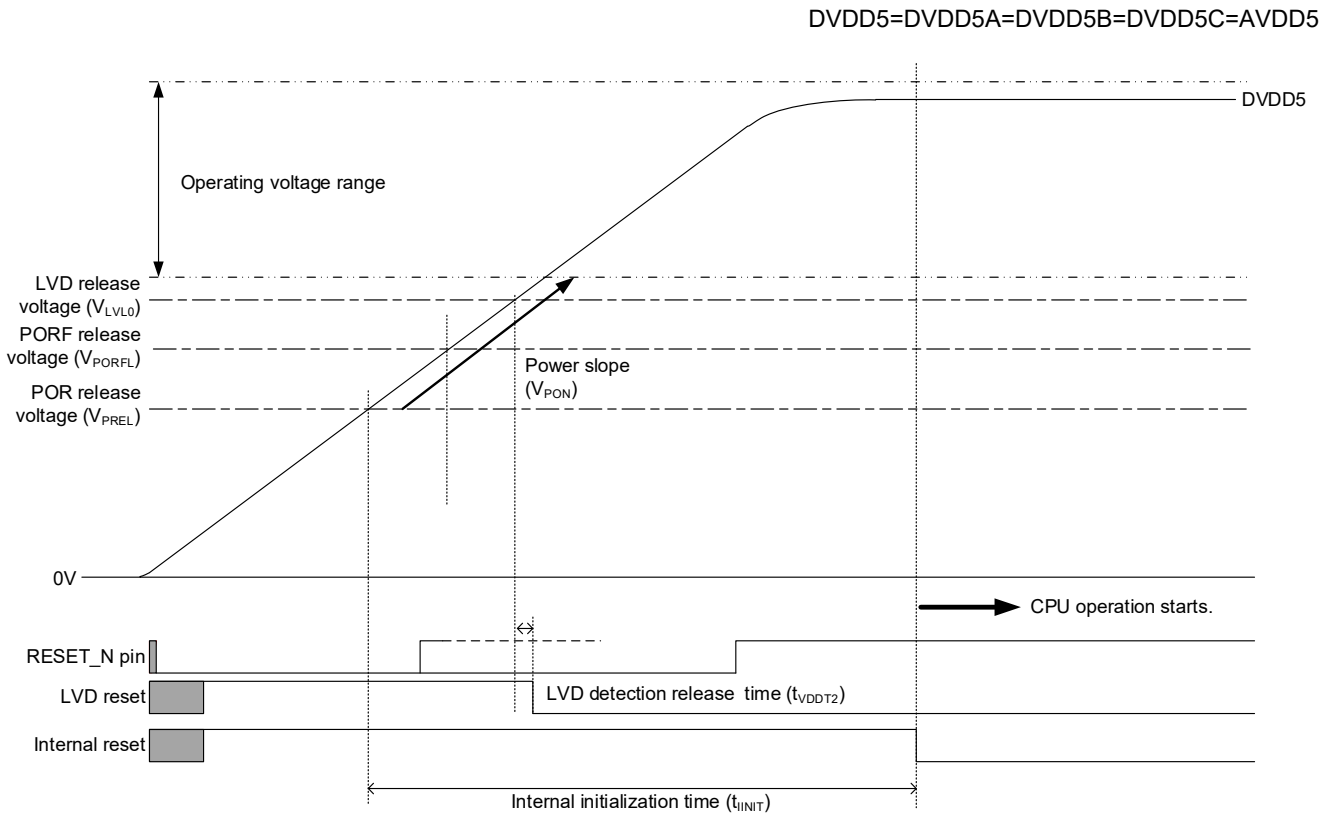
When the power supply is turned on, the timing of reset release by using RESET\_N pin can be controlled.

After a supply voltage exceeds the release voltage of a power-on reset circuit and even after "Internal initialization time" elapsed, if the RESET\_N pin is "Low", internal reset keeps "Low" continuously. After a supply voltage goes up to an operating voltage range, if a RESET\_N pin becomes "High", the internal reset is released after "CPU operation wait time" elapses.



**Figure 3.2 Reset by RESET\_N pin (1)**

In case of RESET\_N pin input change from "Low" to "High" before "Internal initialization time" elapses, internal reset signal is released after "Internal initialization time" elapses. Goes up a supply voltage within an operating voltage range before "Internal initialization time" elapses. The CPU operates after internal reset release.



**Figure 3.3 Reset by RESET\_N Pin (2)**

### 3.2.1.3. Continuation of Reset by LVD

When the power supply voltage has not exceeded the LVD release voltage even after "Internal initialization time" elapsed, LVD generates the reset signal and keeps the reset state. After the power supply voltage exceeds the LVD release voltage and "LVD detection release time" + "CPU operation wait time" elapses, the internal reset is released. And the CPU starts operation. Refer to the Reference Manual "Voltage Detection Circuit" for details of LVD.

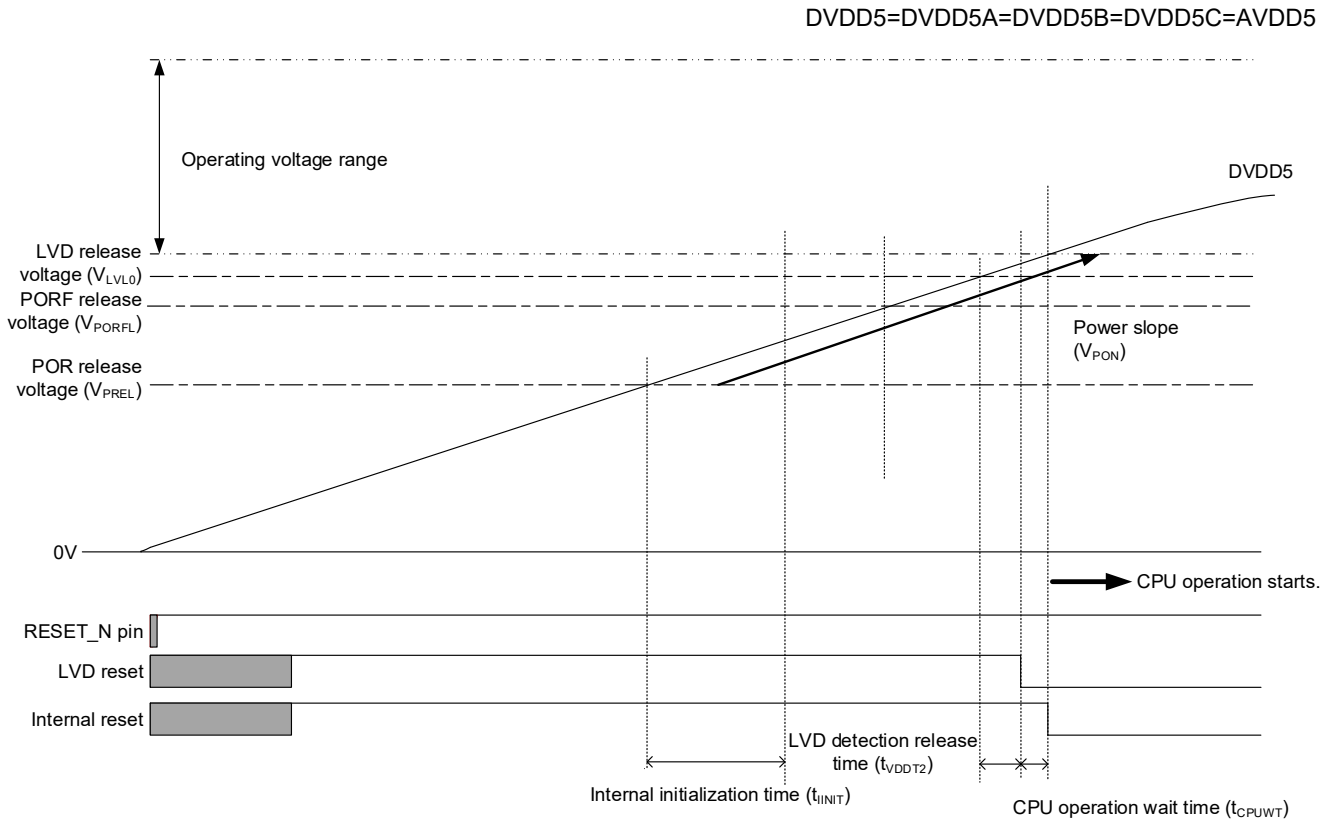


Figure 3.4 Reset Operation by LVD Reset

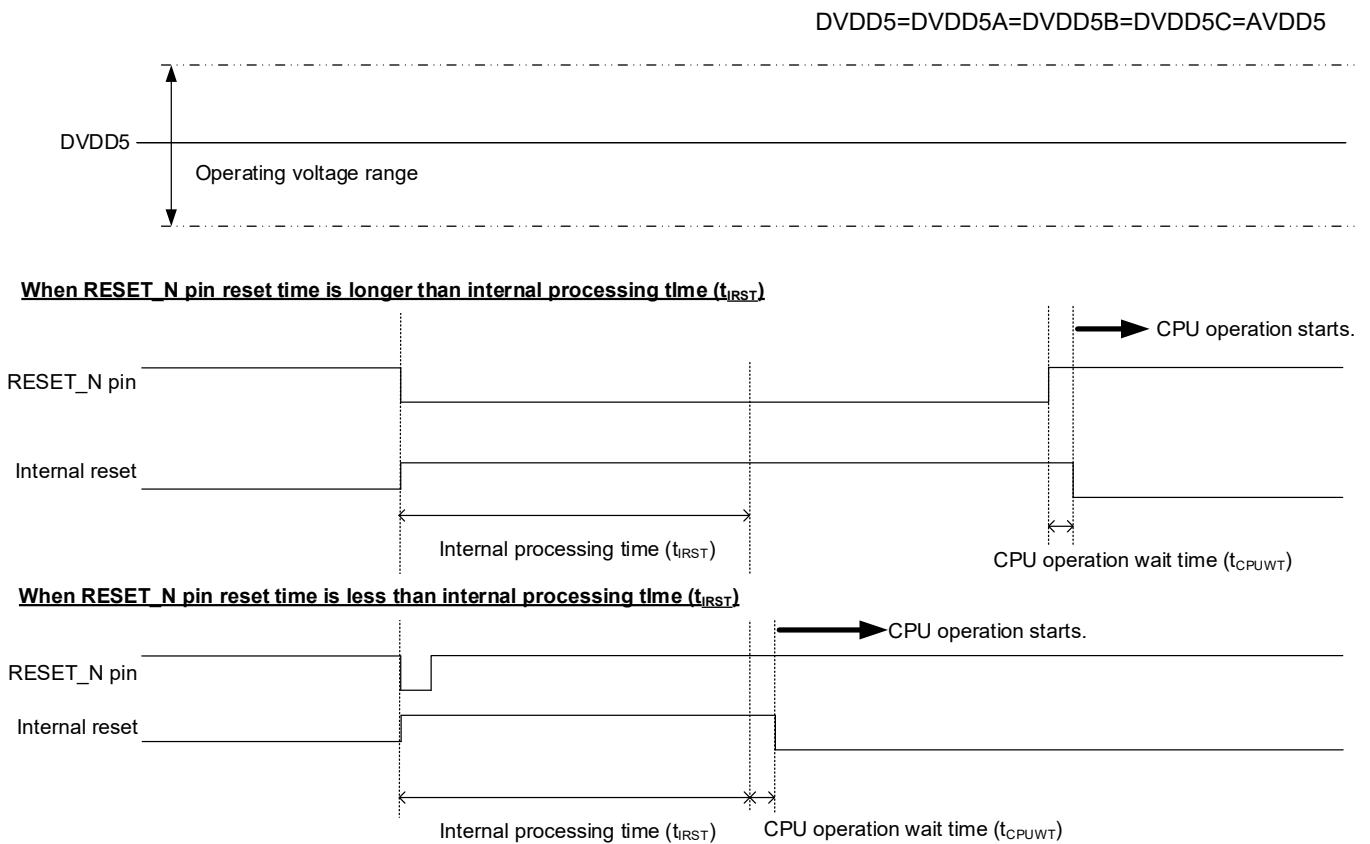
## 3.2.2. Warm Reset

### 3.2.2.1. Warm Reset by RESET\_N Pin

When resetting with the RESET\_N pin, set the RESET\_N pin to "Low" for 17.2  $\mu$ s or more while the power supply voltage is within the operating range.

When the "Low" period of the RESET\_N pin is longer than "Internal processing time", after the RESET\_N pin changes to "High", the internal reset is released after "CPU operation wait time" elapsed.

When the "Low" period of a RESET\_N pin is shorter than "Internal processing time", after internal reset is extended and from a RESET\_N pin changes to "Low", the Internal reset is released after "Internal processing time" + "CPU operation wait time" has elapsed.



**Figure 3.5 Warm Reset Operation**

### 3.2.2.2. Warm Reset by LVD

The LVD resets correctly when the power supply voltage is the LVD release or detection voltage or lower and is within the operating voltage range. When the time which the power supply voltage is the LVD release or detection voltage or lower is longer than the "Internal processing time", the built-in reset is released when the following conditions are satisfied; 1. after "Internal processing time" has elapsed, 2. "LVD detection release time" + "CPU operation wait time" has elapsed after the power supply voltage exceeds to the LVD release voltage. When it is shorter than "Internal processing time", the internal reset is released after "Internal processing time" + "CPU operation wait time" has elapsed from generating LVD reset.

### 3.2.2.3. Warm Reset by Other Internal Resets

When the reset by internal source, such as SIWDT, OFD, LOCKUP, and <SYSRESETREQ> occurs, the internal reset is released after "Internal processing time" + "CPU operation wait time" elapsed.

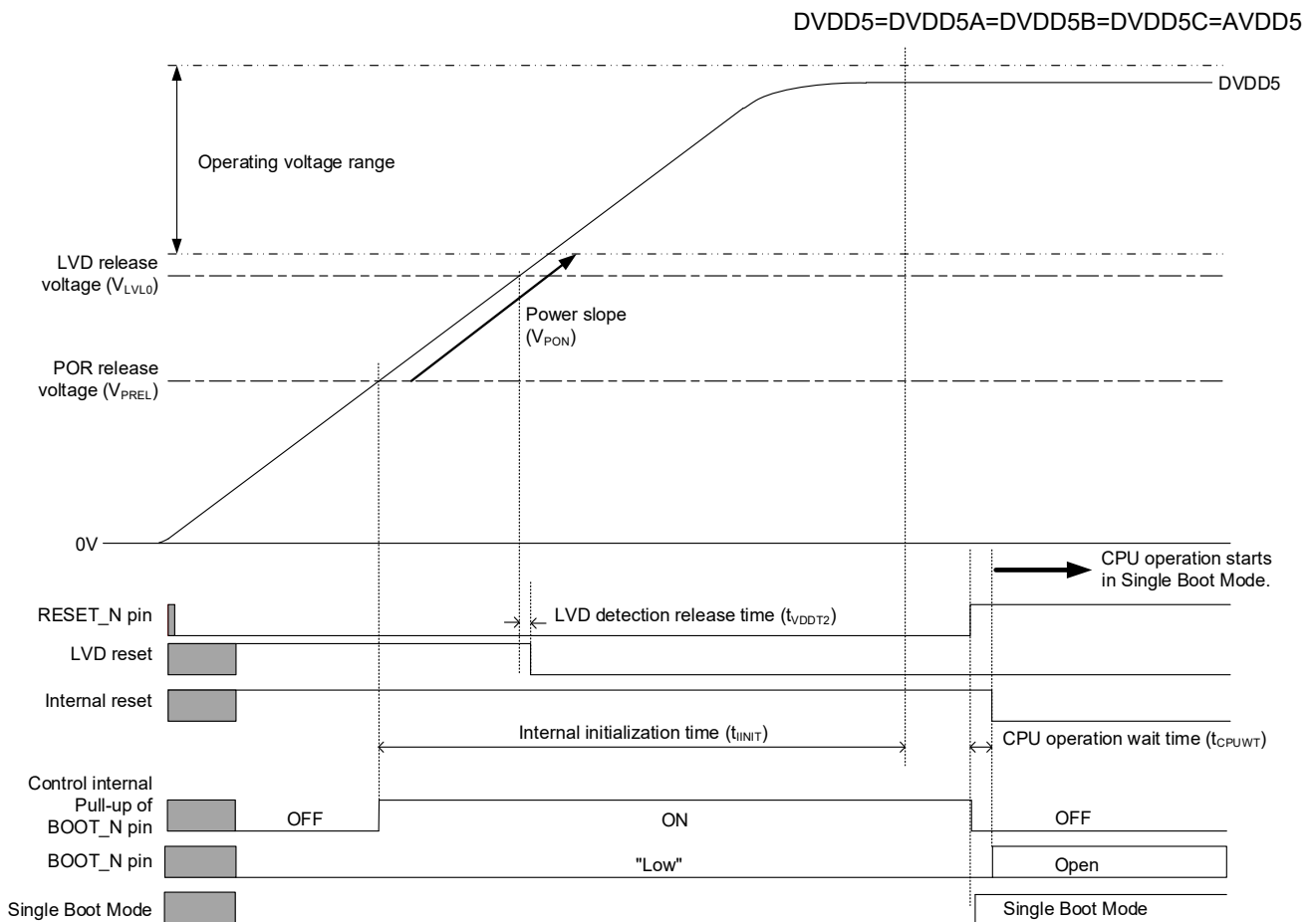
### 3.2.3. Starting Single Boot Mode

Refer to the Reference Manual "Flash Memory" for details of "Single Boot Mode".

#### 3.2.3.1. Starting Single Boot Mode by RESET\_N Pin

When BOOT\_N pin is input "Low", if reset is released by RESET\_N pin (the RESET\_N pin is changed from "Low" to "High"), "Single Boot Mode" is started.

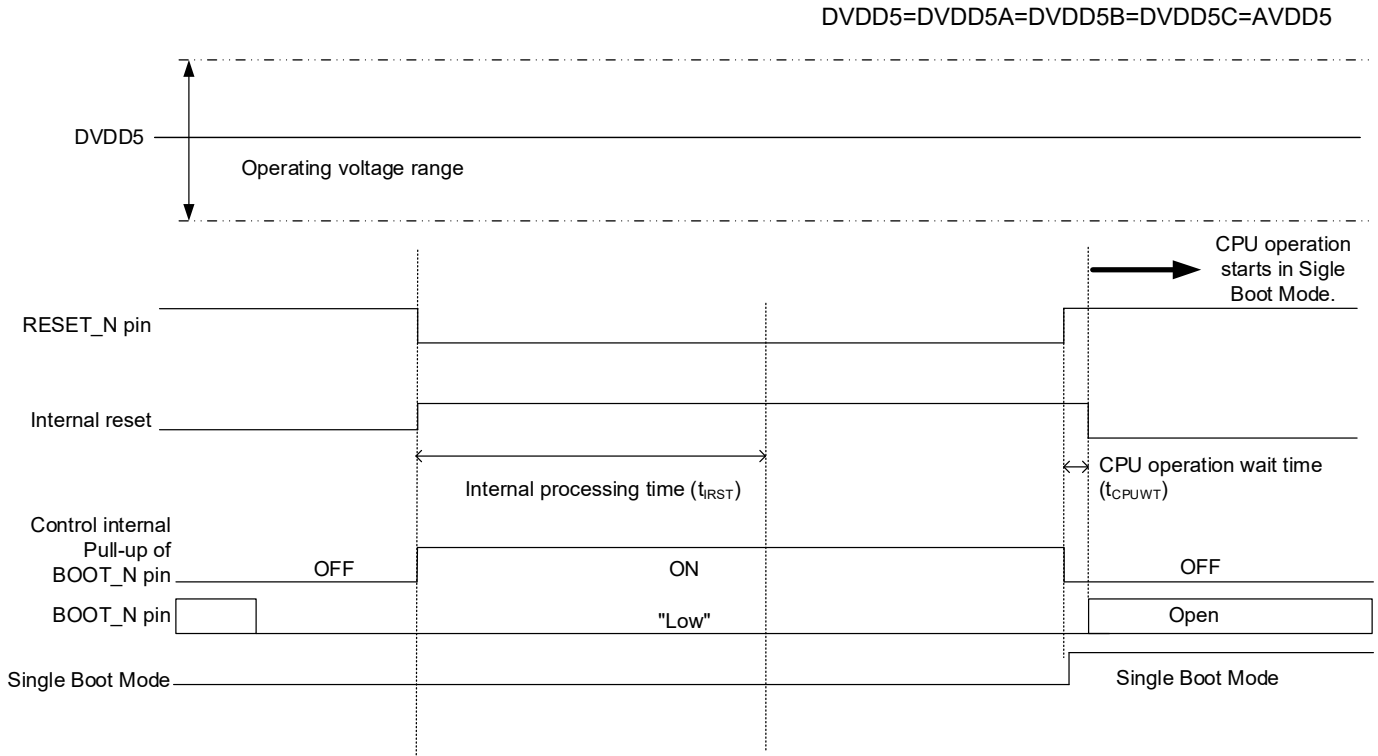
When turn on a power supply, input "Low" to the RESET\_N pin "Internal initialization time" or longer to reset. And release reset after a supply voltage goes up within an operating voltage range.



**Figure 3.6 Starting Single Boot Mode by RESET\_N Pin when Power Supply is Turned On**

**3.2.3.2. Starting Single Boot Mode when Power Supply Voltage is Stable**

When a power supply voltage is stable within an operating voltage range, input "Low" to the RESET\_N pin "Internal initialization time" or longer to reset while the BOOT\_N pin is input "Low". And release reset (the RESET\_N pin is changed from "Low" to "High").



**Figure 3.7 Starting Single Boot Mode when Power Supply Voltage is Stable**

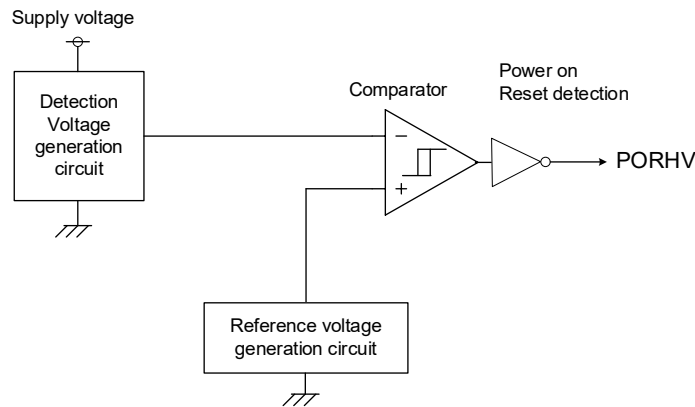
### 3.2.4. Power-on Reset Circuit

The power-on reset circuit (POR) generates a reset signal when the power supply is turned on or turned off.

Note: The power-on reset circuit may not operate correctly due to the fluctuation of the power supply. Equipment should be designed with full consideration of the electrical characteristics.

The power-on reset circuit consists of a detection voltage generation circuit, a reference voltage generation circuit, and a comparator.

The supply voltage in Figure 3.8 means DVDD5 (= DVDD5A = DVDD5B = DVDD5C).



**Figure 3.8 Power-on Reset Circuit**

#### 3.2.4.1. Operation when Power Supply is Turned On

When turn on power supply, while the power supply voltage is power-on reset release voltage ( $V_{PREL}$ ) or lower, the power-on reset signal is generated. Refer to "Figure 3.1 Reset by Power-on Reset Circuit" for details.

While the power-on reset signal is generated, the CPU and peripheral functions are reset.

#### 3.2.4.2. Operation when Power Supply is Turned Off

When turn off power supply or when the power supply voltage is power-on reset release voltage ( $V_{PDET}$ ) or lower, the power-on reset signal is generated.

While the power-on reset signal is generated, the CPU and peripheral functions are reset.

### 3.2.5. Turning Off and Re-turning On of Power Supply

When the power supply is turned off, the power supply voltage must be down gentler gradient than Max value of "Power gradient ( $V_{POFF}$ )" specified in "Electrical Characteristics".

#### 3.2.5.1. When Using External Reset Circuit or Built-in LVD Reset

When the power supply is turned off and the power supply voltage drops below the operation voltage range, the power supply voltage becomes the detection voltage of the external reset circuit or built-in LVD or lower, causing the reset occurs. From this reset state, the power supply voltage must go up by keeping constraints as same as turning on the power supply.

#### 3.2.5.2. When not Using External Reset Circuit and Built-in LVD Reset Output

When the power supply is turned off and the power supply voltage drops below the operation voltage range, the power supply voltage must drop the power-on reset detection voltage ( $V_{PDET}$ ) or lower and this state must be kept for 200  $\mu$ s or more. After that, the power supply voltage must go up by keeping rule as same as turning on the power supply.

If the power supply voltage drops below the power-on reset detection voltage ( $V_{PDET}$ ) and this state cannot be kept for 200  $\mu$ s or more, or if the same constraints as turning on the power supply cannot be kept, TMPM4H Group (1) may not operate properly.

### 3.2.6. After Reset Release

The control register of the Cortex-M4 (with FPU) processor core and control registers (SFR) of the peripheral functions are initialized by reset. But, initialized range of circuits is different depend on the reset factor.

Refer to "Table 3.1 " for the initialized range of circuit by each reset factor.

The reset factor when reset occurs can be checked by the reset flag registers which are *[RLMRSTFLG0]* and *[RLMRSTFLG1]*. For details of *[RLMRSTFLG0]* and *[RLMRSTFLG1]*, refer to the Reference Manual "Exception".

After reset is released, TMPM4H Group (1) starts operation by a clock of internal high-speed oscillator 1 (IHOSC1). The external high-speed oscillator clock and PLL multiple circuit should be set if necessary.

### 3.2.6.1. Reset Factors and Initialized Range of Circuits

The reset factors and initialized range of circuits are shown in Table 3.1.

**Table 3.1 Reset Factors and Initialized Range of Circuits**

Registers and peripheral functions		Reset factors							
		Cold reset	Warm reset						
		POR	Reset pin	OFD reset	SIWDT reset	LVD reset	CPU <SYS RESET REQ> reset	CPU LOCKUP reset	PORF reset
Reset signal name	PORHV	RESET_N	OFD RSTOUT	SIWDT RSTOUT	LVD RSTOUT	SYS RESET REQ	LOCKUP RESET REQ	PORF RESET	
Reset flag	[RLMRSTFLG0] [RLMRSTFLG1]	✓	-	-	-	-	-	-	-
Interrupt control	[IAIMCxx] [IANIC00]	✓	✓	✓	✓	✓	✓	✓	✓
	[IBIMCxxx] [IBNIC00]	✓	✓	✓	✓	✓	✓	✓	✓
Flash memory	[FCBMR]	✓	-	-	-	-	-	-	✓
PORT	All registers	✓	✓	✓	✓	✓	✓	✓	✓
OFD		✓	✓	✓	✓	✓	✓	✓	✓
LVD		✓	✓	-	-	-	-	-	-
Debug interface		✓	-	-	-	-	-	-	✓
Others		✓	✓	✓	✓	✓	✓	✓	✓

- ✓: It is initialized.
- : It is not initialized.

Note: When reset is performed, the data of built-in RAM will not be guaranteed.

## 4. Revision History

**Table 4.1 Revision History**

Revision	Date	Description
1.0	2026-04-24	- First release

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