Toshiba BiCD Process Integrated Circuit Silicon Monolithic

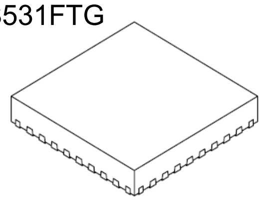
TB67S531FTG

BiCD Constant-Current Two-Phase Bipolar Stepping Motor Driver IC

1. Description

TB67S531FTG is a two-phase bipolar stepping motor driver using a PWM chopper.
Fabricated with the BiCD process, TB67S531FTG is rated at 40 V/2.0 A (Absolute maximum ratings).
A stepping motor can be operated with a single VM power supply by built-in regulator.

TB67S531FTG



P-VQFN32-0505-0.50-008

Weight:0.066 g (typ.)

2. Features

- BiCD process monolithic IC.
- Capable of controlling bipolar stepping motor.
- Advanced Current Detect System (ACDS) realizes a PWM constant-current control without external current detection resistors.
- Advanced Dynamic Mixed Decay (ADMD) realizes a high efficiency PWM constant-current control.
- Phase input control.
- Operational in full, half, quarter step resolutions.
- BiCD process: Use DMOSFET for the output power transistor.
- High voltage / high current drive: 40 V / 2.0 A (Absolute maximum ratings).
- Thermal shutdown (TSD), over-current detection (ISD), and under voltage lockout (UVLO).
- The charge pump requires no external components.
- Package: QFN32 (5 mm × 5 mm).

Start of commercial production
2026-03

3. Block Diagram

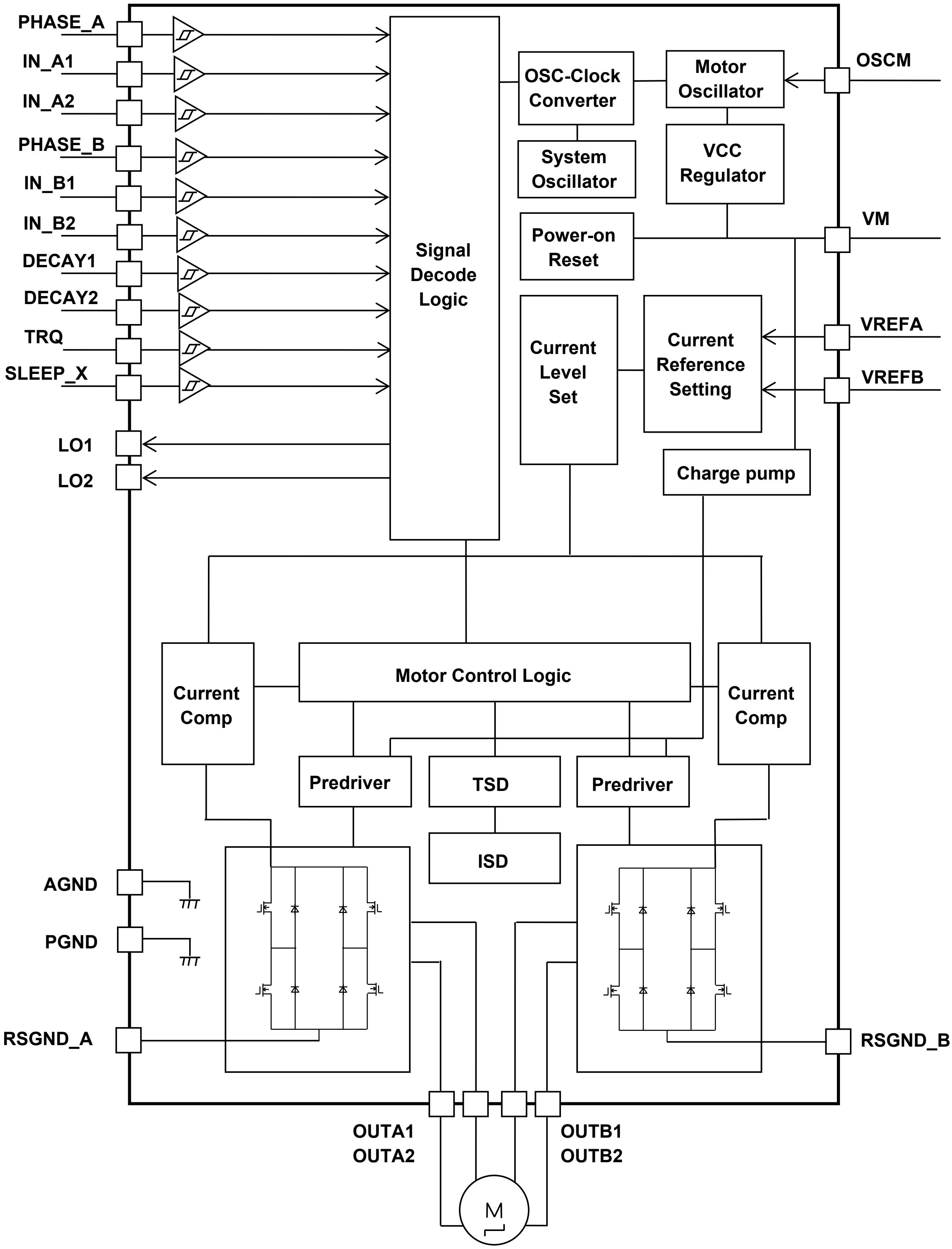


Figure 3.1 Block Diagram

Note: Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Note: All the grounding wires of TB67S531FTG should run on the solder mask on the PCB and be externally terminated at only one point. Also, a grounding method should be considered for efficient heat dissipation. Careful attention should be paid to the layout of the output, VM and GND traces, to avoid short circuits across output pins or to the power supply or ground. If such a short circuit occurs, the device may be permanently damaged. Also, the utmost care should be taken for pattern designing and implementation of the device since it has power supply pins (VM, OUTA1, OUTA2, OUTB1, OUTB2, AGND, PGND, RSGND_A, and RSGND_B) through which a particularly large current may run. If these pins are wired incorrectly, an operation error may occur or the device may be destroyed. The logic input pins must also be wired correctly. Otherwise, the device may be damaged owing to a current running through the IC that is larger than the specified current. Careful attention should be paid to design patterns and mountings.

4. Pin Assignments

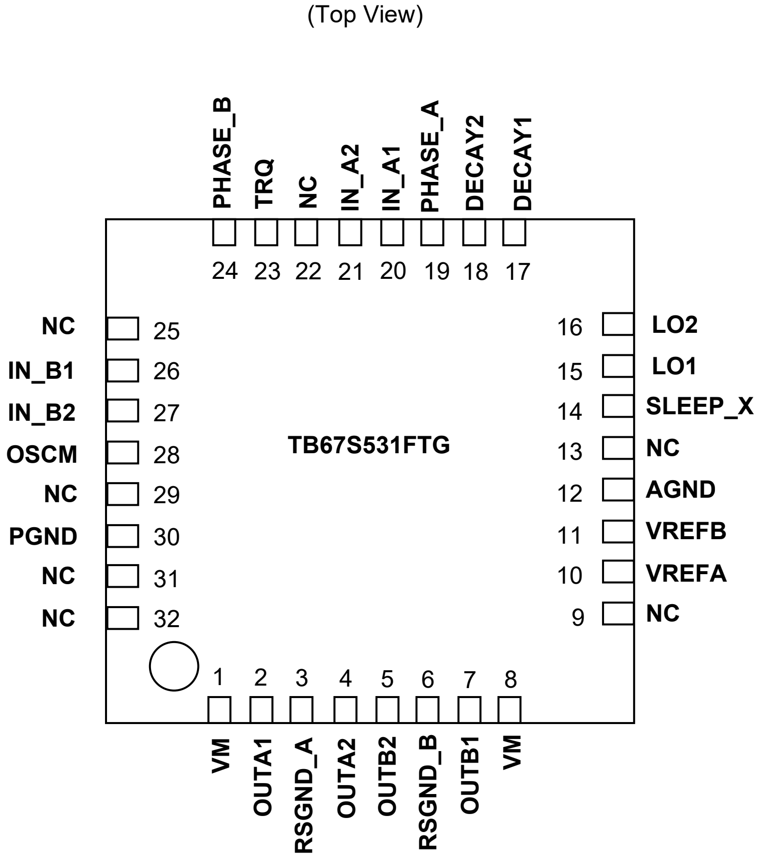


Figure 4.1 Pin Assignments

5. Pin Description

5.1. Pin Function Description TB67S531FTG

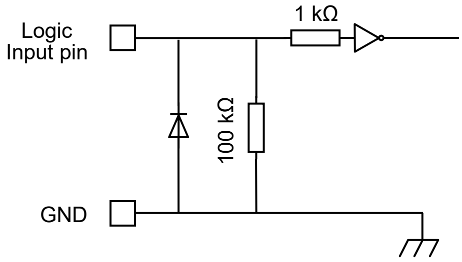
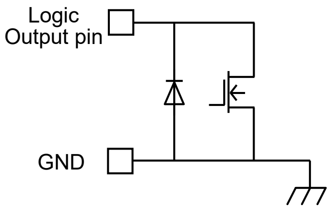
Table 5.1 Pin Function Description

Pin number	Pin name	Function
1	VM	VM voltage input pin
2	OUTA1	Motor A ch output pin
3	RSGND_A	Motor A ch GND pin
4	OUTA2	Motor A ch output pin
5	OUTB2	Motor B ch output pin
6	RSGND_B	Motor B ch GND pin
7	OUTB1	Motor B ch output pin
8	VM	VM voltage input pin
9	NC	Non connection
10	VREFA	A ch output current threshold reference pin
11	VREFB	B ch output current threshold reference pin
12	AGND	GND pin
13	NC	Non connection
14	SLEEP_X	SLEEP signal input pin
15	LO1	Reset signal output pin at error detection
16	LO2	Reset signal output pin at error detection
17	DECAY1	Constant-current chopping control change pin
18	DECAY2	Constant-current chopping control change pin
19	PHASE_A	Control signal input pin for Ach motor output
20	IN_A1	Control signal input pin for Ach motor output
21	IN_A2	Control signal input pin for Ach motor output
22	NC	Non connection
23	TRQ	Torque change pin
24	PHASE_B	Control signal input pin for Bch motor output
25	NC	Non connection
26	IN_B1	Control signal input pin for Bch motor output
27	IN_B2	Control signal input pin for Bch motor output
28	OSCM	Resistor connection pin for OSCM setting
29	NC	Non connection
30	PGND	Motor output GND pin
31	NC	Non connection
32	NC	Non connection

Note: NC pins should be set open.

5.2. Input and Output Equivalent Circuit

Table 5.2 Input and Output Equivalent Circuit

<table>
<tr><th>Pin name</th><th>Input-Output equivalent circuit</th></tr>
<tr><td>PHASE_A, IN_A1, IN_A2
PHASE_B, IN_B1, IN_B2
TRQ, SLEEP_X
DECAY1, DECAY2</td><td>
</td></tr>
<tr><td>LO1</td><td>
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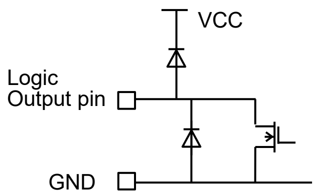
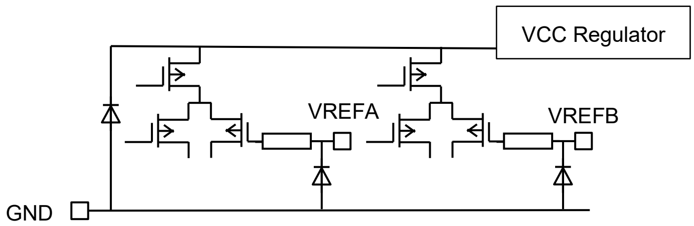
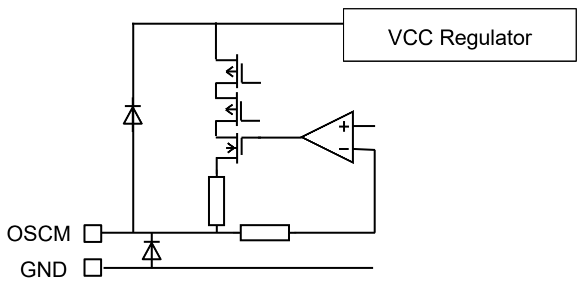
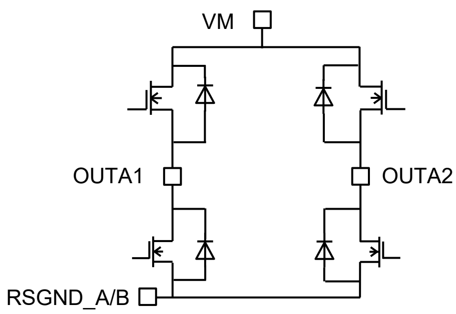
<tr><td>LO2</td><td>
</td></tr>
<tr><td>VREFA
VREFB</td><td>
</td></tr>
<tr><td>OSCM</td><td>
</td></tr>
<tr><td>VM
OUTA1
OUTA2
OUTB1
OUTB2
RSGND_A
RSGND_B</td><td>

Note: Same as OUTB1 and OUTB2</td></tr>
</table>

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

6. Functional Description: TB67S531FTG

6.1. SLEEP_X function

The operation can resume from the output forced off state, which is configured by the thermal shutdown detection (TSD) and the over-current detection (ISD), by setting SLEEP mode once and then setting the normal operation mode again. The SLEEP_X pin is set to Low, and SLEEP mode is set after 114.75 μs(Max). The SLEEP_X pin is set to High, and normal mode resumes after 10 ms(Max).

Table 6.1 SLEEP_X function

SLEEP_X	Function
L	SLEEP mode (Charge pump stop, and VCC Reg stop)
H	Normal operation

6.2. Phase input control mode

6.2.1. Functions of IN_A1, IN_A2, IN_B1, IN_B2, PHASE_A, PHASE_B

Table 6.2 Functions of IN_A1, IN_A2, IN_B1, IN_B2, PHASE_A, PHASE_B

Input			Output		
PHASE_A PHASE_B	IN_A1 IN_B1	IN_A2 IN_B2	OUTA1 OUTB1	OUTA2 OUTB2	IOUT
H	H	H	H	L	100%
	H	L	H	L	71%
	L	H	H	L	38%
	L	L	Output OFF	Output OFF	0%
L	H	H	L	H	-100%
	H	L	L	H	-71%
	L	H	L	H	-38%
	L	L	Output OFF	Output OFF	0%

Definition of current flowing direction at IOUT:
From OUTA1(OUTB1) to OUTA2(OUTB2): Plus current
From OUTA2(OUTB2) to OUTA1(OUTB1): Minus current

6.2.2. Sequence by each drive mode in phase input control mode

6.2.2.1. Full-step resolution

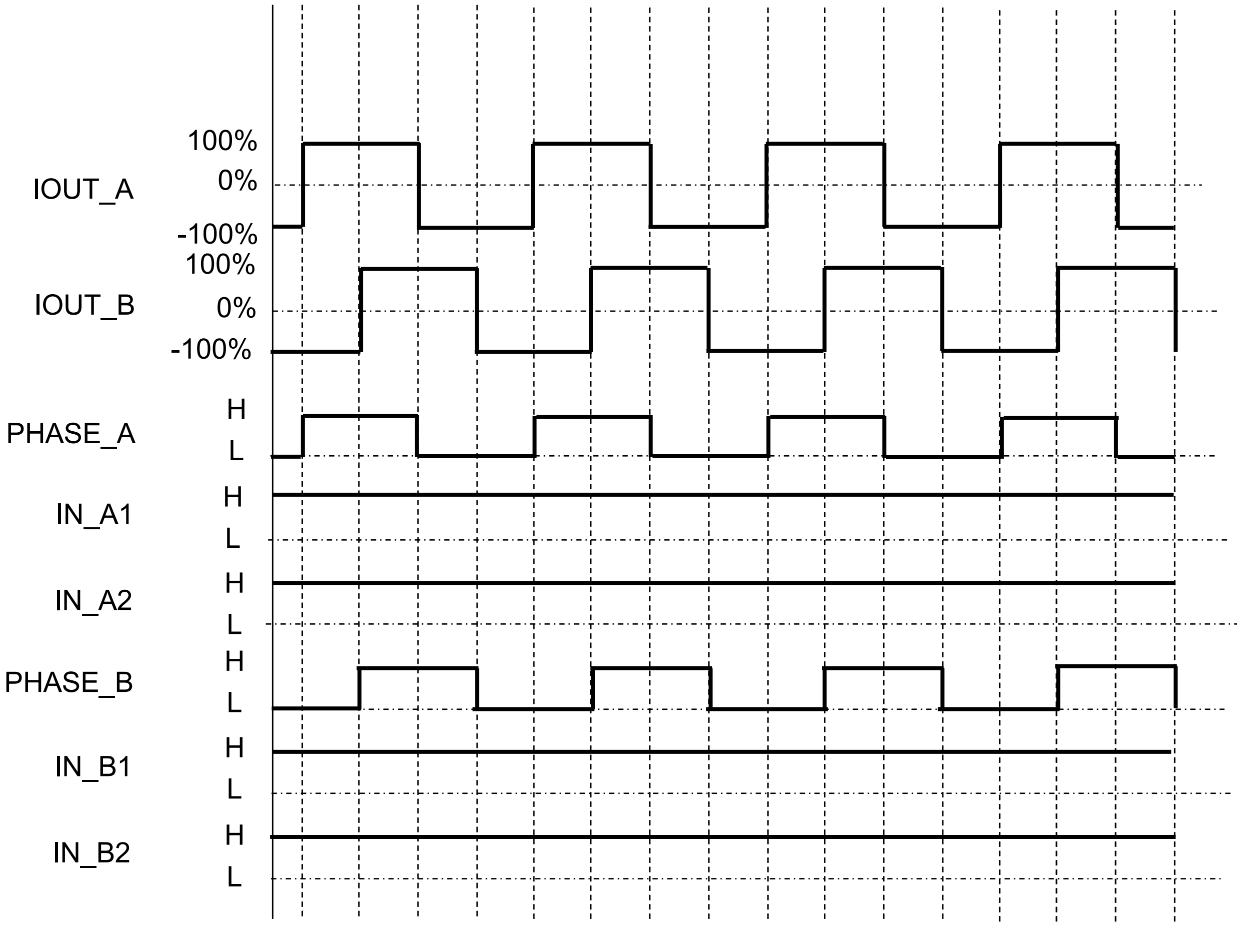


Figure 6.1 Full-step resolution

Note: Timing charts may be simplified for explanatory purpose.

6.2.2.2. Half-step resolution

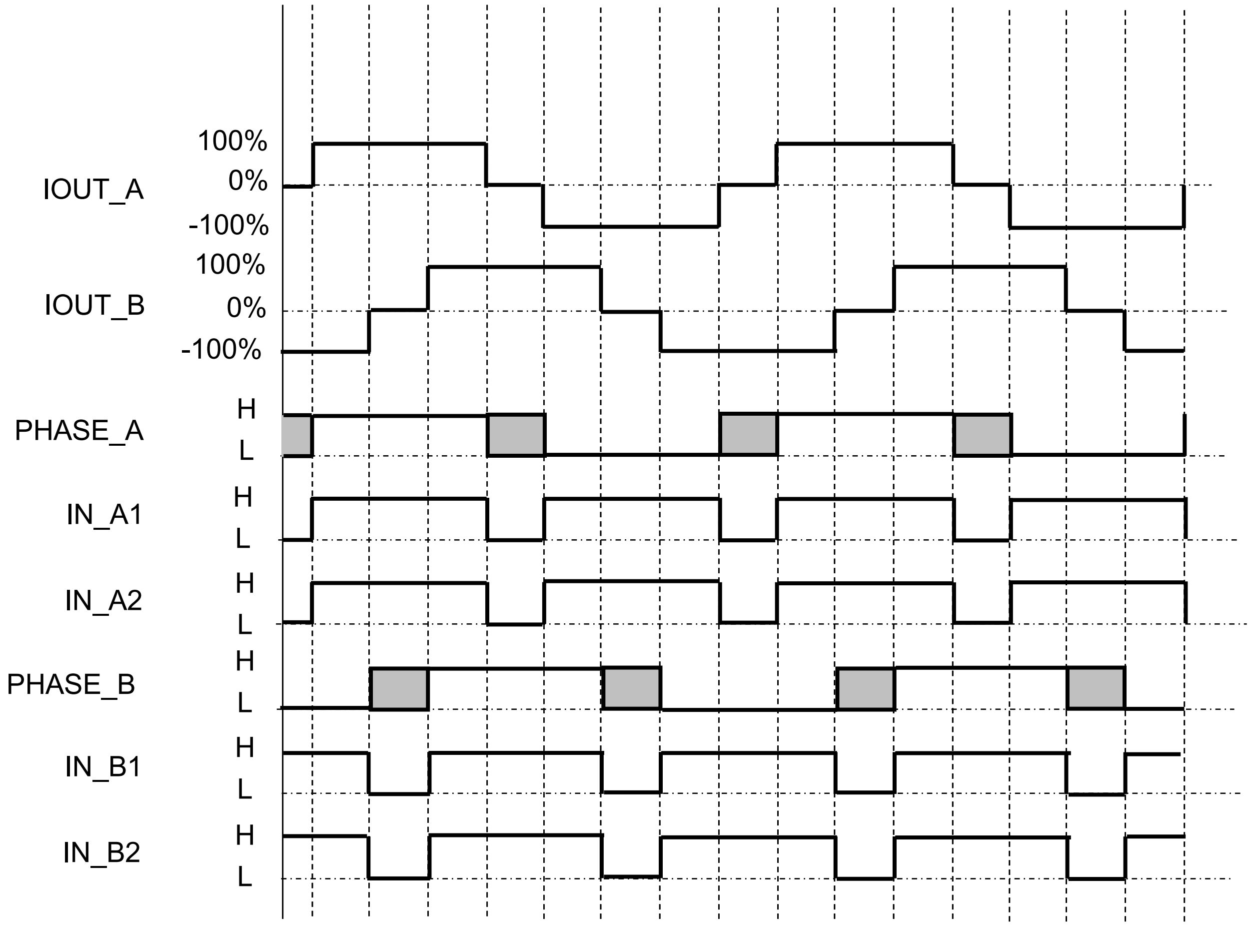


Figure 6.2 Half-step resolution

Note: Timing charts may be simplified for explanatory purpose.

6.2.2.3. Quarter-step resolution

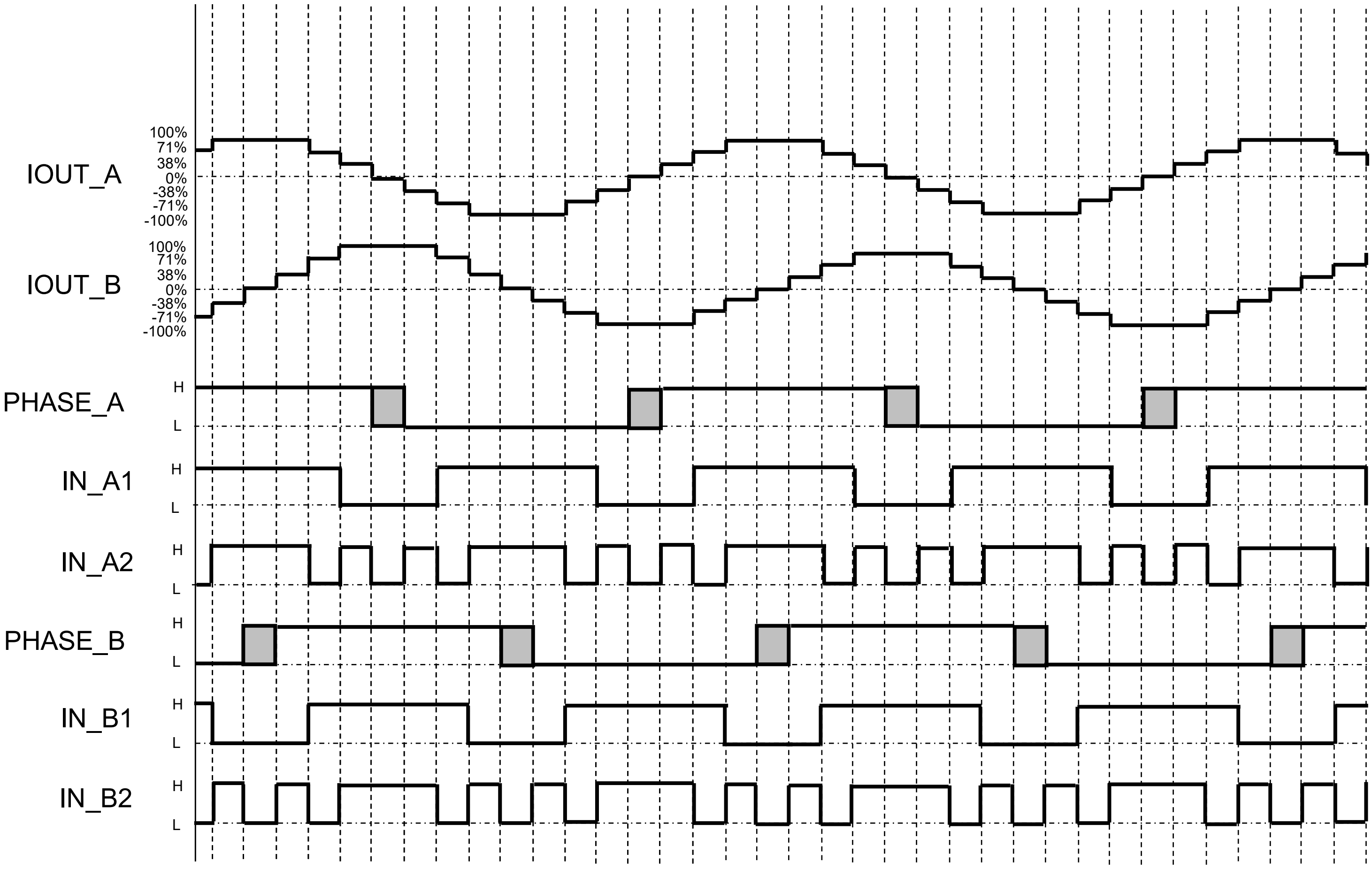


Figure 6.3 Quarter-step resolution

Note: Timing charts may be simplified for explanatory purpose.

6.3. Torque function

TRQ pins set the torque of the motor.

Table 6.3 Torque function

TRQ pin input	Function
L	Torque setting: 100 %
H	Torque setting: 50 %

6.4. Selectable Mixed Decay Function

Selectable Mixed Decay function can adjust the regeneration amount of the current during Decay period using the DECAY pins.
Mixed Decay control is realized by changing three controls: Charge, Slow Decay, and Fast Decay.
The constant-current control can be selected from the following four settings by DECAY pins. When this setting is changed during the constant-current operation, the changed setting is applied from next chopping cycle.

Table 6.4 Selectable Mixed Decay Function

DECAY2 pin	DECAY1 pin	Function
L	L	Mixed Decay
L	H	Slow Decay only
H	L	Fast Decay only
H	H	ADMD

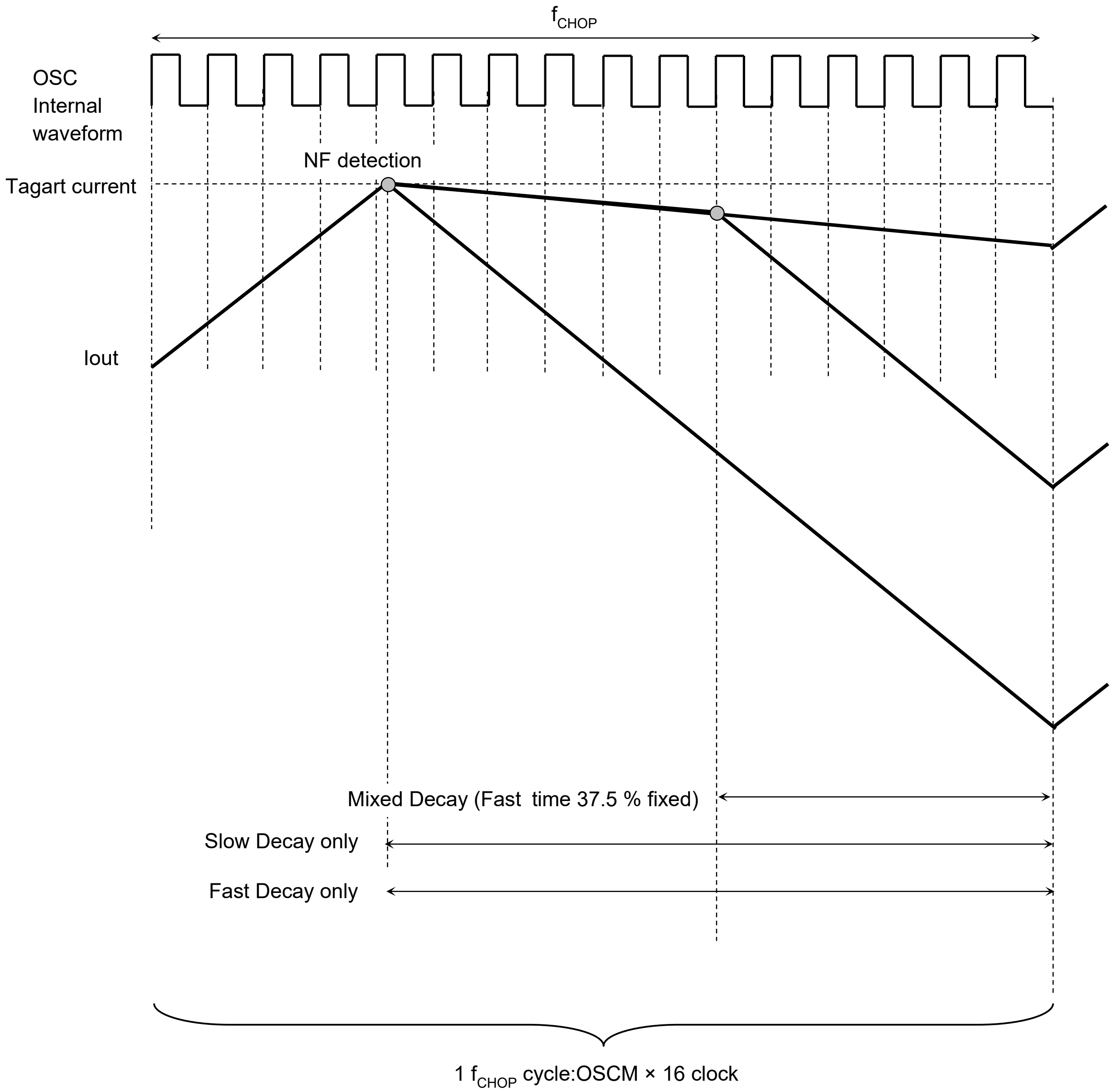


Figure 6.4 Selectable Mixed Decay Function

Note: Timing charts may be simplified for explanatory purpose.

6.4.1. Mixed Decay Waveform (Current Waveform)

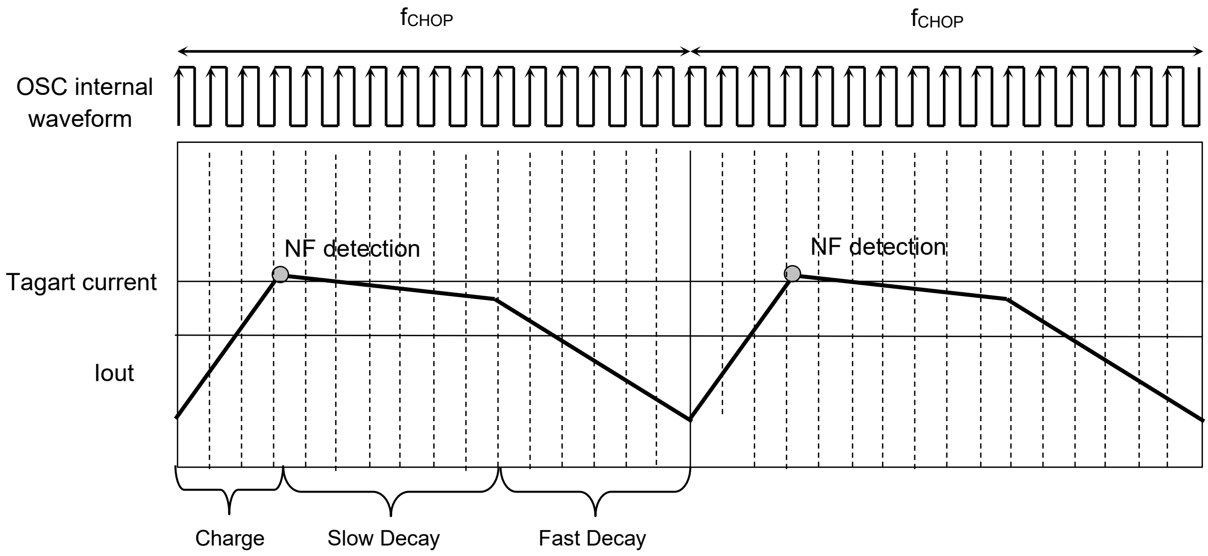


Figure 6.5 Mixed Decay Waveform

Note: Timing charts may be simplified for explanatory purpose.

6.4.2. Each Time of Constant Current PWM Operation

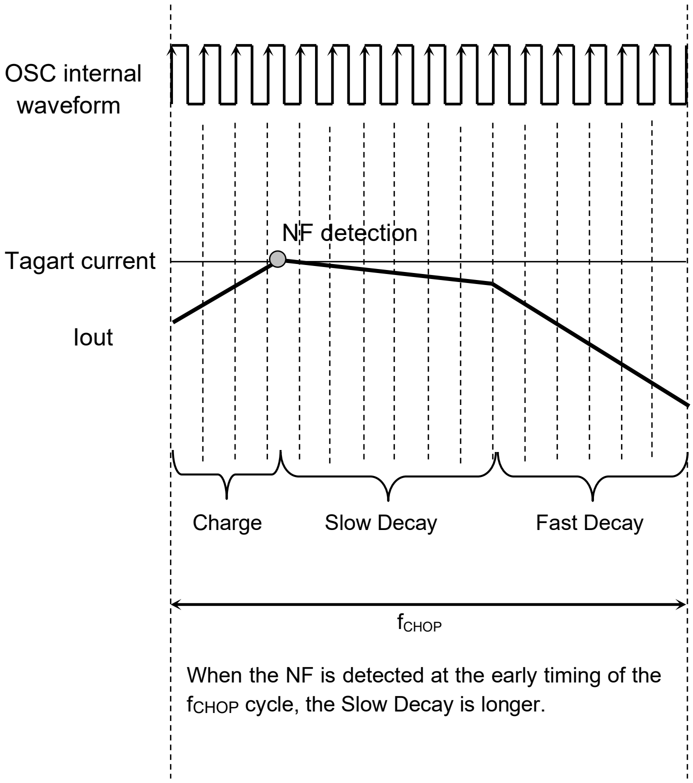


Figure 6.6
Each Time of Constant Current (1)

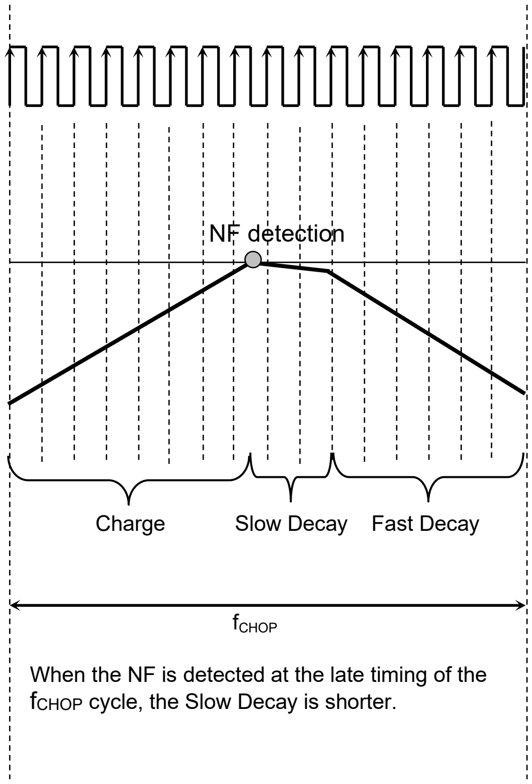


Figure 6.7
Each Time of Constant Current (2)

The Charge period (the time until the motor current reaches the set current value) is determined by the operating status.
Therefore, the NF detection (the motor current reaches the set current value) timing within the chopping cycle will change. When the NF is detected at the early timing of the f_{CHOP} cycle, the Slow Decay is longer. When the NF is detected at the late timing of the f_{CHOP} cycle, the Slow Decay is shorter, as shown above.

Note: The chopping cycle is determined as: f_{CHOP} - (Charge + Fast Decay) = Slow Decay
(Fast Decay time is 37.5 % fixed (OSCM: 6 clocks)
Note: Timing charts may be simplified for explanatory purpose.

6.4.3. Mixed Decay Current Waveform

6.4.3.1. When the set current value is increased

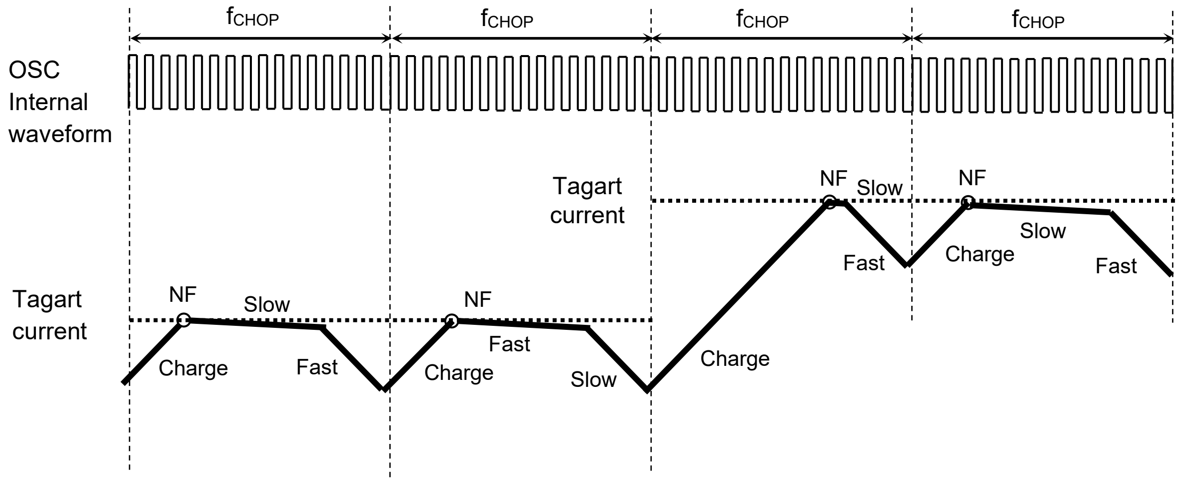


Figure 6.8 When the set current value is increased

6.4.3.2. When the Charge period is more than 1 f_{CHOP} cycle

When the Charge period (the motor current reaches next step of the set current value) is longer than 1 f_{CHOP} cycle, the Charge period extends until the motor current reaches the NF threshold. Once the current reaches the next current step, then the sequence goes on to Mixed Decay control.

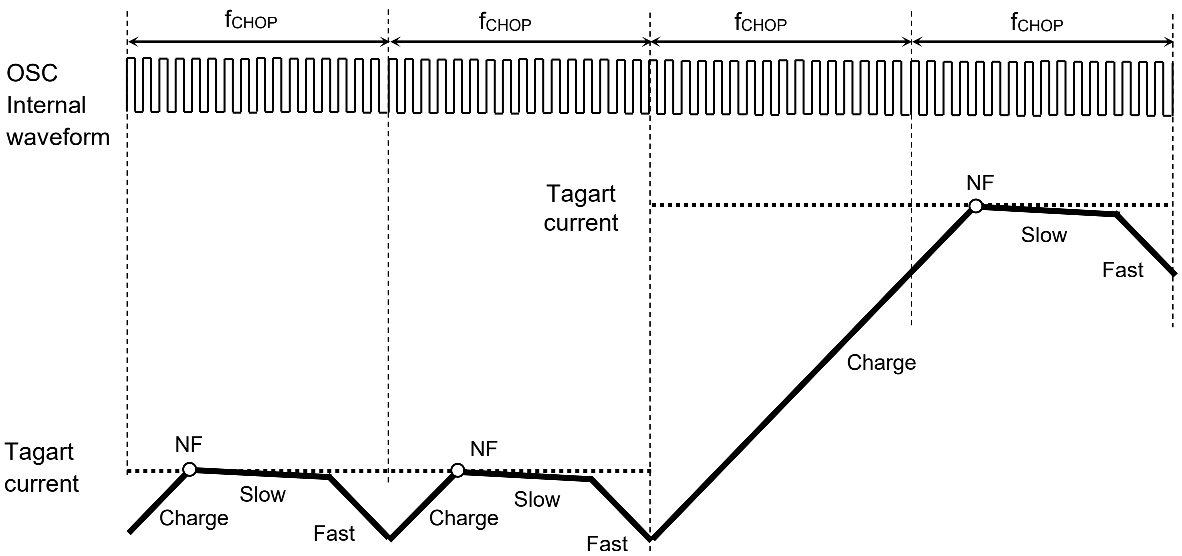


Figure 6.9 When the Charge period is more than 1 f_{CHOP} cycle

6.4.3.3. When the set current value is decreased

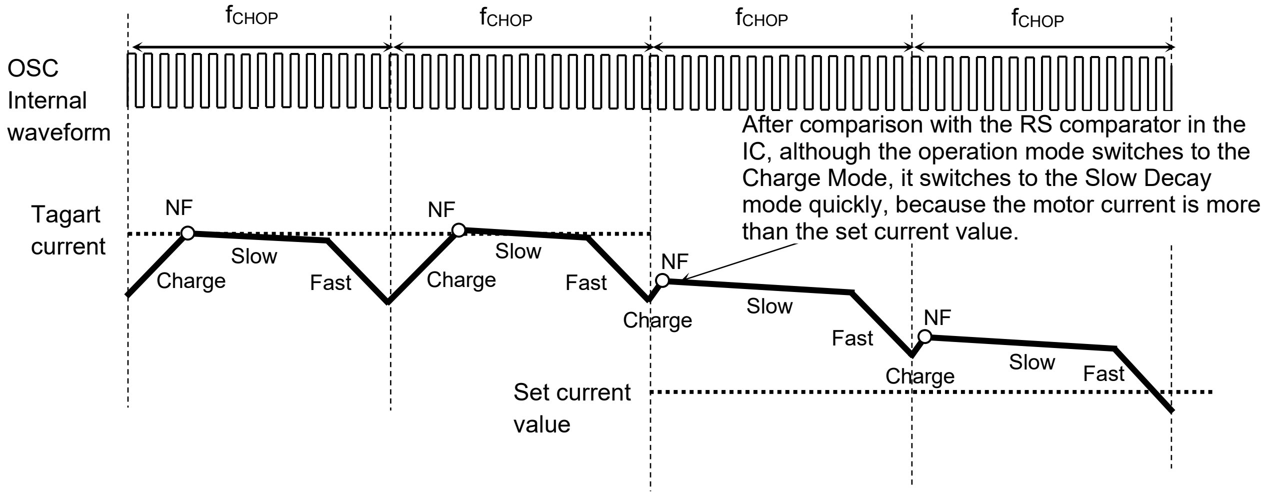


Figure 6.10 When the set current value is decreased

Note: Timing charts may be simplified for explanatory purpose.

6.5. ADMD (Advanced Dynamic Mixed Decay) Constant Current Control

ADMD monitors both the current flowing from the power supply to the motor and the current which regenerates from the motor to the power supply, and performs constant current PWM control.
The basic sequence of the ADMD is as follows.

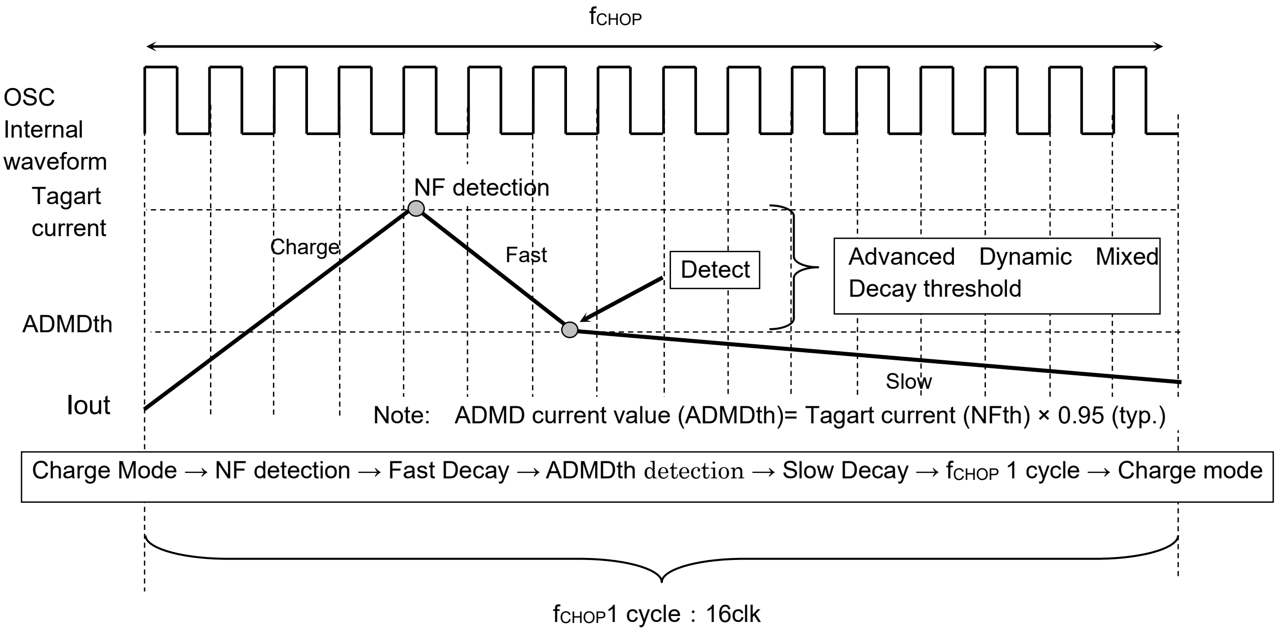


Figure 6.11 ADMD (Advanced Dynamic Mixed Decay) Constant Current Control

Note: Timing charts may be simplified for explanatory purpose. The values in the timing chart are reference values.

Each filter is attached in order to avoid current-detection error caused by the external noise, etc. (Shown in below figure.)
L value of the motor to be used is small, and when the current value reaches ADMDth (ADMD current value) within the ADMDtblank period, it changes to Slow operation after the ADMDtblank period elapsed.
In this case, the ADMD current value (ADMDth) becomes smaller than ''the set current value (NFth) x 0.95 (typ.)''.

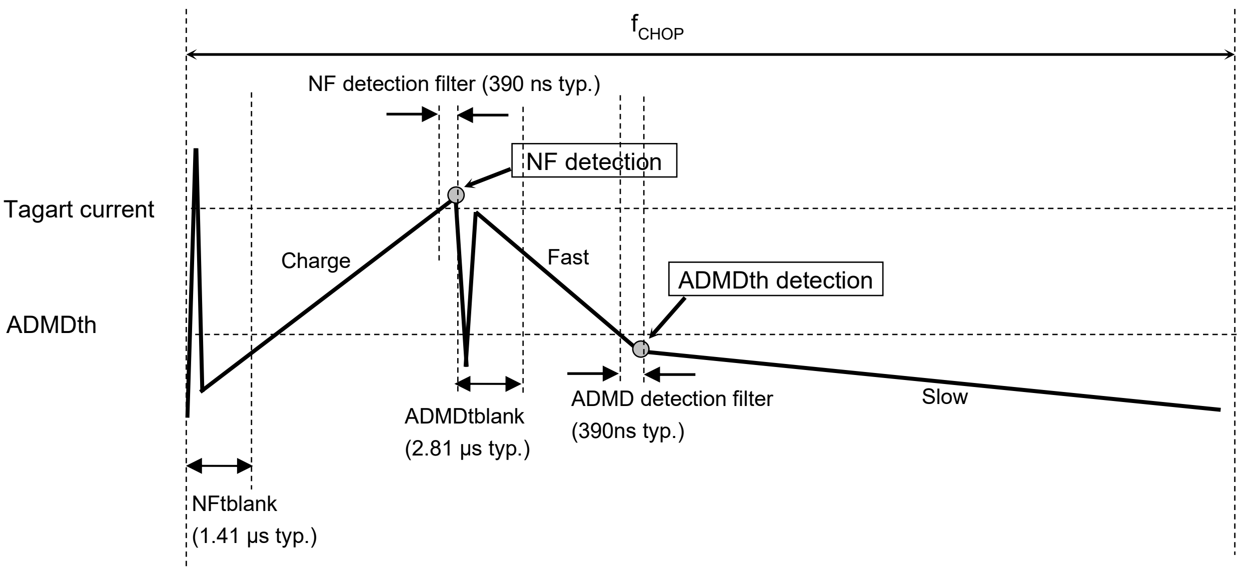


Figure 6.12 Each filter settings

Note: Timing charts may be simplified for explanatory purpose. The values in the timing chart are reference values.

6.6. ADMD Current Waveform

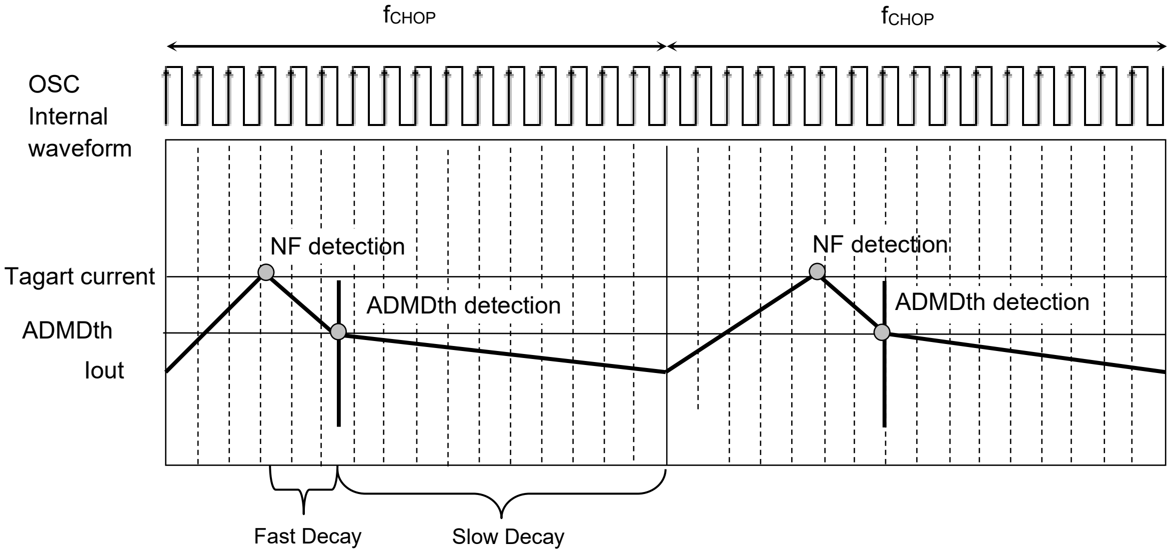


Figure 6.13 Auto Decay Mode Current Waveform

Note: Timing charts may be simplified for explanatory purpose.

6.6.1. When the next current value is increased

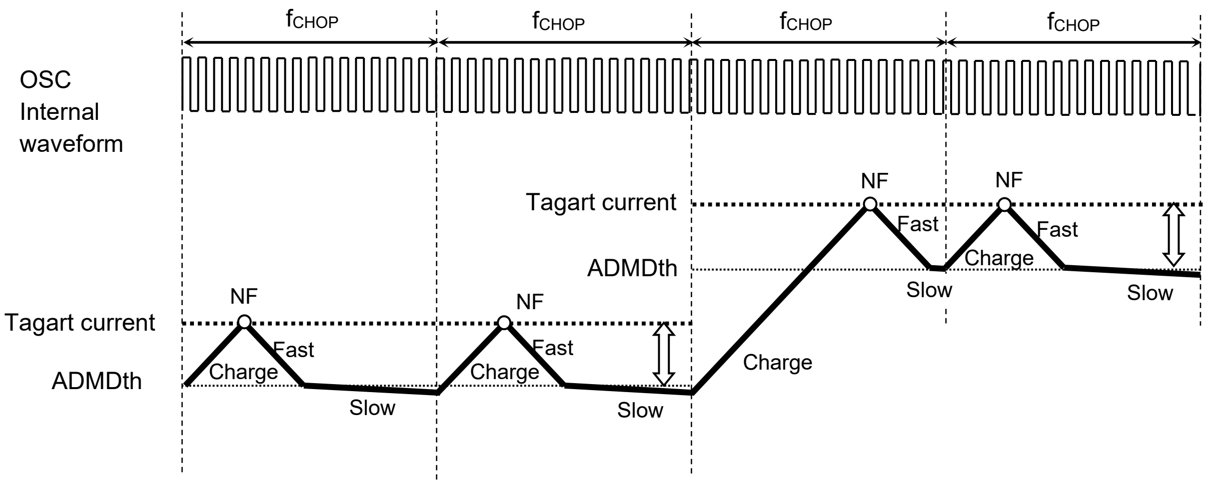


Figure 6.14 When the next current value is increased

6.6.2. When Charge period ≥ 1 f_{CHOP} cycle

When the period until the motor current value reaches the next setting value (Charge period) such as switching.

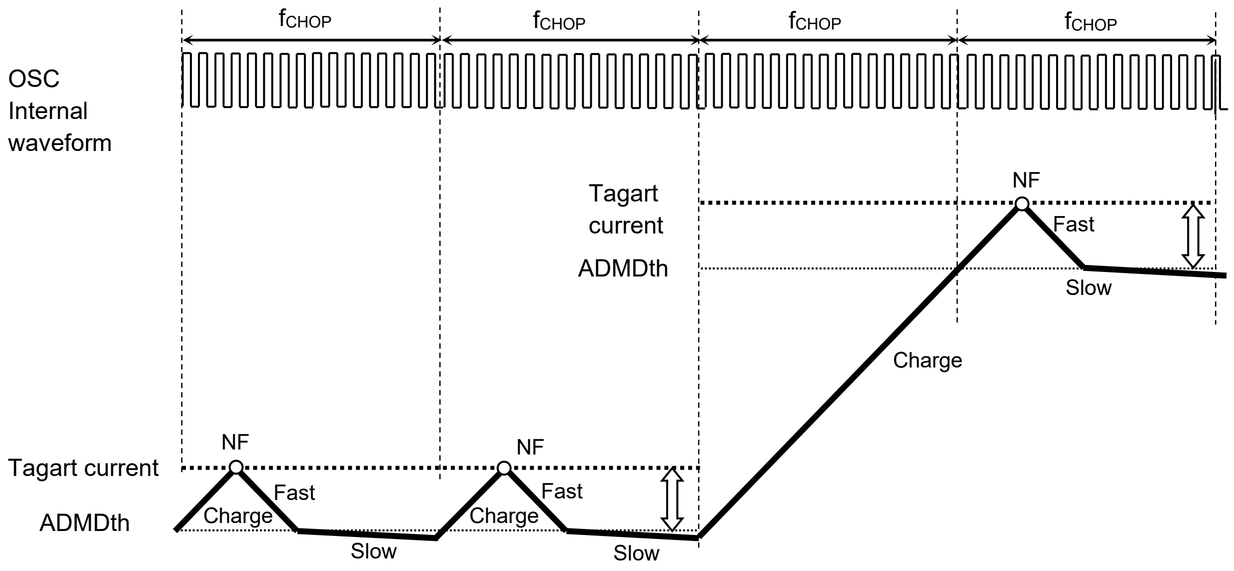


Figure 6.15 When Charge period ≥ 1 f_{CHOP} cycle

Note: Timing charts may be simplified for explanatory purpose.

6.6.3. When the next current value is decreased

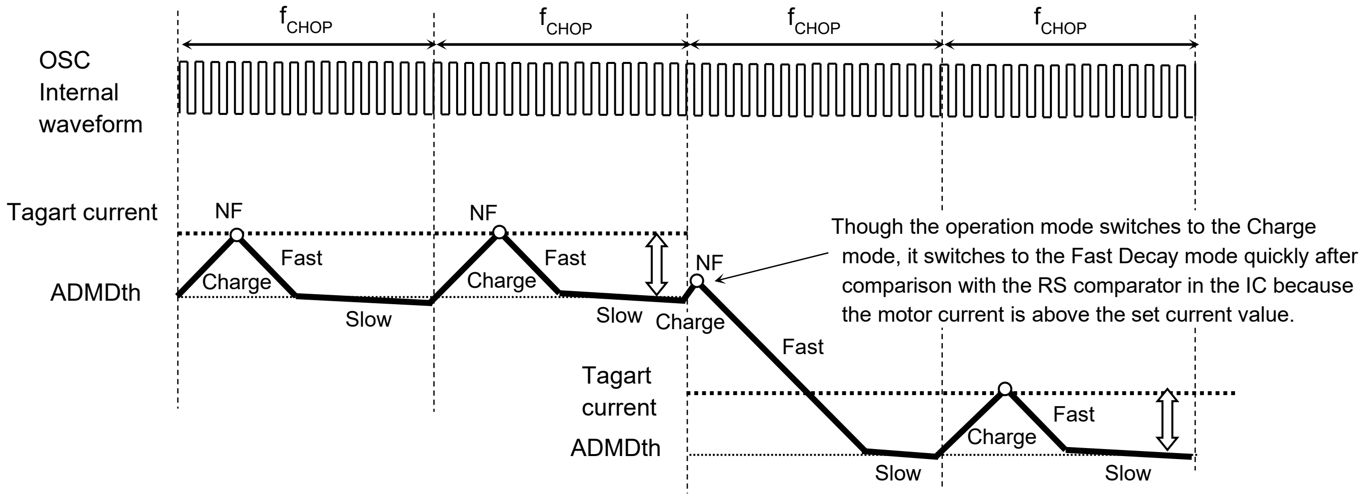


Figure 6.16 When the next current value is decreased

6.6.4. Fast period > 1 f_{CHOP} cycle
(The motor current does not reach the ADMD threshold during 1 f_{CHOP} cycle.)

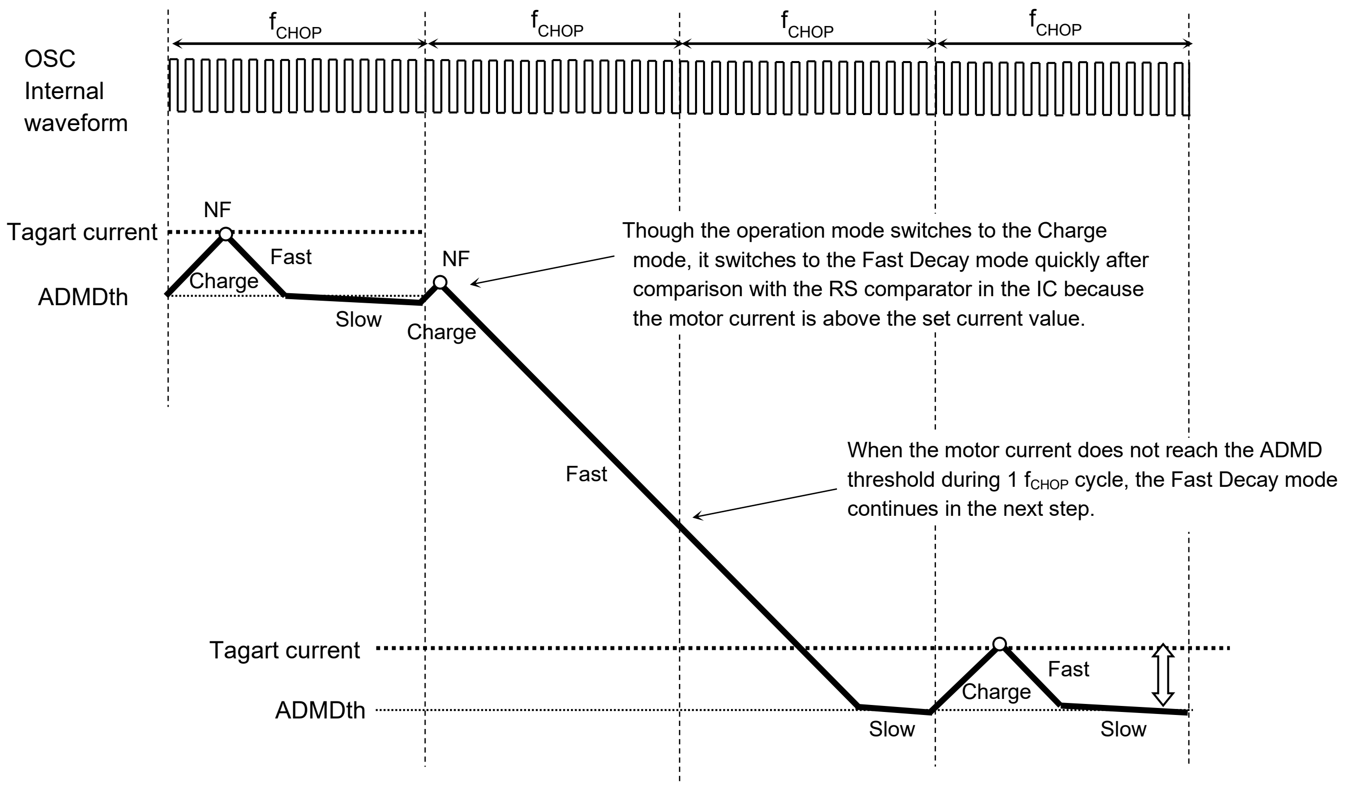


Figure 6.17 Fast period > 1 f_{CHOP} cycle

Note: Timing charts may be simplified for explanatory purpose.

6.7. LO (Error detection flag output) function

The LO function outputs signals when the error detection operates.
Both pins are open drain type. Therefore, to use function properly, the LO1 and LO2 pins should be connected to 3.3 V or 5 V power supply with a pull-up resistor in the range of 10 k to 100 kΩ.
During normal operation, the LO1 pin is high-impedance (the internal MOSFET is OFF). When the error detections (thermal shutdown (TSD) and over-current detection (ISD)) operate, the pins output Low (the internal MOSFET is ON).
The LO2 pin outputs Low only when the TSD is detected.
When reasserting the VM power or using the SLEEP mode to release the error detection status, the LO pins return to “normal operation mode” again. When the LO pins are not used, the pins should be open.

Table 6.5 LO function

LO1 pin output	Function
H (Pull-up)	Normal status (Normal operation)
L	Detected over-current (ISD) and over-temperature (TSD) status

LO2 pin output	Function
H (Pull-up)	Normal status (Normal operation)
L	Detected over-temperature (TSD) status

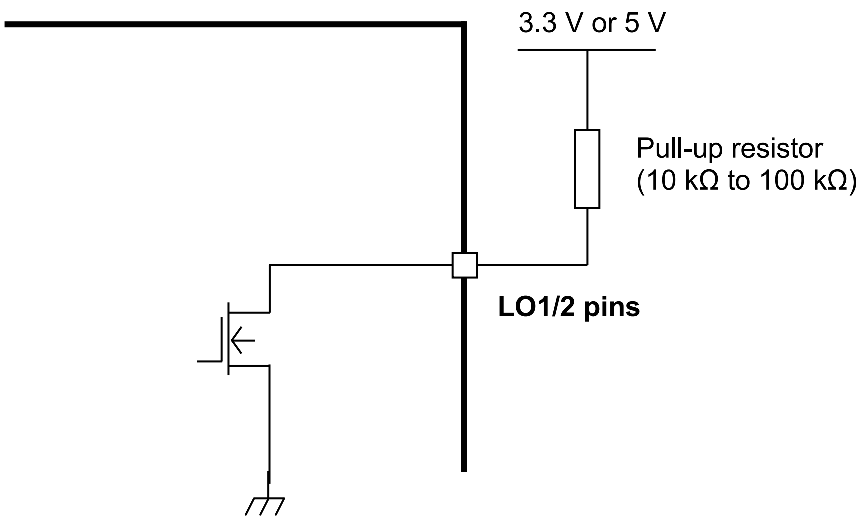


Figure 6.18 LO function Equivalent Circuit

Note: The equivalent circuit diagrams may be simplified or omitted for explanatory purposes.

6.8. Output Transistor Function mode (Advanced Dynamic Mixed Decay)

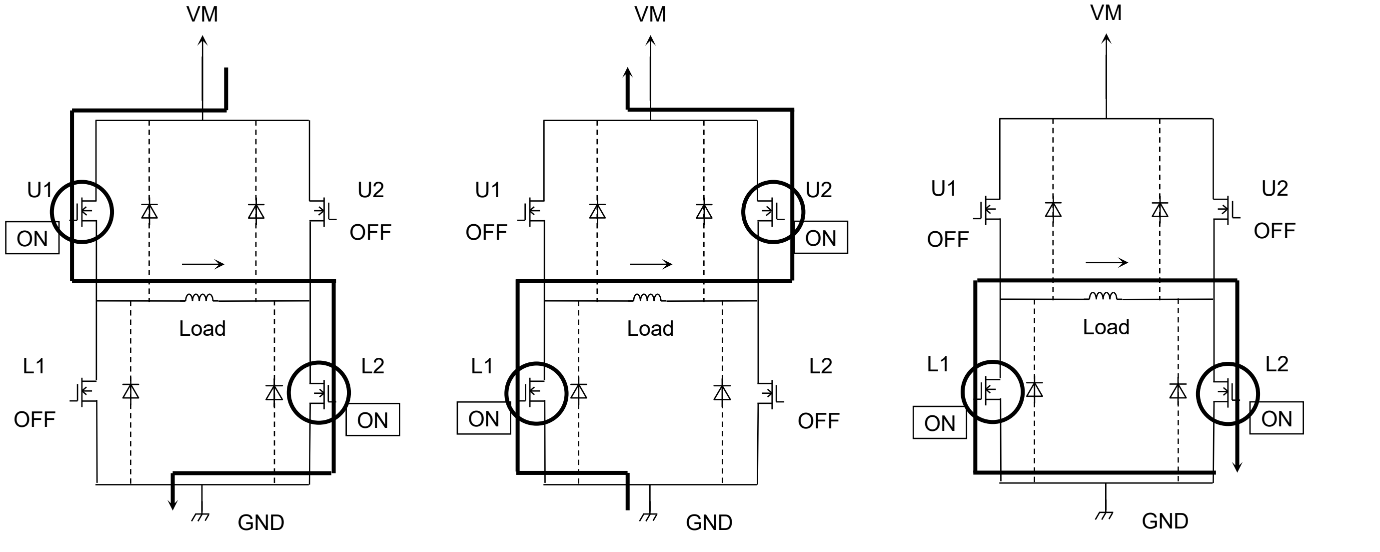


Figure 6.19 Output Transistor Function mode

Note: When the output switches, cross-conduction protection time is provided in the IC to avoid penetrating current.

Table 6.6 Output transistor function

Mode	U1	U2	L1	L2
CHARGE	ON	OFF	OFF	ON
FAST	OFF	ON	ON	OFF
SLOW	OFF	OFF	ON	ON

Note: This table shows an example of when the current flows as indicated by the arrows in the above figures.

When the current flows in the opposite direction, refer to the following table.

Mode	U1	U2	L1	L2
CHARGE	OFF	ON	ON	OFF
FAST	ON	OFF	OFF	ON
SLOW	OFF	OFF	ON	ON

This IC controls the motor current to be constant by 3 modes listed above.
Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

6.9. Set current value (I_{OUT})

The setting current value in the PWM constant-current control mode is determined by the reference voltage (V_{REF}) as follows;

The current value to be set can be calculated by the following formula.

$I_{OUT} = V_{REF} \times 0.556$
e.g.: When V_{REF} = 2.0 V, I_{OUT} = 1.11 A

6.10. Chopping frequency (f_{CHOP})

Chopping frequency of the constant-current control can be configured by the resistor (R_{OSC}) connected to OSCM pin. The IC can operate by the fixed chopping frequency without attaching the external part to OSCM pin.

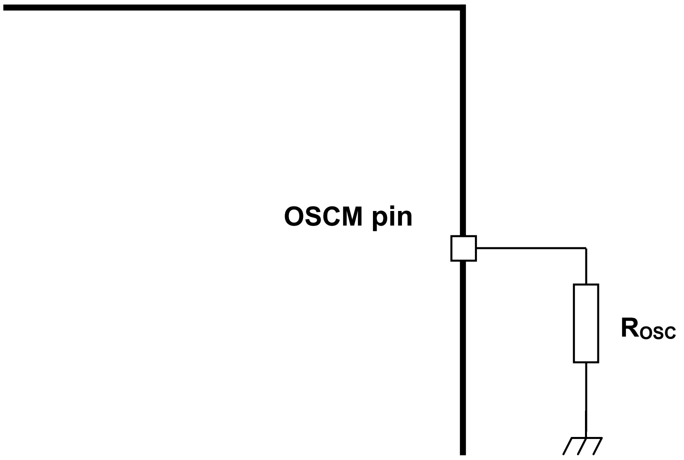


Figure 6.20 OSCM pin Equivalent Circuit

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Chopping frequency (f_{CHOP}) is approximately calculated from the following formula.
Generally, the standard frequency is approximately 70 kHz. A setup in the range of 40 to 100 kHz is recommended.

$f_{CHOP} = f_{OSCM} / 16$
$f_{OSCM} = 1/(\alpha \times R_{OSC} + \beta)$ [MHz] $\alpha = 1.7\times10^{-5}$, $\beta = 0.0285$
e.g.: When R_{OSC}=47 kΩ, f_{OSCM}=1.2 MHz (typ.), f_{CHOP}=75 kHz (typ.)

Under the condition that OSCM pin is open or connected to the GND, the IC operates by the frequency generated automatically (f_{OSCM2}=914 kHz (typ.), f_{CHOP}=57.1 kHz (typ.)).

6.11. Power consumption of the IC

Power of the IC is consumed by the transistor of the output block and that of the logic block mainly.

6.11.1. Power consumption of the power transistor

Power of the output block is consumed by the upper and lower MOSFET of the H-Bridge.

Power consumption of the upper or lower transistor of the H-Bridge is calculated from below formula.

P (out) = Iout (A) × VDS (V) = Iout $(A)^2$ × Ron (Ω)……………………………………………………….(1)

When the current waveform of the motor output corresponds to the complete square waveform in the full-step resolution, average power of output block can be provided as follows

When Ron =0.8 Ω, Iout (peak : Max) = 1.0 A, VM = 24 V,
P (out) = 2 (Tr) × 1.0 $(A)^2$ × 0.8(Ω)……………………………………………………………………………..(2)
= 1.6(W)

6.11.2. Power consumption of logic and IM systems

Power consumptions of logic and IM systems are calculated by separating the states (operating and stopping).

I (IM3) =5.4 mA (typ.) : Operation/axis
I (IM2) = 4.8 mA (typ.) : Stopping/axis
I (IM1) = 0.03 μA (typ.) : Standby/axis

Output system is connected to VM (24V). (Output system: Current consumed by the circuit connected to VM + Current consumed by switching output stages)

Power consumption is calculated as follows;

P (IM3) = 24 (V) × 0.0054 (A)………………………………………………………………………......(3)
= 0.13 (W)

6.11.3. Power consumption

Total power consumption P is calculated from the results of "1" and "2" above.

P = P (out) + P (IM3) = 1.73 (W)

Power consumption in standby mode is as follows;

P (Sleep mode) = 24 (V) × 0.03 (μA) = 0.72 (μW)

About the heat design of the board etc., please evaluate it by the actual board enough, and configure the appropriate margin.

6.12. Detection Function

Built-in below detection functions.

Table 6.7 Detection function

Detection	Target	Detection level	Protection method	Resume method from detection state
Thermal shutdown (TSD)	Chip temperature	160 °C (typ.) or more Dead band time of 5.0 μs (typ.)	All outputs are OFF forcedly.	This function is a latch type that maintains the operation at the time of detection. The operation resumes by below process. ・Power supply is reapplied. ・SLEEP mode is set once and normal mode is set again.
Over-current detection (ISD)	Output current	3 A (typ.) or more Dead band time of 1.25 μs (typ.)	All outputs are OFF forcedly.	
Under voltage lockout (UVLO)	Voltage of VM pin	4.0 V (typ.) or less Dead band time of 1.41 μs (typ.)	All outputs are OFF forcedly. Internal circuits are reset.	VM voltage is raised to 4.2 V (typ.) or higher.

6.12.1. Thermal shutdown detection

(This function is a latch type that maintains the operation at the time of detection.)

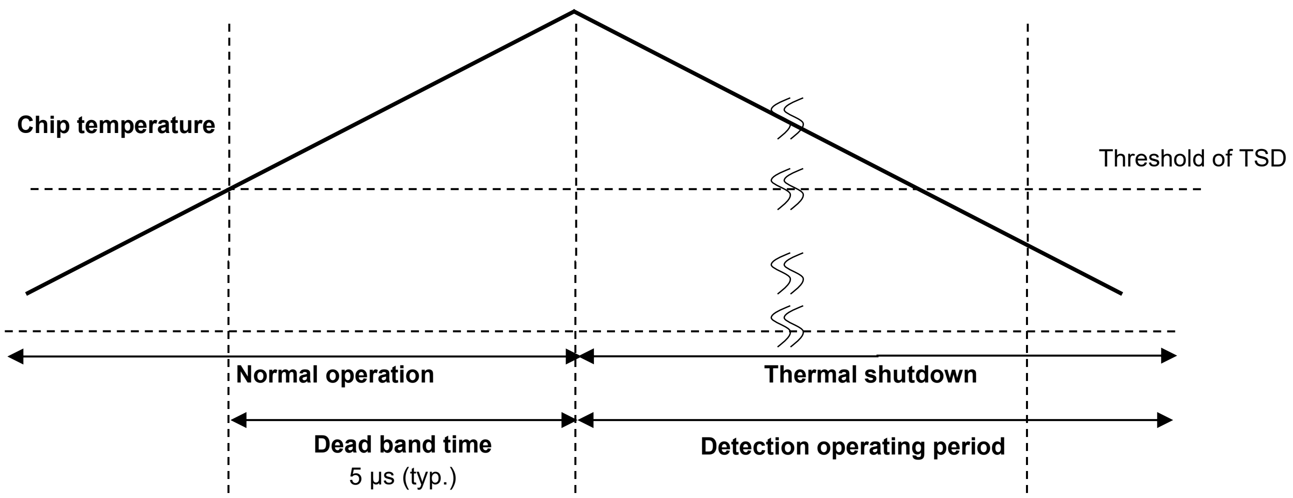
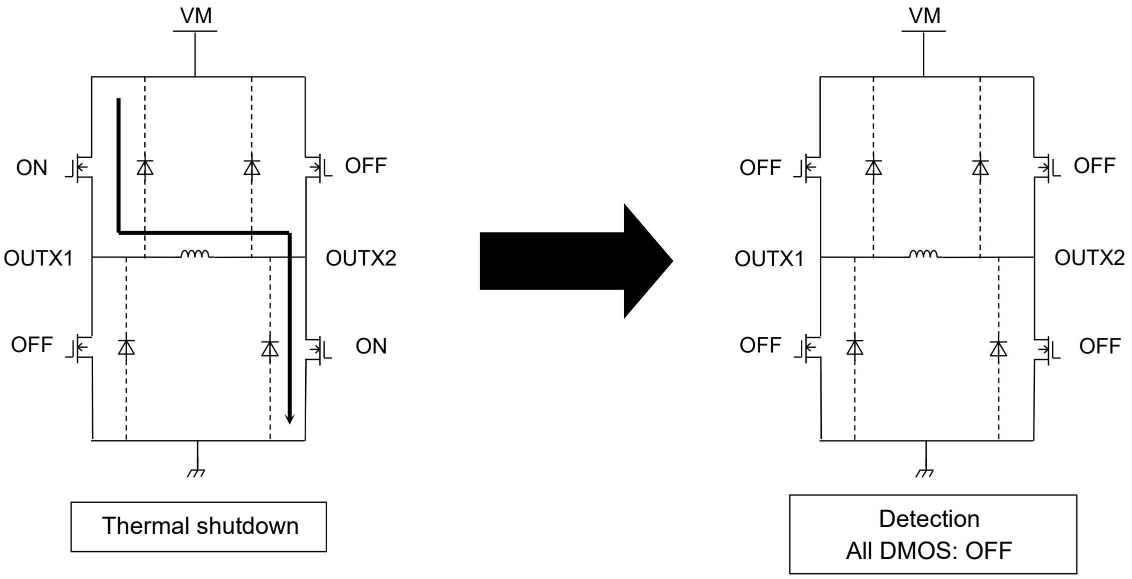


Figure 6.21 Thermal shutdown detection

Note: Timing charts may be simplified for explanatory purposes. The value in the timing chart is the reference value.

6.12.1.1. When over temperature is detected:



X=A or B

Figure 6.22 When over temperature is detected

6.12.2. Over-current detection

(This function is a latch type that maintains the operation at the time of detection.)

This function turns off the IC operation temporarily when the short-circuiting between outputs of motors and the short-circuiting to the power supply or ground occur. It has a dead band time to avoid error detection caused by the spike current which generates in switching and the external noise. When over-current is detected, not only the corresponding channels but both channels are turned off.

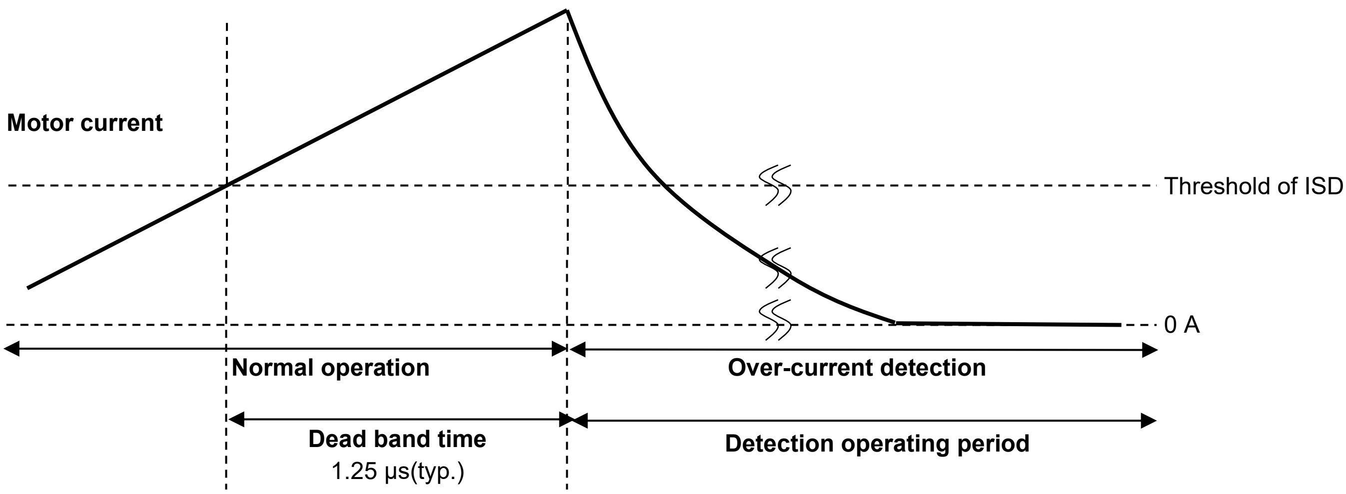
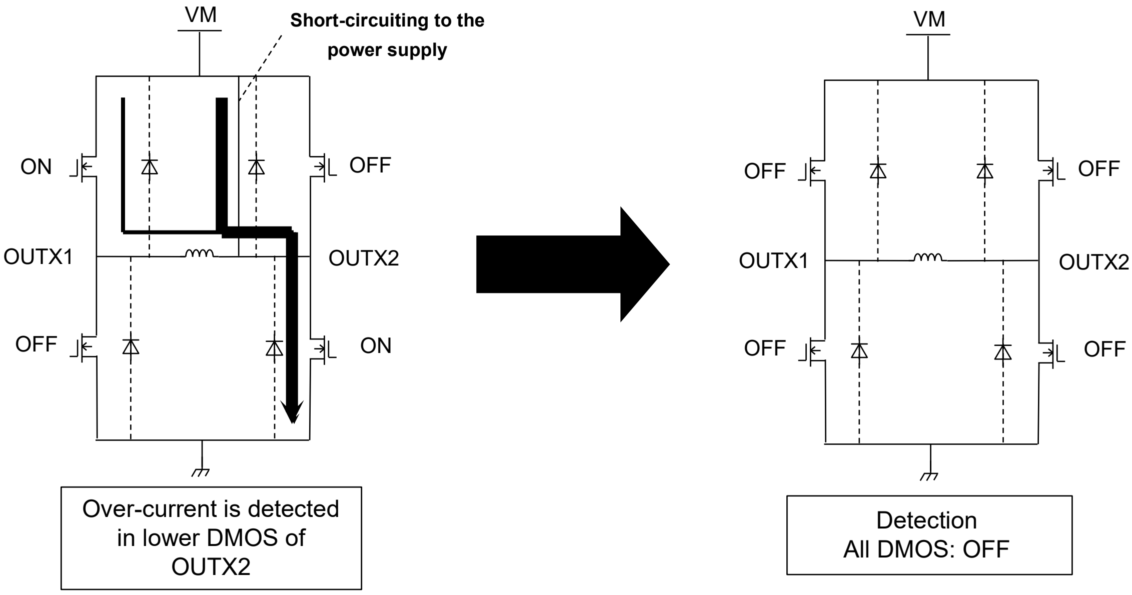


Figure 6.23 Over-current detection timing charts

Note: Timing charts may be simplified for explanatory purposes. The value in the timing chart is the reference value.

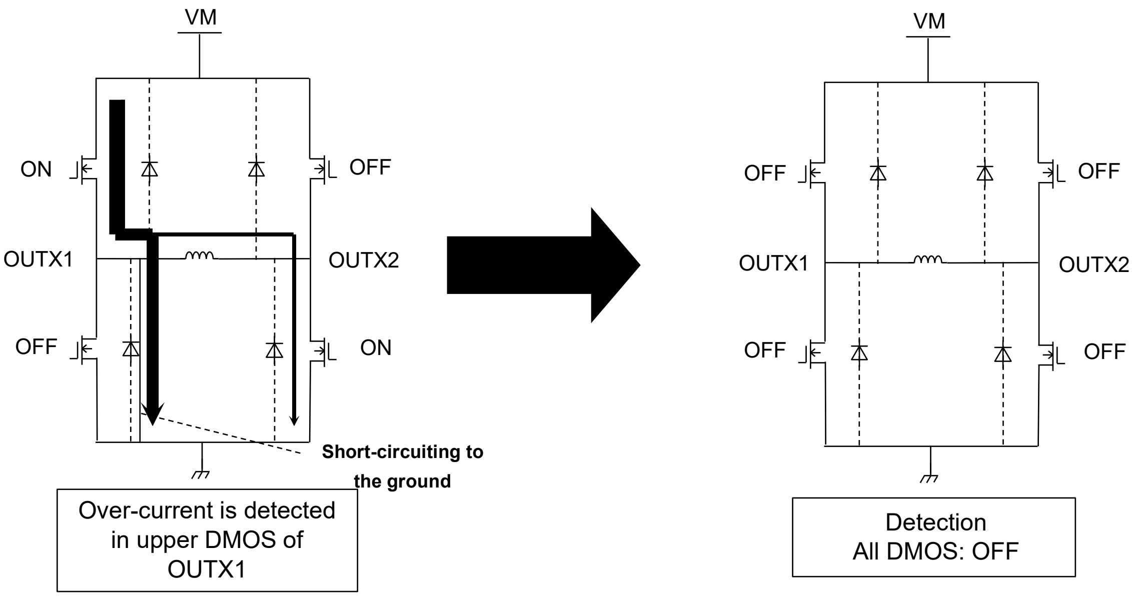
6.12.2.1. When over-current is detected in the lower DMOS of H-bridge by the short-circuiting to the power supply



X=A or B

Figure 6.24 When over-current is detected in the lower DMOS of H-bridge by the short-circuiting to the power supply

6.12.2.2. When over-current is detected in the upper DMOS of H-bridge by the short-circuiting to the ground:



X=A or B

Figure 6.25 When over-current is detected in the upper DMOS of H-bridge by the short-circuiting to the ground

7. Absolute Maximum Ratings (Ta = 25 °C)

Table 7.1 Absolute Maximum Ratings

Characteristics		Symbol	Rating	Unit	Remarks
Motor power supply		V_M	35	V	
Motor output voltage		V_{OUT}	40	V	
Motor output current		I_{OUT}	2.0	A	(Note1)
Voltage for internal regulator		V_{CC}	6.0	V	
Logic input pin voltage		V_{IN}	6.0	V	
V_{REF} reference voltage		V_{REF}	6.0	V	
LO pins voltage		V_{LO}	6.0	V	
Power dissipation	**Device alone**	P_D	1.3	W	(Note2)
	When mounted on a PCB		4.1	W	(Note3)
Operating temperature		T_{opr}	-40 ~ 85	°C	
Storage temperature		T_{stg}	-55 ~ 150	°C	
Junction temperature		$T_{j(MAX)}$	150	°C	

Note1: The maximum current value in normal operation should be kept 1.8 A or less per channel after calculating heat generation. The maximum output current may be further limited in view of the thermal considerations, depending on the ambient temperature and board conditions.

Note2: Device alone. (Ta =25 °C)
If the ambient temperature is above 25 °C, the power dissipation must be de-rated by 10.4 mW/°C.

Note3: When mounted on a specially designed PCB (JEDEC 4-layer board, Ta =25 °C)
If the ambient temperature is above 25 °C, the power dissipation must be de-rated by 32.8 mW/°C.

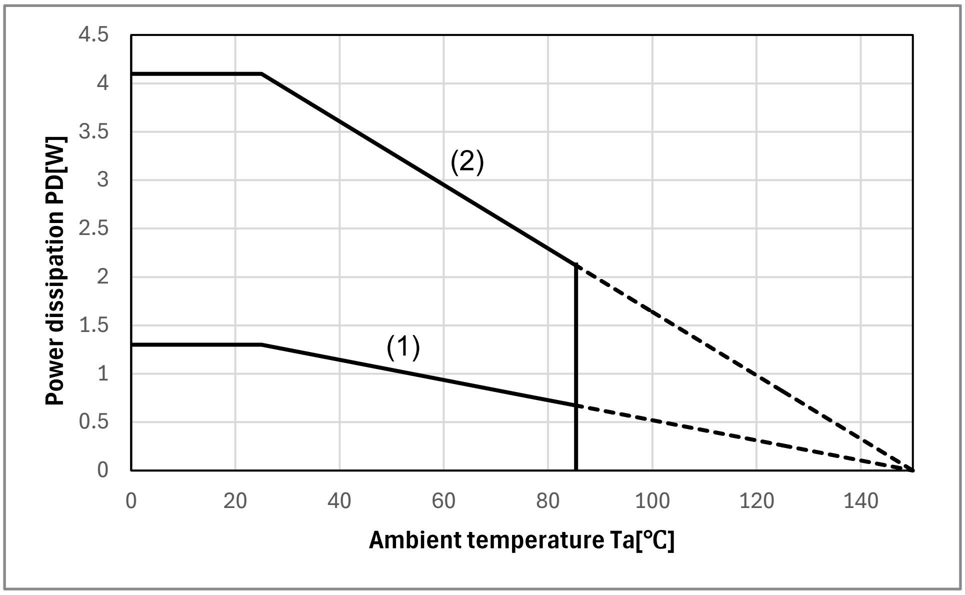
Ta : Ambient temperature of the IC
Topr : Ambient temperature while the IC is active.
Tj : Temperature of the chip while the IC is active. The maximum junction temperature is limited by the thermal shutdown circuit (TSD).

It is advisable to keep the maximum current below a certain level so that the maximum junction temperature, Tj (MAX), will not exceed 120 °C.

Absolute maximum ratings

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion. The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. TB67S531FTG does not have overvoltage detection circuit. Therefore, the device is damaged if a voltage exceeding its rated maximum is applied.
All voltage ratings, including supply voltages, must always be followed. The other notes and considerations described later should also be referred to.

・PD-Ta graph (reference)



(1): Device alone
(2): Measured when mounted on the JEDEC 4-layer board.
θj-a=30.5°C/W. This value is dependent on a substrate pattern and mounting conditions.

Figure 7.1 PD-Ta graph

Note: This value is dependent on a substrate pattern and mounting conditions. Please be careful.
Moreover, the allowable power dissipation decreases as the ambient temperature increases.

8. Operating Ranges (Ta = -40 to 85°C)

Table 8.1 Operating Ranges

Characteristics	Symbol	Min	Typ.	Max	Unit	Remarks
Motor power supply	V_M	4.5	24.0	33	V	(Note1)
Motor output current	I_{OUT}	-	-	1.8	A	Per channel (Note 2)
Logic input voltage	$V_{IN(H)}$	2.0	-	5.5	V	Logic input High level
	$V_{IN(L)}$	-0.5	-	0.8	V	Logic input Low level
Chopping frequency	f_{CHOP}	40	70	150	kHz	-
V_{REF} reference voltage	V_{REF}	0	-	3.6	V	-

Note1: For a slew rate of 0 V to 10 V when the power is turned on, use it under the condition of 1 ms or more.
If you use it under different conditions, please evaluate it thoroughly for your product alone or for the entire system, and decide whether or not it is applicable at your own risk.

Note2: The actual maximum current may be limited by the operating environment (operating conditions such as exciting mode and operating time, or by the surrounding temperature or board heat dissipation). Determine a realistic maximum current by calculating the heat generated under the operating environment.

9. Electrical Characteristics

9.1. Electrical Characteristics 1 (T_a = 25 °C, V_M = 24 V, unless otherwise specified)

Table 9.1 Electrical Characteristics 1

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Logic input pin Input voltage	High	$V_{IN(H)}$	Logic input pin (Note1)	2.0	-	5.5	V
	Low	$V_{IN(L)}$	Logic input pin (Note1)	-0.5	-	0.8	V
Input hysteresis		$V_{IN(HYS)}$	Logic input pin (Note1)	-	150	-	mV
Logic input pin Input current	High	$I_{IN(H)}$	Test logic input pin: 5 V	35	50	75	μA
	Low	$I_{IN(L)}$	Test logic input pin: 0 V	-	-	1	μA
LO pins output voltage		V_{OL}	IOL=5 mA, Output: Low	-	0.2	0.5	V
Power consumption		I_{M1}	Output: Open, Sleep mode	-	0.03	1	μA
		I_{M2}	Output: Open, SLEEP=H, Output stage stop	-	4.8	5.5	mA
		I_{M3}	Output: Open (Full step resolution) SLEEP=H, Normal operation Chopping frequency: 40 kHz	-	5.4	7	mA
Motor output leakage current	Upper	I_{OH}	V_M = 35 V, V_{OUT} = 0 V	-	-	1	μA
	Lower	I_{OL}	V_M = V_{OUT} = 35 V	1	-	-	μA
Output current differential between channels		ΔI_{OUT1}	V_{REF} = 1.8V, I_{OUT} = 1.0 A setting (Note2)	0	-	5	%
Output set current accuracy		ΔI_{OUT2}	V_{REF} = 1.8V, I_{OUT} = 1.0 A setting	-5	0	5	%
Output transistor between drain and source On resistance (upper + lower)		$R_{ON(D-S)}$	T_j = 25 °C I_{OUT} = 2.0 A	-	0.8	0.88	Ω

Note1: $V_{IN(H)}$ is defined as the V_{IN} voltage that changes the output voltage by being applied to the test pin and raising this voltage from 0 V gradually.
$V_{IN(L)}$ is defined as the V_{IN} voltage that changes the output voltage by being applied to the test pin and lowering this voltage gradually.
The difference between $V_{IN(H)}$ and $V_{IN(L)}$ is defined as $V_{IN(HYS)}$.

Note2: Motor current channel differential satisfies the following equation.
The absolute value of the difference in output current settings between any two channels [A] ≤ average of the output setting current values × output current error (Maximum) [A]

9.2. Electrical Characteristics 2 (T_a = 25 °C, V_M = 24 V, unless otherwise specified)

Table 9.2 Electrical Characteristics 2

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
V_{REF} input current	I_{REF}	V_{REF} = 3.6 V	-	0	1	μA
V_{REF} decay ratio	$V_{REF(GAIN)}$	V_{REF}= 2.0 V	0.528	0.556	0.584	-
TSD threshold	T_{jTSD}	-	145	160	175	°C
VM power on reset voltage	V_{MPOR}	-	3.8	4.0	4.2	V
VM power on reset hysteresis	$V_{MPOR(HYS)}$	-	-	200	-	mV
Over-current detection threshold	I_{SD}	-	2.1	3.0	3.6	A

Back-EMF

While a motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF.
If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that TB67S531FTG or other components will be damaged or fail due to the motor back-EMF.

Over-Current Detection (ISD) and Thermal Shutdown (TSD)

The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short-circuit; they do not necessarily guarantee the complete IC safety.

If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged due to short-circuit output.

The ISD circuit is only intended to provide temporary protection against an output short-circuit. If such a condition persists for a long time, the device may be damaged due to overstress. Over-current conditions must be removed immediately by external hardware.

IC Mounting

Do not insert devices incorrectly or in the wrong orientation. Otherwise, it may cause breakdown, damage and/or deterioration of the device.

9.3. AC Electrical Characteristics (Ta = 25 °C, VM = 24 V)

Table 9.3 AC Electrical Characteristics

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Minimum pulse width of logic input signal	$t_{W(H)}$	PHASE_A, PHASE_B, TRQ, IN_A1, IN_A2, IN_B1, IN_B2	600	-	-	ns
		SLEEP_X, DECAY1, DECAY2	1.5	-	-	μs
	$t_{W(L)}$	PHASE_A, PHASE_B, TRQ, IN_A1, IN_A2, IN_B1, IN_B2	600	-	-	ns
		SLEEP_X, DECAY1, DECAY2	1.5	-	-	μs
Output transistor Switching characteristics	t_r	-	40	70	100	ns
	t_f	-	50	80	110	ns
	t_{pLH}	-	-	400	-	ns
	t_{pHL}	-	-	400	-	ns
OSCM oscillation frequency	f_{OSCM1}	R_{OSC}=47 kΩ	1020	1200	1380	kHz
	f_{OSCM2}	OSCM pin: Open or connecting to GND	777	914	1051	kHz
Chopping frequency	f_{CHOP}	f_{OSCM} = 1200 kHz	-	75	-	kHz

9.3.1. AC Electrical Characteristics Timing Chart

TB67S531FTG (Relation between Phase and output)

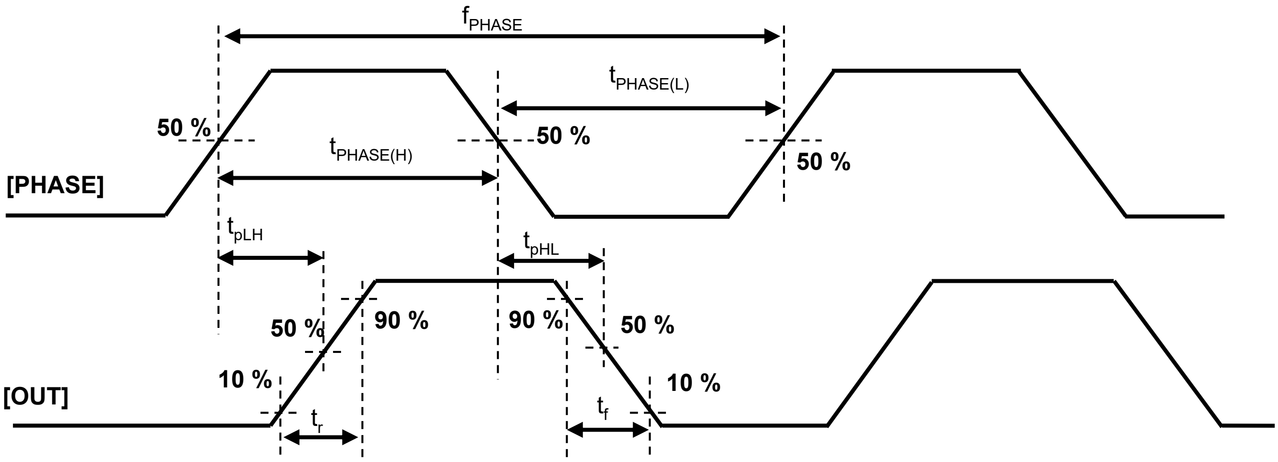


Figure 9.1 TB67S531FTG (Relationship between Phase and output)

Note: Timing charts may be simplified for explanatory purpose.

10. Application Circuit Example

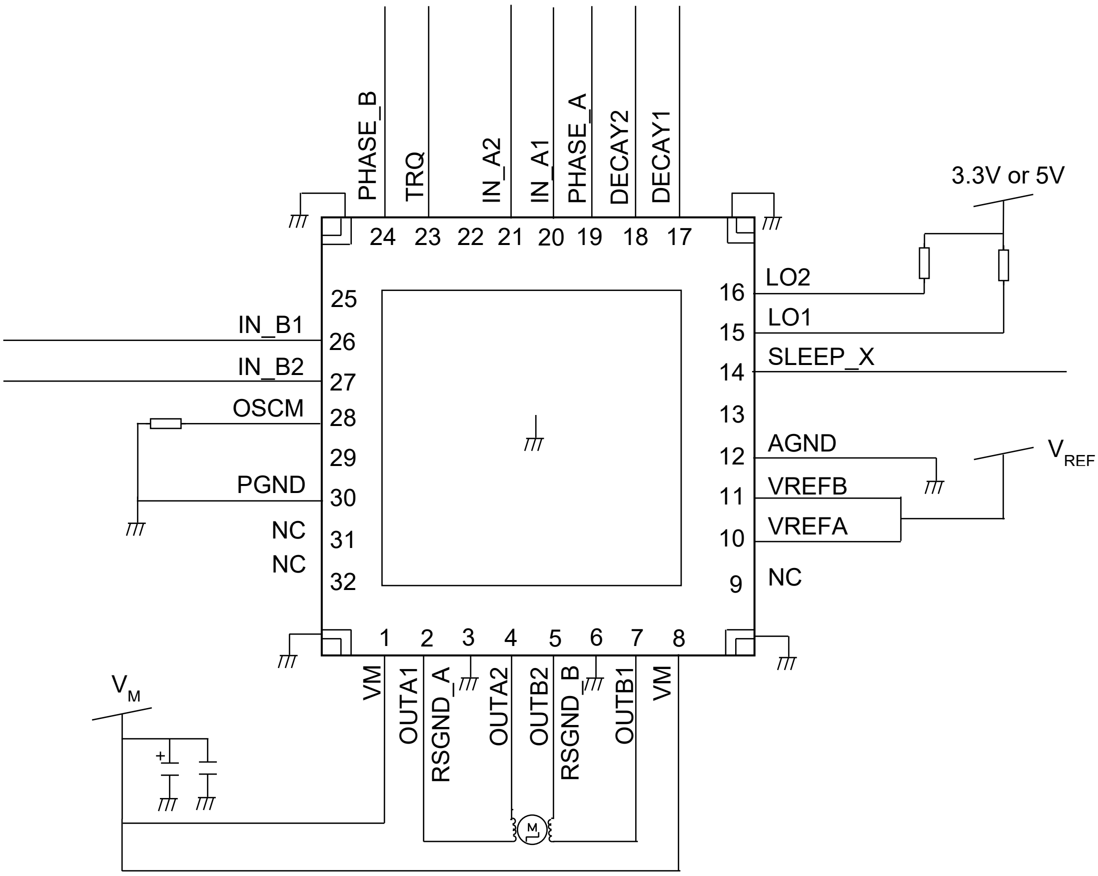


Figure 10.1 Application Circuit Example

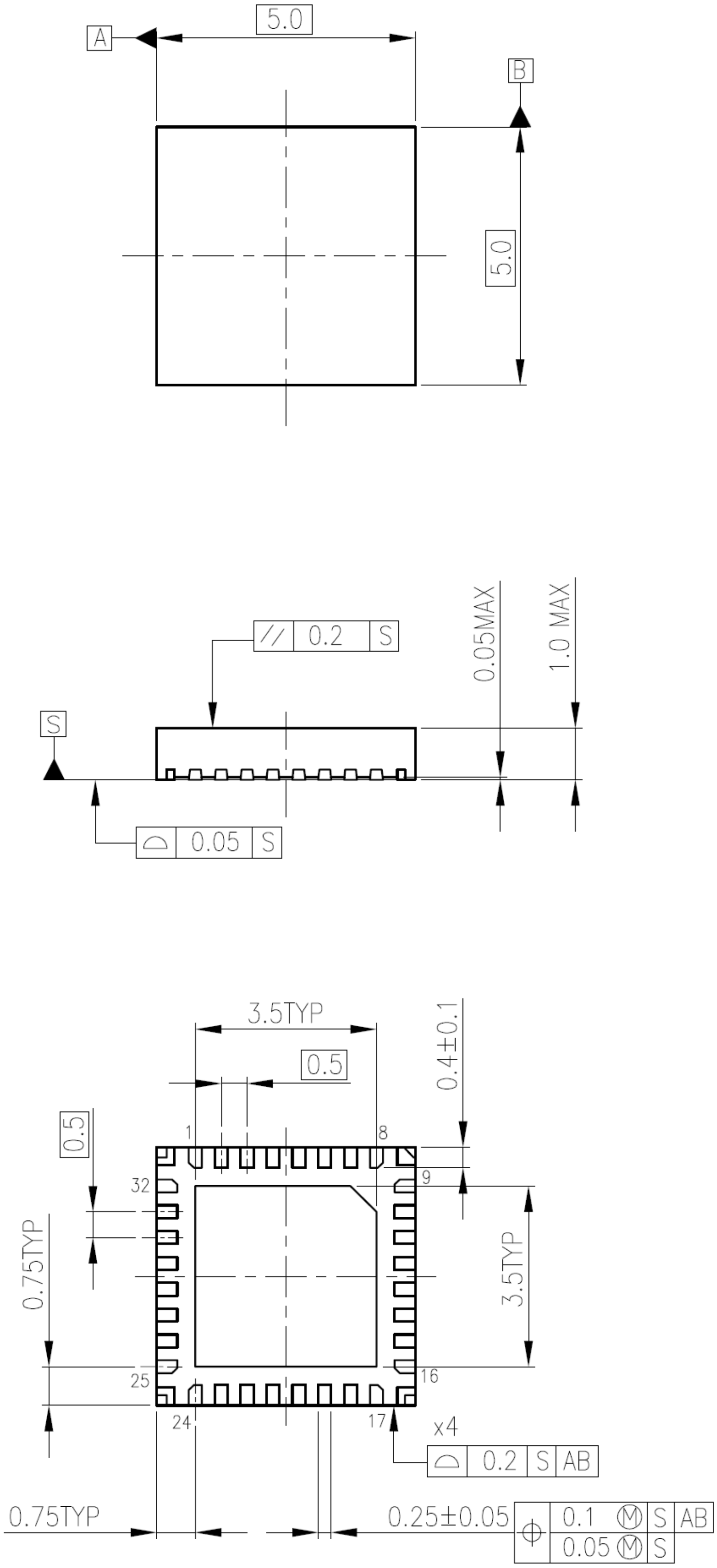
Note: Heat dissipation PAD (4 corners and the center part) on the back of the package is recommended to connect to the GND of the board for improved heat dissipation.

Note: The application circuit example may be simplified or some parts of them may be omitted for explanatory purposes.

11. Package Information

11.1. Package Dimensions

P-VQFN32-0505-0.50-008 **(Unit: mm)**



Weight: 0.066 g (typ.)

Note on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Timing Charts

Timing charts may be simplified for explanatory purposes.

3. Application Circuit Example

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Providing these application circuit examples does not grant a license for industrial property rights.

12. IC Usage Considerations

12.1. Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(3) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over-current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(4) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, over-current or IC failure can cause smoke or ignition. (The over-current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

12.2. Points to Remember on Handling of Ics

(1) Over-current detection circuit

Over-current detection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over-current protection circuits operate against the over-current, clear the over-current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over-current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over-current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal shutdown circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat radiation design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor reverses the rotation direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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