

Photocouplers Infrared LED &amp; Photo IC

# TLP351

## 1. Description

The TOSHIBA TLP351 consists of an infrared emitting diode and an integrated photodetector. This unit is 8-lead DIP package.

TLP351 is suitable for gate driving circuit of IGBT or power MOS FET. Especially TLP351 is capable of "direct" gate drive of lower Power IGBTs.

## 2. Applications

- Industrial Inverter
- Inverter for Air Conditioner
- IGBT/Power MOS FET Gate Drive

## 3. Features

- Peak output current:  $\pm 0.6$  A (max)
- Guaranteed performance over temperature:  $-40$  to  $100$  °C
- Supply current: 2 mA (max)
- Power supply voltage: 10 to 30 V
- Threshold input current :  $I_F = 5$  mA (max)
- Switching time (tpLH/tpHL) : 700 ns (max)
- Common mode transient immunity:  $\pm 10$  kV/ $\mu$ s
- Isolation voltage: 3750 Vrms
- Safety standards  
UL-recognized: UL 1577, File No.E67349  
cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349  
VDE-approved: EN IEC 60747-5-5, EN IEC 62368-1 (Note 1)

Note 1: When a VDE approved type is needed, please designate the Option(D4).

Start of commercial production  
2002-05

## 4. Pin Assignment

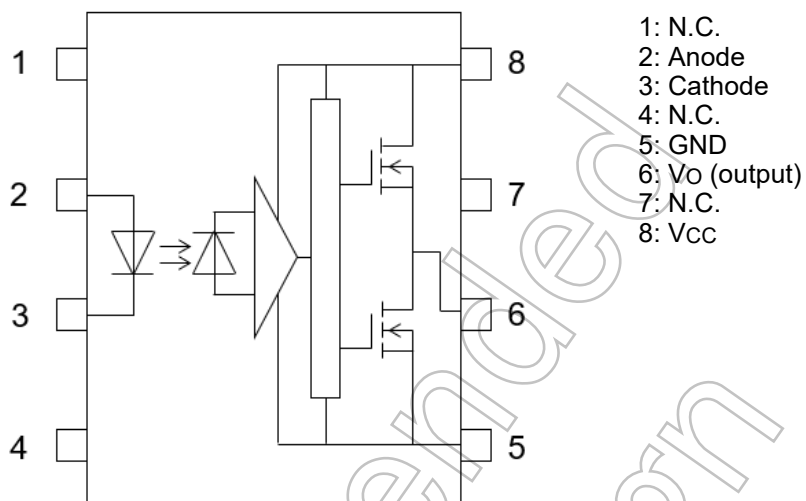


Figure 4.1 Pin Assignment

## 5. Internal Circuit

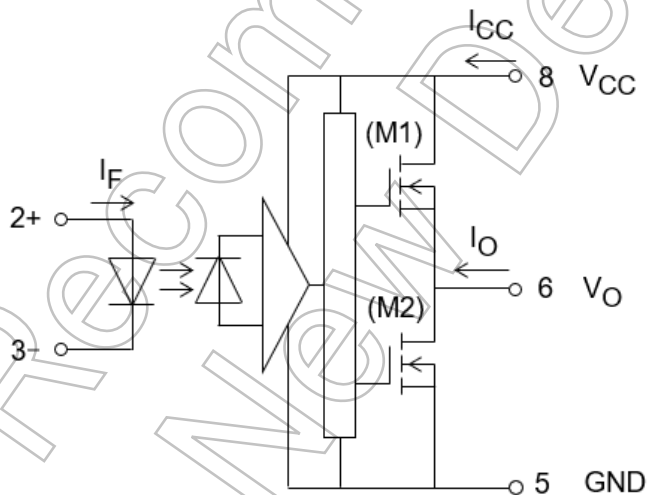


Figure 5.1 Internal Circuit

## 6. Function Description

### 6.1 Truth Table

Input	LED	Tr1	Tr2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

## 7. Absolute Maximum Ratings (Note) (Unless otherwise specified, Ta = 25 °C)

Characteristics		Symbol	Rating	Unit
LED	Forward current	$I_F$	20	mA
	Forward current derating (Ta ≥ 85 °C)	$\Delta I_F / \Delta T_a$	-0.54	mA/°C
	Peak transient forward current (Note 1)	$I_{FP}$	1	A
	Reverse voltage	$V_R$	5	V
	Power Dissipation	$P_D$	40	mW
	Power Dissipation Derating (Ta ≥ 85 °C)	$\Delta P_D / ^\circ C$	-1.0	mW/°C
	Junction temperature	$T_j$	125	°C
Detector	"H" peak output current (Note 2)	$I_{OPH}$	-0.6	A
	"L" peak output current (Note 2)	$I_{OPL}$	0.6	A
	Output voltage	$V_O$	-0.5 to 35	V
	Supply voltage	$V_{CC}$	-0.5 to 35	V
	Output Power Dissipation	$P_O$	260	mW
	Output Power Dissipation Derating (Ta ≥ 85 °C)	$\Delta P_O / ^\circ C$	-6.5	mW/°C
	Junction temperature	$T_j$	125	°C
Operating frequency (Note 3)	$f$	25	kHz	
Operating temperature range	$T_{opr}$	-40 to 100	°C	
Storage temperature range	$T_{stg}$	-55 to 125	°C	
Lead soldering temperature (10 s) (Note 4)	$T_{sol}$	260	°C	
Isolation voltage (AC, 60 s, R.H. ≤ 60 %) (Note 5)	$BV_S$	3750	Vrms	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width  $PW \leq 1 \mu s$ , 300 pps

Note 2: Exponential waveform pulse width  $PW \leq 10 \mu s$ ,  $f \leq 15 \text{ kHz}$

Note 3: Exponential waveform  $I_{OPH} \leq -0.4 \text{ A} (\leq 2.0 \mu s)$ ,  $I_{OPL} \leq +0.4 \text{ A} (\leq 2.0 \mu s)$ ,  $T_a = 100 \text{ }^\circ\text{C}$

Note 4: It is 2 mm or more from a lead root.

Note 5: Device considered a two-terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

### 8. Recommended Operating Conditions (Note)

Characteristics	Symbol	Min	Typ.	Max	Unit
Input current, ON (Note 1)	$I_F$ (ON)	7.5	—	10	mA
Input voltage, OFF	$V_F$ (OFF)	0	—	0.8	V
Supply voltage	$V_{CC}$	10	—	30	V
Peak output current	$I_{OPH}/I_{OPL}$	—	—	$\pm 0.2$	A
Operating temperature	$T_{opr}$	-40	—	100	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note: A ceramic capacitor (1  $\mu$ F) should be connected between pin 8 ( $V_{CC}$ ) and pin 5 (GND) to stabilize the operation of a high-gain linear amplifier. Otherwise, this photocoupler may not switch properly. The bypass capacitor should be placed within 1 cm of each pin.

Note 1: Input signal rise time (fall time) < 0.5  $\mu$ s

### 9. Electrical Characteristics (Note) (unless otherwise specified, $T_a = -40$ to 100 °C)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	
Forward voltage		$V_F$	—	$I_F = 5$ mA, $T_a = 25$ °C	—	1.55	1.70	V	
Temperature coefficient of forward voltage		$\Delta V_F/\Delta T_a$	—	$I_F = 5$ mA	—	-2.0	—	mV/°C	
Input reverse current		$I_R$	—	$V_R = 5$ V, $T_a = 25$ °C	—	—	10	$\mu$ A	
Input capacitance		$C_T$	—	$V = 0$ V, $f = 1$ MHz, $T_a = 25$ °C	—	95	—	pF	
Output current (Note 1)	“H” Level	$I_{OPH1}$	Fig. 12.1.1	$V_{CC} = 15$ V $I_F = 5$ mA	$V_{8-6} = 4$ V	—	-0.4	-0.2	A
		$I_{OPH2}$			$V_{8-6} = 10$ V	—	-0.67	-0.4	
	“L” Level	$I_{OPL1}$	Fig. 12.1.2	$V_{CC} = 15$ V $I_F = 0$ mA	$V_{6-5} = 2$ V	0.2	0.35	—	
		$I_{OPL2}$			$V_{6-5} = 10$ V	0.4	0.63	—	
Output voltage	“H” Level	$V_{OH}$	Fig. 12.1.3	$V_{CC} = 10$ V	$I_O = -100$ mA $I_F = 5$ mA	6.0	8.5	—	V
	“L” Level	$V_{OL}$			Fig. 12.1.4	$I_O = 100$ mA $V_F = 0.8$ V	—	0.4	
Supply current	“H” Level	$I_{CCH}$	Fig. 12.1.5	$V_{CC} = 10$ to 30 V $V_O$ open		$I_F = 10$ mA	—	1.4	2.0
	“L” Level	$I_{CCL}$			Fig. 12.1.6	$I_F = 0$ mA	—	1.3	2.0
Threshold input current	L $\rightarrow$ H	$I_{FLH}$	—	$V_{CC} = 15$ V, $V_O > 1$ V		—	1.1	5	mA
Threshold input voltage	H $\rightarrow$ L	$V_{FHL}$	—	$V_{CC} = 15$ V, $V_O < 1$ V	0.8	—	—	V	
Supply voltage		$V_{CC}$	—	—	10	—	30	V	

Note: All typical values are at  $T_a = 25$  °C

Note 1:  $I_O$  application time  $\leq 50$   $\mu$ s; single pulse.

## 10. Isolation Characteristics (unless otherwise specified, Ta = 25 °C)

Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Capacitance input to output	C <sub>S</sub>	V <sub>S</sub> = 0V, f = 1MHz (Note)	—	1.0	—	pF
Isolation resistance	R <sub>S</sub>	V <sub>S</sub> = 500 V, R.H. ≤ 60 % (Note)	1×10 <sup>12</sup>	10 <sup>14</sup>	—	Ω
Isolation voltage	BV <sub>S</sub>	AC, 60 s	3750	—	—	Vrms

Note : Device considered a two-terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

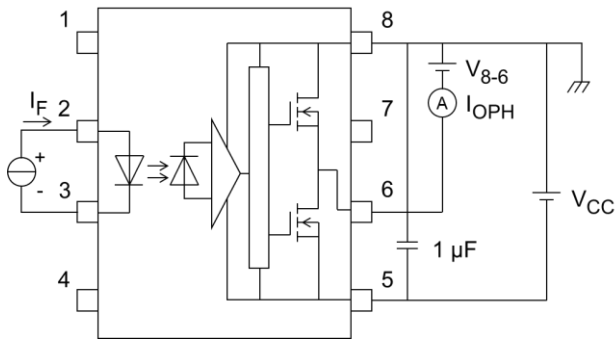
## 11. Switching Characteristics (Note) (unless otherwise specified, Ta = -40 to 100 °C)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit			
Propagation delay time	L → H	t <sub>pLH</sub>	Fig. 12.1.7	V <sub>CC</sub> = 30 V R <sub>g</sub> = 47 Ω C <sub>g</sub> = 3 nF	I <sub>F</sub> = 0 → 5 mA	100	—	700	ns		
	H → L	t <sub>pHL</sub>			I <sub>F</sub> = 5 → 0 mA	100	—	700			
Output rise time (10-90%)		t <sub>r</sub>			Fig. 12.1.8	V <sub>CM</sub> = 1000 Vp-p Ta = 25 °C V <sub>CC</sub> = 30 V	I <sub>F</sub> = 0 → 5 mA	—	50	—	ns
Output fall time (90-10%)		t <sub>f</sub>					I <sub>F</sub> = 5 → 0 mA	—	50	—	
Propagation delay difference between any two parts or channels		PDD  t <sub>pHL</sub> - t <sub>pLH</sub>		V <sub>CC</sub> = 30 V, R <sub>g</sub> = 47 Ω C <sub>g</sub> = 3 nF	-500	—	500	ns			
Common mode transient immunity at high level output		CM <sub>H</sub>	Fig. 12.1.8	V <sub>CM</sub> = 1000 Vp-p Ta = 25 °C V <sub>CC</sub> = 30 V	I <sub>F</sub> = 5 mA V <sub>O (min)</sub> = 26 V	-10	—	—	kV/μs		
Common mode transient immunity at low level output		CM <sub>L</sub>			I <sub>F</sub> = 0 mA V <sub>O (max)</sub> = 1 V	10	—	—			

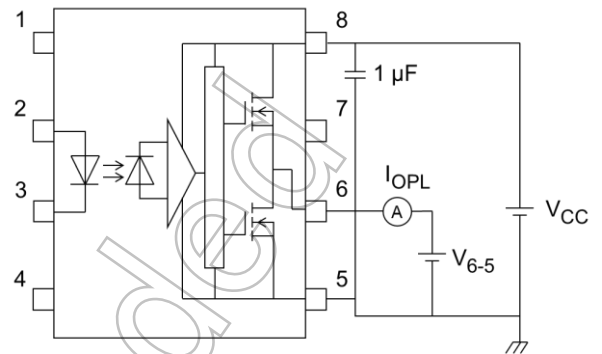
Note: All typical values are at Ta = 25 °C

**12. Test Circuits and Characteristics Curves**

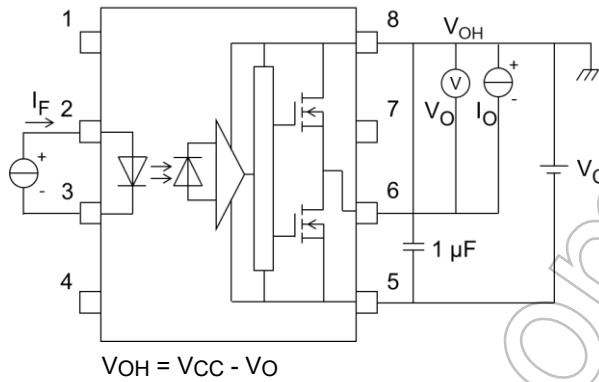
**12.1. Test Circuits**



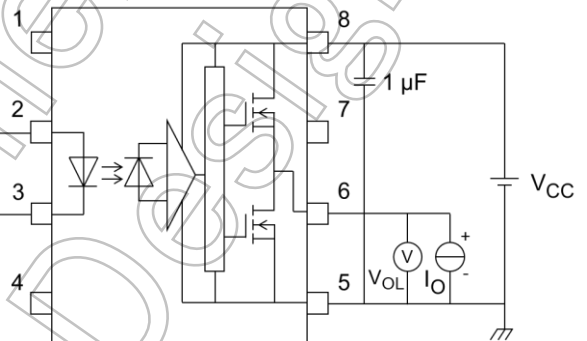
**Fig. 12.1.1 I<sub>OPH</sub> Test Circuit**



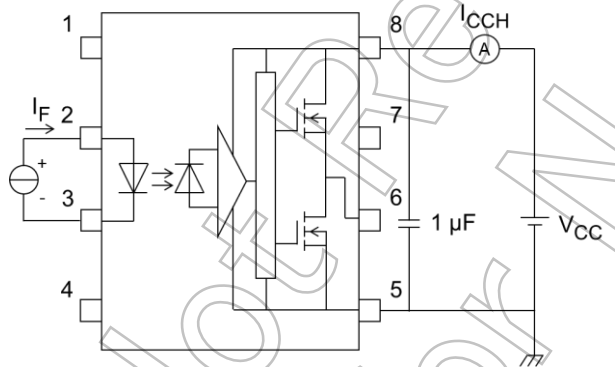
**Fig. 12.1.2 I<sub>OPL</sub> Test Circuit**



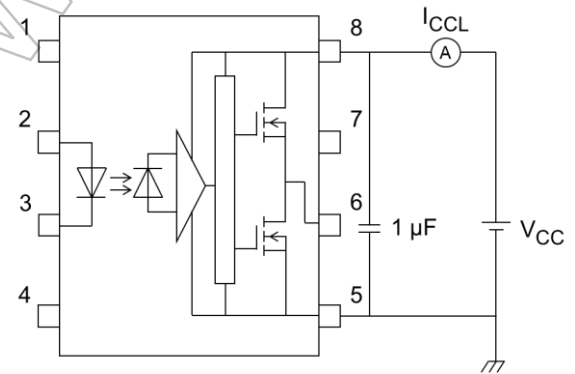
**Fig. 12.1.3 V<sub>OH</sub> Test Circuit**



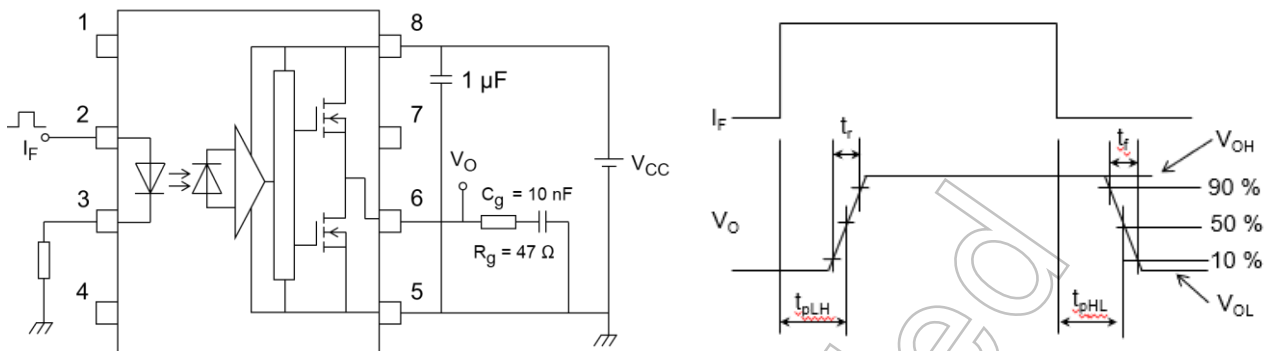
**Fig. 12.1.4 V<sub>OL</sub> Test Circuit**



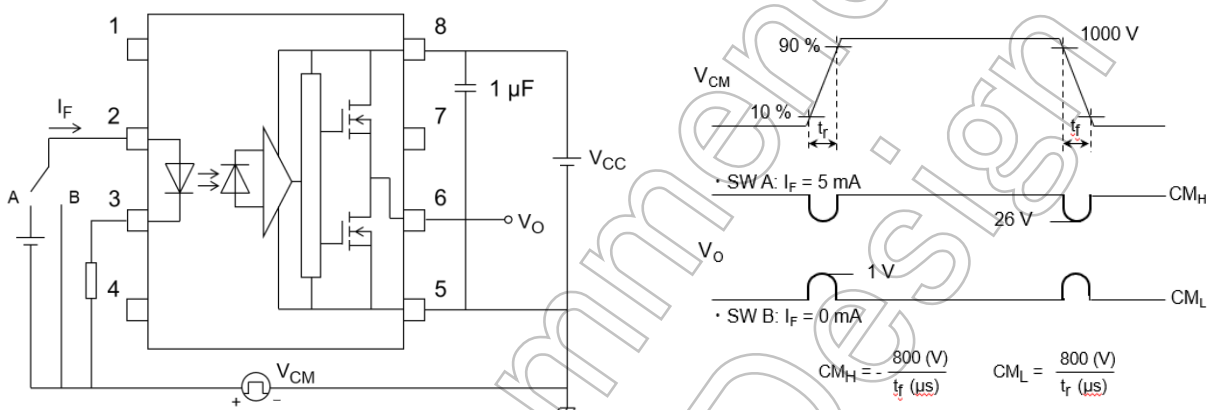
**Fig. 12.1.5 I<sub>CCH</sub> Test Circuit**



**Fig. 12.1.6 I<sub>CCL</sub> Test Circuit**



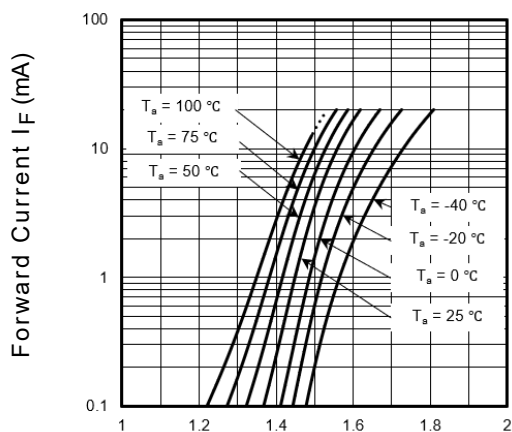
**Fig. 12.1.7  $t_{pLH}$ ,  $t_{pHL}$ ,  $t_r$ ,  $t_f$ , PDD Test Circuit and Waveform**



CML (CMH) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the low (high) state.

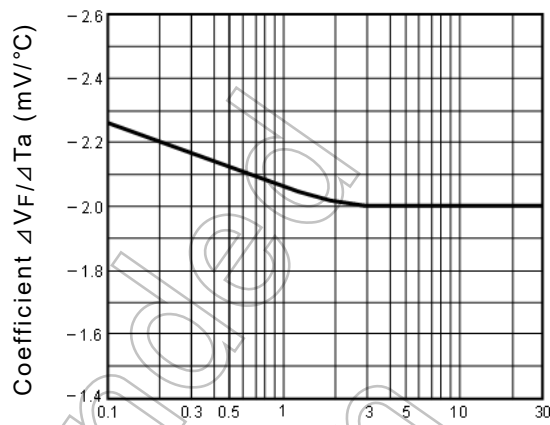
**Fig. 12.1.8  $CM_H$ ,  $CM_L$  Test Circuit and Waveform**

**13. Characteristics Curves (Note)**



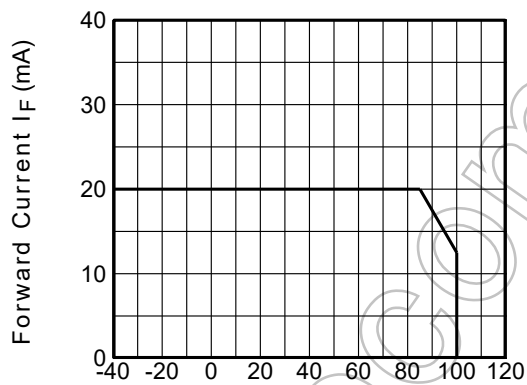
Forward Voltage  $V_F$  (V)

**Figure 13.1  $I_F - V_F$**



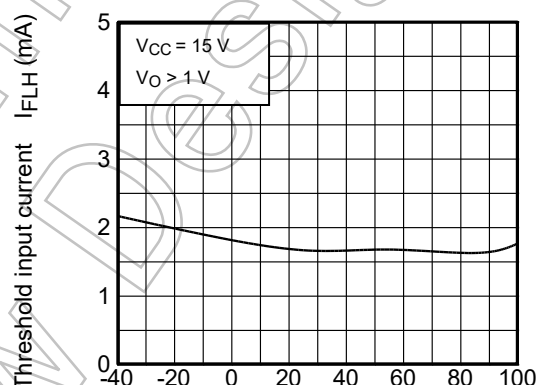
Forward Current  $I_F$  (mA)

**Figure 13.2  $\Delta V_F / \Delta T_a - I_F$**



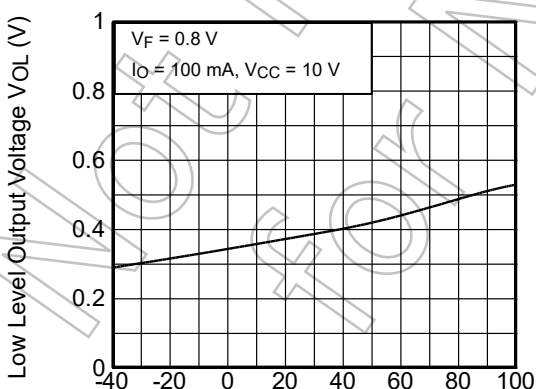
Ambient Temperature  $T_a$  (°C)

**Figure 13.3  $I_F - T_a$**



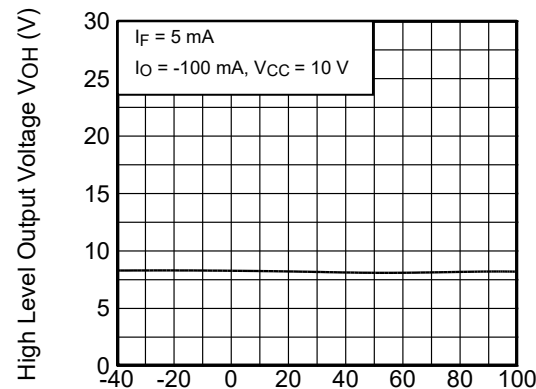
Ambient Temperature  $T_a$  (°C)

**Figure 13.4  $I_{FLH} - T_a$**



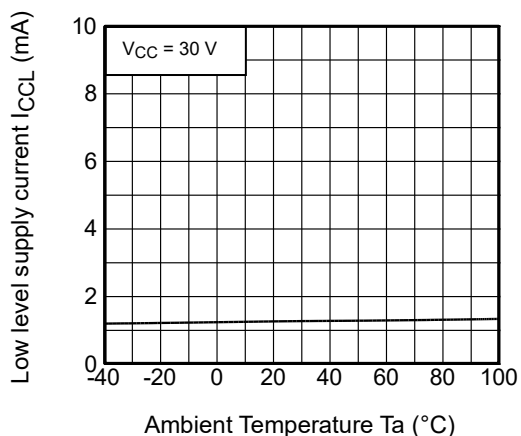
Ambient Temperature  $T_a$  (°C)

**Figure 13.5  $V_{OL} - T_a$**

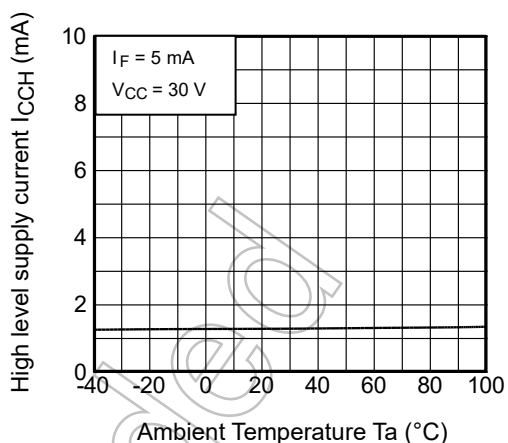


Ambient Temperature  $T_a$  (°C)

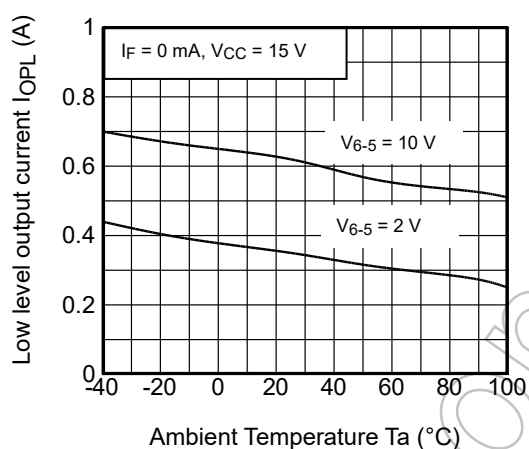
**Figure 13.6  $V_{OH} - T_a$**



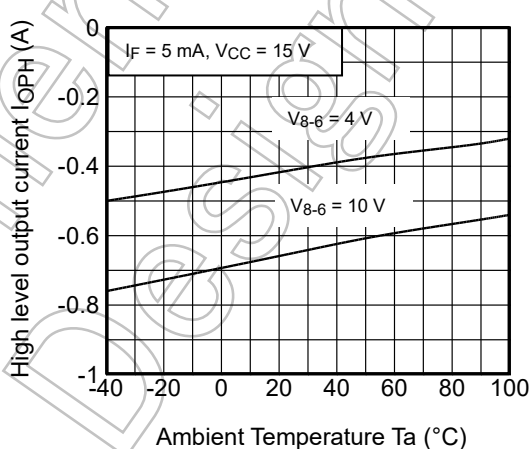
**Figure 13.7 ICCL-Ta**



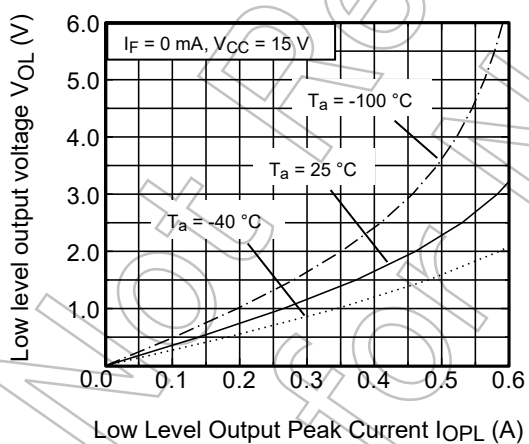
**Figure 13.8 ICCH-Ta**



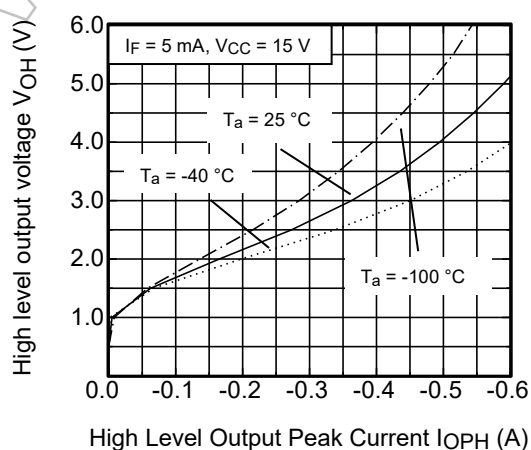
**Figure 13.9 IOPL-Ta**



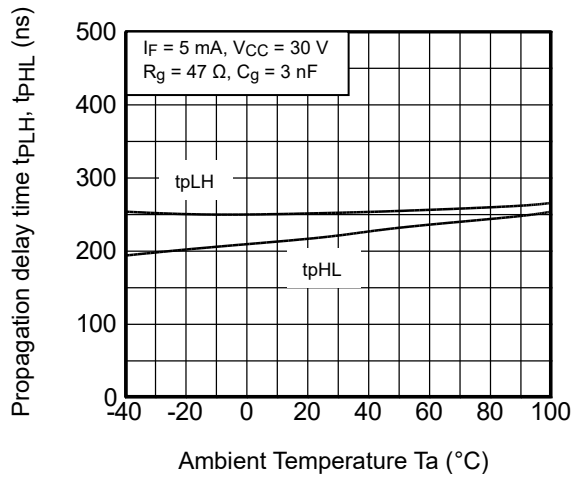
**Figure 13.10 IOPH-Ta**



**Figure 13.11 IOPL-VOL**



**Figure 13.12 IOPH-VOH**

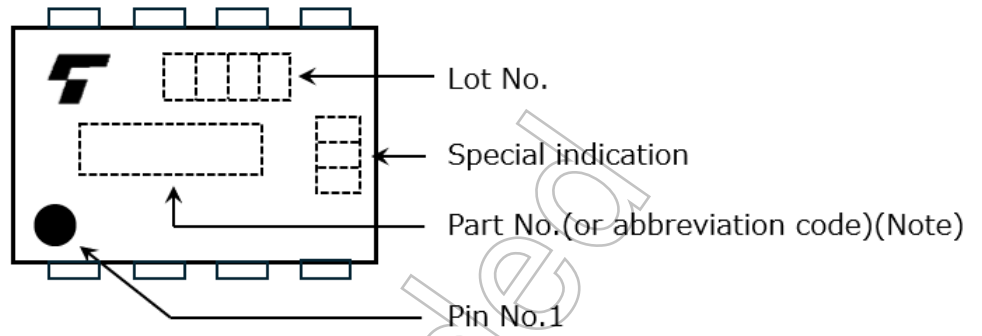


**Figure 13.13  $t_{pHL}, t_{pLH}-T_a$**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Not Recommended for New Design

## 14. Marking

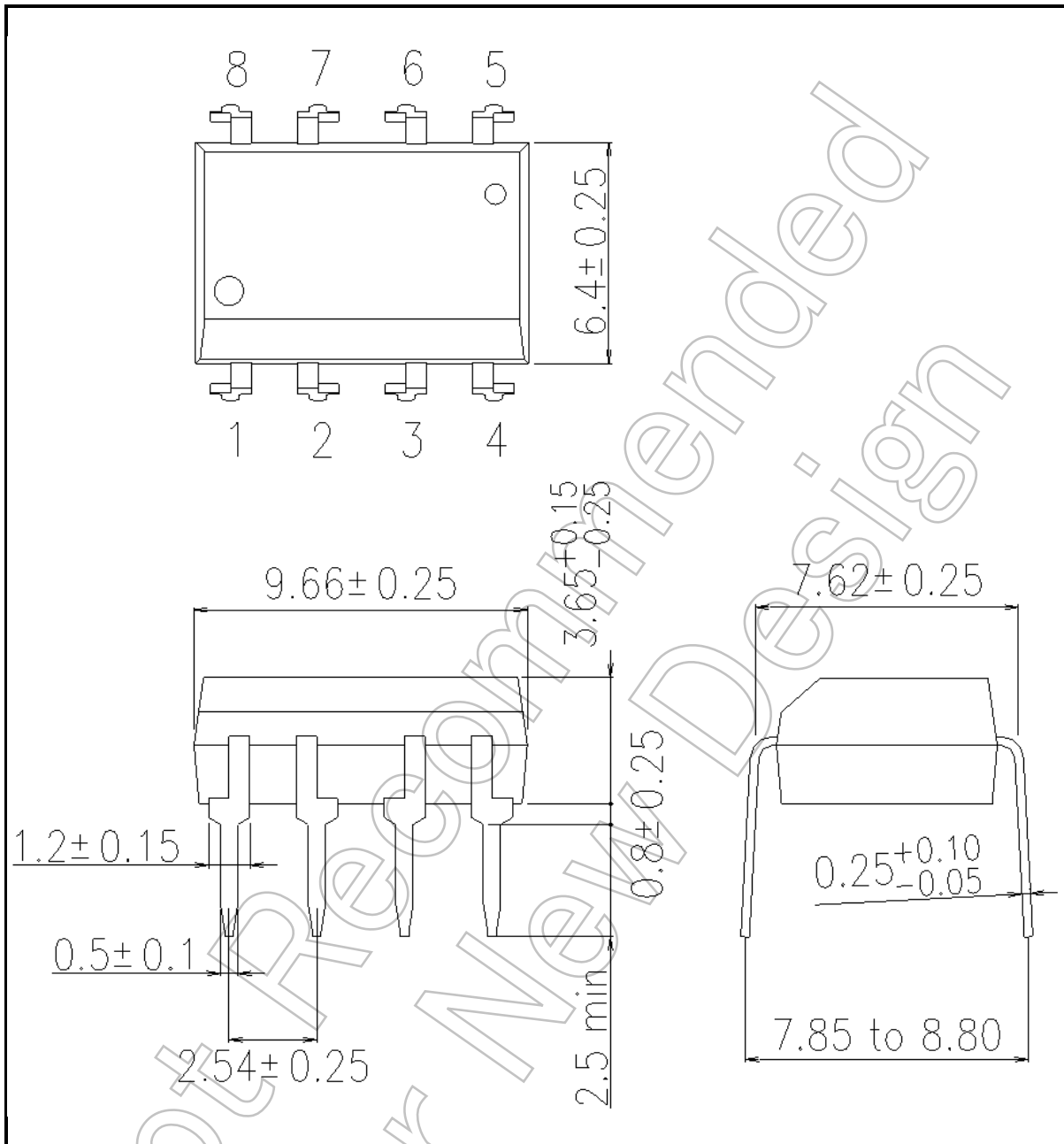


Note: TLP351

Not Recommended for New Design

**15. Package Dimensions**

Unit: mm



Weight: 0.54 g (typ.)

Package Name(s)
TOSHIBA: 11-10C4S

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