TB9104FTG
Application Note

Introduction

This document is provided as a reference to convey technical information to users of the TB9104FTG. Please be sure to use this document only as a supplement, and always refer to the latest datasheet. In particular, please verify all numerical values against the datasheet.

Description

The TB9104FTG is an automotive brushed motor gate driver that integrates two channels of half-bridge gate drivers and can also operate as a single-channel H-bridge gate driver.
It allows various operating parameters to be configured via SPI communication and also enables motor on/off control. The device also incorporates an amplifier or amplifying the small voltage generated across the current-sense resistor.
The TB9104FTG includes a built-in 2× step-up charge pump circuit, allowing the external power MOSFETs to be configured using only N-channel devices.
The TB9104FTG implements dead-time control to prevent shoot-through current.
The TB9104FTG can be placed into a standby state to reduce power consumption while waiting.
The TB9104FTG is equipped with various fault detection functions. In the event of a fault, gate driving is stopped and the fault is reported via the DIAG_X pin. The behavior upon fault occurrence can be configured in advance via SPI communication, and the fault status can also be read out through SPI.

Toshiba Electronic Devices & Storage Corporation

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1. Power Supply Voltage

1.1. Operating Range of Power Supply Voltage

The TB9104FTG has three power supply pins: VB for the gate driver circuitry, VCC for the analog circuitry, and VDD for the digital circuitry.
The operating voltage range of the VB pin is 5.7 to 18 V.
The operating voltage ranges of the VCC and VDD pins are 4.5 to 5.5 V.
The VCC and VDD pins should be connected together directly at the IC pins and driven by the same power supply.
In this document, the voltages of each pin may hereinafter be expressed using the pin names themselves.

1.2. Power-on Sequence with Control input Signals

The power supply system of the TB9104FTG consists of two supply domains: the VB domain and the VCC/VDD domain. The control circuitry operates on VCC and VDD. When the voltage at the VCC pin is low, the control circuitry is initialized and gate driving is disabled. In addition, when the device is placed into the standby state via the STBY_X pin, all circuits stop operating and the control circuitry is initialized.
For explanatory purposes, the pin voltages related to the power supplies and operation are shown in Fig. 1.2.1-1.

1.2.1. Power-on Sequence

The recommended power-on sequence for the VB and VCC/VDD supplies is to apply VB first. In addition, it is recommended to keep the STBY_X pin Low until all power supplies reach their respective operating voltage ranges, so that the TB9104FTG does not operate during power-up.
While the voltage at the VCC pin is lower than VvccUd, the device remains in the reset state. When the voltage at the VCC pin rises above VvccUr, the device transitions from the reset state to either the standby state or the normal state, depending on the state of the STBY_X pin.
If the device transitions to the normal state after reset release, fault detection operation starts immediately. At this time, if the voltage at the VB pin is lower than VvbUd, a VB undervoltage fault is detected, and error handling becomes necessary. To avoid this condition, it is recommended to keep the STBY_X pin Low during power-on.
Even after transitioning from the standby state to the normal operating state, the voltage at the VCP pin does not become sufficiently high until tWAKE has elapsed. After transitioning from the standby state to the normal state, wait for at least the tWAKE period and confirm that the WKUP_sts status is set to 1 before issuing gate drive commands.
The status can be read without issuing the GetStart command; however, if the GetStart command remains at 0, the DIAG_X pin remains Low.
In addition, communication is not possible for the Twakespi period after the STBY_X pin is set High.

Recommended State Transitions:
Reset State → Standby State → Normal State (VCP Boost-Up Wait) → Normal State (Gate Drive Enabled)

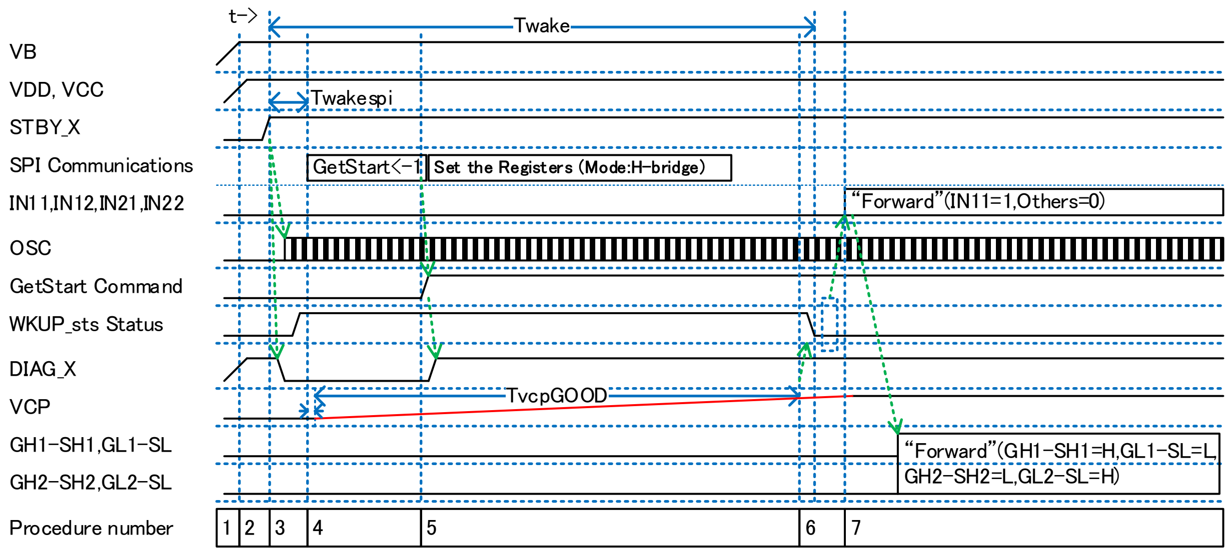

Fig. 1.2.1-1 Example of starting operation procedure.

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

1.2.2. Power-off Sequence

When powering off the device, for safety reasons, set all IN1, IN2, IN3, and IN4 pins to Low and ensure that the motor and other loads are stopped.

The recommended power-off sequence for the VB and VCC/VDD supplies is to turn off VCC and VDD first. At this time, to avoid unintended operation before and after power-off, it is recommended to set the STBY_X pin Low in advance to place the device into the standby state.

Recommended State Transitions:

Normal State (Gate Drive Enabled) → All Gate Drives Off → Standby State → Reset State

2. High Voltage and Negative Voltage Stress Due to Motor Back EMF

Immediately after motor drive is stopped, or when the motor is rotated by an external force, a back electromotive force (back EMF) is generated in the motor, and a voltage is applied from the motor toward the drive circuit. Depending on the conditions, this voltage may exceed the rated voltages of the TB9104FTG pins.

In particular, careful circuit design is required for the SH1 and SH2 pins, which are directly connected to the motor, to ensure that their rated voltages are not exceeded.

In addition, when all external MOSFETs are turned off (high-impedance state), the back EMF raises the voltage at the DH pin via the body diodes of the external MOSFETs. If the sink capability of the power supply is insufficient, the voltages at the DH and VB pins may rise to unexpected levels. The absolute maximum rating between the VB and DH pins, Vvbdh1a, is ±2 V.

Fig. 2-1 shows the current paths of the motor back EMF under these conditions. The current path varies depending on the polarity of the generated voltage.

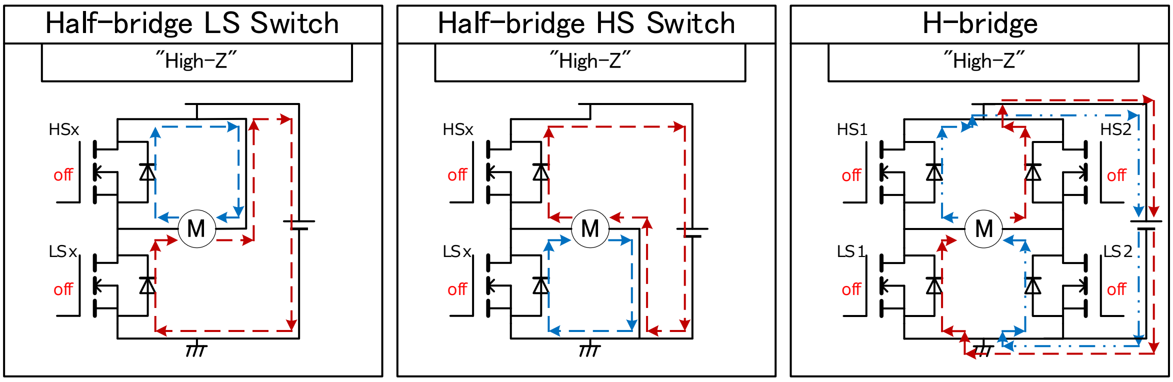

Fig. 2-1 Current Paths of Motor Back EMF

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

Motor back EMF varies depending on the operating conditions and the characteristics of the motor.

Please ensure, under your specific operating conditions, that there is no risk of damage to or malfunction of the IC, as well as no risk of damage to or malfunction of the surrounding circuitry.

2.1. Terminal Voltage Limits

For the pins affected by the motor, the constraints specified in the datasheet are excerpted and summarized in Table 2.1-1.

Table 2.1-1 Constraints on Pins Affected by Back EMF

Target	Constraint1	Constraint2	Unit
VB pin voltage	Absolute Maximum Ratings Vvb1a, Vvb2a	(-0.3 to 0) or (0 to Vvcp1a+0.3) and (0 to 18) or [(18 to Vvcp2a+0.3) and (18 to 40)] at ≤1s	V
DH pin voltage	Absolute Maximum Ratings Vdh1a, Vdh2a	(-0.3 to 0) or (0 to 18) or [(18 to 40)] at ≤1s	V
SH1 pin voltage, SH2 pin voltage	Absolute Maximum Ratings Vsh1a, Vsh2a, Vsh3a	[(-14 to -7)] at ≤1μs or (-7 to 0) or (0 to Vvcp1a+0.3) and (0 to 32.5) or [(32.5 to Vvcp2a+0.3) and (32.5 to 40)] at ≤1s	V
SL pin voltage	Absolute Maximum Ratings Vsl1a, Vsl2a, Vsl3a	[(-10 to -7)] at ≤1μs or (-7 to 0) or (0 to Vvb1a+0.3) and (0 to 32.5) or [(32.5 to Vvb2a+0.3) and (32.5 to 40)] at ≤1s	V
Voltage between VB and DH pins (VB-DH)	Absolute Maximum Ratings Vvbdh1a	(-2 to 0) or (0 to 2)	V

2.2. Example of Protection Circuit

An example of a protection circuits is shown in Fig. 2.2-1.

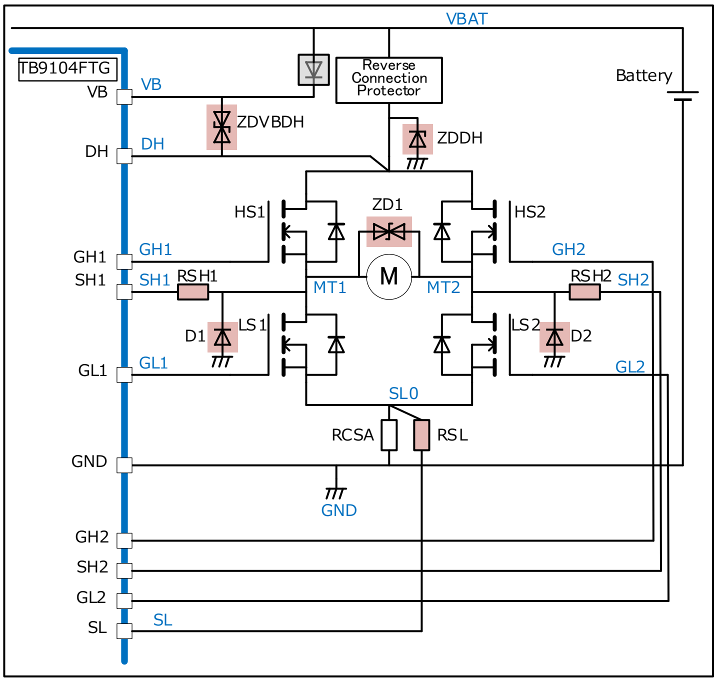

Fig. 2.2-1 High-Voltage and Negative-Voltage Protection in an H-Bridge Circuit

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

The bidirectional Zener diode ZD1 is connected close to the motor and limits the maximum value of the electromotive force generated by the motor.

The bidirectional Zener diode ZDVBDH limits the maximum voltage between the VB and DH pins.

The Zener diode ZDDH limits the voltage at the DH pin.

Diodes D1 and D2 divert and share the current flowing through the SH1 and SH2 pins during negative voltage conditions.

Resistors RSH1 and RSH2 limit the current flowing through the SH1 and SH2 pins. In addition, they also provide slew-rate control by limiting the gate drive current.

Resistor RSL is set equal to RSH1 and RSH2 to match the slew rates of MOSFETs HS1 and LS1, and HS2 and LS2.

No current-sharing diode is connected to the SL pin because it is connected to GND through the low-resistance current-sense resistor RCSA. Depending on the application conditions, it may be necessary to provide a diode in the same manner as D1 and D2.

This circuit is shown as an example. Please implement appropriate countermeasures as required to suit your operating environment.

3. Gate Drive Voltage versus VB

The TB9104FTG employs a 2× step-up charge pump. Depending on the VB voltage used and the external MOSFETs, the gate drive voltage may fall below the minimum required level. Please verify that the external MOSFETs can be properly driven by the gate drive voltage at the minimum VB voltage.

The graph of gate drive voltage versus VB is shown below.

Under Preparation

Fig. 3-1 Gate Drive Voltage versus VB

4. Application Circuit Example

4.1. Application Circuit Example for H-Bridge Mode

An example application circuit for H-bridge mode is shown in Fig. 4.1-1.

The capacitors connected to the VB and VCC pins are used for smoothing and noise suppression. Adjust their values as appropriate for the operating environment.

The resistor connected to the CPDO pin (≤7.5Ω) is used to limit the current for noise reduction. Measure the charge pump capability and the generated noise level under the actual operating conditions and adjust the resistor value accordingly.

The resistors connected to the GH1, GL1, GH2, and GL2 pins are used to limit the current when turning the external N-channel MOSFETs on and off. Adjust these resistor values to suit the operating environment.

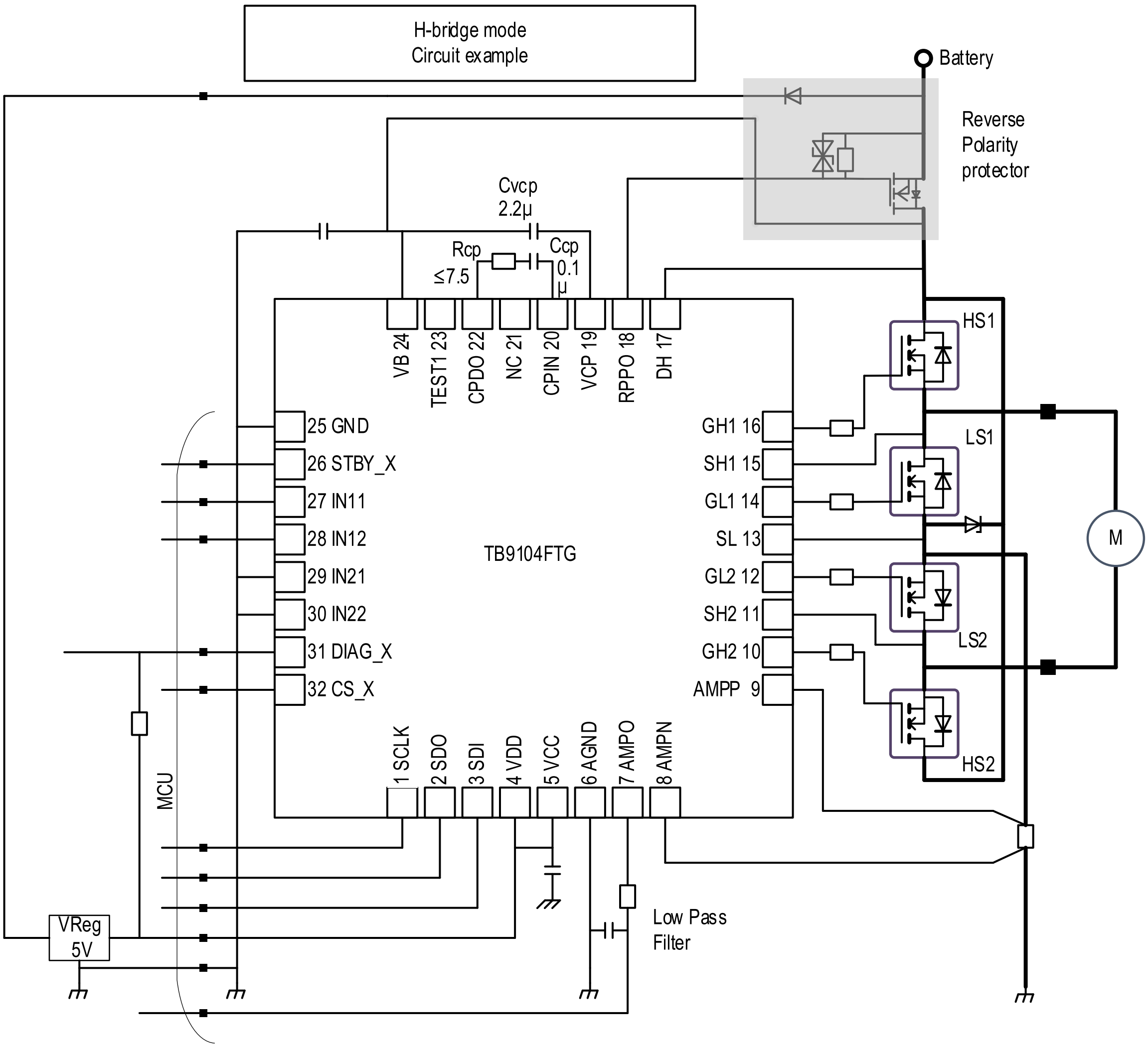

Fig. 4.1-1 Application Circuit Example for H-Bridge Mode

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

4.2. Application Circuit Example for Half-Bridge Mode

An example application circuit for half-bridge mode is shown in Fig. 4.2-1.

The capacitors connected to the VB and VCC pins are used for smoothing and noise suppression. Adjust their values as appropriate for the operating environment.

The resistor connected to the CPDO pin (≤7.5Ω) is used to limit the current for noise reduction. Measure the charge pump capability and the generated noise level under the actual operating conditions and adjust the resistor value accordingly.

The resistors connected to the GH1, GL1, GH2, and GL2 pins are used to limit the current when turning the external N-channel MOSFETs on and off. Adjust these resistor values to suit the operating environment.

The half-bridge circuits can be operated independently as two separate channels.

The motor connected in parallel with the external N-channel MOSFET HS1 starts rotating when LS1 is turned on. The motor connected in parallel with LS2 starts rotating when HS2 is turned on.

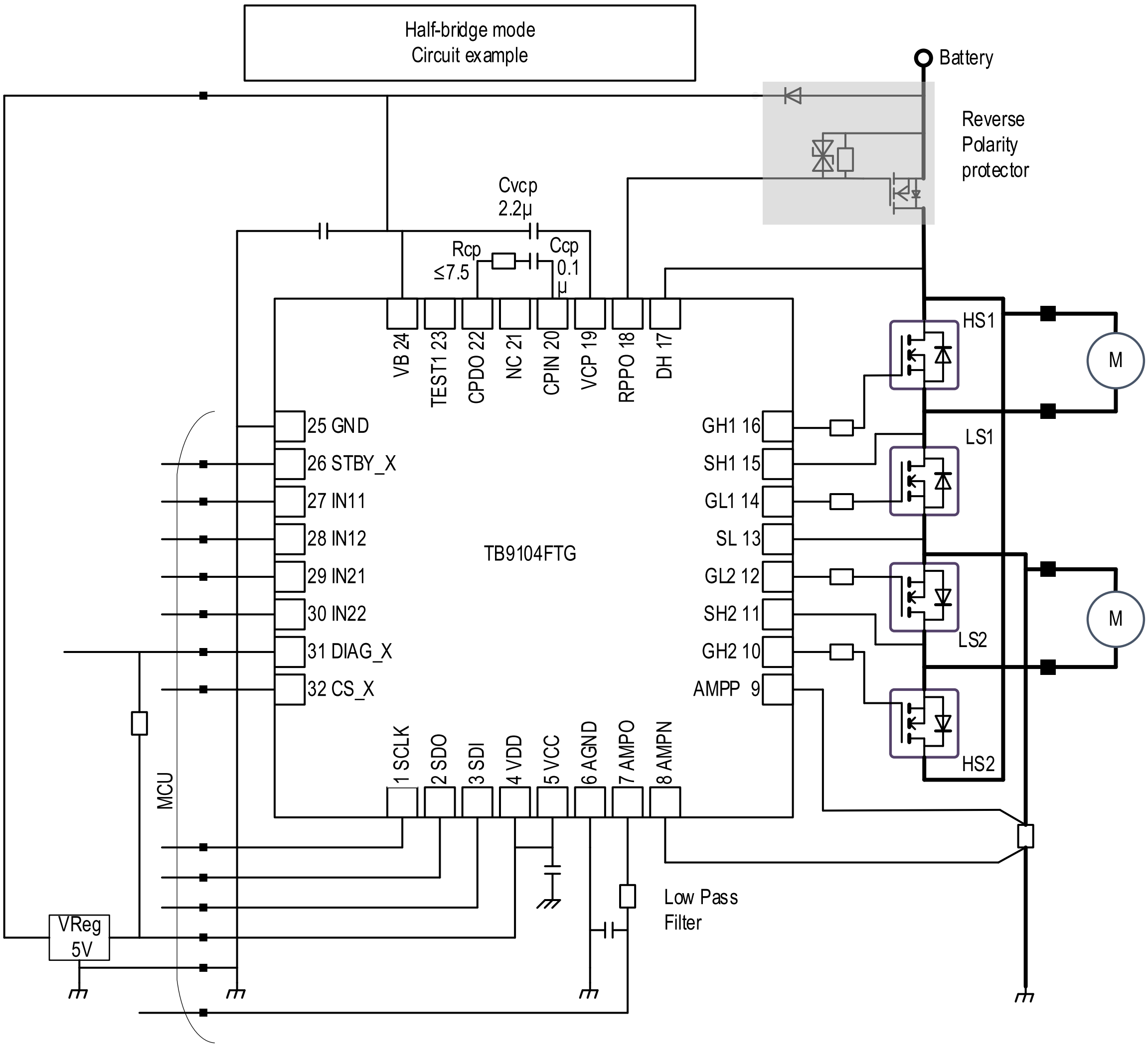

Fig. 4.2-1 Application Circuit Example for Half-Bridge Mode

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

5. Power Dissipation

Under Preparation

Fig. 5-1 Power Dissipation

Condition: Mounted on a JEDEC four-layer board

Allowable power dissipation varies depending on the ambient temperature and heat dissipation conditions. Carefully evaluate these factors and design with sufficient margin.

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