

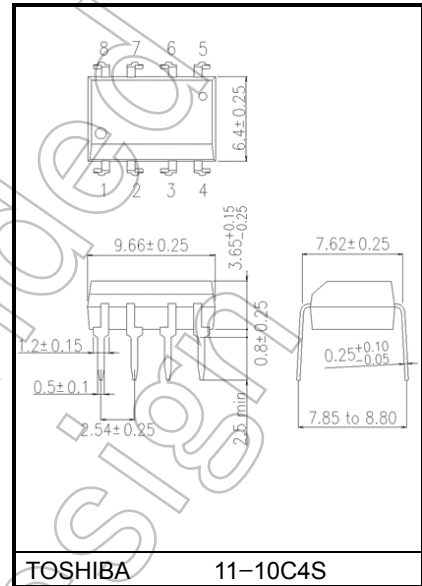
TLP550

Microprocessor System Interfaces
 Digital Logic Ground Isolation
 Line Receiver
 Switching Power Supply Feedback Control
 Transistor Inverter

Unit: mm

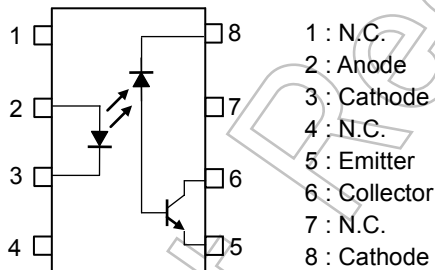
TLP550 consists of a high-output infrared emitting diode and a one chip photo diode-transistor.
 TLP550 has no base connection, and is suitable for application at noisy environmental condition.
 This unit is 8-lead DIP package.

- Isolation voltage : 2500 Vrms (min)
- Propagation delay time (t_{pHL} / t_{pLH}):
 $t_{pHL} = 0.5\mu s$ (typ.),
 $t_{pLH} = 0.6\mu s$ (typ.)
 $(R_L = 1.9 k\Omega)$
- TTL compatible
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A
 File No.E67349

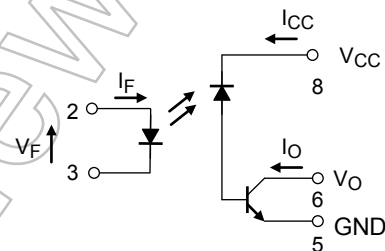


Weight: 0.54 g (typ.)

Pin Configuration (top view)



Schematic



Start of commercial production
 1981-09

Current Transfer Ratio

Classification	Current Transfer Ratio (%) (I_C/I_F)		Marking of Classification
	Min	Max	
(None)	10	—	Blank, O, Y
Rank O	19	—	O
Rank Y	35	—	Y

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current (Note 1)	I_F	25	mA
	Pulse forward current (Note 2)	I_{FP}	50	mA
	Peak transient forward current (Note 3)	I_{FPT}	1	A
	Reverse voltage	V_R	5	V
	Diode power dissipation (Note 4)	P_D	45	mW
Detector	Output current	I_O	8	mA
	Peak output current	I_{OP}	16	mA
	Supply voltage	V_{CC}	-0.5 to 15	V
	Output voltage	V_O	-0.5 to 15	V
	Output power dissipation (Note 5)	P_O	100	mW
Operating temperature range		T_{opr}	-55 to 100	°C
Storage temperature range		T_{stg}	-55 to 125	°C
Lead solder temperature (10 s)		T_{sol}	260	°C
Isolation voltage (AC, 60 s, R.H. ≤ 60 %) (Note 6)		BV_S	2500	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(Note 1) Derate 0.8mA above 70 °C.

(Note 2) 50 % duty cycle, 1 ms pulse width. Derate 1.6 mA / °C above 70 °C.

(Note 3) Pulse width 1 μs, 300 pps.

(Note 4) Derate 0.9 mW / °C above 70 °C.

(Note 5) Derate 2 mW / °C above 70 °C.

(Note 6) Device considered two-terminal device: Pins 1, 2, 3 and 4 shorted together and pin 5, 6, 7 and 8 shorted together.

Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
LED	Forward voltage	V_F	$I_F = 16 \text{ mA}$	1.45	1.65	1.85	V
	Forward voltage temperature coefficient	$\Delta V_F / \Delta T_a$	$I_F = 16 \text{ mA}$	—	-2	—	mV / °C
	Reverse current	I_R	$V_R = 5 \text{ V}$	—	—	10	μA
	Capacitance between terminal	C_T	$V_F = 0 \text{ V}, f = 1 \text{ MHz}$	—	60	—	pF
Detector	High level output current	$I_{OH(1)}$	$I_F = 0 \text{ mA}, V_{CC} = V_O = 5.5 \text{ V}$	—	3	500	nA
		$I_{OH(2)}$	$I_F = 0 \text{ mA}, V_{CC} = V_O = 15 \text{ V}$	—	—	5	μA
		I_{OH}	$I_F = 0 \text{ mA}, V_{CC} = 15 \text{ V}$ $V_O = 15 \text{ V}, T_a = 70 \text{ }^\circ\text{C}$	—	—	50	
	High level supply voltage	I_{CCH}	$I_F = 0 \text{ mA}, V_{CC} = 15 \text{ V}$	—	0.01	1	μA
	Supply voltage	V_{CC}	$I_{CC} = 0.01 \text{ mA}$	15	—	—	V
	Output voltage	V_O	$I_O = 0.5 \text{ mA}$	15	—	—	V

Coupled Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit	
Current transfer ratio	I_O / I_F	$I_F = 16 \text{ mA}, V_{CC} = 4.5 \text{ V}, V_O = 0.4 \text{ V}$	Rank O	10	40	—	%
			Rank Y	19	40	—	
		$I_F = 16 \text{ mA}, V_{CC} = 4.5 \text{ V}, V_O = 0.4 \text{ V}, T_a = 0 \text{ to } 70 \text{ }^\circ\text{C}$	Rank O, Y	35	50	—	
			Rank O, Y	5	—	—	
Low level output voltage	V_{OL}	$I_F = 16 \text{ mA}, V_{CC} = 4.5 \text{ V}, I_O = 1.1 \text{ mA}$ (Rank O: $I_O = 2.4 \text{ mA}$)	—	—	0.4	V	

Isolation Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Capacitance (input-output) (Note 7)	C_S	$V_S = 0 \text{ V}, f = 1 \text{ MHz}$	—	0.8	—	pF
Resistance (input-output) (Note 7)	R_S	R.H. $\leq 60 \%$, $V_S = 1 \text{ kVDC}$	5×10^{10}	10^{14}	—	Ω
Isolation voltage (Note 7)	BV_S	AC, 60 s	2500	—	—	V_{rms}

(Note 7) Device considered two-terminal device: Pins 1, 2, 3 and 4 shorted together and pin 5, 6, 7 and 8 shorted together.

Switching Characteristics (Ta = 25°C, Vcc = 5V)

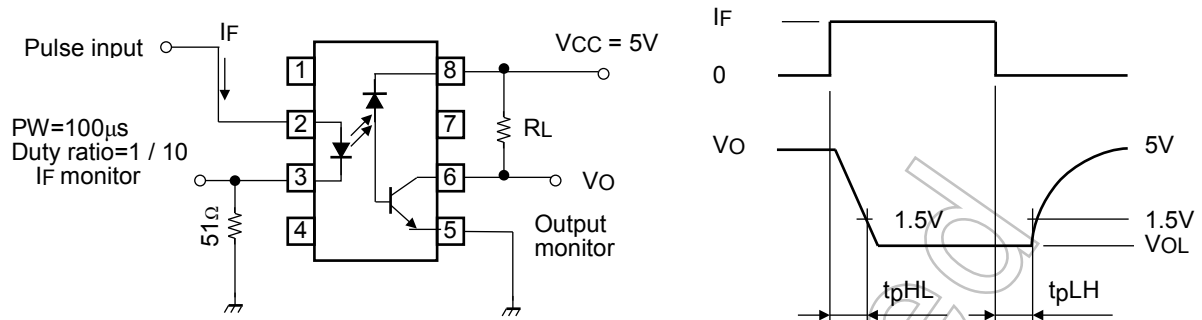
Characteristic	Symbol	Test Circuit.	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (H→L)	t _{pHL}	1	I _F = 0→16 mA, V _{CC} = 5 V, R _L = 4.1 kΩ	—	0.3	0.8	μs
			Rank O: R _L = 1.9 kΩ	—	0.5	0.8	
Propagation delay time (L→H)	t _{pLH}	1	I _F = 16→0 mA, V _{CC} = 5 V, R _L = 4.1 kΩ	—	1	2	μs
			Rank O: R _L = 1.9 kΩ	—	0.6	1.2	
Common mode transient immunity at high output level	CMH	2	I _F = 0 mA, V _{CM} = 200 V _{p-p} R _L = 4.1 kΩ (rank O: R _L = 1.9 kΩ) (Note 8)	—	1500	—	V/μs
Common mode transient immunity at low output level	CML		I _F = 16 mA, V _{CM} = 200 V _{p-p} R _L = 4.1 kΩ (rank O: R _L = 1.9 kΩ) (Note 8)	—	~1500	—	V/μs

(Note 8) CML is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V).

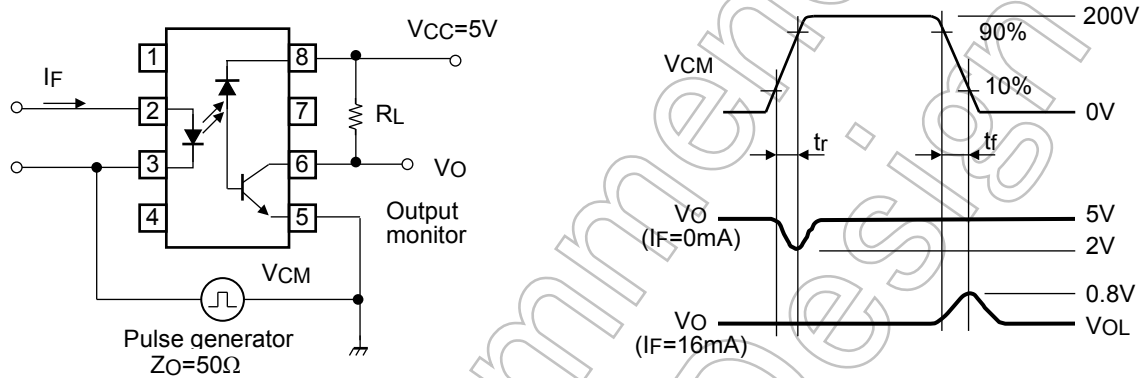
CMH is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V).

Not Recommended for New Designs

Test Circuit 1: Switching Time Test Circuit

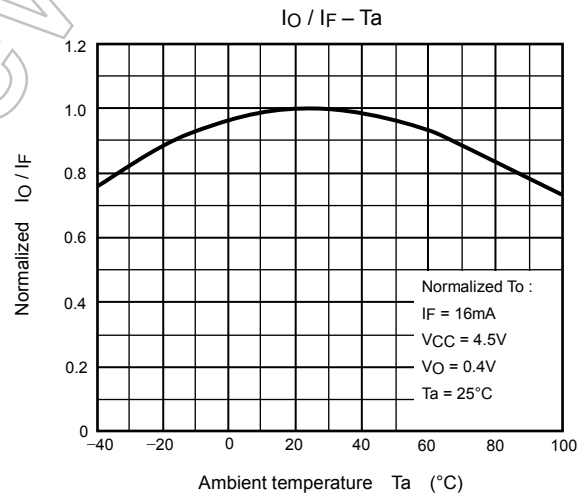
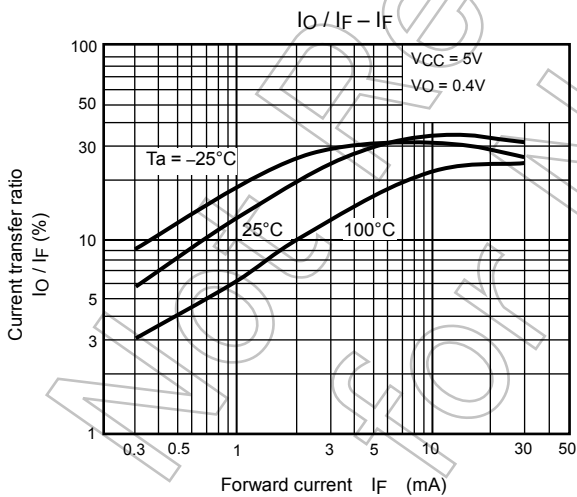
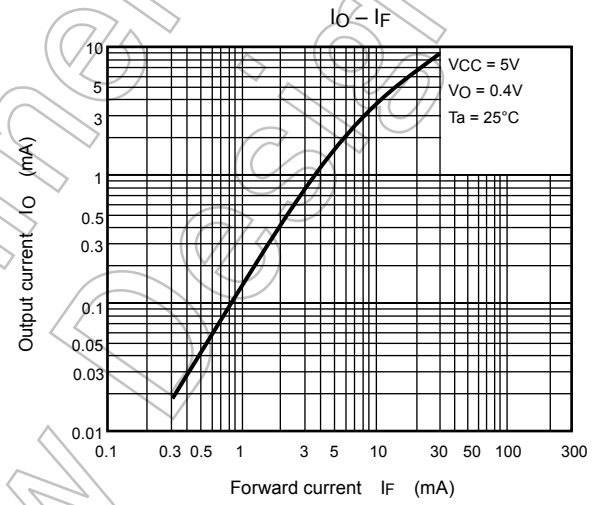
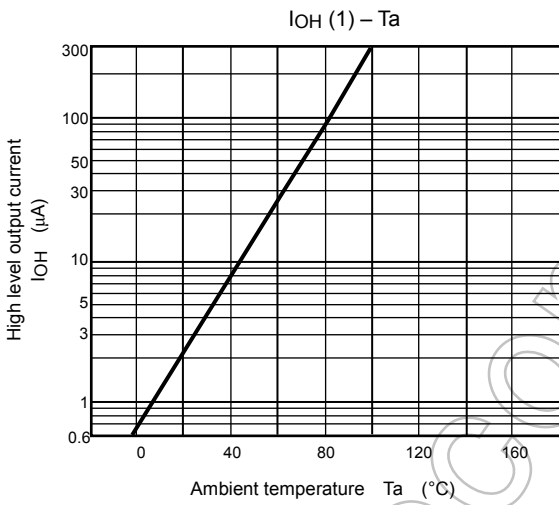
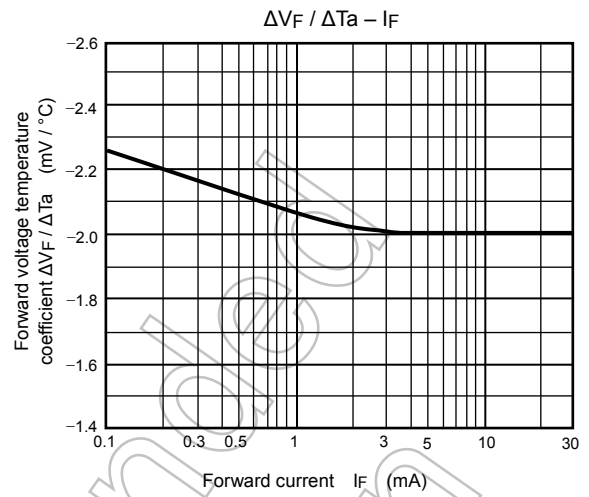
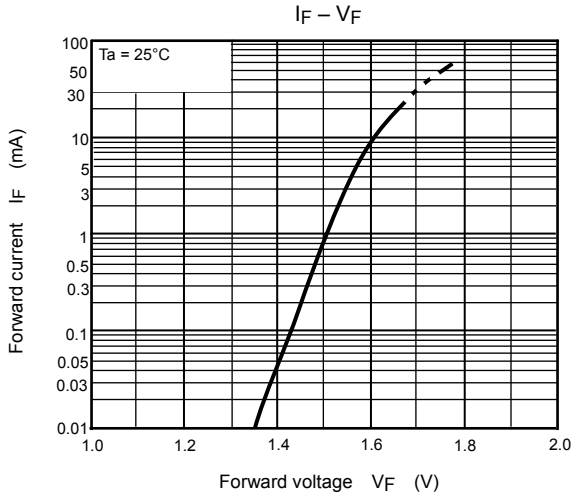


Test Circuit 2: Common Mode Noise Immunity Test Circuit

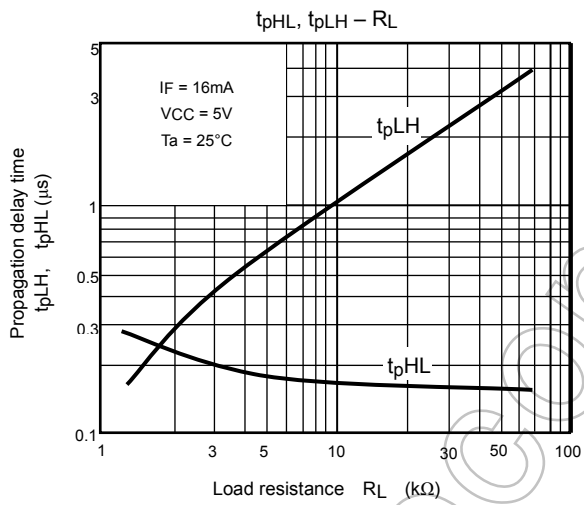
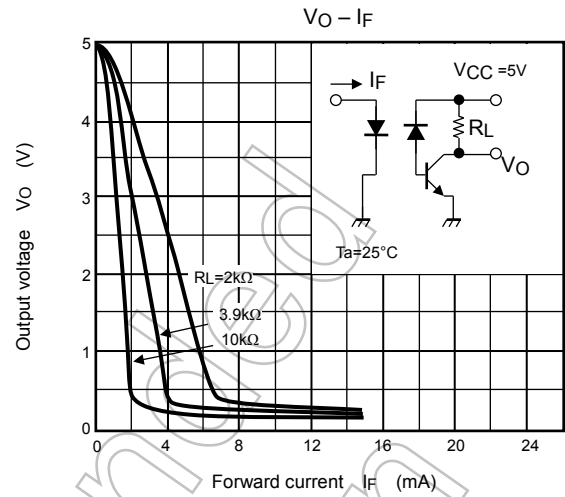
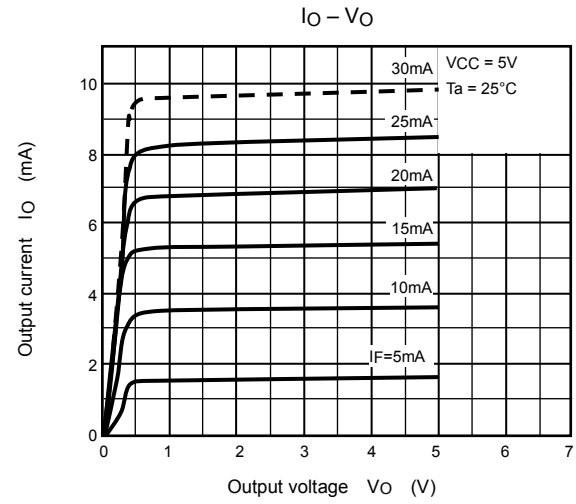


$$CM_H = \frac{160(V)}{t_r(\mu s)}, CM_L = \frac{160(V)}{t_f(\mu s)}$$

Not Recommended for New Design



NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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