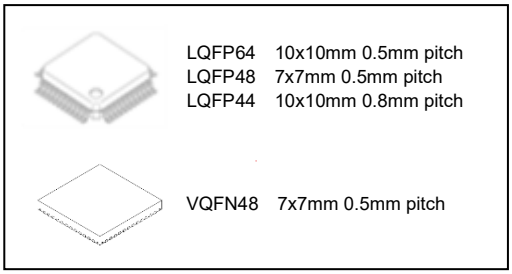
CMOS Digital Integrated Circuit Silicon Monolithic

TMPM4L Group(1)



General Description

- Arm® Cortex®-M4 processor with FPU, Operation frequency: 1 to 80MHz. Operation voltage: 2.7 to 5.5 V
- Flash memory: 128 to 256 KB.
- Package: 44 to 64 pins, 4 types of packages are available.
- Hardware IPs such as A-VE2, 12-bit ADC, and A-PMD2 are provided for implementation of vector control and PFC control

Applications

Motors, consumer equipment with motors, and industrial equipment, etc.

Features

- Cortex-M4 processor with FPU
  - Operating frequency: 1 to 80MHz
  - Support Memory Protection Unit (MPU)
- Operating voltage and low-power consumption mode
  - Operating voltage: 2.7 to 5.5V
  - Low-power consumption mode: IDLE, STOP1 and STOP2 mode
- Operating temperature: -40 to 105°C
- Internal memory
  - Code flash: 128 to 256 KB, rewrite frequencies: up to 100,000 times
  - Data flash: 64 KB, rewrite frequencies: up to 100,000 times (Only product with 128KB code flash)
  - RAM: 32KB, support parity
  - VE RAM: 4KB, not support parity
  - It is possible to rewrite one area while executing instructions in another area.
- Clock
  - External high-speed oscillator (EHOSC): 6 to 24MHz (ceramic and crystal oscillator)
  - External high-speed clock input (EHCLKIN): 6 to 24MHz
  - Internal high-speed oscillator (IHOSC1): 10 MHz, support user trimming
  - PLL: 80MHz
- Oscillation frequency detector (OFD): Abnormal system clock detection
- Voltage detection circuit (LVD): 8 levels, Interrupt or reset signal selectale
- Interrupt
  - External factors: 9 to 21
    Support noise filter (analog/digital)
  - Internal: 72 to 84 factors
- I/O port: 31 to 51 ports
  - Support pull-up and up-down registor, open-drain output, and 5V tolerant input
  - Drive capability of some ports can be selected
- Onchip debug (JTAG/SW/TRACE)
- Trigger selection circuit (TRGSEL)
  - Expand trigger request of DMA controller, timer counter and etc.
- DMA controller (DMAC)
  - Trigger requests: 28 to 32 factors by internal and external triggers
- CRC calculation circuit (CRC): 1 channel
  - CRC32 and CRC16
- Asynchronous serial communication circuit (UART): 4 to 6 channels
  - Up to 5Mbps, support FIFO (transmission: 8 stages, reception: 8 stages)
- Serial peripheral interface (TSPI): 2, 3 channels
  - SIO/SPI mode, up to 20MHz, support FIFO (transmission: 16 bits × 8 stages, reception: 16 bits × 8 stages)
- I^2C Interface version A (EI2C): 1, 2 channels
  - Support multi controller and 10-bit addressing
- Serial memory interface (SMIF): 1 channel
  - Up to two serial memories can be connected
  - Memory capacity 64 KB to 128 MB
  - SPI, Dual, DPI, Quad, QPI
- 12-bit analog to digital converter (ADC): 2 units, 8 to 14 analog inputs
  - Conversion time: 0.975μs at f_{SCLK} = 40MHz
  - Self-diagnosis support function

Start of commercial production
2026-04

- Advanced programmable motor control circuit 2 (A-PMD2): 1 channel
  - Synchronized operation with 3-phase complementary PWM output and 12-bit ADC
  - PFC: support 3-phase interleaved PFC control
  - Emergency stop function (EMG,OVV detection)
- Advanced encoder input circuit 2 (A-ENC2): 1 channel
  - Encoder/sensor (3 types)/timer/phase counter mode
- Advanced vector engine 2 (A-VE2): 1 channel
  - Vector control coprocessor cooperates with ADC/A-PMD2
  - 1-shunt current detection area can be enlarged
  - Dead time compensation control, non-interference control
- Comparator (COMP): 6 channels
  - OVV/EMG detection or interrupt output
- 8-bit DA Converter (DAC): 2 channels
  - Generates reference voltage for comparator
- 32-bit timer event counter (T32A)
  - 5 channels as 32-bit timer, 10 channels as 16-bit timer
  - Interval timer, event counter, input capture, 2-phase plus count, PPG output, synchronous start, and trigger start and stop
- Clock selective watchdog timer (SIWDT): 1 channel
  - Clock other than the system clock can be selected as source clock.
  - Clear window, interrupt or reset output selectable
- Secure access memory (SAM)
  - Flash and RAM access is determined by the settings.

Products Lists Categorized by Functions

The product under development is contained in this table.
For the newest status of each product, Please contact your sales representative.

Table 1.1 Products Lists

Built-in Functions		TMPM4L4FYAUG TMPM4L4FWAUG	TMPM4L2FYADUG TMPM4L2FWADUG	TMPM4L2FYAQG TMPM4L2FWAQG	TMPM4L1FYAUG TMPM4L1FWAUG
Memory	Code Flash (KB)	256 128	256 128	256 128	256 128
	Data Flash (KB)	- 64	- 64	- 64	- 64
	RAM (KB)	32	32	32	32
	VE RAM (KB)	4	4	4	4
I/O port	PORT (pin)	51	35	35	31
External interrupt	Factors	21	13	13	9
	Pins	21	13	13	9
DMA	DMAC (ch)	32	30	30	28
Timer function	T32A (ch)	5	5	5	5
Serial communication function	UART (ch)	6	5	5	4
	EI2C (ch)	2	2	2	1
	TSPI (ch)	3	2	2	2
	SMIF (ch)	1	1	1	1
Analog function	12-bit ADC Unit A/B (AIN ch)	14 / 14	9 / 9	9 / 9	8 / 8
	8-bit DAC (ch)	2	2	2	2
	COMP (ch)	6	6	6	6
Motor control function	A-PMD2 (ch)	1	1	1	1
	A-ENC2 (ch)	1	1	1	1
	A-VE2 (ch)	1	1	1	1
Other function	CRC (ch)	1	1	1	1
	RAMP (ch)	1	1	1	1
System function	LVD (ch)	1	1	1	1
	SIWDT (ch)	1	1	1	1
	OFD (ch)	1	1	1	1
	POR (ch)	1	1	1	1
Security function	SAM	1	1	1	1
Debug interface	DEBUG	JTAG/SW TRACE(2bits)	JTAG/SW	JTAG/SW	JTAG/SW
Package	Package type	LQFP64 (10 mm × 10 mm, 0.5 mm pitch)	LQFP48 (7 mm × 7 mm, 0.5 mm pitch)	VQFN48 (7 mm × 7 mm, 0.5 mm pitch)	LQFP44 (10 mm × 10 mm, 0.8 mm pitch)

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Preface

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC2	Advanced Encoder input Circuit 2
A-PMD2	Advanced Programmable Motor Control Circuit 2
A-VE2	Advanced Vector Engine 2
COMP	Comparator
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
EHOSC	External High-speed Oscillator
EI2C	I^2C Interface Version A
Fm	Fast-mode
IHOSC	Internal High-speed Oscillator
INT	Interrupt
LVD	Voltage Detection Circuit
NMI	Non-maskable Interrupt
OFD	Oscillation Frequency Detector
POR	Power-on Reset Circuit
RAMP	RAM parity
SCOUT	Source Clock Output
SIWDT	Clock Selective Watchdog Timer
SMIF	Serial Memory Interface
TRGSEL	Trigger Selection Circuit
TRM	Trimming Circuit
TSPI	Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Asynchronous Serial Communication Circuit

1. Block Diagram

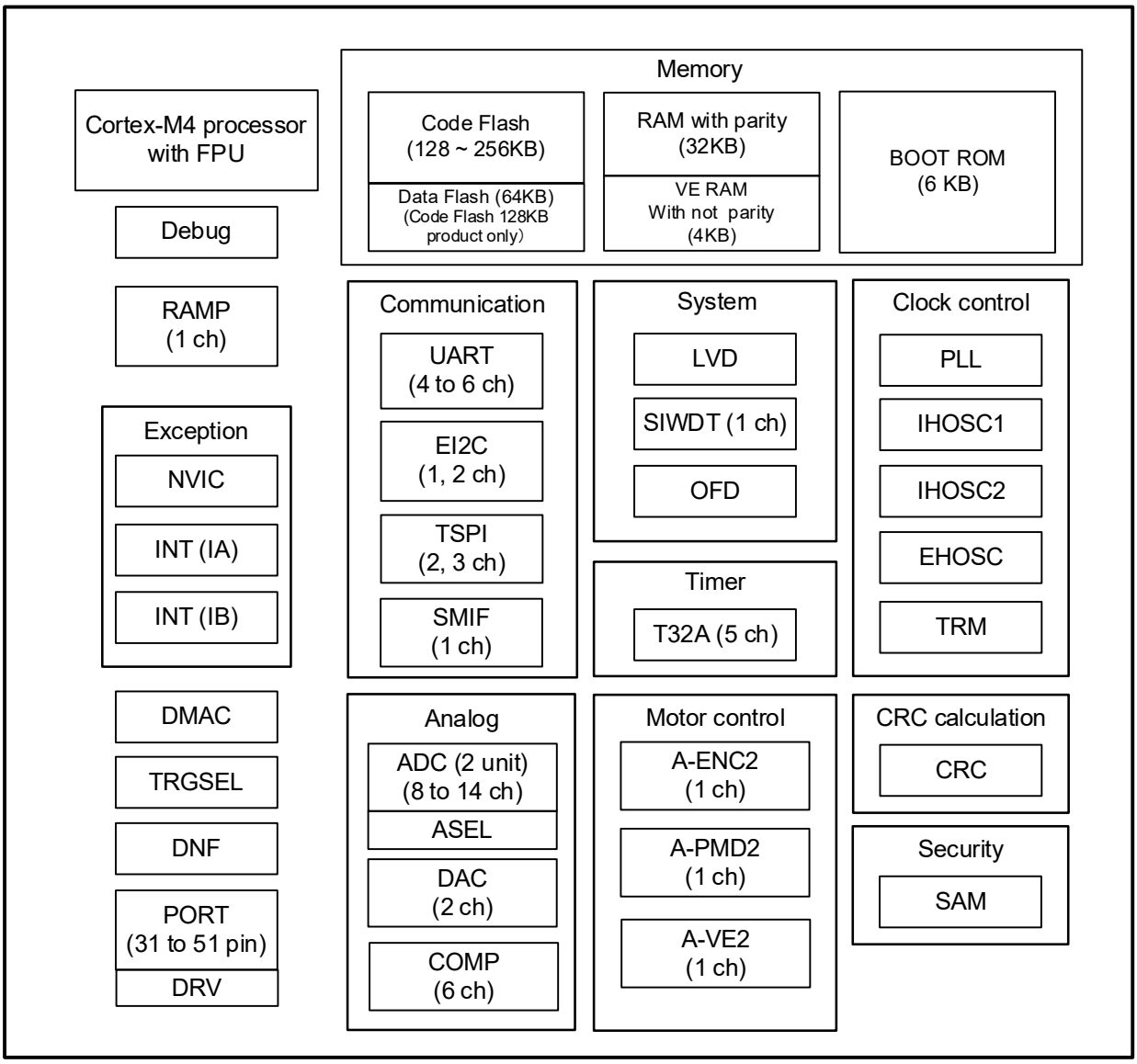
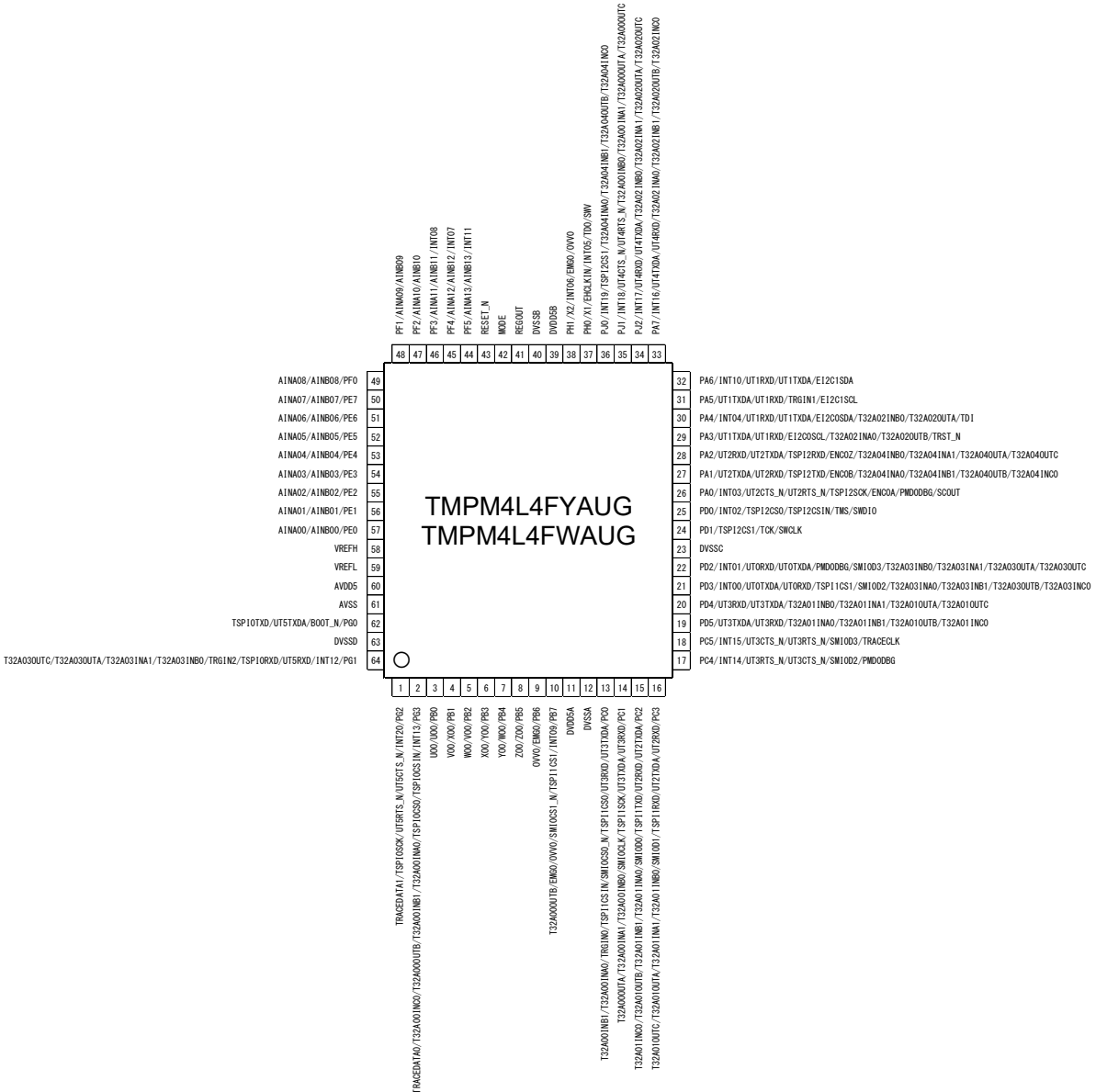


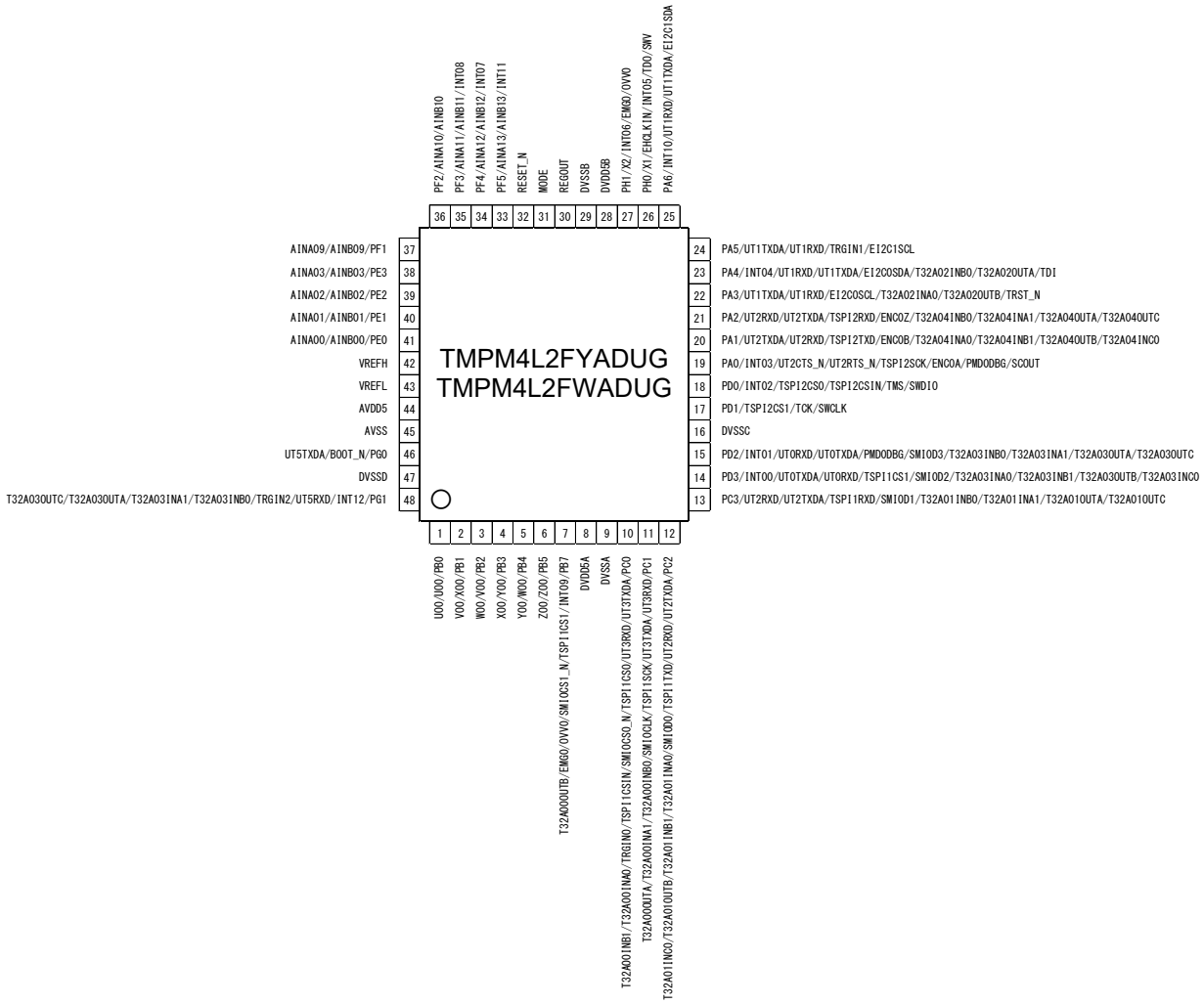
Figure 1.1 Block Diagram of TMPM4L Group(1)

2. Pin Assignment

2.1. LQFP64



2.2. LQFP48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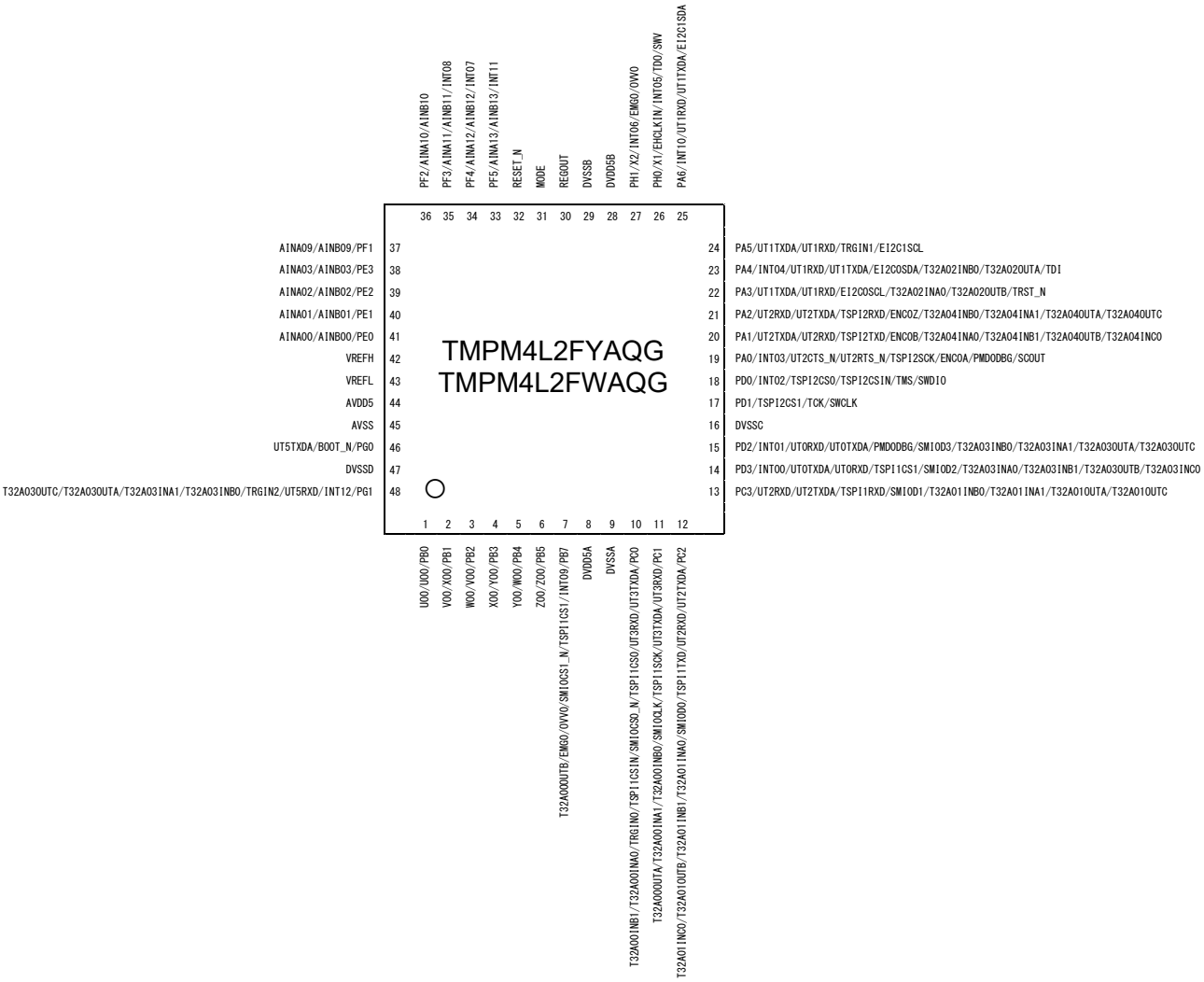
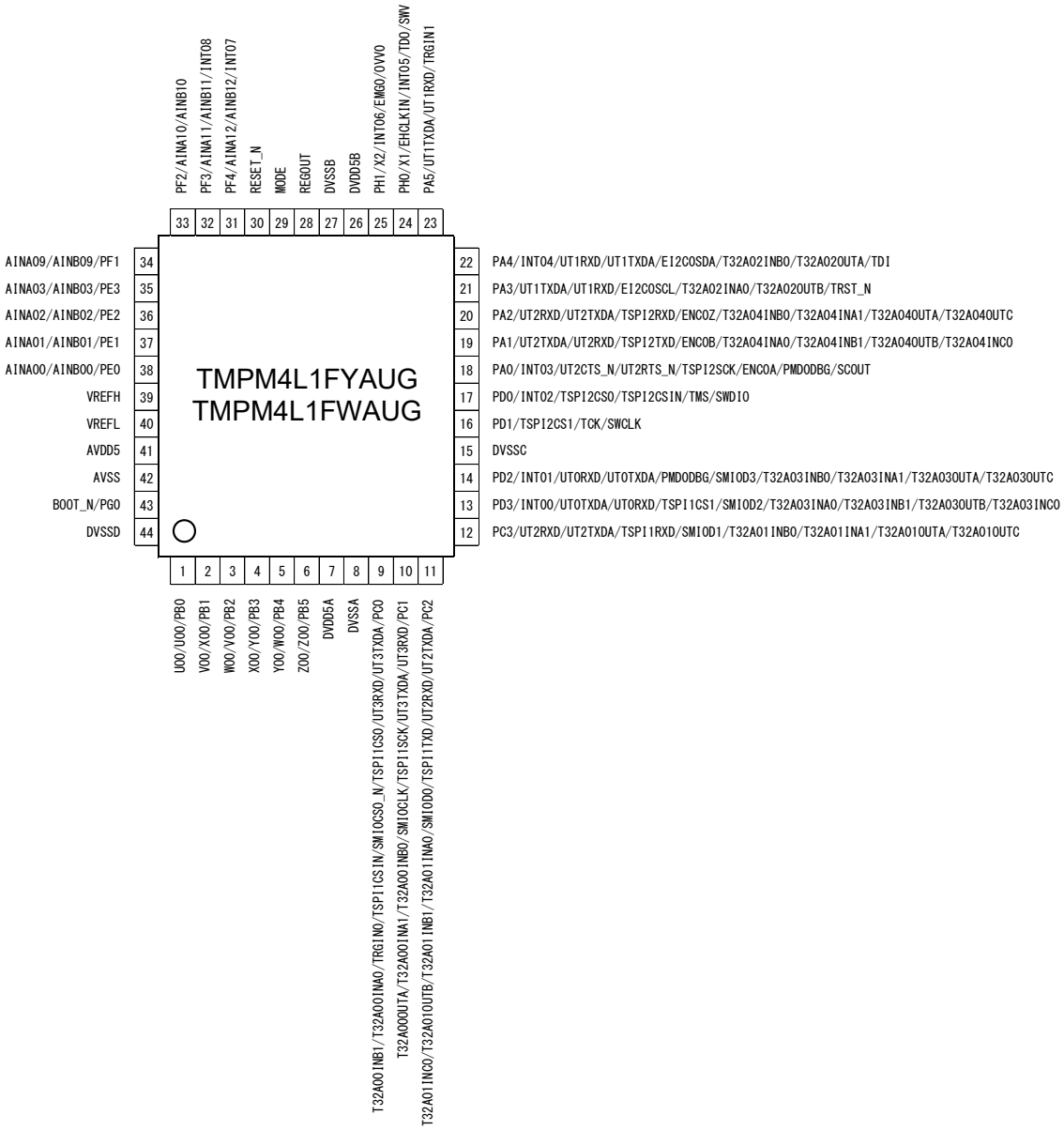
TMPM4L2FWADUG
1 U0O/U0O/PB0
2 V0O/X0O/PB1
3 W0O/Y0O/PB2
4 X0O/Y0O/PB3
5 Y0O/W0O/PB4
6 Z0O/Z0O/PB5
7 T32A00OUTB/EMG0/OVV0/SMI0CS1_N/TSPI1CS1/INT09/PB7
8 DVDD5A
9 DVSSA
10 T32A01NB1/T32A01NA0/TRGIN0/TSPI1CSIN/SMI0CS0_N/TSPI1CS0/UT3RXD/UT3TXDA/PC0
11 T32A00OUTA/T32A01NA1/T32A01NB0/SMI0CLK/TSPI1SCK/UT3TXDA/UT3RXD/PC1
12 T32A01NC0/T32A01OUTB/T32A01INB1/T32A01INA0/SMI0DD0/TSPI1TXD/UT2RXD/UT2TXDA/PC2
13 PC3/UT2RXD/UT2TXDA/TSPI1RXD/SMI0D1/T32A01INB0/T32A01INA1/T32A01OUTA/T32A01OUTC
14 PD3/INT00/UT0TXDA/UT0RXD/TSPI1CS1/SMI0D2/T32A03INA0/T32A03INB1/T32A03OUTB/T32A03INC0
15 PD2/INT01/UT0RXD/UT0TXDA/PMD0DBG/SMI0D3/T32A03INB0/T32A03INA1/T32A03OUTA/T32A03OUTC
16 DVSSC
17 PD1/TSPI2CS1/TCK/SWCLK
18 PD0/INT02/TSPI2CS0/TSPI2CSIN/TMS/SWDIO
19 PA0/INT03/UT2CTS_N/UT2RTS_N/TSPI2SCK/ENC0A/PMD0DBG/SCOUT
20 PA1/UT2TXDA/UT2RXD/TSPI2TXD/ENC0B/T32A04INA0/T32A04INB1/T32A04OUTB/T32A04INC0
21 PA2/UT2RXD/UT2TXDA/TSPI2RXD/ENC0Z/T32A04INB0/T32A04INA1/T32A04OUTA/T32A04OUTC
22 PA3/UT1TXDA/UT1RXD/EI2C0SCL/T32A02INA0/T32A02OUTB/TRST_N
23 PA4/INT04/UT1RXD/UT1TXDA/EI2C0SDA/T32A02INB0/T32A02OUTA/TDI
24 PA5/UT1TXDA/UT1RXD/TRGIN1/EI2C1SCL
25 PA6/INT10/UT1RXD/UT1TXDA/EI2C1SDA
26 PH0/X1/EHCLKIN/INT05/TDO/SWV
27 PH1/X2/INT06/EMG0/OVV0
28 DVDDSB
29 DVSSB
30 REGOUT
31 MODE
32 RESET_N
33 PF5/AINA13/AINB13/INT11
34 PF4/AINA12/AINB12/INT07
35 PF3/AINA11/AINB11/INT08
36 PF2/AINA10/AINB10
37 AINA09/AINB09/PF1
38 AINA03/AINB03/PE3
39 AINA02/AINB02/PE2
40 AINA01/AINB01/PE1
41 AINA00/AINB00/PE0
42 VREFH
43 VREFL
44 AVDD5
45 AVSS
46 UT5TXDA/BOOT_N/PG0
47 DVSSD
48 T32A03OUTC/T32A03OUTA/T32A03INA1/T32A03INB0/TRGIN2/UT5RXD/INT12/PG1

2.3. VQFN48


TMPM4L2FYAQG
TMPM4L2FWAQG
1 UO0/UO0/PB0
2 VO0/XO0/PB1
3 WO0/YO0/PB2
4 XO0/YO0/PB3
5 YO0/WO0/PB4
6 ZO0/ZO0/PB5
7 T32A00OUTB/EMG0/OVV0/SMI0CS1_N/TSPI1CS1/INT09/PB7
8 DVDD5A
9 DVSSA
10 T32A01INB1/T32A00INA0/TRGIN0/TSPI1CSIN/SMI0CSO_N/TSPI1CSO/UT3RXD/UT3TXDA/PD0
11 T32A00OUTA/T32A00INA1/T32A00INB0/SMI0CLK/TSPI1SCK/UT3TXDA/UT3RXD/PC1
12 T32A01INC0/T32A01OUTB/T32A01INB1/T32A01INA0/SMI0DO/TSPI1TXD/UT2RXD/UT2TXDA/PC2
13 PC3/UT2RXD/UT2TXDA/TSPI1RXD/SMI0D1/T32A01INB0/T32A01INA1/T32A01OUTA/T32A01OUTC
14 PD3/INT00/UT0TXDA/UT0RXD/TSPI1CS1/SMI0D2/T32A03INA0/T32A03INB1/T32A03OUTB/T32A03INC0
15 PD2/INT01/UT0RXD/UT0TXDA/PMD0DBG/SMI0D3/T32A03INB0/T32A03INA1/T32A03OUTA/T32A03OUTC
16 DVSSC
17 PD1/TSPI2CS1/TCK/SWCLK
18 PD0/INT02/TSPI2CS0/TSPI2CSIN/TMS/SWDIO
19 PA0/INT03/UT2CTS_N/UT2RTS_N/TSPI2SCK/ENC0A/PMD0DBG/SCOUT
20 PA1/UT2TXDA/UT2RXD/TSPI2TXD/ENC0B/T32A04INA0/T32A04INB1/T32A04OUTB/T32A04INC0
21 PA2/UT2RXD/UT2TXDA/TSPI2RXD/ENC0Z/T32A04INB0/T32A04INA1/T32A04OUTA/T32A04OUTC
22 PA3/UT1TXDA/UT1RXD/EI2C0SCL/T32A02INA0/T32A02OUTB/TRST_N
23 PA4/INT04/UT1RXD/UT1TXDA/EI2C0SDA/T32A02INB0/T32A02OUTA/TDI
24 PA5/UT1TXDA/UT1RXD/TRGIN1/EI2C1SCL
25 PA6/INT10/UT1RXD/UT1TXDA/EI2C1SDA
26 PH0/X1/EHCLKIN/INT05/TDO/SWV
27 PH1/X2/INT06/EMG0/OVV0
28 DVDD5B
29 DVSSB
30 REGOUT
31 MODE
32 RESET_N
33 PF5/AINA13/AINB13/INT11
34 PF4/AINA12/AINB12/INT07
35 PF3/AINA11/AINB11/INT08
36 PF2/AINA10/AINB10
37 AINA09/AINB09/PF1
38 AINA03/AINB03/PE3
39 AINA02/AINB02/PE2
40 AINA01/AINB01/PE1
41 AINA00/AINB00/PE0
42 VREFH
43 VREFL
44 AVDD5
45 AVSS
46 UT5TXDA/BOOT_N/PG0
47 DVSSD
48 T32A03OUTC/T32A03OUTA/T32A03INA1/T32A03INB0/TRGIN2/UT5RXD/INT12/PG1

2.4. LQFP44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TMPM4L1FWAUG
1 U00/UO0/PB0
2 V00/XO0/PB1
3 W00/VO0/PB2
4 X00/YO0/PB3
5 Y00/WO0/PB4
6 Z00/ZO0/PB5
7 DVDD5A
8 DVSSA
9 T32A00INB1/T32A00INA0/TRG1NO/TSPI1CS0_N/TSPI1CS0/UT3RXD/UT3TXDA/PC0
10 T32A00OUTA/T32A00INA1/T32A00INB0/SMI0CLK/TSPI1SCK/UT3TXDA/UT3RXD/PC1
11 T32A01ING0/T32A01OUTB/T32A01INB1/T32A01INA0/SMI0DO/TSPI1TXD/UT2RXD/UT2TXDA/PC2
12 PC3/UT2RXD/UT2TXDA/TSPI1RXD/SMI0D1/T32A01INB0/T32A01INA1/T32A01OUTA/T32A01OUTC
13 PD3/INT00/UT0TXDA/UT0RXD/TSPI1CS1/SMI0D2/T32A03INA0/T32A03INB1/T32A03OUTB/T32A03INC0
14 PD2/INT01/UT0RXD/UT0TXDA/PMD0DBG/SMI0D3/T32A03INB0/T32A03INA1/T32A03OUTA/T32A03OUTC
15 DVSSC
16 PD1/TSPI2CS1/TCK/SWCLK
17 PD0/INT02/TSPI2CS0/TSPI2CSIN/TMS/SWDIO
18 PA0/INT03/UT2CTS_N/UT2RTS_N/TSPI2SCK/ENC0A/PMD0DBG/SCOUT
19 PA1/UT2TXDA/UT2RXD/TSPI2TXD/ENC0B/T32A04INA0/T32A04INB1/T32A04OUTB/T32A04INC0
20 PA2/UT2RXD/UT2TXDA/TSPI2RXD/ENC0Z/T32A04INB0/T32A04INA1/T32A04OUTA/T32A04OUTC
21 PA3/UT1TXDA/UT1RXD/EI2C0SCL/T32A02INA0/T32A02OUTB/TRST_N
22 PA4/INT04/UT1RXD/UT1TXDA/EI2C0SDA/T32A02INB0/T32A02OUTA/TDI
23 PA5/UT1TXDA/UT1RXD/TRG1N1
24 PH0/X1/EHCLKIN/INT05/TDO/SWV
25 PH1/X2/INT06/EMG0/OVV0
26 DVDD5B
27 DVSSB
28 RE0OUT
29 MODE
30 RESET_N
31 PF4/AINA12/AINB12/INT07
32 PF3/AINA11/AINB11/INT08
33 PF2/AINA10/AINB10
34 AINA09/AINB09/PF1
35 AINA03/AINB03/PE3
36 AINA02/AINB02/PE2
37 AINA01/AINB01/PE1
38 AINA00/AINB00/PE0
39 VREFH
40 VREFL
41 AVDD5
42 AVSS
43 BOOT_N/PG0
44 DVSSD

3. Pin Description

3.1. Functional Pin Names and Functions

3.1.1. Functional Pins of Peripheral

Table 3.1 Functional Pin Names and Functions

Peripheral function	Pin name	Input or Output	Function
Clock control and operation mode (CG)	SCOUT	Output	Clock output
Interrupt control (IA/IB)	INTx	Input	External interrupt input External input pin provides the noise filter (analog/digital).
32-bit timer event counter (T32A)	T32AxINA0	Input	16-bit timer A input capture input 0
	T32AxINA1	Input	16-bit timer A input capture input 1
	T32AxOUTA	Output	16-bit timer A output
	T32AxINB0	Input	16-bit timer B input capture input 0
	T32AxINB1	Input	16-bit timer B input capture input 1
	T32AxOUTB	Output	16-bit timer B output
	T32AxINC0	Input	32-bit timer input capture input 0
	T32AxOUTC	Output	32-bit timer output
Serial peripheral interface (TSPI)	TSPIxSCK	I/O	Clock input/output
	TSPIxRXD	Input	Data input
	TSPIxTXD	Output	Data output
	TSPIxCSIN	Input	Chip select input
	TSPIxCS0	Output	Chip select output 0
	TSPIxCS1	Output	Chip select output 1
Asynchronous serial communication circuit (UART)	UTxRXD	Input	Data input
	UTxTXDA	Output	Data output A
	UTxCTS_N	Input	Transmission possible input
	UTxRTS_N	Output	Transmission request output
I^2C interface version A (EI2C)	EI2CxSDA	I/O	Data input/output
	EI2CxSCL	I/O	Clock input/output
Serial memory Interface (SMIF)	SMIxCLK	Output	Clock output
	SMIxD0	I/O	Data input/output 0
	SMIxD1	I/O	Data input/output 1
	SMIxD2	I/O	Data input/output 2
	SMIxD3	I/O	Data input/output 3
	SMIxCS0_N	Output	Chip select 0
	SMIxCS1_N	Output	Chip select 1
Advanced programmable motor control circuit 2 (A-PMD2)	EMGx	Input	Emergency detection input
	OVVx	Input	Overvoltage detection input
	UOx	Output	U-phase output
	VOx	Output	V-phase output
	WOx	Output	W-phase output
	XOx	Output	X-phase output
	YOx	Output	Y-phase output
	ZOx	Output	Z-phase output
	PMDxDBG	Output	Debug output for motor control

Peripheral function	Pin name	Input or Output	Function
Advanced encoder input circuit 2 (A-ENC2)	ENCxA	Input	Encoder input A
	ENCxB	Input	Encoder input B
	ENCxZ	Input	Encoder input Z
12-bit analog to digital converter (ADC)	AINAx/ AINBx	Input	Analog input
Trigger selection circuit (TRGSEL)	TRGINx	Input	External trigger input

Note: "x" means channel number, unit number or interrupt number.

3.1.2. Debug Pins

Table 3.2 Debug Pin Names and Functions

Debug PORT	Pin name	Input or Output	Function
JTAG	TMS	Input	JTAG test mode selection input
	TCK	Input	JTAG serial clock input
	TDO	Output	JTAG serial data output
	TDI	Input	JTAG serial data input
	TRST_N	Input	JTAG test reset input
SW	SWDIO	I/O	Serial wire data input/output
	SWCLK	Input	Serial wire clock input
	SWV	Output	Serial wire viewer output
TRACE	TRACECLK	Output	Trace clock output
	TRACEDATA0	Output	Trace data output 0
	TRACEDATA1	Output	Trace data output 1

3.1.3. Control Pins

Table 3.3 Control Pin Names and Functions

	Pin name	Input or Output	Function
Control Pin	X1	Input	This pin connects high-speed oscillator.
	X2	Output	This pin connects high-speed oscillator.
	EHCLKIN	Input	External clock input
	BOOT_N	Input	BOOT mode control The BOOT mode control pin is sampled on the rising edge of the RESET_N pin input. It is not sampled by internal reset factor. If the BOOT mode control pin is "Low" level, the MCU enters single boot mode. If it is "High" level, the MCU enters single chip mode. For details of single boot mode, refer to the Reference Manual "Flash Memory".
	RESET_N	Input	Reset signal
	MODE	Input	This pin must be fixed to "Low" level.

3.1.4. Power Supply Pins

Table 3.4 Power Supply Pin Names and Functions

	Pin name	Function
Power Supply	DVDD5A (Note1) DVDD5B (Note1)	Power supply for digital DVDD5A/B supplies the power to the following pins: PA to PD, PG, PH, PJ, MODE, RESET_N
	DVSSA (Note2) DVSSB (Note2) DVSSC (Note2) DVSSD (Note2)	GND for digital
	REGOUT (Note3)	This pin connects capacitor for regulator. (Note4)
	AVDD5 VREFH	These pins are the power supply (AVDD5) for analog and the reference power (VREFH) for analog. AVDD5 supplies the power to the following pins: PE, PF
	AVSS VREFL	These pins are the GND (AVSS) for analog and the reference GND (VREFL) for analog.

Note1: Apply same voltage to DVDD5A and DVDD5B except the case that the pins are not provided.

Note2: Apply same voltage to DVSSA, DVSSB, DVSSC, and DVSSD except the case that the pins are not provided.

Note3: For REGOUT, do not cause a short circuit with DVDD5A, DVDD5B, or DVSSA, DVSSB, DVSSC, or DVSSD.

Note4: For the capacitor value, refer to the "6.14. Regulator".

3.1.5. Capacitors between Power Supply Pins

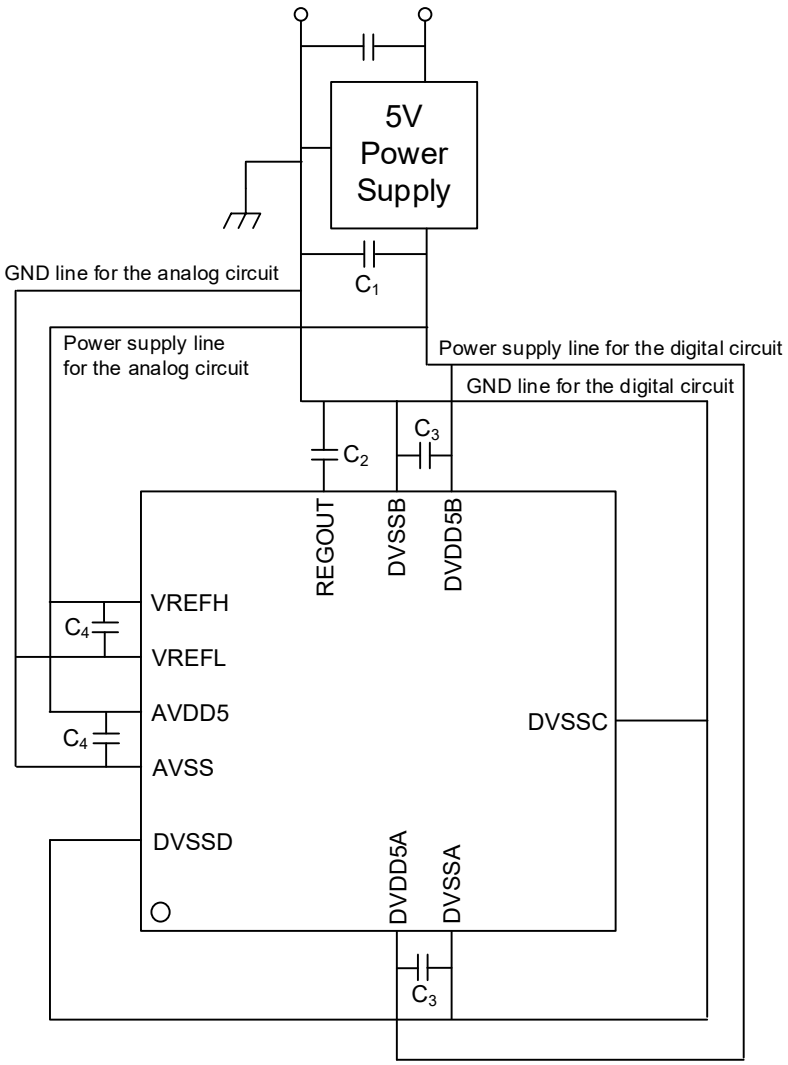


Figure 3.1 Connection Diagram of Capacitors between Power Supply Pins

Note1: Insert a ceramic capacitor (C_1) near the output pin of the power supply. The power gradient with C_1 must be satisfied V_{PON} and V_{POFF} in "6.5. Characteristics of Internal Processing at RESET".

Note2: Insert the bypass capacitor ((C_3, C_4:0.01 µF to 0.1 µF) between the power supply and GND near each MCU power supply pin.

Note3: Insert the power supply stabilizing ceramic capacitor (C_2) of the same capacity into the capacitor connection pin for the internal regulator (REGOUT). The capacitor should be placed near DVSSB pin. Regarding value of capacitor, refer to "6.14. Regulator".

Note4: In order to suppress noise mixing from the power supply for digital to the analog circuit, separate the power supply line for analog and the power supply line for digital near the power supply output pin.

Note5: In order to suppress noise mixing from the peripheral circuit to the analog circuit, when inserting a filter circuit or pull-up/down resistor to the input/output pin of the analog power supply system, connect the components that make up these circuits to the power supply line for analog.

Note6: In order to suppress high-frequency noise received from the loop circuit by the power supply line, the GND line, and the capacitor, do not separate the power supply line and the GND line from each other.

3.2. Functional Pins and Ports Assignment (in pin number order)

Following table shows the pin number for each product and the port assignment which were seen from the functional pin.

"-" means that it does not have a pin or there is no assignment of a function.

Table 3.5 Signal Connection List (1/6)

Function	Combination functional pin name	Port name	M4L4 (LQFP64)	M4L2 (LQFP48/VQFN48)	M4L1 (LQFP44)
UART ch 0	UT0RXD	PD2	22	15	14
		PD3	21	14	13
	UT0TXDA	PD2	22	15	14
		PD3	21	14	13
UART ch 1	UT1RXD	PA3	29	22	21
		PA4	30	23	22
		PA5	31	24	23
		PA6	32	25	-
	UT1TXDA	PA3	29	22	21
		PA4	30	23	22
		PA5	31	24	23
		PA6	32	25	-
UART ch 2	UT2RXD	PC2	15	12	11
		PC3	16	13	12
		PA1	27	20	19
		PA2	28	21	20
	UT2TXDA	PC2	15	12	11
		PC3	16	13	12
		PA1	27	20	19
		PA2	28	21	20
	UT2CTS_N	PA0	26	19	18
	UT2RTS_N	PA0	26	19	18
UART ch 3	UT3RXD	PC0	13	10	9
		PC1	14	11	10
		PD5	19	-	-
		PD4	20	-	-
	UT3TXDA	PC0	13	10	9
		PC1	14	11	10
		PD5	19	-	-
		PD4	20	-	-
	UT3CTS_N	PC4	17	-	-
		PC5	18	-	-
	UT3RTS_N	PC4	17	-	-
		PC5	18	-	-
UART ch 4	UT4RXD	PA7	33	-	-
		PJ2	34	-	-
	UT4TXDA	PA7	33	-	-
		PJ2	34	-	-
	UT4CTS_N	PJ1	35	-	-
	UT4RTS_N	PJ1	35	-	-
UART ch 5	UT5RXD	PG1	64	48	-
	UT5TXDA	PG0	62	46	-
	UT5CTS_N	PG2	1	-	-
	UT5RTS_N	PG2	1	-	-

Table 3.6 Signal Connection List (2/6)

Function	Combination functional pin name	Port name	M4L4 (LQFP64)	M4L2 (LQFP48/VQFN48)	M4L1 (LQFP44)
EI2C ch 0	EI2C0SCL	PA3	29	22	21
	EI2C0SDA	PA4	30	23	22
EI2C ch 1	EI2C1SCL	PA5	31	24	-
	EI2C1SDA	PA6	32	25	-
TSPI ch 0	TSPI0RXD	PG1	64	-	-
	TSPI0TXD	PG0	62	-	-
	TSPI0SCK	PG2	1	-	-
	TSPI0CSIN	PG3	2	-	-
	TSPI0CS0	PG3	2	-	-
TSPI ch 1	TSPI1RXD	PC3	16	13	12
	TSPI1TXD	PC2	15	12	11
	TSPI1SCK	PC1	14	11	10
	TSPI1CSIN	PC0	13	10	9
	TSPI1CS0	PC0	13	10	9
	TSPI1CS1	PD3	21	14	13
		PB7	10	7	-
TSPI ch 2	TSPI2RXD	PA2	28	21	20
	TSPI2TXD	PA1	27	20	19
	TSPI2SCK	PA0	26	19	18
	TSPI2CSIN	PD0	25	18	17
	TSPI2CS0	PD0	25	18	17
	TSPI2CS1	PD1	24	17	16
		PJ0	36	-	-
SMIF ch 0	SMI0CS0_N	PC0	13	10	9
	SMI0CS1_N	PB7	10	7	-
	SMI0CLK	PC1	14	11	10
	SMI0D0	PC2	15	12	11
	SMI0D1	PC3	16	13	12
	SMI0D2	PC4	17	-	-
		PD3	21	14	13
	SMI0D3	PC5	18	-	-
		PD2	22	15	14

Table 3.7 Signal Connection List (3/6)

Function	Combination functional pin name	Port name	M4L4 (LQFP64)	M4L2 (LQFP48/VQFN48)	M4L1 (LQFP44)
T32A ch 0	T32A00INA0	PG3	2	-	-
		PC0	13	10	9
	T32A00INA1	PC1	14	11	10
		PJ1	35	-	-
	T32A00OUTA	PC1	14	11	10
		PJ1	35	-	-
	T32A00INB0	PC1	14	11	10
		PJ1	35	-	-
	T32A00INB1	PG3	2	-	-
		PC0	13	10	9
	T32A00OUTB	PG3	2	-	-
		PB7	10	7	-
	T32A00INC0	PG3	2	-	-
	T32A00OUTC	PJ1	35	-	-
T32A ch 1	T32A01INA0	PC2	15	12	11
		PD5	19	-	-
	T32A01INA1	PC3	16	13	12
		PD4	20	-	-
	T32A01OUTA	PC3	16	13	12
		PD4	20	-	-
	T32A01INB0	PC3	16	13	12
		PD4	20	-	-
	T32A01INB1	PC2	15	12	11
		PD5	19	-	-
	T32A01OUTB	PC2	15	12	11
		PD5	19	-	-
	T32A01INC0	PC2	15	12	11
		PD5	19	-	-
	T32A01OUTC	PC3	16	13	12
		PD4	20	-	-
T32A ch 2	T32A02INA0	PA3	29	22	21
		PA7	33	-	-
	T32A02INA1	PJ2	34	-	-
	T32A02OUTA	PA4	30	23	22
		PJ2	34	-	-
	T32A02INB0	PA4	30	23	22
		PJ2	34	-	-
	T32A02INB1	PA7	33	-	-
	T32A02OUTB	PA3	29	22	21
		PA7	33	-	-
	T32A02INC0	PA7	33	-	-
	T32A02OUTC	PJ2	34	-	-

Table 3.8 Signal Connection List (4/6)

Function	Combination functional pin name	Port name	M4L4 (LQFP64)	M4L2 (LQFP48/VQFN48)	M4L1 (LQFP44)
T32A ch 3	T32A03INA0	PD3	21	14	13
	T32A03INA1	PD2	22	15	14
		PG1	64	48	-
	T32A03OUTA	PD2	22	15	14
		PG1	64	48	-
	T32A03INB0	PD2	22	15	14
		PG1	64	48	-
	T32A03INB1	PD3	21	14	13
	T32A03OUTB	PD3	21	14	13
	T32A03INC0	PD3	21	14	13
	T32A03OUTC	PD2	22	15	14
		PG1	64	48	-
T32A ch 4	T32A04INA0	PA1	27	20	19
		PJ0	36	-	-
	T32A04INA1	PA2	28	21	20
	T32A04OUTA	PA2	28	21	20
	T32A04INB0	PA2	28	21	20
	T32A04INB1	PA1	27	20	19
		PJ0	36	-	-
	T32A04OUTB	PA1	27	20	19
		PJ0	36	-	-
	T32A04INC0	PA1	27	20	19
		PJ0	36	-	-
	T32A04OUTC	PA2	28	21	20
12-bit ADC unit A unit B	AINA13/ AINB13	PF5	44	33	-
	AINA12/ AINB12	PF4	45	34	31
	AINA11/ AINB11	PF3	46	35	32
	AINA10/ AINB10	PF2	47	36	33
	AINA09/ AINB09	PF1	48	37	34
	AINA08/ AINB08	PF0	49	-	-
	AINA07/ AINB07	PE7	50	-	-
	AINA06/ AINB06	PE6	51	-	-
	AINA05/ AINB05	PE5	52	-	-
	AINA04/ AINB04	PE4	53	-	-
	AINA03/ AINB03	PE3	54	38	35
	AINA02/ AINB02	PE2	55	39	36
	AINA01/ AINB01	PE1	56	40	37
	AINA00/ AINB00	PE0	57	41	38

Table 3.9 Signal Connection List (5/6)

Function	Combination functional pin name	Port name	M4L4 (LQFP64)	M4L2 (LQFP48/VQFN48)	M4L1 (LQFP44)
INT	INT00	PD3	21	14	13
	INT01	PD2	22	15	14
	INT02	PD0	25	18	17
	INT03	PA0	26	19	18
	INT04	PA4	30	23	22
	INT05	PH0	37	26	24
	INT06	PH1	38	27	25
	INT07	PF4	45	34	31
	INT08	PF3	46	35	32
	INT09	PB7	10	7	-
	INT10	PA6	32	25	-
	INT11	PF5	44	33	-
	INT12	PG1	64	48	-
	INT13	PG3	2	-	-
	INT14	PC4	17	-	-
	INT15	PC5	18	-	-
	INT16	PA7	33	-	-
	INT17	PJ2	34	-	-
	INT18	PJ1	35	-	-
	INT19	PJ0	36	-	-
	INT20	PG2	1	-	-
A-PMD2 ch 0	EMG0	PB6	9	-	-
		PB7	10	7	-
		PH1	38	27	25
	OVV0	PB6	9	-	-
		PB7	10	7	-
		PH1	38	27	25
	UO0	PB0	3	1	1
	VO0	PB1	4	2	2
		PB2	5	3	3
	WO0	PB2	5	3	3
		PB4	7	5	5
	XO0	PB1	4	2	2
		PB3	6	4	4
	YO0	PB3	6	4	4
		PB4	7	5	5
	ZO0	PB5	8	6	6
	PMD0DBG	PC4	17	-	-
		PD2	22	15	14
		PA0	26	19	18
A-ENC2 ch 0	ENC0A	PA0	26	19	18
	ENC0B	PA1	27	20	19
	ENC0Z	PA2	28	21	20

Table 3.10 Signal Connection List (6/6)

Function	Combination functional pin name	Port name	M4L4 (LQFP64)	M4L2 (LQFP48/VQFN48)	M4L1 (LQFP44)
TRGSEL	TRGIN0	PC0	13	10	9
	TRGIN1	PA5	31	24	23
	TRGIN2	PG1	64	48	-
JTAG/SW	TMS	PD0	25	18	17
	TCK	PD1	24	17	16
	TDO	PH0	37	26	24
	TDI	PA4	30	23	22
	TRST_N	PA3	29	22	21
	SWDIO	PD0	25	18	17
	SWCLK	PD1	24	17	16
	SWV	PH0	37	26	24
TRACE	TRACECLK	PC5	18	-	-
	TRACEDATA0	PG3	2	-	-
	TRACEDATA1	PG2	1	-	-
Control pin	X1	PH0	37	26	24
	X2	PH1	38	27	25
	EHCLKIN	PH0	37	26	24
	SCOUT	PA0	26	19	18
	BOOT_N	PG0	62	46	43
	RESET_N		43	32	30
	MODE		42	31	29
Power supply pin	VREFH		58	42	39
	VREFL		59	43	40
	AVDD5		60	44	41
	AVSS		61	45	42
	DVDD5A		11	8	7
	DVDD5B		39	28	26
	DVSSA		12	9	8
	DVSSB		40	29	27
	DVSSC		23	16	15
	DVSSD		63	47	44
	REGOUT		41	30	28

3.3. Port List

The symbols of each table of the port have the following meanings.

- Combination Function A and B: These are the functions which are assigned without setting port function registers.
- Combination Function 1 to 8: These are the functions which are assigned with setting port function registers.

- Input/Output: Input or/and output of port
  - Input: Input port
  - Output: Output port
  - I/O: Input/Output port

- PU/PD: Programmable pull-up or/and pull-down register
  - PU: Programmable pull-up resistor can be enabled.
  - PD: Programmable pull-down resistor can be enabled.

- OD: Programmable open-drain output
  - YES: Supported
  - NO: Not supported

- 5V_T: 5V-tolerant input
  - YES: Supported
  - N/A: Not available

- SMT/CMOS: Input gate
  - SMT: Schmitt trigger input
  - CMOS: CMOS input

- DRV: Drive capability selection
  - YES: Supported
  - NO: Not supported

- Under Reset: Port state under reset
  - Hi-Z: High impedance
  - PU: Pull-up resistor enabled
  - PD: Pull-down resistor enabled

- After Reset: Port state after reset
  - Hi-z: High impedance
  - PU: Pull-up resistor enabled
  - PD: Pull-down resistor enabled

Table 3.11 Port List

M4L4 LQFP64	M4L2 LQFP48 VQFN48	M4L1 LQFP44	Pin name	Combination function A	Combination function B	Combination function 1	Combination function 2	Combination function 3	Combination function 4	Combination function 5	Combination function 6	Combination function 7	Combination function 8	Input/ output	PU/PD	OD	5V_T	SMT/ CMOS	DRV	Under reset	After reset
1	-	-	PG2		INT20	UT5CTS_N	UT5RTS_N	TSPI0SCK					TRACEDATA1	I/O	PU/PD	YES	N/A	SMT	YES	Hi-Z	Hi-Z
2	-	-	PG3		INT13		TSPI0CSIN	TSPI0CS0	T32A00INA0	T32A00INB1	T32A00OUTB	T32A00INC0	TRACEDATA0	I/O	PU/PD	YES	N/A	SMT	YES	Hi-Z	Hi-Z
3	1	1	PB0								UO0	UO0		I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
4	2	2	PB1								XO0	VO0		I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
5	3	3	PB2								VO0	WO0		I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
6	4	4	PB3								YO0	XO0		I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
7	5	5	PB4								WO0	YO0		I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
8	6	6	PB5								ZO0	ZO0		I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
9	-	-	PB6								EMG0	OVV0		I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
10	7	-	PB7		INT09			TSPI1CS1	SMI0CS1_N		OVV0	EMG0	T32A00OUTB	I/O	PU/PD	YES	N/A	SMT	YES	Hi-Z	Hi-Z
11	8	7	DVDD5A											-	-	-	-	-	-	-	-
12	9	8	DVSSA											-	-	-	-	-	-	-	-
13	10	9	PC0			UT3TXDA	UT3RXD	TSPI1CS0	SMI0CS0_N	TSPI1CSIN	TRGIN0	T32A00INA0	T32A00INB1	I/O	PU/PD	YES	N/A	SMT	YES	Hi-Z	Hi-Z
14	11	10	PC1			UT3RXD	UT3TXDA	TSPI1SCK	SMI0CLK		T32A00INB0	T32A00INA1	T32A00OUTA	I/O	PU/PD	YES	N/A	SMT	YES	Hi-Z	Hi-Z
15	12	11	PC2			UT2TXDA	UT2RXD	TSPI1TXD	SMI0D0	T32A01INA0	T32A01INB1	T32A01OUTB	T32A01INC0	I/O	PU/PD	YES	N/A	SMT	YES	Hi-Z	Hi-Z
16	13	12	PC3			UT2RXD	UT2TXDA	TSPI1RXD	SMI0D1	T32A01INB0	T32A01INA1	T32A01OUTA	T32A01OUTC	I/O	PU/PD	YES	N/A	SMT	YES	Hi-Z	Hi-Z
17	-	-	PC4		INT14	UT3RTS_N	UT3CTS_N		SMI0D2				PMD0DBG	I/O	PU/PD	YES	N/A	SMT	YES	Hi-Z	Hi-Z
18	-	-	PC5		INT15	UT3CTS_N	UT3RTS_N		SMI0D3				TRACECLK	I/O	PU/PD	YES	N/A	SMT	YES	Hi-Z	Hi-Z
19	-	-	PD5			UT3TXDA	UT3RXD		T32A01INA0	T32A01INB1	T32A01OUTB	T32A01INC0		I/O	PU/PD	YES	YES	SMT	NO	Hi-Z	Hi-Z
20	-	-	PD4			UT3RXD	UT3TXDA		T32A01INB0	T32A01INA1	T32A01OUTA	T32A01OUTC		I/O	PU/PD	YES	YES	SMT	NO	Hi-Z	Hi-Z
21	14	13	PD3		INT00	UT0TXDA	UT0RXD	TSPI1CS1	SMI0D2	T32A03INA0	T32A03INB1	T32A03OUTB	T32A03INC0	I/O	PU/PD	YES	N/A	SMT	YES	Hi-Z	Hi-Z
22	15	14	PD2		INT01	UT0RXD	UT0TXDA	PMD0DBG	SMI0D3	T32A03INB0	T32A03INA1	T32A03OUTA	T32A03OUTC	I/O	PU/PD	YES	N/A	SMT	YES	Hi-Z	Hi-Z
23	16	15	DVSSC											-	-	-	-	-	-	-	-
24	17	16	PD1				TSPI2CS1						TCK/SWCLK	I/O	PU/PD	YES	N/A	SMT	YES	PD (Note 2)	PD (Note 2)
25	18	17	PD0		INT02			TSPI2CS0	TSPI2CSIN				TMS/SWDIO	I/O	PU/PD	YES	N/A	SMT	YES	PU (Note 2)	PU (Note 2)
26	19	18	PA0		INT03	UT2CTS_N	UT2RTS_N	TSPI2SCK	ENC0A			PMD0DBG	SCOUT	I/O	PU/PD	YES	N/A	SMT	YES	Hi-Z	Hi-Z
27	20	19	PA1			UT2TXDA	UT2RXD	TSPI2TXD	ENC0B	T32A04INA0	T32A04INB1	T32A04OUTB	T32A04INC0	I/O	PU/PD	YES	N/A	SMT	YES	Hi-Z	Hi-Z
28	21	20	PA2			UT2RXD	UT2TXDA	TSPI2RXD	ENC0Z	T32A04INB0	T32A04INA1	T32A04OUTA	T32A04OUTC	I/O	PU/PD	YES	N/A	SMT	YES	Hi-Z	Hi-Z
29	22	21	PA3			UT1TXDA	UT1RXD			EI2C0SCL	T32A02INA0	T32A02OUTB	TRST_N	I/O	PU/PD	YES	YES	SMT	NO	PU (Note 2)	PU(注 2)
30	23	22	PA4		INT04	UT1RXD	UT1TXDA			EI2C0SDA	T32A02INB0	T32A02OUTA	TDI	I/O	PU/PD	YES	YES	SMT	NO	PU (Note 2)	PU (Note 2)
31	24	23	PA5			UT1TXDA	UT1RXD		TRGIN1	EI2C1SCL				I/O	PU/PD	YES	YES	SMT	NO	Hi-Z	Hi-Z
32	25	-	PA6		INT10	UT1RXD	UT1TXDA			EI2C1SDA				I/O	PU/PD	YES	YES	SMT	NO	Hi-Z	Hi-Z
33	-	-	PA7		INT16	UT4TXDA	UT4RXD			T32A02INA0	T32A02INB1	T32A02OUTB	T32A02INC0	I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
34	-	-	PJ2		INT17	UT4RXD	UT4TXDA			T32A02INB0	T32A02INA1	T32A02OUTA	T32A02OUTC	I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
35	-	-	PJ1		INT18	UT4CTS_N	UT4RTS_N			T32A00INB0	T32A00INA1	T32A00OUTA	T32A00OUTC	I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
36	-	-	PJ0		INT19		TSPI2CS1			T32A04INA0	T32A04INB1	T32A04OUTB	T32A04INC0	I/O	PU/PD	YES	N/A	SMT	YES	Hi-Z	Hi-Z
37	26	24	PH0	X1	EHCLKIN/INT05								TDO/SWV	I/O	PD	YES	N/A	SMT	NO	Hi-Z (Note 3)	Hi-Z (Note 3)
38	27	25	PH1	X2	INT06						EMG0	OVV0		I/O	PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
39	28	26	DVDD5B											-	-	-	-	-	-	-	-
40	29	27	DVSSB											-	-	-	-	-	-	-	-
41	30	28	REGOUT											-	-	-	-	-	-	-	-
42	31	29	MODE											Input	PD	-	-	SMT	-	-	-
43	32	30	RESET_N											Input	PU	-	-	SMT	-	-	-
44	33	-	PF5	AINA13/AINB13	INT11									I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
45	34	31	PF4	AINA12/AINB12	INT07									I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
46	35	32	PF3	AINA11/AINB11	INT08									I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
47	36	33	PF2	AINA10/AINB10										I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
48	37	34	PF1	AINA09/AINB09										I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
49	-	-	PF0	AINA08/AINB08										I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
50	-	-	PE7	AINA07/AINB07										I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
51	-	-	PE6	AINA06/AINB06										I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
52	-	-	PE5	AINA05/AINB05										I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
53	-	-	PE4	AINA04/AINB04										I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z

M4L4 LQFP64	M4L2 LQFP48 VQFN48	M4L1 LQFP44	Pin name	Combination function A	Combination function B	Combination function 1	Combination function 2	Combination function 3	Combination function 4	Combination function 5	Combination function 6	Combination function 7	Combination function 8	Input/ output	PU/PD	OD	5V_T	SMT/ CMOS	DRV	Under reset	After reset
54	38	35	PE3	AINA03/AINB03										I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
55	39	36	PE2	AINA02/AINB02										I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
56	40	37	PE1	AINA01/AINB01										I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
57	41	38	PE0	AINA00/AINB00										I/O	PU/PD	YES	N/A	SMT	NO	Hi-Z	Hi-Z
58	42	39	VREFH											-	-	-	-	-	-	-	-
59	43	40	VREFL											-	-	-	-	-	-	-	-
60	44	41	AVDD5											-	-	-	-	-	-	-	-
61	45	42	AVSS											-	-	-	-	-	-	-	-
62	46	43	PG0	BOOT_N		UT5TXDA		TSPI0TXD						Output (Note 1)	PU/PD	YES	N/A	SMT	YES	Hi-Z (Note 1)	Hi-Z
63	47	44	DVSSD											-	-	-	-	-	-	-	-
64	48	-	PG1		INT12	UT5RXD		TSPI0RXD	TRGIN2	T32A03INB0	T32A03INA1	T32A03OUTA	T32A03OUTC	I/O	PU/PD	YES	N/A	SMT	YES	Hi-Z	Hi-Z

Note1: During the reset period caused by the reset pin (RESET_N), pull-up and input are enabled, and the state of the BOOT_N pin can be input.

Note2: The initial value is assigned to the debug pin, and the internal pull-up or pull-down resistor is enabled.

Note3: This pin does not become output until the command is received from the tool.

4. Functional Description and Operation Description

4.1. Reference Manuals

For more information of built-in functions on TMPM4L Group(1), refer to the Reference Manuals below;
In addition, the following product-specific information is listed in "Product Information," so refer to that as well.

- Base address of peripheral functions
- Signal connection between peripheral functions
- Product-specific specification for peripheral functions
- Product-specific restriction for peripheral functions
- Register that have specific value for each product
- Register that must be set to specific value for each product

Table 4.1 Reference Manuals for TMPM4L Group(1)

Reference manual	IP symbol	Category
Clock Control and Operation Mode (TMPM4L Group(1))	CG-M4L(1)	System
Exception (TMPM4L Group(1))	EXCEPT-M4L(1)	System
Input/Output Ports (TMPM4L Group(1))	PORT-M4L(1)	System
Product Information (TMPM4L Group(1))	PINFO-M4L(1)	System
Trimming Circuit	TRM-C	Peripheral
Oscillation Frequency Detector	OFD-A	Peripheral
Voltage Detection Circuit	LVD-D2	Peripheral
Digital Noise Filter Circuit	DNF-A	Peripheral
Debug Interface	DEBUG-A	Peripheral
DMA Controller	DMAC-B	Peripheral
Asynchronous Serial Communication Circuit	UART-C	Peripheral
Serial Peripheral Interface	TSPI-E	Peripheral
Serial Memory Interface	SMIF-D	Peripheral
I^2C Interface version A	EI2C-A2	Peripheral
8-bit Digital to Analog Converter	DAC-B	Peripheral
12-bit Analog to Digital Converter	ADC-F	Peripheral
Comparator	COMP-D	Peripheral
Advanced Programmable Motor Control Circuit 2	A-PMD2-A	Peripheral
Advanced Encoder Input Circuit 2	A-ENC2-A	Peripheral
Advanced vector engine 2	A-VE2-A	Peripheral
32-bit Timer Event Counter	T32A-C	Peripheral
Clock Selective Watchdog Timer	SIWDT-A	Peripheral
Flash Memory	FLASH256F-A	Peripheral
Security Function	SECG2-A	Peripheral
Secure Access Memory	SAM-A	Peripheral
CRC Calculation Circuit	CRC-A	Peripheral
RAM Parity	RAMP-B	Peripheral

4.2. Processor Core

The TMPM4L Group(1) incorporates a high-performance 32-bit processor core (Cortex-M4 processor with FPU).
For the operation of the processor core, refer to the "Arm Cortex-M4 Processor Technical Reference Manual".
This section explains the product-specific information.

4.2.1. Core Information

The Cortex-M4 processor with FPU revision used in the TMPM4L Group(1) is shown as below:

Table 4.2 Core Revision

Group name	Core revision
TMPM4L Group(1)	r0p1

4.2.2. Configurable Options

In the Cortex-M4 processor with FPU, some blocks can be selected to implement. The following table shows the configurations of the TMPM4L Group(1).

Table 4.3 Configurable Options and Their Implementations

Configurable option	Implementation
FWB	Literal comparator: 2 Instruction comparator: 6
DWT	Comparator: 4
ITM	Available
MPU	Available
ETM	Available
AHB-AP	Available
AHB trace macro cell interface	Not available
TPIU	Available
WIC	Not available
Debug port	JTAG/Serial wire
Bit band	Available
Sequential control of AHB	Not available

4.3. Clock Control and Operating Mode (CG)

The clock control and operating mode (CG) selects a clock gear ratio and the prescaler clock, or warm-up time of the oscillator.

There are NORMAL mode and low-power consumption mode as operating modes. Power consumption can be decreased by operating mode transition for use purposes.

The outline of the clock/mode control circuit is as follows:

- Internal high-speed oscillator (IHOSC1): 10MHz
- Selectable from the external high-speed oscillator (EHOSC) or internal high-speed oscillator (IHOSC1).
- Clock multiplication circuit (PLL):
  For system clock, capable of 80MHz output by changing the multiplication ratio according to fosc.
- Clock gear:
  The high-speed clock can be divided by 1, 2, 4, 8, or 16 and used as the system clock (fsys).
- Low-power consumption mode:
  IDLE mode: Only CPU is stopped. The operation of each peripheral circuit can be enabled or disabled.
  STOP1 mode: All the internal circuits including the internal high-speed oscillator are brought to a stop.
  STOP2 mode: Some functions are retained and the internal power supply is shut down.

4.4. Flash Memory

The flash memory is organized as follows:

- Page: 128B
- Block: 8KB
- Area: 128KB (maximum)

Writing is done in page units.

Erasing is done in blocks, areas, or the entire chip.

Writing/erasing can be prohibited in block units. (Flash protect function)

There are two areas, areas 0 and 1, and it is possible to rewrite one area while rewriting another area. (Dual mode)

In products with 128KB code flash, 64KB of area 1 is used as data flash.

4.5. Oscillator

External high-speed oscillator (EHOSC):	Pins of EHOSC are connected crystal resonator or ceramic resonator. Use as clock source for system clock (fsys).
Internal high-speed oscillator 1 (IHOSC1):	The oscillation frequency is 10MHz. Use as clock source for system clock (fsys).
Internal high-speed oscillator 2 (IHOSC2):	The oscillation frequency is 10MHz. Use as the reference clock of OFD and clock source of SIWDT.

4.6. Trimming Circuit (TRM)

The trimming circuit (TRM) can adjust oscillation frequency of the internal high-speed oscillator 1 (IHOSC1).

4.7. Oscillation Frequency Detector (OFD)

The oscillation frequency detector (OFD) can detect an abnormal system clock. The external high-speed clock (f_{EHOSC}) or high-speed clock (fc) can be selected as the target of detection.

The selected clock is measured by the internal high-speed oscillator 2 (IHOSC2) which is used as the reference clock of OFD. If the clock frequency of f_{EHOSC} or fc is out of the specified range, a reset signal occurs.

The upper limit and lower limit of detection frequency ranges can be specified respectively.

4.8. Voltage Detection Circuit (LVD)

The voltage detection circuit (LVD) detects whether a power-supply voltage is lower or higher than the preset voltage. When a lower or higher voltage than the preset voltage is detected, the LVD generates an interrupt request or internal reset signal.

Setting voltage can be selected from eight voltages. The LVD is set to enable from resetting when the power supply is turned on.

4.9. Digital Noise Filter Circuit (DNF)

The digital noise filter circuit (DNF) can eliminate the noise of signal from an external interrupt input pin. The high and low noise from an external interrupt signal INTx is eliminated.

4.10. Debug Interface (DEBUG)

The serial wire debug ports (SWCLK and SWDIO) and the JTAG debug ports (TDI, TDO, TMS, TCK, and TRST_N) use for the interface for connecting debug tool. These pins are connected with the debug tool and used for the program development. And also the trace clock (TRACECLK), trace outputs (TRACEDATA0, 1) are used to reduce the debug process.

4.11. DMA Controller (DMAC)

The DMA controller (DMAC) is the peripheral function to move the data between peripheral function and the memory, or between memories. These operations are performed separately from the CPU control; thus, the CPU load can be greatly reduced by using the DMA.

TMPM4L Group(1) products have one unit of DMAC. One DMAC has the DMA requests of the 32 channels.

4.12. Asynchronous Serial Communication Circuit (UART)

The asynchronous serial communication circuit (UART) is asynchronous serial communication function. It can select the data length of 7, 8 or 9 bits, use or not use parity bit, and a STOP bit length of 1 or 2 bits. Moreover, selection of the MSB first/LSB first, data signal polarity can be performed and pin exchanged of UTxTXDA/UTxRXD can be performed by a port setting.

The FIFO buffer supports data communication on 9 bits × 8 stages at transmission; and on 9 bits × 8 stages at reception.

4.13. Serial Peripheral Interface (TSPI)

The serial peripheral interface (TSPI) on TMPM4L Group(1) products supports SPI mode which uses a CS (Chip Select) signal and SIO mode which does not use a CS signal at communications. It performs the serial communication with other device at high speed.

It can change the data length from 7 bits with a parity bit to 32 bits without a parity bit on a per bit basis

The TSPI has the reception and transmission 16-bit FIFO on 8 stages. The TSPI on TMPM4L Group(1) products supports the controller device operation and target device operation.

The TSPI can use the frame mode (frame length: 8 to 32 bits) or sector mode (sector length: 2 to 4 sectors and frame length: 8 to 128 bits).

4.14. Serial Memory Interface (SMIF)

SMIF is an interface for connecting to devices (SPI Flash and others) with serial I/O or multiple I/O communication interface devices. Up to two serial memories can be connected per channel. The access method supports direct access and indirect access. For communication mode between SMIF and serial memory, read / write is supported for STR-SPI (Standard SPI compatible), STR-Dual (direct access only), STR-DPI (direct access only), STR-Quad, STR-QPI.

4.15. I^2C Interface Version A (EI2C)

The I^2C Interface version A (EI2C) is compatible with two-wire bidirectional serial communications of I^2C interface between the controller and target devices. The EI2C supports the multi-controller bus which two or more controller devices on the same bus in.

And also, it supports standard-mode (transfer speed: up to 100kHz), fast-mode (transfer speed: up to 400kHz), and fast-mode Plus (transfer speed: up to 1MHz) . Its addressing mode supports 7-bit and 10-bit addressing.

4.16. 8-bit Digital to Analog Converter (DAC)

The DAC is an R-2R type 8-bit digital to analog converter that can output the specified voltage. The DAC can be used as a reference voltage for the comparator (COMP).

4.17. 12-bit Analog to Digital Converter (ADC)

The 12-bit analog to digital converter (ADC) is a successive-approximation analog-to-digital converter. The combination of conversion result register and analog input can be programmed for each AD conversion start factor.

The AD conversion start factor is selected from a software or the peripheral functions (trigger output of A-PMD, timer/event counter output, or port input).

The monitor function is available and it can generate an interrupt request when the compare conditions are matched.

The ADC incorporates a selector to connect VREFH/VREFL with reference power supply. Controlling by software can support self-diagnosis function.

4.18. Comparator (COMP)

The comparator compares the analog input voltage with a reference voltage. The reference voltage uses the DAC output.

The comparison condition can be selected as greater than or less than the reference voltage. This function allows the comparator of two channels to be configured as a window comparator.

The comparison result can be output as an interrupt, or as either EMG detection or OVV detection for use with the A-PMD2.

4.19. Advanced Programmable Motor Control Circuit 2 (A-PMD2)

The advanced programmable motor control circuit 2 (A-PMD2) controls the brushless DC motors easily. It incorporates the pulse modulation circuit and dead-time circuit, and easily generates waveforms for motor control by coordinating with the 3-phase complementary PWM and ADC.

It also provides the over-voltage detection input and abnormal detection input to support safety measures.

Furthermore, it can provide the 3-phase interleaved PFC control for power factor improvement.

4.20. Advanced Encoder Input Circuit 2 (A-ENC2)

The advanced encoder input circuit 2 (A-ENC2) supports an incremental encoder to acquire the motor position easily. The noise canceller is built-in the signal input pin of A-ENC32, so that the signals from an incremental encoder or Hall sensor can be input directly.

The A-ENC32 provides six operating modes: encoder mode, sensor modes (3 types), timer mode, and phase counter mode.

4.21. Advanced Vector Engine 2 (A-VE2)

The Advanced Vector Engine 2 executes with the ADC and A-PMD2 to perform vector calculation processing in hardware.

Also, it provides 1-shunt current detection area enlargement process, dead time compensation control, and non-interfere control.

When working with the ADC, the ADC connection selection circuit (ASEL) selects which of the two units to work with. For details about ASEL, refer to "12-bit Analog-to-Digital Converter (ADC)" of "Product Specific Information" in the Reference Manual.

4.22. 32-bit Timer Event Counter (T32A)

The 32-bit timer event counter (T32A) is a timer event counter that can operate as a 32-bit timer or two 16-bit timers. The option to select whether T32A operates as a 32-bit timer or a 16-bit timer is available. When the T32A operates as 32-bit timer, the T32A operates as timer C incorporating a 32-bit counter. When the T32A operates as 16-bit timer, the T32A operates as timer A and B incorporating a 16-bit counter.

The T32A has various functions such as an interval timer, event counter, input capture, 2-phase pulse count, PPG output, synchronous start, and trigger start and stop.

4.23. Clock Selective Watchdog Timer (SIWDT)

The clock selective watchdog timer (SIWDT) is a peripheral function that detects an overflow of the counter and generates an interrupt request or reset signal. This state occurs when a counter cannot be cleared within the preset detection time because the CPU executes mal function (a runaway) caused by a noise or others.

The count clock for the counter can be selected from three clocks: system clock (fsys) of 4 division, internal high-speed oscillation clock 1 (f_{IHOSC1}), or internal high-speed oscillation clock 2 (f_{IHOSC2}).

It also provides the count-clear window function that can clear the binary counter only for the specified period.

Moreover, change of a register can be prohibited by setting to protected mode until the MCU is reset. (the counter can be cleared in the protection mode.)

4.24. Secure Access Memory (SAM)

The secure access memory (SAM) monitors flash and RAM access from bus manager.

It has three states, and it can set the accessible areas for each state.

4.25. CRC Calculation Circuit (CRC)

The TMPM4L Group(1) products incorporate the hardware calculation circuit for CRC32 and CRC16.

It can be used for detecting errors by processing a memory and communication data.

4.26. RAM Parity (RAMP)

The RAM parity (RAMP) generates an even parity for one byte data at the timing of writing data to RAM and stores it to RAM at same time. The RAMP checks that the total number of 1s in the data and parity bit is even when the CPU read data in RAM. When parity errors is detected, the RAM parity interrupt occurs.

The error status and address which the error generated in can be monitored.

A parity error can be is detected in real time, since parity generating/checking is performed by the hardware.

4.27. Measures for Security Risk

TMPM4L group(1) has five security risk measures to protect internal data, product controls, and other assets. The assumed access paths and protection targets are shown for each operation mode.

For more information, refer to the reference manual “Security Function”.

4.27.1. Configuration

Figure 4.1 outlines the relationship between the functions in the product and the security functions.

Specifications for the Flash Writer Mode and the TOSHIBA Test Mode are not disclosed.

NBDIF is not implemented in some products.

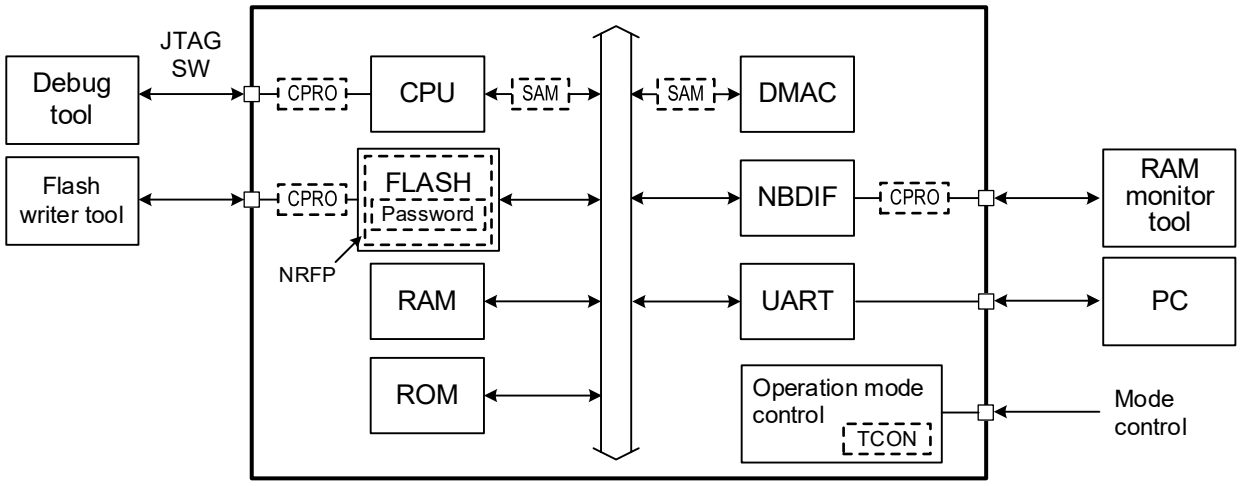


Figure 4.1 Measures for Security Risk

4.27.2. Outline

(1) Chip Protect (CPRO)
The Chip Protect prohibits communication with debug tools and RAM monitor tools. It also prohibits flash writer tools from reading and writing to flash memory. If the Secure Access Memory is also enabled, the Flash Writer Mode is prohibited.

Table 4.1 Access Paths and Protection Targets (1)

Operation mode	Access path	Protected object
Single Chip Mode Single Boot Mode	JTAG/SW/NBDIF	CPU FLASH/ROM/RAM
Flash Writer Mode	Flash writer	FLASH

(2) Password in RAM Transfer Command
The Single Boot Mode is operated by sending a command via UART communication.
The RAM transfer command is authenticated by the password.

Table 4.2 Access Paths and Protection Targets (2)

Operation mode	Access path	Protected object
Single Boot Mode	UART	CPU FLASH/ROM/RAM

(3) Non-releasable Flash Protect (NRFP)

The Non-releasable Flash Protect prohibits writing and erasing of the specified area of the Flash memory. Combined use of the Lock setting will prevent the user from releasing the Non-releasable Flash Protection.

The Single Boot Mode and the Flash Writer Mode are not started when the Non-releasable Flash Protect is enabled.

Table 4.3 Access Paths and Protection Targets (3)

Operation mode	Access path	Protected object
Single Chip Mode	JTAG/SW Internal bus	FLASH

(4) Secure Access Memory (SAM)

The Secure Access Memory controls the access (read, write, and execute) from the bus manager to specified areas of the Flash memory and RAM. Combined use of the Lock setting will prevent the user from releasing the Secure Access Memory.

The Single Boot Mode is not started when the Secure Access Memory is enabled.

Table 4.4 Access Paths and Protection Targets (4)

Operation mode	Access path	Protected object
Single Chip Mode	Internal bus	FLASH/RAM

(5) TOSHIBA Test Mode Control (TCON)

The TOSHIBA Test Mode Control prohibits the start of our test mode.

The Flash Writer Mode is not started when the TOSHIBA Test Mode Control is enabled.

Table 4.5 Access Paths and Protection Targets (5)

Operation mode	Access path	Protected object
TOSHIBA Test Mode	Not disclosed	CPU FLASH/ROM/RAM

4.27.3. Disclaimer

Refer to "RESTRICTIONS ON PRODUCT USE" at the end of this manual.

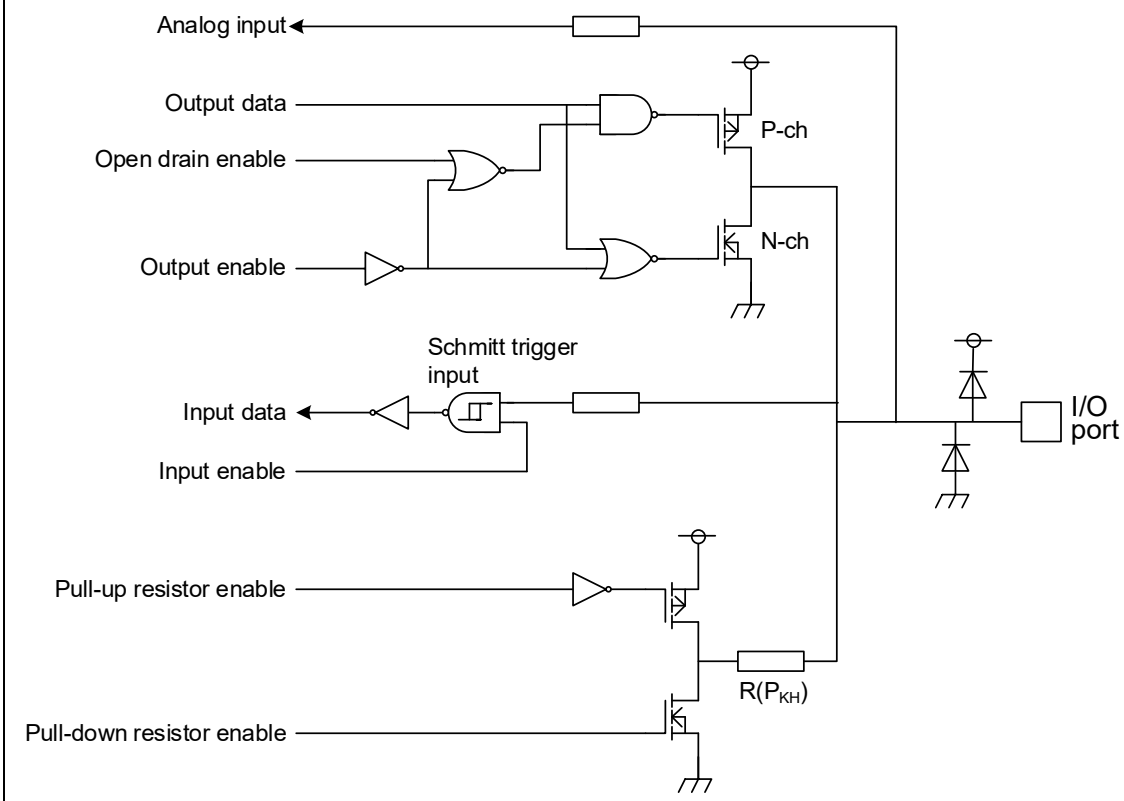
5. Equivalent Circuit

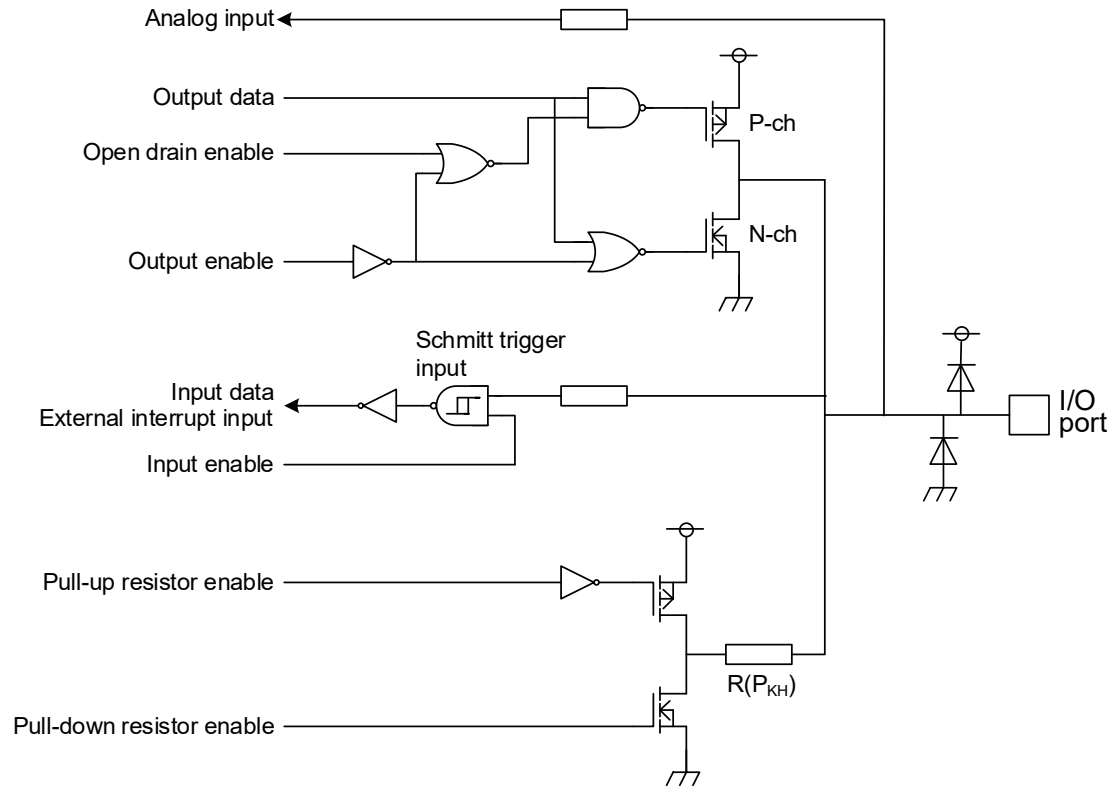
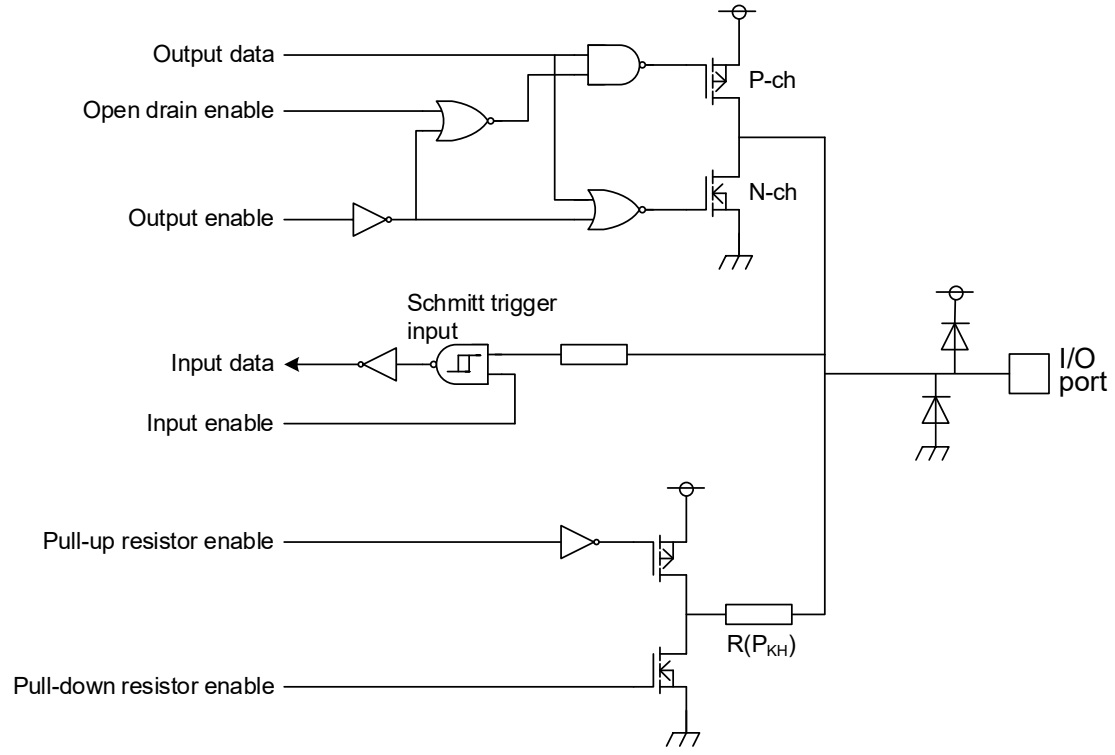
Basically, the gate symbols written are the same as those used for the standard CMOS logic IC “74HCXX” series.
The input protection resistor ranges from several tens of Ω to several hundred Ω.
For details on the drive capability selection function, refer to "I/O Ports" in the reference manual.

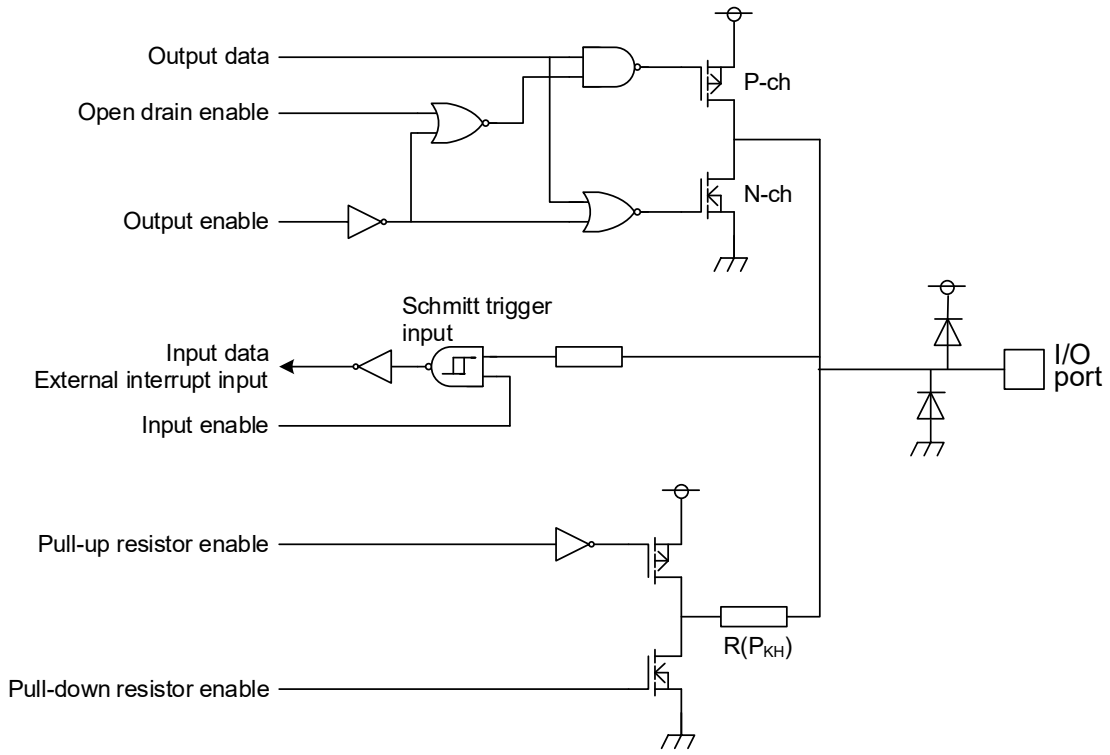
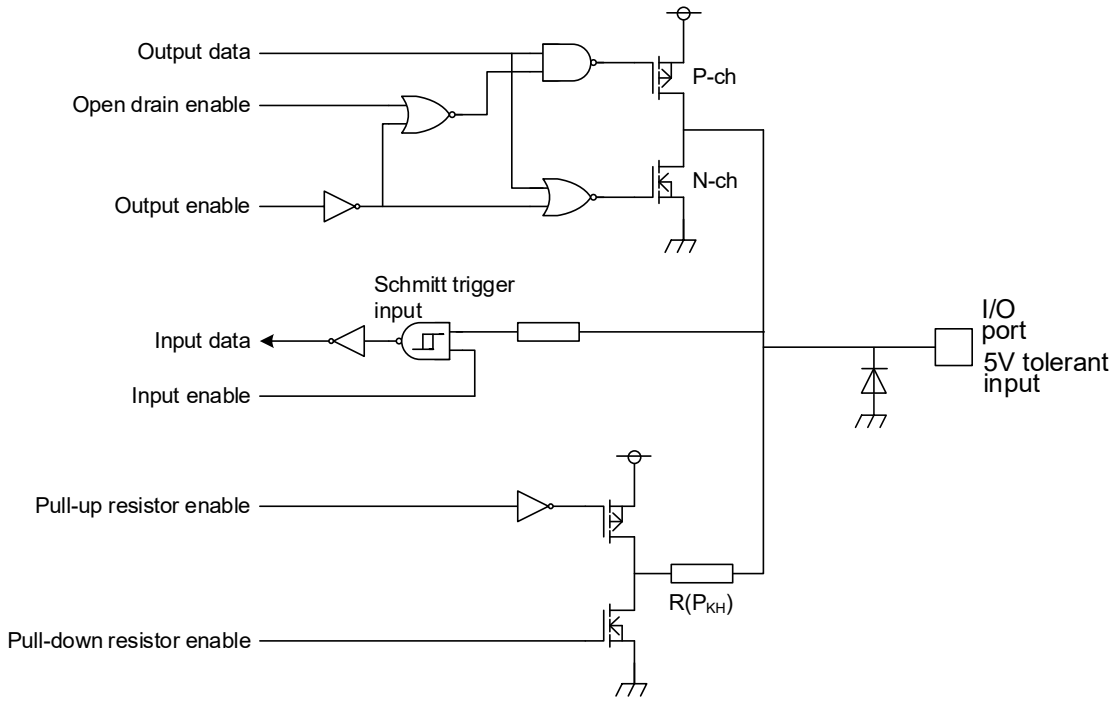
Note: The resistor without the symbol in the figure shows input protection resistor.

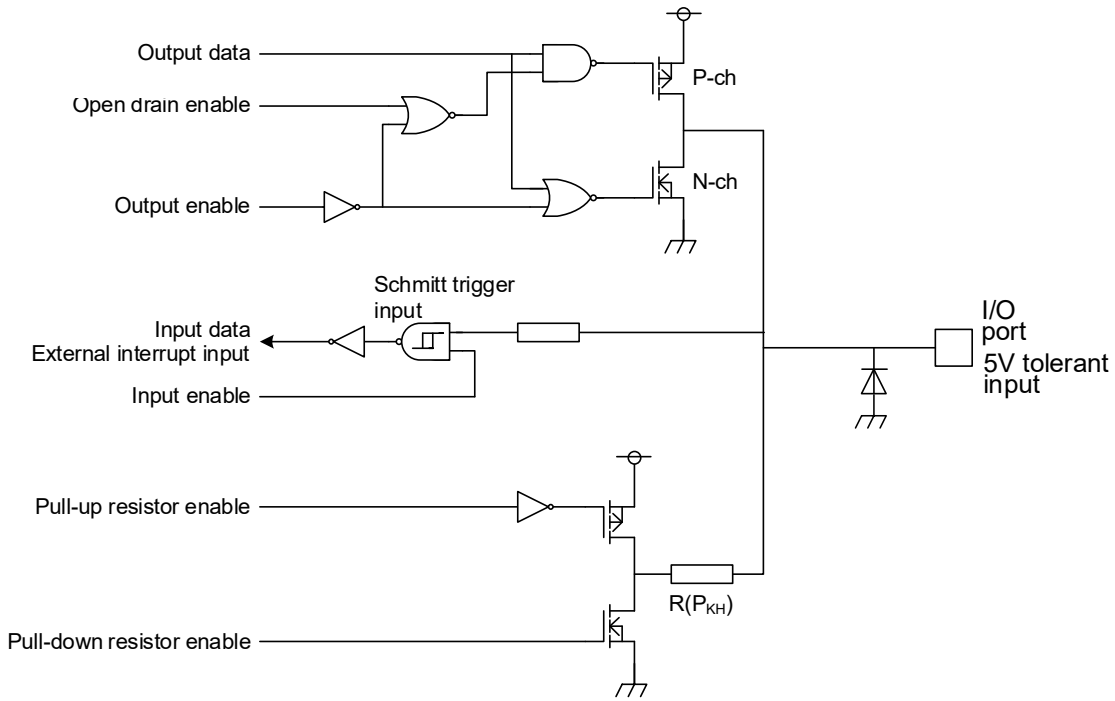
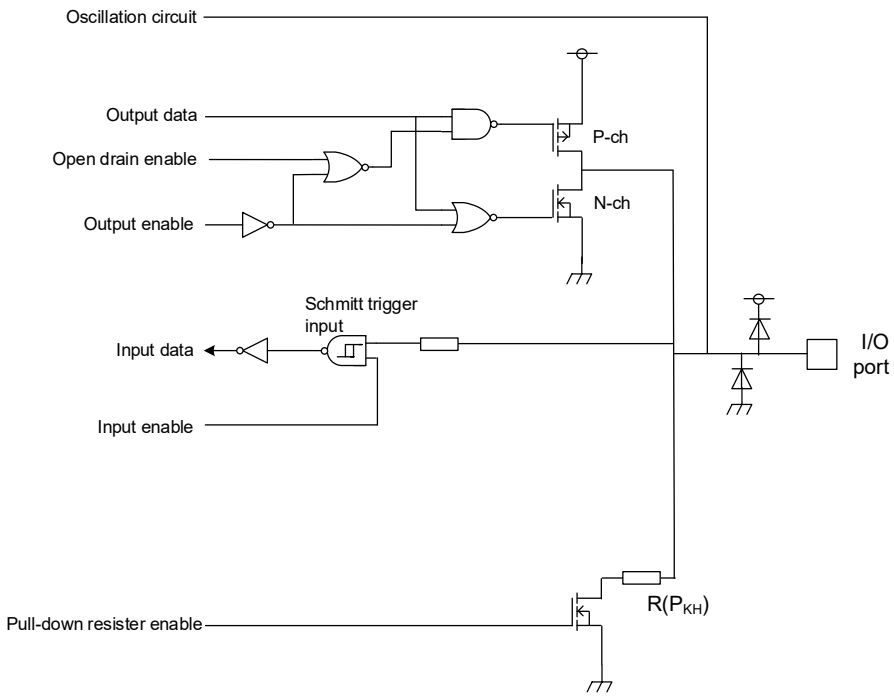
5.1. Port

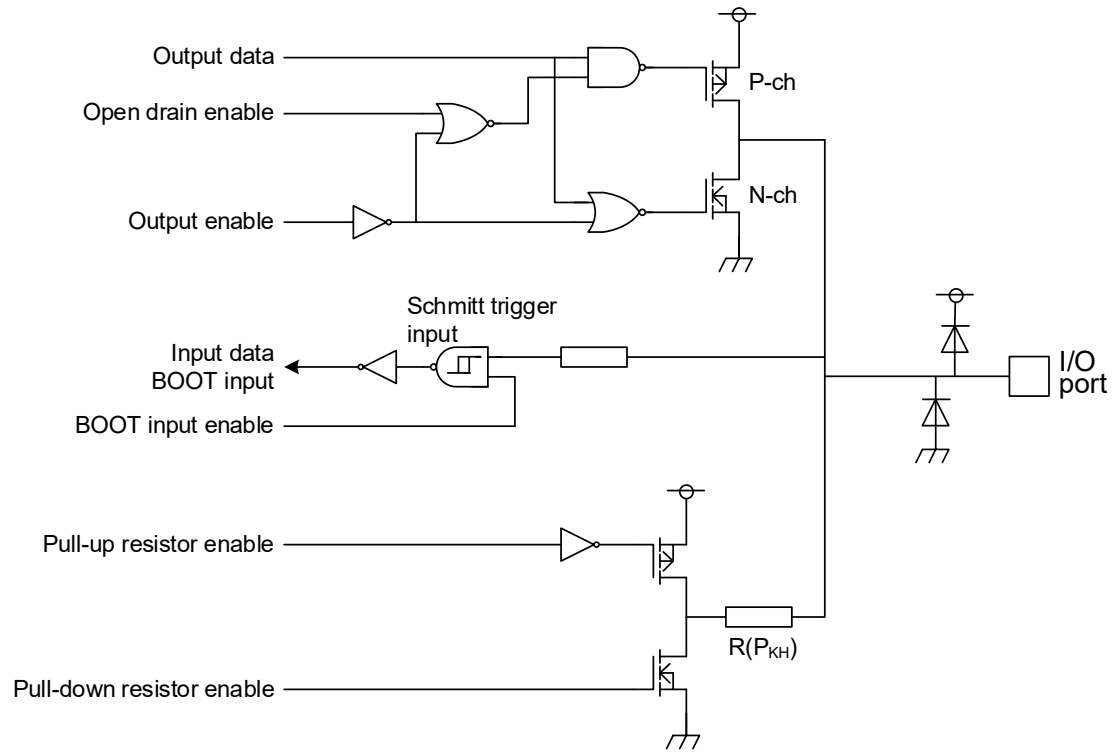
PE0 to PE7 PF0 to PF2	Programmable pull-up or/and pull-down resistor supported, programable open-drain output supported, analog input supported, and schmitt trigger input



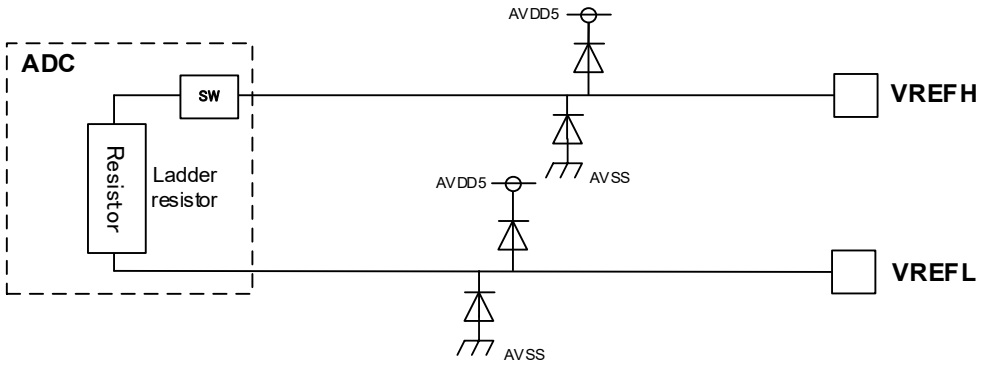
PF3 to PF5	Programmable pull-up or/and pull-down resistor supported, programable open-drain output supported, analog input supported, external interrupt input, and schmitt trigger input 
PA1, PA2, PB0 to PB6, PC0 to PC3, PD1	Programmable pull-up or/and pull-down resistor supported, programable open-drain output supported, and schmitt trigger input  Drive capability can be selected for PA1, PA2, PC0 to PC3, and PD1.

PA0, PA7, PB7, PC4, PC5, PD0, PD2, PD3, PG1 to PG3, PJ0 to PJ2	Programmable pull-up or/and pull-down resistor supported, programable open-drain output supported, external interrupt input, and schmitt trigger input  Drive capability can be selected for PA0, PB7, PC4, PC5, PD0, PD2, PD3, PG1 to PG3, and PJ0.
PA3, PA5 PD4, PD5	5V tolerant input supported, programmable pull-up or/and pull-down resistor supported, programable open-drain output supported, and schmitt trigger input 

PA4, PA6	5V tolerant input supported, programmable pull-up or/and pull-down resistor supported, programable open-drain output supported, external interrupt input, and schmitt trigger input 
PH0, PH1	Programmable pull-down resistor supported, oscillation circuit, and schmitt trigger input 

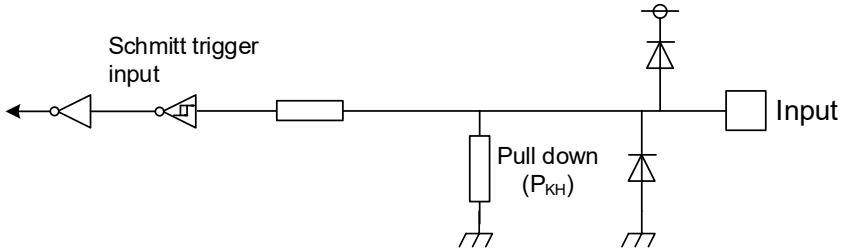
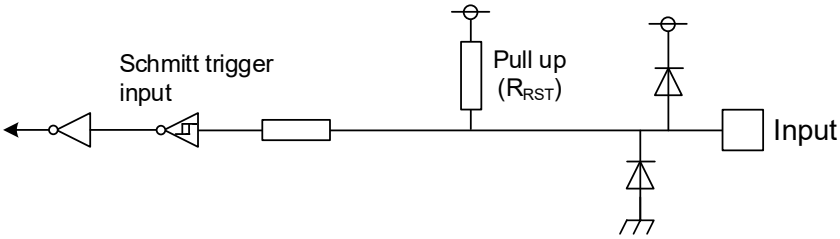
PG0/BOOT_N	Programmable pull-up or/and pull-down resistor supported, programable open-drain output supported, and schmitt trigger input  Drive capability can be selected for PG0.

5.2. Power Supply Pin for Analog

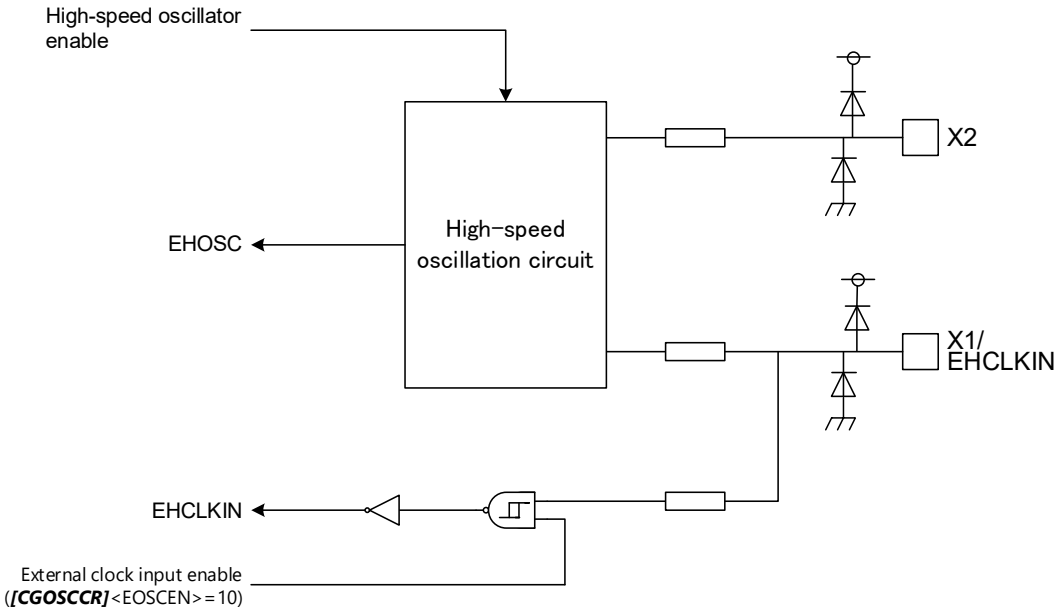
VREFH VREFL	

Note: SW: ON/OFF Switch Circuit

5.3. Control Pins

MODE	Mode Pin must be connected to GND. 
RESET_N	

5.4. Clock Control Pins

X1, X2	

6. Electrical Characteristics

DVDD5 is a generic name for DVDD5A and DVDD5B.
DVSS is a generic name for DVSSA, DVSSB, DVSSC and DVSSD.

6.1. Absolute Maximum Ratings

Table 6.1 Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Power supply voltage		DVDD5	-0.3 to 6.0	V
		AVDD5	-0.3 to 6.0	
Input voltage	PA0 to PA2, PA7, PB0 to PB7, PC0 to PC5, PD0 to PD3, PG1 to PG3, PH0, PH1, PJ0 to PJ2, MODE, RESET_N, BOOT_N	V_{IN1}	-0.3 to DVDD5+0.3 (≤6.0V) (Note2)	
	PE0 to PE7, PF0 to PF5	V_{IN2}	-0.3 to AVDD5+0.3 (≤6.0V) (Note2)	
	PA3 to PA6, PD4, PD5	V_{IN3}	-0.3 to 6.0	
Low level output current	Per pin PA0 to PA2, PA7, PB0 to PB7, PC0 to PC5, PD0 to PD3, PE0 to PE7, PF0 to PF5, PG0 to PG3, PH0, PH1, PJ0 to PJ2	I_{OL1}	5	mA
	Per pin PA3 to PA6, PD4, PD5	I_{OL2}	12	
	Total of all pins	ΣI_{OL}	50	
High level output current	Per pin PA0 to PA2, PA7, PB0 to PB7, PC0 to PC5, PD0 to PD3, PE0 to PE7, PF0 to PF5, PG0 to PG3, PH0, PH1, PJ0 to PJ2	I_{OH1}	-5	
	Per pin PA3 to PA6, PD4, PD5	I_{OH2}	-5	
	Total of all pins	ΣI_{OH}	-50	
Soldering temperature		T_{SOLDER}	260	°C
Storage temperature		T_{STG}	-55 to 125	
Operating temperature		T_{OPR}	-40 to 105	
Junction temperature (Note3)		Tj	-40 to 125	

Note1: Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions. The equipment manufacturer should design so that no Absolute maximum rating value is exceeded with respect to current, voltage, power consumption, temperature, etc. Exposure to conditions beyond those listed above may cause permanent damage to the device or affect device reliability, which could increase potential risks of personal injury due to IC blow up and/or burning.

Note2: Apply the same voltage to DVDD5 and AVDD5 from power-on to power-off.

Note3: The calculation formula for the maximum junction temperature (Tj) is shown below.

$Tj\ (Max) = T_{OPR}\ (Max) + PD\ (Max) \times \theta ja$

Refer to Table 6.2 for θja (thermal resistance of the package (°C/W)).
The calculation formula for maximum power dissipation (PD (Max)) is shown below.

$PD\ (Max) = V_{DD} \times I_{DD}\ (Max) + \Sigma\ (I_{OL} \times V_{OL}) + \Sigma\ ((V_{DD} - V_{OH}) \times I_{OH})$

I_{OL}: "Low" level output current
I_{OH}: "High" level output current
V_{OL}: "Low" level output voltage
V_{OH}: "High" level output voltage

I_{DD} (Max) is the current consumed by internal circuits excluding port. Refer to "6.3. DC Electrical Characteristics (2/2)".
Table 6.3 shows the current consumption per channel or unit for certain functions. These values are specified by design. Use these values as a reference for current consumption considerations.

Table 6.2 Thermal Resistance of Package

Parameter	Symbol	Package	Board condition	Value	Unit
Thermal resistance of package	θja	P-LQFP64-1010-0.50-003	JESD51-2, JESD51-3 compliant (1s)	55.2	°C/W
			JESD51-2, JESD51-7 compliant (2s-2p)	34.3	
		P-LQFP48-0707-0.50-002	JESD51-2, JESD51-3 compliant (1s)	61.0	
			JESD51-2, JESD51-7 compliant (2s-2p)	38.3	
		P-VQFN48-0707-0.50-006	JESD51-2, JESD51-5, JESD51-3 compliant (1s)	67.2	
			JESD51-2, JESD51-5, JESD51-7 compliant (2s-2p)	26.8	
		P-LQFP44-1010-0.80-003	JESD51-2, JESD51-3 compliant (1s)	57.7	
			JESD51-2, JESD51-7 compliant (2s-2p)	38.1	

Table 6.3 Current Consumption Per Channel/Unit

Ta = -40 to 105°C

Parameter	Condition	Min	Typ.	Max	Unit
ADC	3.6V < DVDD5 = AVDD5 ≤ 5.5V fsys = ADCLK = 80MHz, SCLK = 40MHz	-	-	3.8	mA
	2.7V ≤ DVDD5 = AVDD5 ≤ 3.6V fsys = ADCLK = 80MHz, SCLK = 40MHz	-	-	3.7	
VE	2.7V ≤ DVDD5 = AVDD5 ≤ 5.5V fsys = ΦT0 = 80MHz	-	-	0.9	
ENC		-	-	0.6	
SMIF		-	-	1.2	
TSPI		-	-	0.7	
UART		-	-	0.5	
T32A		-	-	0.8	

6.2. DC Electrical Characteristics (1/2)

3.6V < DVDD5 = AVDD5 ≤ 5.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Power supply voltage	DVDD5, AVDD5	VDD	f_{OSC} = 6 to 24MHz fsys = 1 to 80MHz	3.6	-	5.5	V
Low level Input voltage	PA0 to PA2, PA7, PB0 to PB7, PC0 to PC5, PD0 to PD3, PG1 to PG3, PH0, PH1, PJ0 to PJ2, MODE, RESET_N, BOOT_N	V_{IL1}	-	-0.3	-	DVDD5×0.25	V
	PE0 to PE7, PF0 to PF5	V_{IL2}				AVDD5×0.25	
	PA3 to PA6, PD4, PD5	V_{IL3}				DVDD5×0.25	
High level Input voltage	PA0 to PA2, PA7, PB0 to PB7, PC0 to PC5, PD0 to PD3, PG1 to PG3, PH0, PH1, PJ0 to PJ2, MODE, RESET_N, BOOT_N	V_{IH1}	-	DVDD5×0.75	-	DVDD5+0.3	V
	PE0 to PE7, PF0 to PF5	V_{IH2}		AVDD5×0.75		AVDD5+0.3	
	PA3 to PA6, PD4, PD5	V_{IH3}		DVDD5×0.75		5.8	
Low level output voltage	PA0 to PA2, PB7, PC0 to PC5, PD0 to PD3, PG0 to PG3, PJ0	V_{OL1}	1mA setting DVDD5 = 4.5V I_{OL} = 0.8mA	-	-	0.4	V
		V_{OL2}	2mA setting DVDD5 = 4.5V I_{OL} = 1.6mA	-	-	0.4	
		V_{OL3}	3mA setting DVDD5 = 4.5V I_{OL} = 2.4mA	-	-	0.4	
		V_{OL4}	4mA setting DVDD5 = 4.5V I_{OL} = 3.2mA	-	-	0.4	
	PA7, PB0 to PB6, PH0, PH1, PJ1, PJ2	V_{OL5}	DVDD5 = 4.5V I_{OL} = 1.6mA	-	-	0.4	
	PE0 to PE7, PF0 to PF5	V_{OL6}	AVDD5 = 4.5V I_{OL} = 1.6mA	-	-	0.4	
	PA3 to PA6, PD4, PD5	V_{OL7}	AVDD5 = 4.5V I_{OL} = 8mA	-	-	1.0	
High level output voltage	PA0 to PA2, PB7, PC0 to PC5, PD0 to PD3, PG0 to PG3, PJ0	V_{OH1}	1mA setting DVDD5 = 4.5V I_{OH} = -0.7mA	DVDD5-0.4	-	-	V
		V_{OH2}	2mA setting DVDD5 = 4.5V I_{OH} = -1.5mA	DVDD5-0.4	-	-	
		V_{OH3}	3mA setting DVDD5 = 4.5V I_{OH} = -2.4mA	DVDD5-0.4	-	-	
		V_{OH4}	4mA setting DVDD5 = 4.5V I_{OH} = -3.2mA	DVDD5-0.4	-	-	
	PA3 to PA7, PB0 to PB6, PD4, PD5, PH0, PH1, PJ1, PJ2	V_{OH5}	DVDD5 = 4.5V I_{OH} = -1.5mA	DVDD5-0.4	-	-	
	PE0 to PE7, PF0 to PF5	V_{OH6}	AVDD5 = 4.5V I_{OH} = -1.5mA	AVDD5-0.4	-	-	

Note: Apply same voltage to DVDD5 and AVDD5.

3.6V < DVDD5 = AVDD5 ≤ 5.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Leak current		I_{LI}	0.0V ≤ VIN ≤ DVDD5 0.0V ≤ VIN ≤ AVDD5	-5	±0.05	5	μA
Schmitt trigger Input width		V_{TH}	DVDD5 = AVDD5 = 5.0V	0.3	0.6	-	V
Reset pull-up resistor		R_{RST}	-	30	50	150	kΩ
Programmable pull-up/pull-down resistor		P_{KH}	Pull-up	30	50	150	
			Pull-down	30	50	150	
Pin capacity (except power supply pin)		C_{IO}	fc = 1MHz	-	-	10	pF
Low level output current	Per pin PA0 to PA2, PA7, PB0 to PB7, PC0 to PC5, PD0 to PD3, PE0 to PE7, PF0 to PF5, PG0 to PG3, PH0, PH1, PJ0 to PJ2	I_{OL1}	DVDD5 = AVDD5 = 5.0V	-	-	2 (Note3)	mA
	Per pin PA3 to PA6, PD4, PD5	I_{OL2}	DVDD5 = 5.0V	-	-	8 (Note3)	
	Total of PA0 to PA7, PB0 to PB7, PC0 to PC5, PD0 to PD5, PG0 to PG3, PH0, PH1, PJ0 to PJ2	ΣI_{OL1}	DVDD5 = 5.0V	-	-	35 (Note4)	
	Total of PE0 to PE7, PF0 to PF5	ΣI_{OL2}	AVDD5 = 5.0V	-	-	35 (Note4)	
High level output current	Per pin	I_{OH}	DVDD5 = AVDD5 = 5.0V	-2 (Note3)	-	-	mA
	Total of PA0 to PA7, PB0 to PB7, PC0 to PC5, PD0 to PD5, PG0 to PG3, PH0, PH1, PJ0 to PJ2	ΣI_{OH1}	DVDD5 = 5.0V	-35 (Note4)	-	-	
	Total of PE0 to PE7, PF0 to PF5	ΣI_{OH2}	AVDD5 = 5.0V	-35 (Note4)	-	-	

Note1: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5.0V, unless otherwise noted.

Note2: Apply same voltage toDVDD5 and AVDD5.

Note3: The sum of the pin currents in each group should not exceed the total current of each group.

Note4: The sum of each group current should not exceed the absolute maximum rating.

2.7V < DVDD5 = AVDD5 ≤ 3.6V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Power supply voltage	DVDD5, AVDD5	VDD	f_{OSC} = 6 to 24MHz fsys = 1 to 80MHz	2.7	-	3.6	V
Low level Input voltage	PA0 to PA2, PA7, PB0 to PB7, PC0 to PC5, PD0 to PD3, PG1 to PG3, PH0, PH1, PJ0 to PJ2, MODE, RESET_N, BOOT_N	V_{IL1}	-	-0.3	-	DVDD5×0.25	V
	PE0 to PE7, PF0 to PF5	V_{IL2}	-			AVDD5×0.25	
	PA3 to PA6, PD4, PD5	V_{IL3}	-			DVDD5×0.25	
High level Input voltage	PA0 to PA2, PA7, PB0 to PB7, PC0 to PC5, PD0 to PD3, PG1 to PG3, PH0, PH1, PJ0 to PJ2, MODE, RESET_N, BOOT_N	V_{IH1}	-	DVDD5×0.75	-	DVDD5+0.3	V
	PE0 to PE7, PF0 to PF5	V_{IH2}	-	AVDD5×0.75		AVDD5+0.3	
	PA3 to PA6, PD4, PD5	V_{IH3}	-	DVDD5×0.75		5.8	
Low level output voltage	PA0 to PA2, PB7, PC0 to PC5, PD0 to PD3, PG0 to PG3, PJ0	V_{OL1}	1mA setting DVDD5 = 2.7V I_{OL} = 0.4 mA	-	-	0.4	V
		V_{OL2}	2mA setting DVDD5 = 2.7V I_{OL} = 0.9 mA	-	-	0.4	
		V_{OL3}	3mA setting DVDD5 = 2.7V I_{OL} = 1.5 mA	-	-	0.4	
		V_{OL4}	4mA setting DVDD5 = 2.7V I_{OL} = 2.1 mA	-	-	0.4	
	PA7, PB0 to PB6, PH0, PH1, PJ1, PJ2	V_{OL5}	DVDD5 = 2.7V I_{OL} = 0.9 mA	-	-	0.4	
	PE0 to PE7, PF0 to PF5	V_{OL6}	AVDD5 = 2.7V I_{OL} = 0.9 mA	-	-	0.4	
	PA3 to PA6, PD4, PD5	V_{OL7}	DVDD5 = 2.7V I_{OL} = 5.5 mA	-	-	1.0	
High level output voltage	PA0 to PA2, PB7, PC0 to PC5, PD0 to PD3, PG0 to PG3, PJ0	V_{OH1}	1mA setting DVDD5 = 2.7V I_{OH} = -0.4 mA	DVDD5-0.4	-	-	V
		V_{OH2}	2mA setting DVDD5 = 2.7V I_{OH} = -0.9 mA	DVDD5-0.4	-	-	
		V_{OH3}	3mA setting DVDD5 = 2.7V I_{OH} = -1.5 mA	DVDD5-0.4	-	-	
		V_{OH4}	4mA setting DVDD5 = 2.7V I_{OH} = -2.1 mA	DVDD5-0.4	-	-	
	PA3 to PA7, PB0 to PB6, PD4, PD5, PH0, PH1, PJ1, PJ2	V_{OH5}	DVDD5 = 2.7V I_{OH} = -0.9 mA	DVDD5-0.4	-	-	
	PE0 to PE7, PF0 to PF5	V_{OH6}	DVDD5 = 2.7V I_{OH} = -0.9 mA	DVDD5-0.4	-	-	

Note: Apply same voltage toDVDD5 and AVDD5.

2.7V < DVDD5 = AVDD5 ≤ 3.6V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Leak current		I_{LI}	0.0V ≤ VIN ≤ DVDD5 0.0V ≤ VIN ≤ AVDD5	-5	±0.05	5	μA
Schmitt trigger Input width		V_{TH}	DVDD5 = AVDD5 = 3.0V	0.2	0.4	-	V
Reset pull-up resistor		R_{RST}	-	30	50	150	kΩ
Programmable pull-up/pull-down resistor		P_{KH}	Pull-up	30	50	150	
			Pull-down	30	50	150	
Pin capacity (except power supply pin)		C_{IO}	fc = 1MHz	-	-	10	pF
Low level output current	Per pin PA0 to PA2, PA7, PB0 to PB7, PC0 to PC5, PD0 to PD3, PE0 to PE7, PF0 to PF5, PG0 to PG3, PH0, PH1, PJ0 to PJ2	I_{OL1}	DVDD5 = AVDD5 = 3.3V	-	-	2 (Note3)	mA
	Per pin PA3 to PA6, PD4, PD5	I_{OL2}	DVDD5 = 3.3V	-	-	8 (Note3)	
	Total of PA0 to PA7, PB0 to PB7, PC0 to PC5, PD0 to PD5, PG0 to PG3, PH0, PH1, PJ0 to PJ2	ΣI_{OL1}	DVDD5 = 3.3V	-	-	35 (Note4)	
	Total of PE0 to PE7, PF0 to PF5	ΣI_{OL2}	AVDD5 = 3.3V	-	-	35 (Note4)	
High level output current	Per pin	I_{OH}	DVDD5 = AVDD5 = 3.3V	-2 (Note3)	-	-	mA
	Total of PA0 to PA7, PB0 to PB7, PC0 to PC5, PD0 to PD5, PG0 to PG3, PH0, PH1, PJ0 to PJ2	ΣI_{OH1}	DVDD5 = 3.3V	-35 (Note4)	-	-	
	Total of PE0 to PE7, PF0 to PF5	ΣI_{OH2}	AVDD5 = 3.3V	-35 (Note4)	-	-	

Note1: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 3.3V, unless otherwise noted.
Note2: Apply same voltage toDVDD5 and AVDD5.
Note3: The sum of the pin currents in each group should not exceed the total current of each group.
Note4: The sum of each group current should not exceed the absolute maximum rating.

6.3. DC Electrical Characteristics (2/2)

Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
NORMAL mode	I_{DD}	Refer to the Table 6.4 and Table 6.5 for detail.	-	43.9	61.6	mA
IDLE mode			-	5.1	16.0	
STOP1 mode			-	0.51	9.38	
STOP2 mode			-	2.4	60.8	μA

Note1: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5.0V, unless otherwise noted.

Note2: Apply same voltage to DVDD5 and AVDD5.

Note3: Current consumption includes AVDD5 and VREF current.

Table 6.4 IDD Measurement Condition (Pin Setting and Oscillation Circuit)

		NORMAL mode	IDLE mode	STOP1 mode	STOP2 mode
Pin setting	DVDD5 and AVDD5	5.0V (Typ.), 5.5V (max)			
	X1 and X2 pins	External high-speed oscillator connected (10MHz)			
	Input pins	Fixed			
	Output pins	Opened			
Operation condition (Oscillation circuit)	System clock (fsys)	80MHz		Stopped	
	External high-speed oscillator (EHOSC)	Oscillation		Stopped	
	Internal high-speed oscillator 1 (IHOSC1)	stopped			
	PLL	Operated		Stopped	

Table 6.5 IDD Measurement Condition (CPU and Peripheral Function)

Peripheral function	Number of built-in peripherals	NORMAL mode	IDLE mode	STOP1 mode	STOP2 mode
CPU	1	Operated (DhrystoneVer.2.1)	Stopped		
DMAC	1	Operated (Request from UART ch0 TX destination: RAM)	Stopped		
ADC	2	All units operated (Conversion time: 1.0μs, Repeated conversion)	Stopped		
DAC	2	All channels operated	Stopped		
RAMP	1	Operated	Stopped		
T32A	5	All channels operated	Stopped		
A-PMD2	1	Operated	Stopped		
A-ENC2	1	Operated	Stopped		
A-VE2	1	Operated	Stopped		
SIWDT	1	Operated	Stopped		
UART	6	6 channels operated, transmission (transfer speed: 5Mbps)	Stopped		
EI2C	2	Stopped			
TSPI	3	3 channels operated, transmission (transfer speed 20MHz)	Stopped		
SMIF	1	1 channel operated, transmission (transfer speed 25MHz)	Stopped		
CRC	1	Stopped			
LVD	1	Stopped			
OFD	1	Stopped			
DEBUG	1	Stopped			
PORT	-	Operated	Stopped		

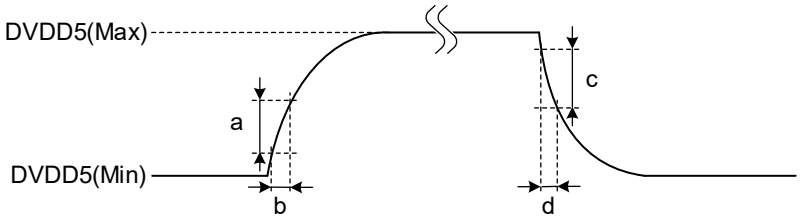
Ta= -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog power consumption (Includes VREF current)	I_{AVDD}	AVDD5 = 5.0V (Typ.) 5.5V(Max), AVSS = 0V ADC. DAC and COMP operated	-	5.8	8.5	mA

6.4. Power Supply Voltage Fluctuation

DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Power gradient	V_{PON}	Rising slope at power-on	0.3	-	250	mV/μs
	V_{POFF1}	Falling slope at power-off (2.7V ≤ DVDD5)	-	-	50	
	V_{POFF2}	Falling slope at power-off (0V ≤ DVDD5 < 2.7V)	-	-	2.5	
Power supply fluctuation rate	V_{fr}	2.7V ≤ DVDD5 = AVDD5 ≤ 5.5V	-50	-	50	



Vfr = a / b, c / d

Figure 6.1 Power Supply Fluctuation Rate

6.5. Characteristics of Internal Processing at RESET

DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Internal initialized time	t_{IINIT}	Power On	-	-	2.57	ms
Internal processing time for reset	t_{IRST}	When STOP2 mode is released by reset (RESET_N pin, LVD).	-	-	1.16	
		When STOP2 mode is released by interrupt.	-	-	0.54	
		When reset operation other than releasing STOP2 mode is performed.	-	-	0.18	
Waiting time till CPU operation (Note)	t_{CPUWT}	Power-on Reset operation by LVD in STOP1 or STOP2 mode Reset operation by RESET_N pin in STOP1 or STOP2 mode	12	-	15	μs
		Reset operation by LVD in NORMAL or IDLE mode Reset operation by RESET_N pin in NORMAL or IDLE mode Reset operation by SIWDT, OFD, LOCKUP, or SYSRESET in NORMAL or IDLE mode	55	-	59	

Note: Except reset operation by SIWDT, OFD, LOCKUP, or SYSRESET, when reset factor repeats, t_{CPUWT} (Waiting time till CPU running) starts measuring elapse time after releasing this factor.

6.6. Characteristics of Power-on Reset

DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Release voltage	V_{PREL}	Power increases	2.22	2.33	2.44	V
Detection voltage	V_{PDET}	Power decreases	2.17	2.28	2.39	
Detection pulse width 1	T_{PDET1}	-	200	-	-	μs

6.7. Characteristics of PORF

DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Release voltage	V_{PORFL}	Power increases	2.57	2.64	2.71	V
Detection voltage	V_{PORFD}	Power decreases	2.52	2.59	2.66	
Detection pulse width 2	T_{PDET2}	-	200	-	-	μs

6.8. Characteristics of Voltage Detection Circuit

DVDD5 = AVDD5 = 2.7 to 5.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage in NORMAL/IDLE/STOP1 mode	V_{LVL0}	Power up	2.64	2.70	2.76	V
		Power down	2.59	2.65	2.71	
	V_{LVL1}	Power up	2.69	2.75	2.81	V
		Power down	2.64	2.70	2.76	
	V_{LVL2}	Power up	2.79	2.85	2.91	V
		Power down	2.74	2.80	2.86	
	V_{LVL3}	Power up	2.89	2.95	3.01	V
		Power down	2.84	2.90	2.96	
	V_{LVL4}	Power up	3.97	4.05	4.13	V
		Power down	3.92	4.00	4.08	
	V_{LVL5}	Power up	4.17	4.25	4.33	V
		Power down	4.12	4.20	4.28	
	V_{LVL6}	Power up	4.37	4.45	4.53	V
		Power down	4.32	4.40	4.48	
	V_{LVL7}	Power up	4.57	4.65	4.73	V
		Power down	4.52	4.60	4.68	
Detection voltage in STOP2 mode	V_{LVL0}	Power up	2.62	2.70	2.78	V
		Power down	2.57	2.65	2.73	
	V_{LVL1}	Power up	2.67	2.75	2.83	V
		Power down	2.62	2.70	2.78	
	V_{LVL2}	Power up	2.77	2.85	2.93	V
		Power down	2.72	2.80	2.88	
	V_{LVL3}	Power up	2.87	2.95	3.03	V
		Power down	2.82	2.90	2.98	
	V_{LVL4}	Power up	3.95	4.05	4.15	V
		Power down	3.90	4.00	4.10	
	V_{LVL5}	Power up	4.15	4.25	4.35	V
		Power down	4.10	4.20	4.30	
	V_{LVL6}	Power up	4.35	4.45	4.55	V
		Power down	4.30	4.40	4.50	
	V_{LVL7}	Power up	4.55	4.65	4.75	V
		Power down	4.50	4.60	4.70	
Detection response time	t_{VDDT1}	Power down	-	-	100	μs
Release response time	t_{VDDT2}	Power up	-	-	100	
Setup time	t_{LVDEN}	-	-	-	100	
Detection Minimum pulse width	t_{LVDPW}	-	200	-	-	

6.9. 12-bit AD Converter Characteristics

6.9.1. AD Converter Characteristics

DVDD5 = AVDD5 = 2.7 to 5.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog reference voltage (+)	VREFH	-	2.7	-	5.5	V
Analog input voltage	VAIN	-	VREFL	-	VREFH	
Difference between analog power supply and reference voltage	ΔVREF	VREFH ≤ AVDD5	0	-	0.5	
Integral nonlinear error (INL)	-	1 unit operation 3.6V < AVDD5 ≤ 5.5V 3.6V < VREFH ≤ 5.5V AVSS = VREFL = 0V AIN load resistor = 600 Ω AIN load capacity ≥ 0.1μF	-5	-	5	LSB
Differential nonlinear error (DNL)			-1	-	2	
Zero-scale error			-5	-	5	
Full-scale error			-5	-	5	
Total errors			-7	-	5	
Integral nonlinear error (INL)	-	1 unit operation 2.7V ≤ AVDD5 ≤ 3.6V 2.7V ≤ VREFH ≤ 3.6V AVSS = VREFL = 0V AIN load resistor = 600 Ω AIN load capacity ≥ 0.1μF	-5	-	5	LSB
Differential nonlinear error (DNL)			-1	-	2	
Zero-scale error			-5	-	5	
Full-scale error			-5	-	5	
Total errors			-7	-	6	
Integral nonlinear error (INL)	-	2 units operation (Simultaneous conversion start) 3.6V < AVDD5 ≤ 5.5V 3.6V < VREFH ≤ 5.5V AVSS = VREFL = 0V AIN load resistor = 600 Ω AIN load capacity ≥ 0.1μF	-5.5	-	5.5	LSB
Differential nonlinear error (DNL)			-1	-	2.5	
Zero-scale error			-5.5	-	5.5	
Full-scale error			-6.5	-	6.5	
Total errors			-7.5	-	6.5	
Integral nonlinear error (INL)	-	2 units operation (Simultaneous conversion start) 2.7V ≤ AVDD5 ≤ 3.6V 2.7V ≤ VREFH ≤ 3.6V AVSS = VREFL = 0V AIN load resistor = 600 Ω AIN load capacity ≥ 0.1μF	-5.5	-	5.5	LSB
Differential nonlinear error (DNL)			-1	-	3	
Zero-scale error			-5.5	-	5.5	
Full-scale error			-6.5	-	6.5	
Total errors			-7.5	-	7.5	
Integral nonlinear error (INL)	-	2 units operation (Conversion start at 0.5μs difference) 3.6V < AVDD5 ≤ 5.5V 3.6V < VREFH ≤ 5.5V AVSS = VREFL = 0V AIN load resistor = 600 Ω AIN load capacity ≥ 0.1μF Conversion time = 0.975μs	-5.5	-	5.5	LSB
Differential nonlinear error (DNL)			-1	-	2.5	
Zero-scale error			-5.5	-	5.5	
Full-scale error			-6.5	-	6.5	
Total errors			-7.5	-	6.5	
Integral nonlinear error (INL)	-	2 units operation (Conversion start at 0.5μs difference) 2.7V ≤ AVDD5 ≤ 3.6V 2.7V ≤ VREFH ≤ 3.6V AVSS = VREFL = 0V AIN load resistor = 600 Ω AIN load capacity ≥ 0.1μF Conversion time = 0.975μs	-5.5	-	5.5	LSB
Differential nonlinear error (DNL)			-1	-	3	
Zero-scale error			-5.5	-	5.5	
Full-scale error			-6.5	-	6.5	
Total errors			-7.5	-	7.5	

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
SCLK frequency	f_{SCLK}	-	4	-	40	MHz
Sampling time	t_{smpl}	-	0.25	-	-	μs
Conversion time	t_{conv}	-	0.975	-	-	
Stable time	t_{sta}	After initializing or changing of registers	3	-	-	

Note1: Typ. value is in Ta = 25 °C, DVDD5 = AVDDA5 = 5.0V, unless otherwise noted.

Note2: 1LSB = (VREFH - AVSS (VREFL)) / 4096 [V]

Note3: The characteristic when single AD converter operates.

6.9.2. Reference Supply Voltage

DVDD5 = AVDD5 = 2.7 to 5.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Conditions	Min	Typ.	Max	Unit
Reference power	Unit A: ch16 selected Unit B: ch16 selected	1.35	-	1.65	V

6.10. 8-bit DA Converter Characteristics

DVDD5 = AVDD5 = 2.7 to 5.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog reference voltage (+)	VREFH	-	-	AVDD5	-	V
Integral nonlinearity error (INL)	-	-	-2	-	2	LSB
Differential nonlinearity error (DNL)			-1	-	1	
Zero scale error			-3	-	3	
Full scale error			-3	-	3	
Stable time	t_{sta}		5.6	-	-	μs

Note 1: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5.0V or Ta = 25 °C, DVDD5 = AVDD5 = 3.3V, unless otherwise noted.

Note 2: 1LSB = (AVDD5 (VREFH) - AVSS (VREFL)) / 256 [V]

Note 3: This is the characteristic in case only DA converter is operating.

6.11. Comparator Characteristics

DVDD5 = AVDD5 = 2.7 to 5.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
AIN input voltage range	VINC	-	VREFL	-	VREFH	V
Reference voltage range (Note 1)	VREFC		0.2	-	AVDD5-0.5	
Response time (Note 2)	-		-	-	0.5	μs
Comparator enable time	T_{sta}		-	-	5	

Note 1: Output of internal 8-bit DA converter (DAC0)

Note 2: In case of the VINC change from VREFC - 100mV to VREFC + 100mV, or from VREFC + 100mV to VREFC - 100mV.

Note 3: This is the characteristic in case only comparator is operation.

6.12. AC Electrical Characteristics

The values shown in the "AC Electrical Characteristics" of this chapter do not include clock errors.
In practice, the AC characteristics can be affected by both errors (a) and (b).

(a) Oscillation frequency error of the clock used as fosc
(b) PLL error (maximum ±3%)

6.12.1. Serial Peripheral Interface (TSPI)

6.12.1.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5 V
- Ta = -40 to 105°C
- Input/output level: High = 0.5 × DVDD5, Low = 0.5 × DVDD5
- Load capacity: CL = 30pF
- Output drive capability: 4mA setting

6.12.1.2. AC Electrical Characteristics

"T" indicates an operation clock cycle of the TSPI. This operation clock has the same cycle of the system clock (fsys). This cycle depends on the clock gear setting.

The value of "k1" is specified with ***[TSPIxFMTR0]***<CSSCKDL[3:0]>; the value of "k2" is specified with ***[TSPIxFMTR0]***<SCKCSDL[3:0]>. These values are 1 to 16. The value of k3 is the value specified with ***[TSPIxCR2]***<RXDLY[2:0]> plus 1. These values are 1 to 8.

(1) SPI mode controller

3.6V < DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Min	Max	Unit
TSPIxSCK output frequency	f_{CYC}	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	$1/f_{CYC}$	-	ns
TSPIxSCK low level output pulse width	t_{WL}	$(t_{CYC} / 2) - 13$	-	
TSPIxSCK high level output pulse width	t_{WH}	$(t_{CYC} / 2) - 13$	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	$(t_{CYC} \times k1) - 20$	$(t_{CYC} \times k1) + 9$	
TSPIxSCK rise/fall → TSPIxCSn hold time	t_{CHD}	$(t_{CYC} \times (k2 + 0.5)) - 20$	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	$37 - k3 \times T$	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	$k3 \times T – 1.5$	-	
TSPIxSCK rise/fall → TSPIxTXD hold time	t_{ODLY1}	-17	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	17	
TSPIxCSn fall → TSPIxTXD delay time	t_{ODLY3}	$(t_{CYC} \times (k1 - 0.5)) - 25$	$(t_{CYC} \times (k1 - 0.5)) + 9$	

2.7V ≤ DVDD5 = AVDD5 ≤ 3.6V

Parameter	Symbol	Min	Max	Unit
TSPIxSCK output frequency	f_{CYC}	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	$1/f_{CYC}$	-	ns
TSPIxSCK low level output pulse width	t_{WL}	$(t_{CYC} / 2) – 16$	-	
TSPIxSCK high level output pulse width	t_{WH}	$(t_{CYC} / 2) – 16$	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	$(t_{CYC} \times k1) - 20$	$(t_{CYC} \times k1) + 11$	
TSPIxSCK rise/fall → TSPIxCSn hold time	t_{CHD}	$(t_{CYC} \times (k2 + 0.5)) – 22.5$	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	$37 - k3 \times T$	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	$k3 \times T - 1.5$	-	
TSPIxSCK rise/fall → TSPIxTXD hold time	t_{ODLY1}	-17	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	17	
TSPIxCSn fall → TSPIxTXD delay time	t_{ODLY3}	$(t_{CYC} \times (k1 - 0.5)) - 25$	$(t_{CYC} \times (k1 - 0.5)) + 13$	

(2) SPI mode target

3.6V < DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Min	Max	Unit
TSPIxSCK Input frequency	f_{CYC}	-	10	MHz
TSPIxSCK Input cycle	t_{CYC}	1 / f_{CYC}	-	ns
TSPIxSCK low level Input pulse width	t_{WL}	37	-	
TSPIxSCK high level Input pulse width	t_{WH}	37	-	
TSPIxCSIN Input (1st) ← TSPIxSCK rise/fall time	t_{CSU1}	170	-	
TSPIxCSIN Input (2nd) ← TSPIxSCK rise/fall time	t_{CSU2}	80	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time (1st)	t_{CHD}	80	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time (2nd)	t_{CHD}	7	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	
TSPIxSCK rise/fall → TSPIxTXD hold time	t_{ODLY1}	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	43	
TSPIxCSIN fall → TSPIxTXD delay time	t_{ODLY3}	-	46	
TSPIxCSIN high level input pulse width (1st)	t_{WDIS}	T × 5 + 20	-	
TSPIxCSIN high level input pulse width (2nd)	t_{WDIS}	T × 2 + 20	-	

2.7V ≤ DVDD5 = AVDD5 ≤ 3.6V

Parameter	Symbol	Min	Max	Unit
TSPIxSCK Input frequency	f_{CYC}	-	10	MHz
TSPIxSCK Input cycle	t_{CYC}	1 / f_{CYC}	-	ns
TSPIxSCK low level Input pulse width	t_{WL}	37	-	
TSPIxSCK high level Input pulse width	t_{WH}	37	-	
TSPIxCSIN Input (1st) ← TSPIxSCK rise/fall time	t_{CSU1}	170	-	
TSPIxCSIN Input (2nd) ← TSPIxSCK rise/fall time	t_{CSU2}	80	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time (1st)	t_{CHD}	80	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time (2nd)	t_{CHD}	7	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	
TSPIxSCK rise/fall → TSPIxTXD hold time	t_{ODLY1}	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	43	
TSPIxCSIN fall → TSPIxTXD delay time	t_{ODLY3}	-	46	
TSPIxCSIN high level input pulse width (1st)	t_{WDIS}	T × 5 + 20	-	
TSPIxCSIN high level input pulse width (2nd)	t_{WDIS}	T × 2 + 20	-	

(3) SIO mode controller (TSPI0/1/2/3/4)

3.6V < DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Min	Max	Unit
TSPIxSCK output frequency	f_{CYC}	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	1 / f_{CYC}	-	ns
TSPIxSCK low-level output pulse width	t_{WL}	(t_{CYC} / 2) - 13	-	
TSPIxSCK high-level output pulse width	t_{WH}	(t_{CYC} / 2) - 13	-	
TSPIxRXD input ← TSPIxSCK rise/fall time	t_{DSU}	37 - k3 × T	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	k3 × T - 1.5	-	
TSPIxSCK rise/ fall → TSPIxTXD hold time	t_{ODLY1}	-17	-	
TSPIxSCK Rise/ fall → TSPIxTXD delay time	t_{ODLY2}	-	17	

2.7V ≤ DVDD5 = AVDD5 ≤ 3.6V

Parameter	Symbol	Min	Max	Unit
TSPIxSCK output frequency	f_{CYC}	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	1 / f_{CYC}	-	ns
TSPIxSCK low-level output pulse width	t_{WL}	(t_{CYC} / 2) - 16	-	
TSPIxSCK high-level output pulse width	t_{WH}	(t_{CYC} / 2) - 16	-	
TSPIxRXD input ← TSPIxSCK rise/fall time	t_{DSU}	37 - k3 × T	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	k3 × T - 1.5	-	
TSPIxSCK rise/ fall → TSPIxTXD hold time	t_{ODLY1}	-17	-	
TSPIxSCK Rise/ fall → TSPIxTXD delay time	t_{ODLY2}	-	17	

(4) SIO mode target (TSPI0/1/2/3/4)

3.6V < DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Min	Max	Unit
TSPIxSCK input frequency	f_{CYC}	-	10	MHz
TSPIxSCK input cycle	t_{CYC}	1 / f_{CYC}	-	ns
TSPIxSCK low-level input pulse width	t_{WL}	37	-	
TSPIxSCK high-level input pulse width	t_{WH}	37	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time	t_{CHD}	7	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	
TSPIxSCK rise/fall → TSPIxTXD hold time	t_{ODLY1}	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	43	

2.7V ≤ DVDD5 = AVDD5 ≤ 3.6V

Parameter	Symbol	Min	Max	Unit
TSPIxSCK input frequency	f_{CYC}	-	10	MHz
TSPIxSCK input cycle	t_{CYC}	1 / f_{CYC}	-	ns
TSPIxSCK low-level input pulse width	t_{WL}	37	-	
TSPIxSCK high-level input pulse width	t_{WH}	37	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time	t_{CHD}	7	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	
TSPIxSCK rise/fall → TSPIxTXD hold time	t_{ODLY1}	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	43	

(1) 1st clock edge sampling (Controller)

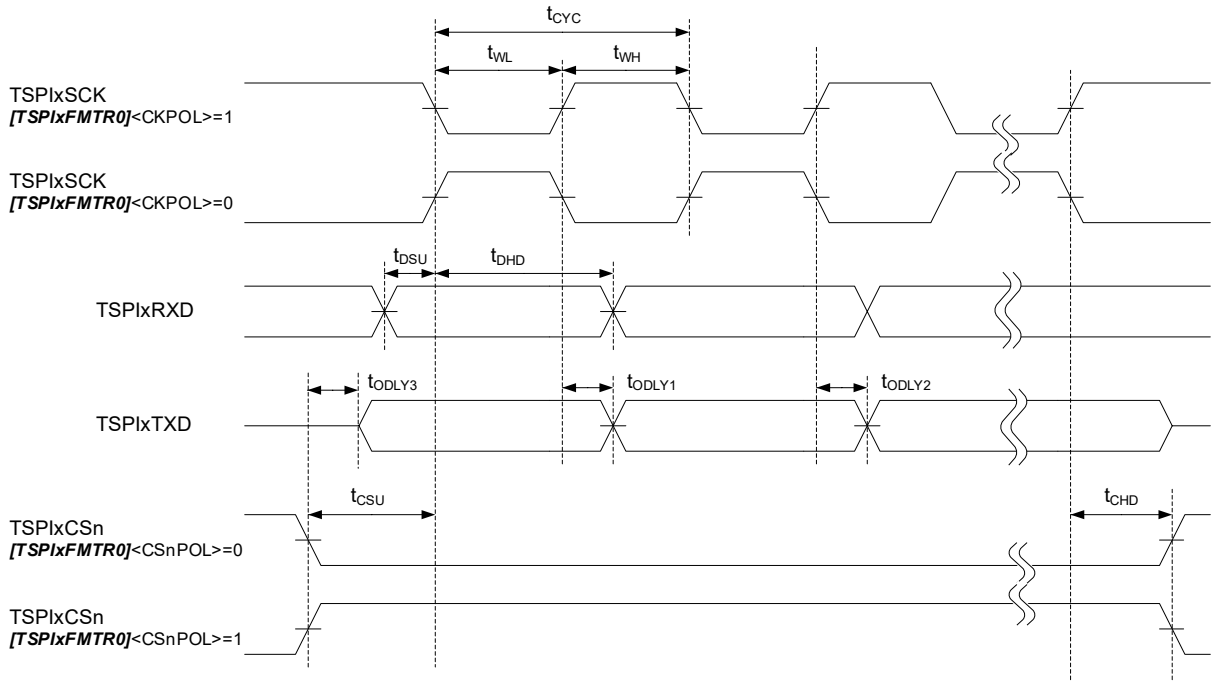


Figure 6.2 1st Clock Edge Sampling (Controller)

(2) 2nd clock edge sampling (Controller)

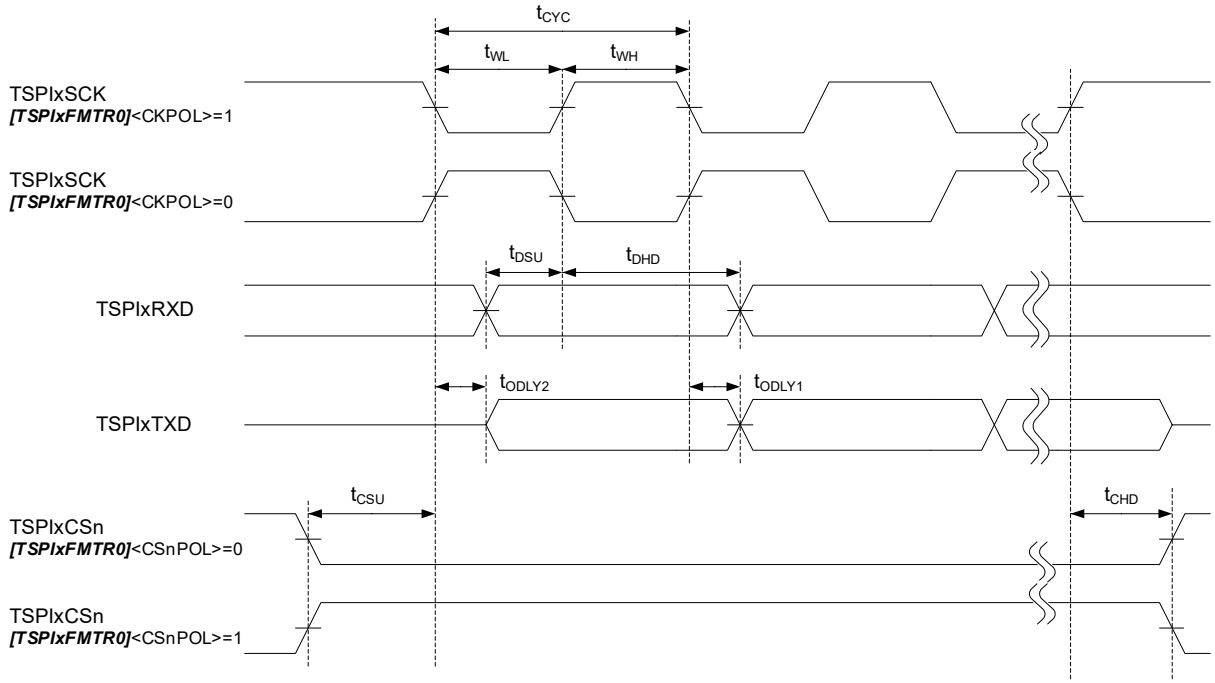


Figure 6.3 2nd Clock Edge Sampling (Controller)

(3) 1st clock edge sampling (Target)

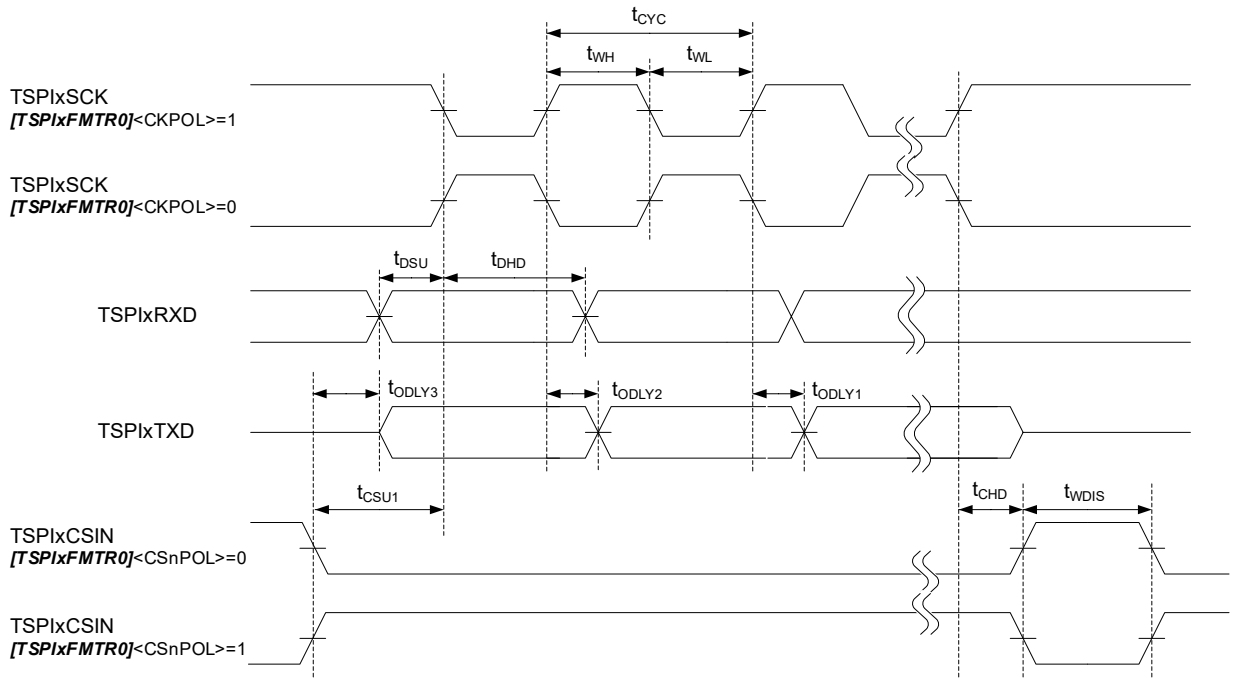


Figure 6.4 1st Clock Edge Sampling (Target)

(4) 2nd clock edge sampling (Target)

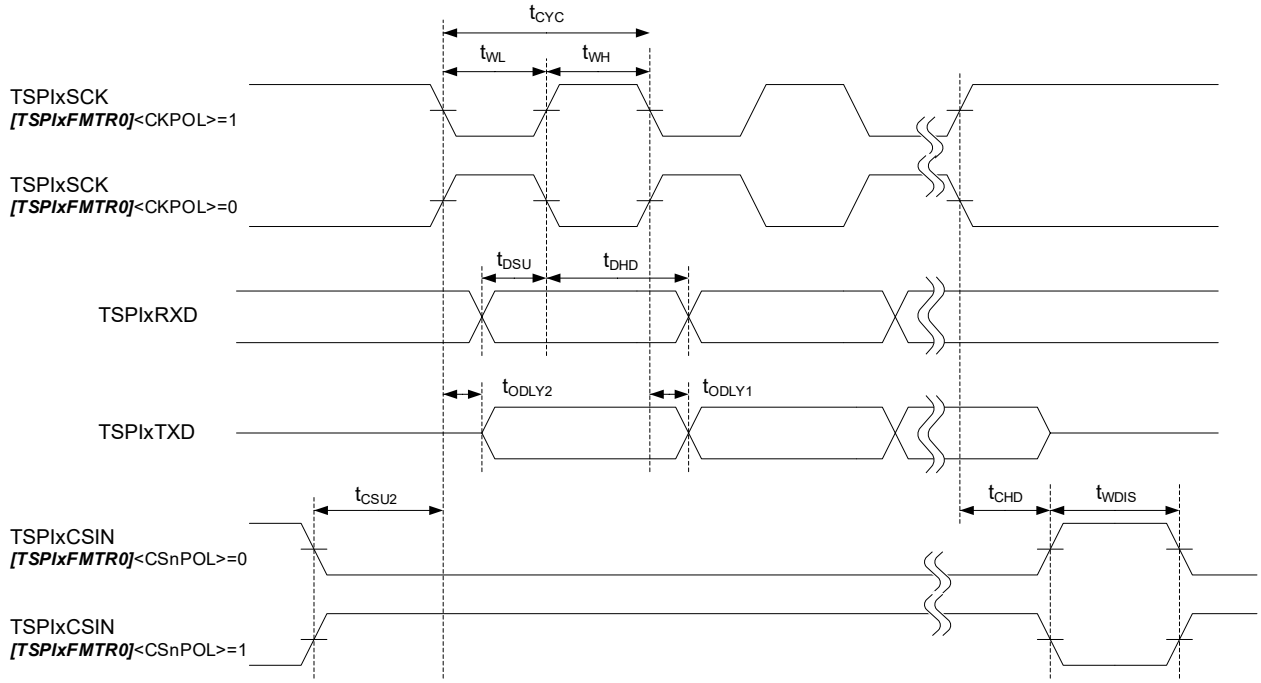


Figure 6.5 2nd Clock Edge Sampling (Target)

6.12.2. Serial Memory Interface (SMIF)

6.12.2.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5 V
- Ta = -40 to 105°C
- Input/output level: High = 0.5 × DVDD5, Low = 0.5 × DVDD5
- Load capacity: CL = 30pF
- Output drive capability: 4mA setting

6.12.2.2. AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
SMIIxSCK clock frequency	f_{CYC}	-	20	MHz
SMIxSCK clock cycle	t_{CYC}	1 / f_{CYC}	-	ns
SMIxD input setup time	t_{DSU}	12	-	
SMIxD input hold time	t_{DHD}	23.5	-	
SMIxD output hold time	t_{DDLY1}	-17	-	
SMIxD output delay time	t_{DDLY2}	-	17	
SMIxCSx_N enabled → SMIxSCK rising/falling delay time	t_{CDLY2}	t_{CYC} × 1.5 - 20	-	
SMIxSCK rising/falling → SMIxCSx_N disabled time	t_{CDLY1}	t_{CYC} × 1.0 - 20	-	

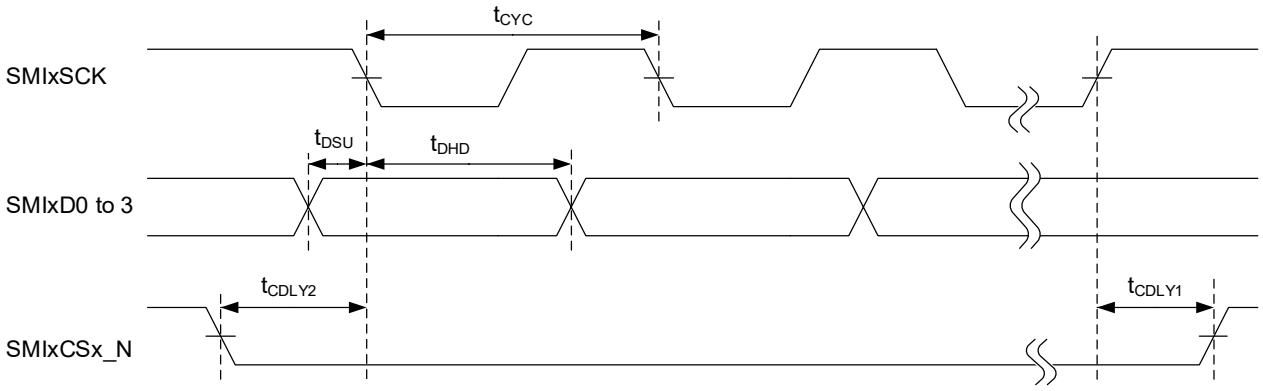


Figure 6.6 AC Timing of SMIF Read

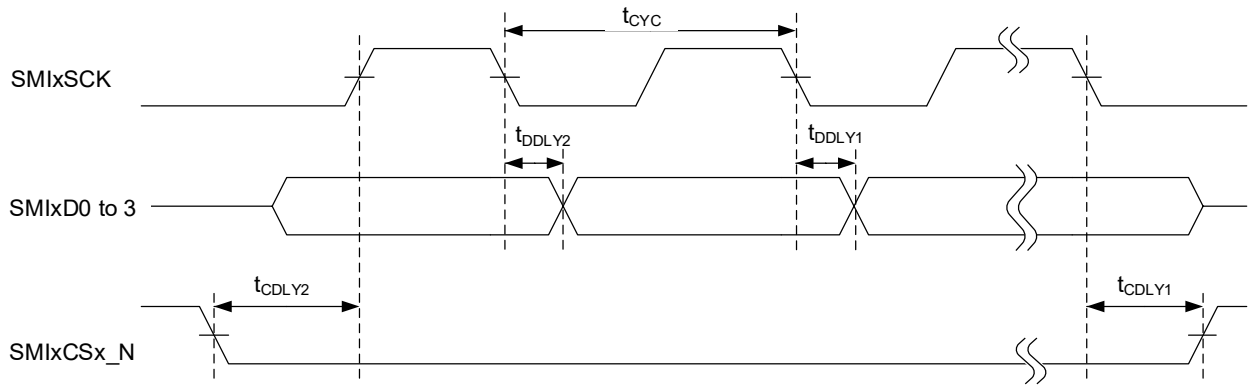


Figure 6.7 AC Timing of SMIF Write

6.12.3. I²C Interface Version A (EI2C)

6.12.3.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5= 2.7 to 5.5 V
- Ta = -40 to 105°C
- Output level: Low = 0.4V
- Input level: High = 0.7 × DVDD5, Low = 0.3 × DVDD5

6.12.3.2. AC Electrical Characteristics

Parameter	Symbol	Standard mode		Fast mode		Fast mode plus		Unit
		Min	Max	Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	0	1000	kHz
Start condition hold time	$t_{HD;STA}$	4.0	-	0.6	-	0.26	-	μs
SCL clock Low width (Input) (Note1)	t_{LOW}	4.7	-	1.3	-	0.5	-	
SCL clock High width (Input) (Note1)	t_{HIGH}	4.0	-	0.6	-	0.26	-	
Re-start condition setup time	$t_{SU;STA}$	4.7	-	0.6	-	0.26	-	
Data hold time (Input) (Note2)	$t_{HD;DAT}$	0	-	0	-	0	-	
Data setup time	$t_{SU;DAT}$	250	-	100	-	50	-	ns
Stop condition setup time	$t_{SU;STO}$	4.0	-	0.6	-	0.26	-	μs
Bus free time between stop condition and start condition (Note3)	t_{BUF}	4.7	-	1.3	-	0.5	-	

Note1: On I²C bus standard, the maximum speed of standard mode/fast mode/fast mode plus is 100kHz/400 kHz/1000kHz, respectively. For the frequency setting of the internal SCL clock, refer to the calculation formula in chapter 3.3.1 of "I²C Interface Version A" in reference manual.

Note2: On I²C bus standard, it is described that a data internal hold time should be set at least 300 ns to avoid unstable condition on the falling of the SCL when the SDA is input; however, this precaution is not supported in this MCU. Also, the edge slope control function for the SCL is not available. Therefore, when the customer designs the MCU, make sure to follow the data hold time (input) in the table above. Note that t_r/t_f on the SCL/SDA should be included in the data hold time.

Note3: To keep the time by software.

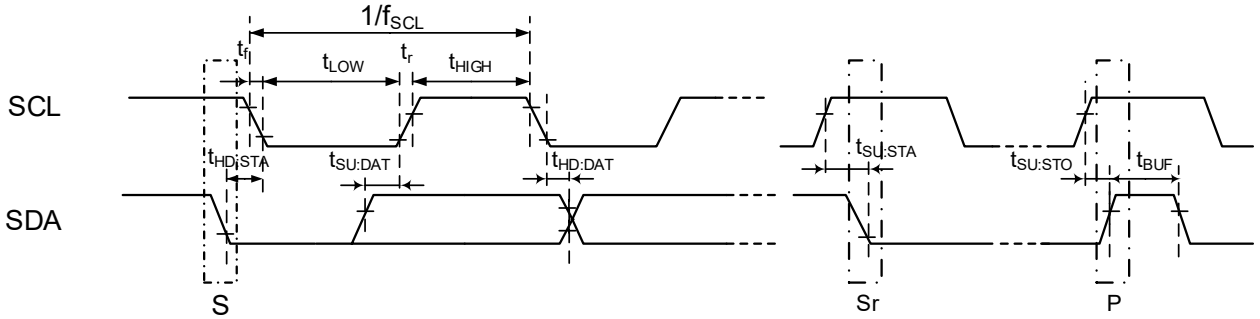


Figure 6.8 AC Timing of EI2C

6.12.4. 32-bit Timer Event Counter (T32A)

This section describes AC characteristics of T32AxINA0/A1, T32AxINB0/B1, and T32AxINC0/C1.

6.12.4.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5 V
- Ta = -40 to 105°C
- Input level: High = 0.5 × DVDD5, Low = 0.5 × DVDD5

6.12.4.2. AC Electrical Characteristics

"T" in the table below indicates the operation clock cycle of the T32A. The operation clock of the T32A is the same cycle as the ΦT0 clock. This cycle is depending on the prescaler clock setting.

(1) Operation other than the pulse count

Parameter	Symbol	Min	Max	Unit
Low level pulse width	t_{VCKL}	2T + 20	-	ns
High level pulse width	t_{VCKH}	2T + 20	-	

(2) Operation at the pulse count

Parameter	Symbol	Min	Max	Unit
Pulse cycle	t_{DCYC}	1000	-	ns
Low level pulse width	t_{PWL}	500	-	
High level pulse width	t_{PWH}	500	-	
Input setup	t_{ABS}	(NF+1) × T + 20	-	
Input hold	t_{ABH}	(NF+1) × T + 20	-	

The value of NF in above table depends on the ***[T32AxPLSCR]***<NF[1:0]> setting as follows.

[T32AxPLSCR]<NF[1:0]>	NF Value of Formula
00	0
01	2
10	4
11	8

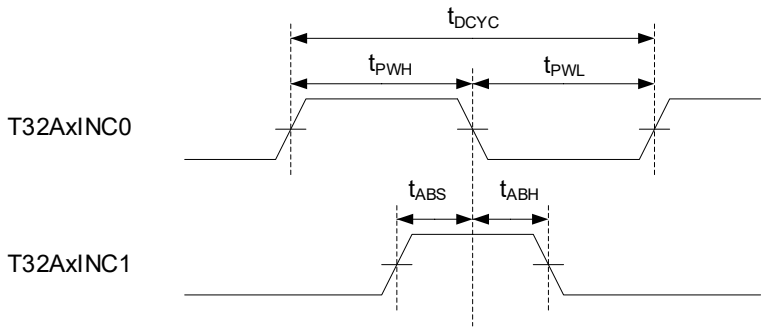


Figure 6.9 Count Pulse Input

6.12.5. External Interrupt

6.12.5.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5 V
- Ta = -40 to 105°C
- Input level: High = 0.5 × DVDD5, Low = 0.5 × DVDD5

6.12.5.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

(1) NORMAL and IDLE mode

Parameter	Symbol	Min	Max	Unit
Low level pulse width	t_{INTAL1}	T + 100	-	ns
High level pulse width	t_{INTAH1}	T + 100	-	

(2) STOP1 mode

Parameter	Symbol	Min	Max	Unit
Low level pulse width	t_{INTCL2}	125	-	ns
High level pulse width	t_{INTCH2}	125	-	

6.12.6. Pin Trigger Input (TRGINx)

6.12.6.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5V
- Ta = -40 to 105°C
- Input level: High = 0.5 × DVDD5, Low = 0.5 × DVDD5

6.12.6.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

Parameter	Symbol	Min	Max	Unit
Low level pulse width	t_{ADL}	2T + 20	-	ns
High level pulse width	t_{ADH}	2T + 20	-	

6.12.7. Debug Communication

6.12.7.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5V
- Ta = -40 to 105°C
- Input/output level: High = 0.5 ×DVDD5, Low = 0.5 × DVDD5
- Load capacity: CL = 30pF
- Output drive capability: 4mA setting

6.12.7.2. SWD Interface

3.6V < DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Min	Max	Unit
CLK high level width	t_{dckh}	50	-	ns
CLK low level width	t_{dckl}	50	-	
Output data hold time from on the rising edge of CLK	t_{d1}	1	-	
Output data valid time from on the rising edge of CLK	t_{d2}	-	35	
Rising time of CLK from input data valid	t_{ds}	20	-	
Input data hold time from on the rising edge of CLK	t_{dh}	15	-	

2.7V ≤ DVDD5 = AVDD5 ≤ 3.6V

Parameter	Symbol	Min	Max	Unit
CLK high level width	t_{dckh}	50	-	ns
CLK low level width	t_{dckl}	50	-	
Output data hold time from on the rising edge of CLK	t_{d1}	1	-	
Output data valid time from on the rising edge of CLK	t_{d2}	-	45	
Rising time of CLK from input data valid	t_{ds}	20	-	
Input data hold time from on the rising edge of CLK	t_{dh}	15	-	

6.12.7.3. JTAG Interface

3.6V < DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Min	Max	Unit
CLK high level width	t_{dckh}	50	-	ns
CLK low level width	t_{dckl}	50	-	
Output data hold time from on the falling edge of CLK	t_{d1}	1	-	
Output data valid time from on the falling edge of CLK	t_{d2}	-	35	
Rising time of CLK from input data valid	t_{ds}	20	-	
Input data hold time from on the rising edge of CLK	t_{dh}	15	-	

2.7V ≤ DVDD5 = AVDD5 ≤ 3.6V

Parameter	Symbol	Min	Max	Unit
CLK high level width	t_{dckh}	50	-	ns
CLK low level width	t_{dckl}	50	-	
Output data hold time from on the falling edge of CLK	t_{d1}	1	-	
Output data valid time from on the falling edge of CLK	t_{d2}	-	45	
Rising time of CLK from input data valid	t_{ds}	20	-	
Input data hold time from on the rising edge of CLK	t_{dh}	15	-	

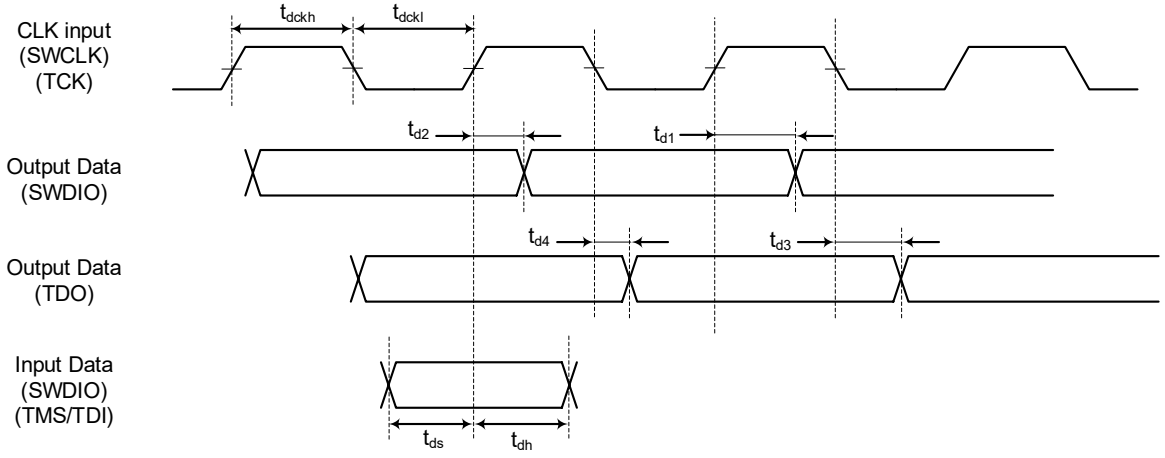


Figure 6.10 JTAG/SWD Signal Waveform

6.12.7.4. ETM Interface

3.6V < DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Min	Max	Unit
TRACECLK cycle	t_{tclk}	50	-	ns
Data valid time from rising on TRACECLK	t_{setupr}	2	-	
TRACEDATA hold time from on the rising edge of TRACECLK	t_{holdr}	1	-	
TRACEDATA valid time from on the falling edge of TRACECLK	t_{setupf}	2	-	
TRACEDATA hold time from on the falling edge of TRACECLK	t_{holdf}	1	-	

2.7V ≤ DVDD5 = AVDD5 ≤ 3.6V

Parameter	Symbol	Min	Max	Unit
TRACECLK cycle	t_{tclk}	100	-	ns
Data valid time from rising on TRACECLK	t_{setupr}	2	-	
TRACEDATA hold time from on the rising edge of TRACECLK	t_{holdr}	1	-	
TRACEDATA valid time from on the falling edge of TRACECLK	t_{setupf}	2	-	
TRACEDATA hold time from on the falling edge of TRACECLK	t_{holdf}	1	-	

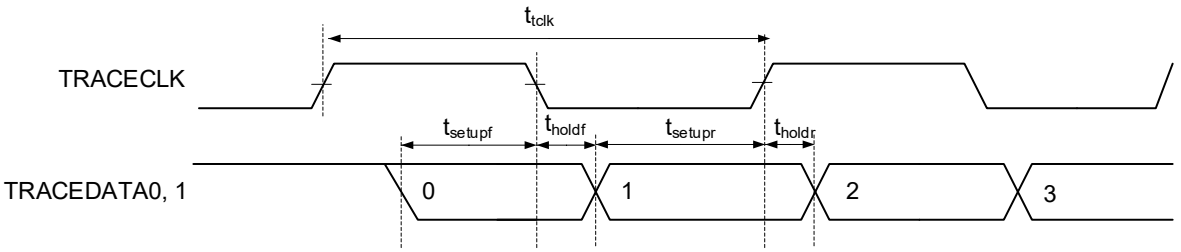


Figure 6.11 Trace Signal Waveform

6.12.8. SCOUT Pin

6.12.8.1. AC Measurement Conditions

The AC characteristics are the result of the measurement conditions below:

- DVDD5 = AVDD5= 2.7 to 5.5V
- Ta = -40 to 105°C
- Output level: High = 0.5 × DVDD5, Low = 0.5 × DVDD5
- Load capacity: CL = 30pF
- Output drive capability: 4mA setting

6.12.8.2. AC Electrical Characteristics

"T" in the table indicates the cycle of the SCOUT output waveform.

Parameter	Symbol	Min	Max	Unit
Low level pulse width	t_{SCL}	0.5 × T- 15	-	ns
High level pulse width	t_{SCH}	0.5 × T- 15	-	

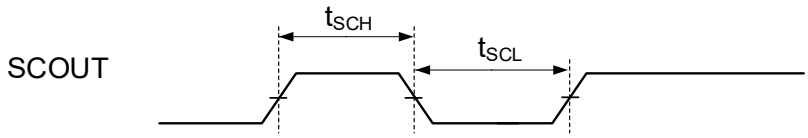


Figure 6.12 SCOUT Waveform Output

6.12.9. External Clock Input

6.12.9.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5V
- Ta = -40 to 105°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5

6.12.9.2. AC Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Clock frequency ($1/t_{ehcin}$)	$f_{EHCLKIN}$	6	-	24	MHz
Clock duty	-	45	-	55	%
Clock rising time	t_r	-	-	10	ns
Clock falling time	t_f	-	-	10	ns

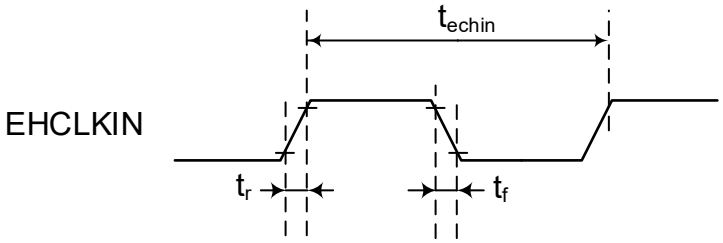


Figure 6.13 External Clock Input Waveform

6.13. Noise Filter (Analog) Characteristics

DVDD5 = AVDD5 = 2.7 to 5.5V
Ta = -40 to 105°C

Parameter	Condition	Min	Typ.	Max	Unit
Noise cancel width	-	120	-	-	ns

6.14. Flash Memory Characteristics

6.14.1. Program and Erase Characteristics

DVDD5 = AVDD5 = 2.7 to 5.5V
Ta = -40 to 105°C

Parameter	Condition	Min	Typ.	Max	Unit
Rewrite frequencies	-	-	-	100,000	cycles
Programming time	Programming time for a word	-	75.0	84.4	μs
Erase time	Block erase time	-	6.8	7.5	ms
	Area erase time (Note)	-	108.8	120.0	
	Chip erase time (Note)	-	217.6	240.0	

Note: In case that flash memory has no block with effective protection.

6.14.2. Forced CPROTCON Release Characteristics

DVDD5 = AVDD5 = 2.7 to 5.5V
Ta = -40 to 105°C

Parameter	Condition	Min	Typ.	Max	Unit
Forced CPROTCON release time	-	-	224.4	247.5	ms

6.15. Regulator Characteristics

DVDD5 = AVDD5 = 2.7 to 5.5V
Ta = -40 to 105°C

Parameter	Condition	Min	Typ.	Max	Unit
Capacitance of REGOUT capacitor	-	0.8	4.7	5.64	μF

6.16. Oscillation Circuit Characteristics

6.16.1. Internal Oscillator

DVDD5 = AVDD5 = 2.7 to 5.5V
Ta = -40 to 105°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{IHOSC1}	-	9.9	10	10.1	MHz
	f_{IHOSC2}		9	10	11	

6.16.2. External Oscillator

DVDD5 = AVDD5 = 2.7 to 5.5V
Ta = -40 to 105°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{EHOSC}	-	6	-	24	MHz

Note1: Use in an environment where oscillation within 1% accuracy is always supplied.
Note2: Please contact the oscillator vendor, regarding the matching data of the device and the oscillator.

6.16.3. Oscillation Circuit

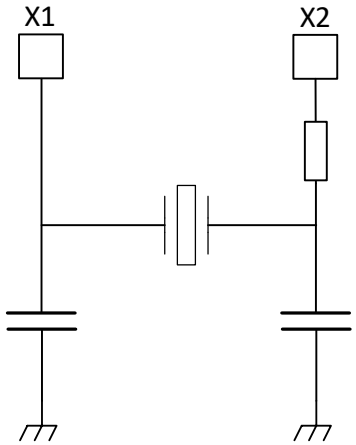


Figure 6.14 Example of Oscillation Circuit

To obtain a stable oscillation, load capacity and the position of the oscillator must be configured properly.
Since these factors are strongly affected by substrate patterns, please evaluate oscillation stability using the substrate you use.
This product has been evaluated by the oscillator vendor below. Please refer this information when selecting external parts.

6.16.4. Ceramic Oscillator

This product has been evaluated by the ceramic oscillator by Murata Manufacturing Co., Ltd.
Please refer to the company's website for details.

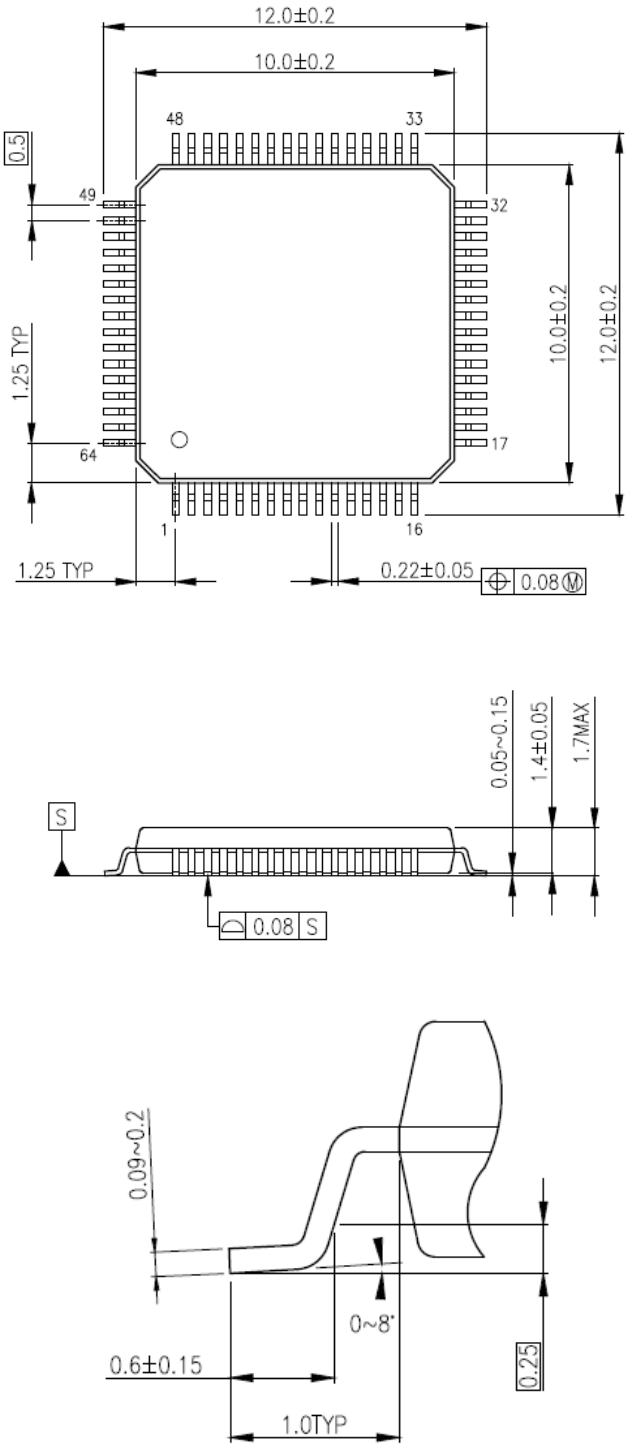
6.16.5. Precautions for Designing Printed Circuit Board

Be sure to design printed circuit board patterns that connect a crystal unit with other oscillation elements so that the length of such patterns become shortest possible to prevent deterioration of characteristics due to stray capacitances and wiring inductance. For multi-layer circuit boards, it is important not to wire the ground and other signal patterns right beneath the oscillation circuit. For more information, please refer to the URL of the oscillator vendor.

7. Package Dimensions

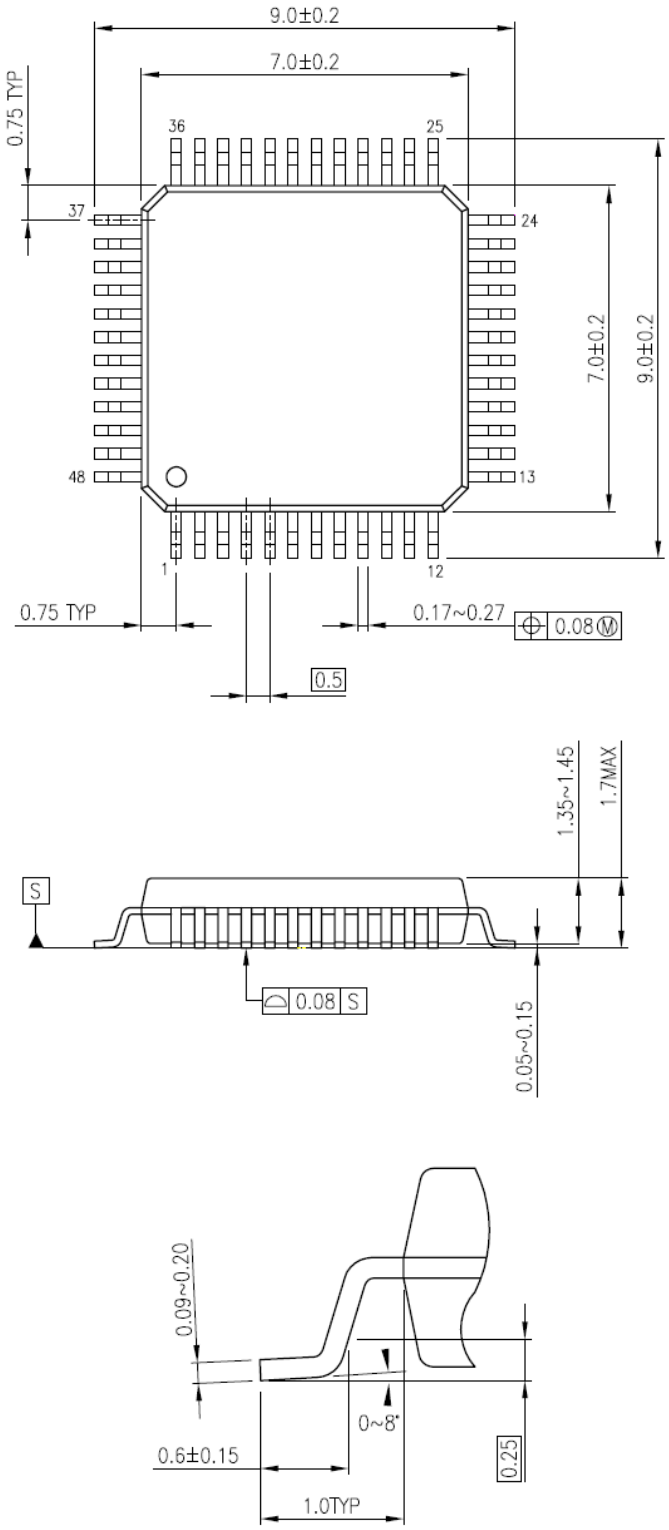
7.1. P-LQFP64-1010-0.50-003

Unit: mm



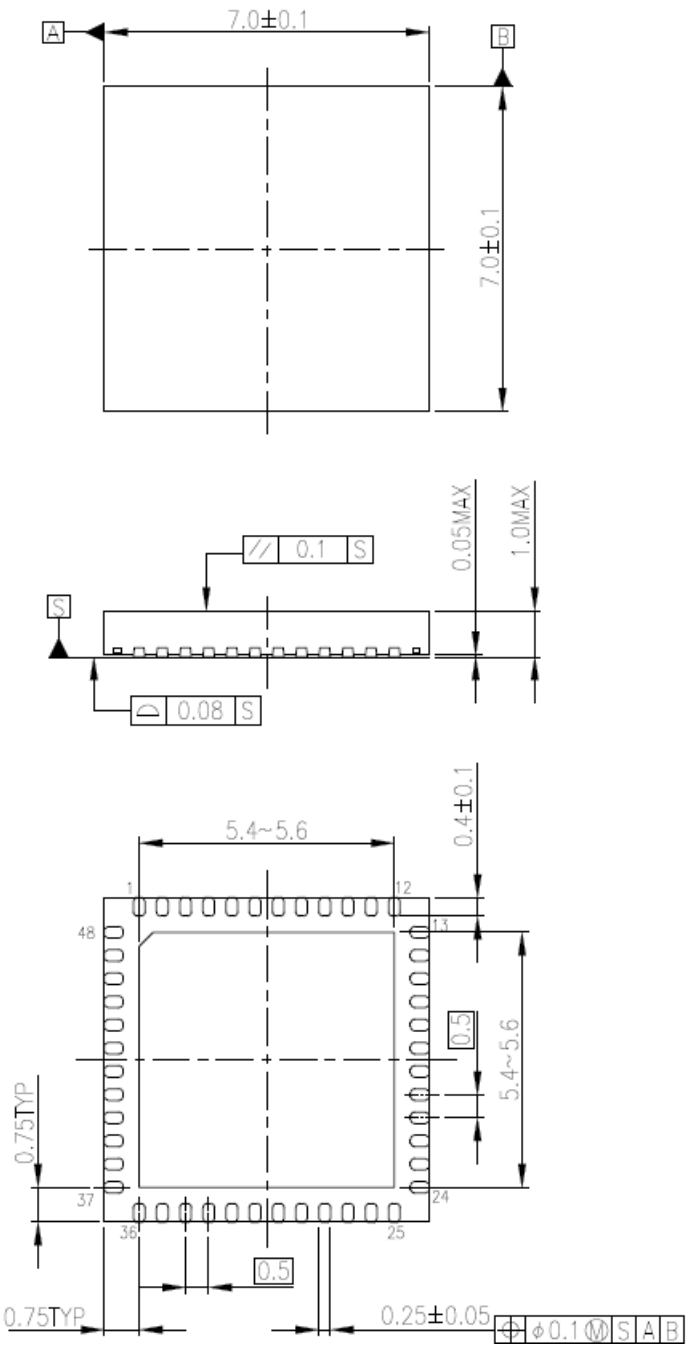
7.2. P-LQFP48-0707-0.50-002

Unit: mm



7.3. P-VQFN48-0707-0.50-006

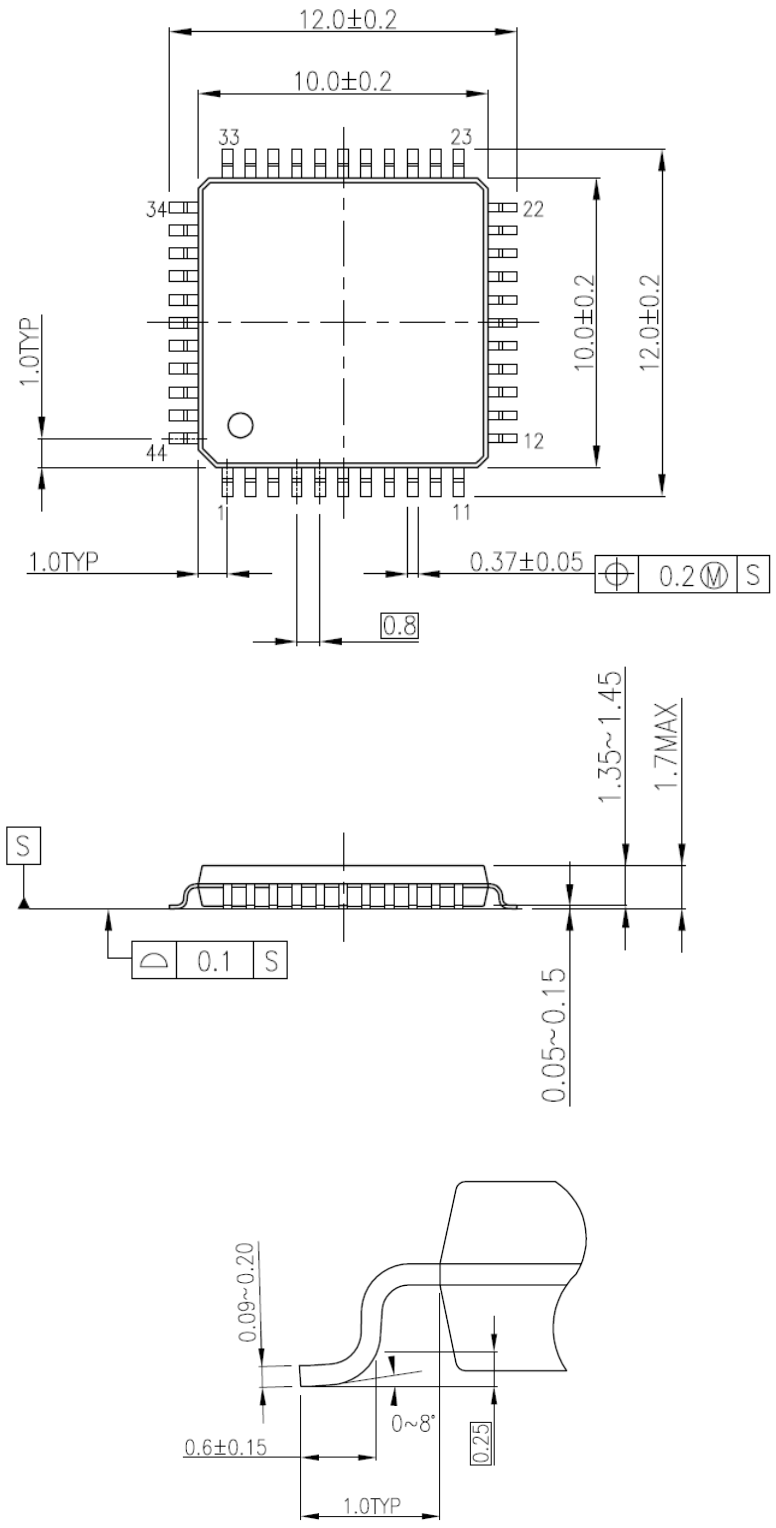
Unit: mm



Note: Connect exposed pad (E-Pad) to GND.

7.4. P-LQFP44-1010-0.80-003

Unit: mm



8. Precautions

This Page explains general precautions on the use of our MCUs.

Note that if there is a difference between the general precautions and the description in the body of the document, the description in the body of the document has higher priority.

(1) The MCUs' operation at power on

At power on, internal state of the MCUs is unstable. Therefore, state of the pins is undefined until reset operation is completed.

When a reset is performed by an external reset pin, pins of the MCUs that use the reset pin are undefined until reset operation by the external pin is completed.

Also, when a reset is performed by the internal power on reset, pins of the MCUs that use the internal power on reset are undefined until power supply voltage reaches the voltage at which power on reset is valid.

(2) Unused pins

Unused input/output ports of the MCUs are prohibited to use. The pins are high impedance.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

(3) Clock oscillation stability

A reset state must be released after the clock oscillation becomes stable. If the clock is changed to another clock while the program is in progress, wait until the clock is stable.

9. Revision History

Table 9.1 Revision History

Revision	Date	Description
1.0	2026-01-30	- First release

Part Naming Conventions

TMP M4 L 4 F Y x UG

The identification of Toshiba microcontrollers

Core

Symbol	Description
M4	Arm Cortex-M4 with FPU
M3	Arm Cortex-M3
M0	Arm Cortex-M0

Revision

Package

Symbol	Description
QG	Plastic shrink quad outline non-leaded package, dry-packed
UG, DUG, FG, DFG	Plastic quad flat package, dry-packed
MG, DMG	Plastic small outline package, dry-packed
XBG	Plastic ball grid array, dry-packed

Product group

Family	Symbol	Main application
TXZ/ TXZ+	H	For general-purpose/consumer electronics equipment
	K	For control of motors/inverter control/industrial equipment (Analog combo)
	M	For control of motors/inverter control/industrial equipment (Analog combo), CAN built-in
	G	For OA/digital equipment/industrial equipment
	N	For industrial network/IoT information management device/Ethernet, USB and CAN built-in
	E	For precision instrument
	L	For control of one motor/inverter control/industrial equipment
	V	For general-purpose/consumer electronics equipment (Entry Series)

ROM Size

Symbol	Size [KB]
M	32
P	48
S	64
U	96
W	128
Y	256
Z	384
D	512
E	768
10	1024
15	1536
20	2048

Pin count

Symbol		Pin count	Symbol		Pin count
0	G	32 pins or less	7	P	101 to 128 pins
1	H	33 to 44 pins	8	Q	129 to 144 pins
2	J	45 to 48 pins	9	R	145 to 176 pins
3	K	49 to 52 pins	A	S	177 to 200 pins
4	L	53 to 64 pins	B	T	201 to 224 pins
5	M	65 to 80 pins	C	U	225 to 250 pins
6	N	81 to 100 pins	D	V	251 to 300 pins

ROM type

Symbol	Type
F	Flash

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