300W Isolated DC-DC Converter (Upgraded)

Design Guide

RD249-DGUIDE-01

Toshiba Electronic Devices & Storage Corporation

Table of Contents

1. Introduction

This design guide describes the design overview of each circuit block of the 300W isolated DC-DC converter (Upgraded) (hereafter referred to as “this design”). This design is based on the existing “300W Isolated DC-DC Converter Power Supply” released in August 2018, and achieves improved conversion efficiency through replacement of the secondary-side switching MOSFETs with the latest generation devices and circuit optimization.

As with the existing design, this design features a wide input voltage range of DC 36 to 75V, and can be applied to telecom equipment where 48V distribution lines are available, industrial equipment connected to 48V batteries, and various other applications. Provided as a reference design, this design offers comprehensive design information and helps reduce design effort when adapting to actual specifications.

This design adopts compact surface-mount power MOSFETs for both the primary-side and secondary-side switching devices of the DC-DC converter. By also using compact surface-mount components elsewhere, and while employing a general-purpose wound-structure transformer, this design achieves a compact footprint (82mm × 82mm) and high efficiency (94.6%). The use of a wound-structure transformer facilitates deployment in real-world applications and enables constructing the power circuit directly on the host equipment’s PCB instead of relying on external power modules.

2. Main Components

This chapter describes the main components used in this design.

2.1. Power MOSFET TPN1200APL

This design uses the N-channel MOSFET TPN1200APL as the primary-side main switching device in the Phase Shift Full Bridge (PSFB) circuit. The main features of the TPN1200APL are as follows:

- High-speed switching
- Small gate charge: Q_{SW} = 7.5nC (Typ.)
- Small output charge: Q_{oss} = 24nC (Typ.)
- Low drain-source on-resistance: $R_{DS(ON)}$ = 9.8mΩ (Typ.) (V_{GS} = 10V)
- Low leakage current: I_{DSS} = 10μA (Max) (V_{DS} = 100V)
- Enhancement mode: V_{th} = 1.5 to 2.5V (V_{DS} = 10V, I_D = 0.3mA)

Appearance and Terminal Layout

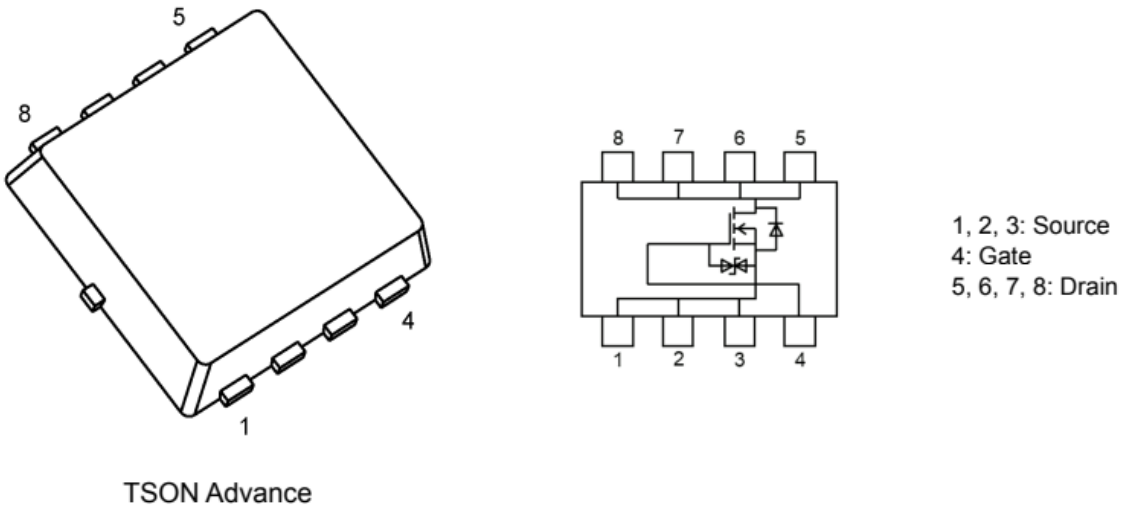

Fig 2.1 TPN1200APL Appearance and Terminal Layout

2.2. Power MOSFET TPH2R70AR5

This design uses the N-channel MOSFET TPH2R70AR5 as the secondary-side synchronous rectification device. The main features of the TPH2R70AR5 are as follows:

- Fast reverse recovery time : t_{rr} = 52ns (Typ.)
- Small reverse recovery charge : Q_{rr} = 55nC (Typ.)
- Small gate charge: Q_{SW} = 17nC (Typ.)
- Low drain-source on-resistance: $R_{DS(ON)}$ = 2.3mΩ (Typ.) (V_{GS} = 10V)
- Low leakage current: I_{DSS} = 10μA (Max) (V_{DS} = 100V)
- Enhancement mode: V_{th} = 2.9 to 4.3V (V_{DS} = 10V, I_D = 1.0mA)

Appearance and Terminal Layout

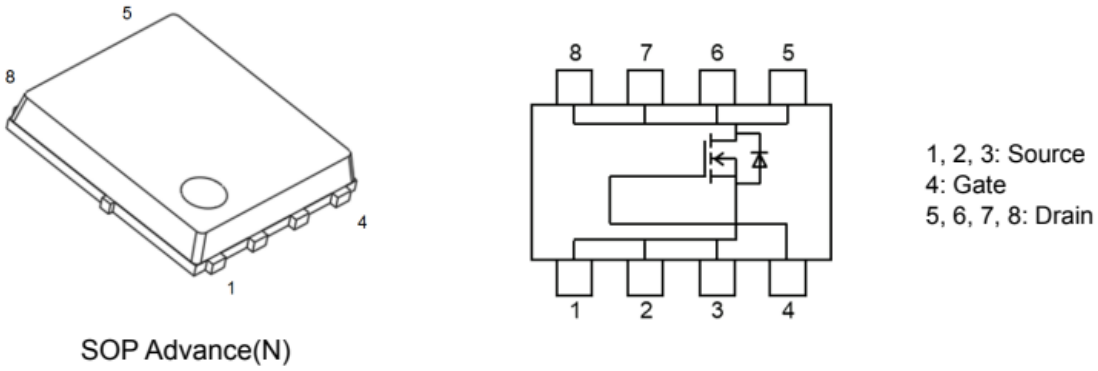

Fig 2.2 TPH2R70AR5 Appearance and Terminal Layout

2.3. Standard Digital Isolator DCL520C00

This design uses the standard digital isolator DCL520C00 to transmit gate-drive signals from the controller located on the primary side to the MOSFET drive circuit on the secondary side. The main features of the DCL520C00 are as follows:

- Data rate : Up to 150Mbps
- Supply voltage : 2.25V to 5.5V
- Temperature Range : -40°C to 125°C
- Propagation Delay :10.9ns Typical (5.0V operation)
- Default Output : High and Low Options
- High CMTI (Typ.) : 150kV/μs
- Withstand Voltage : 3.0kVrms

Appearance and Terminal Layout

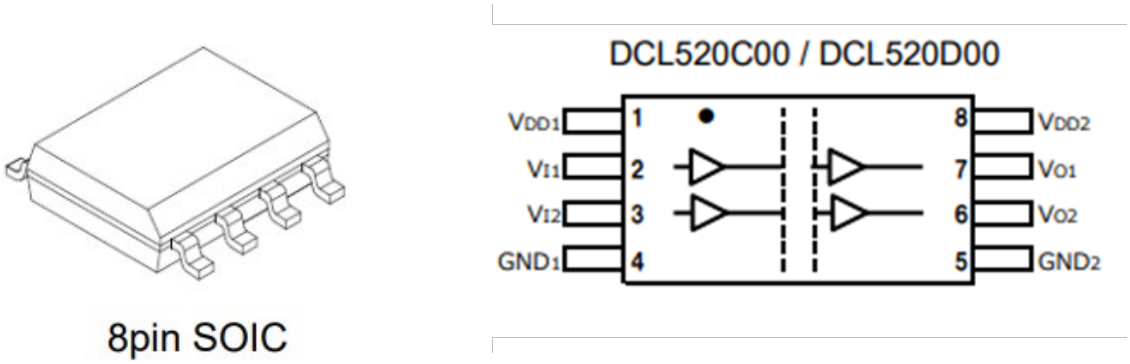

Fig 2.3 DCL520C00 Appearance and Terminal Layout

3. Phase Shift Full Bridge（PSFB) Circuit Design

This design generates a 12V output using a PSFB circuit. In the PSFB topology, the high-side and low-side MOSFETs of each primary leg are alternately switched on and off at a 50% duty cycle, and the output voltage is controlled by adjusting the phase of the on-timing between the legs. Dead time is provided at the high-side/low-side transition to prevent shoot-through; during this interval, resonant behavior enables Zero Volt Switching (ZVS). ZVS reduces switching losses and allows realization of a high-efficiency power supply.

In this design, a PSFB circuit is implemented using the LM5046, a Phase-Shifted Full-Bridge PWM controller with an integrated MOSFET driver manufactured by Texas Instruments (hereafter referred to as the “PSFB PWM controller”) to construct the PSFB circuit. The following describes the basic design items of the PSFB circuit in this design. For detailed design around the controller, refer to the Texas Instruments LM5046 datasheet and related documentation. For the detailed specifications of this design, refer to the reference guide (RD249-RGUIDE-xx); for the schematic refer to RD249-SCHEMATIC-xx and for the bill of materials refer to RD249-BOM-xx.

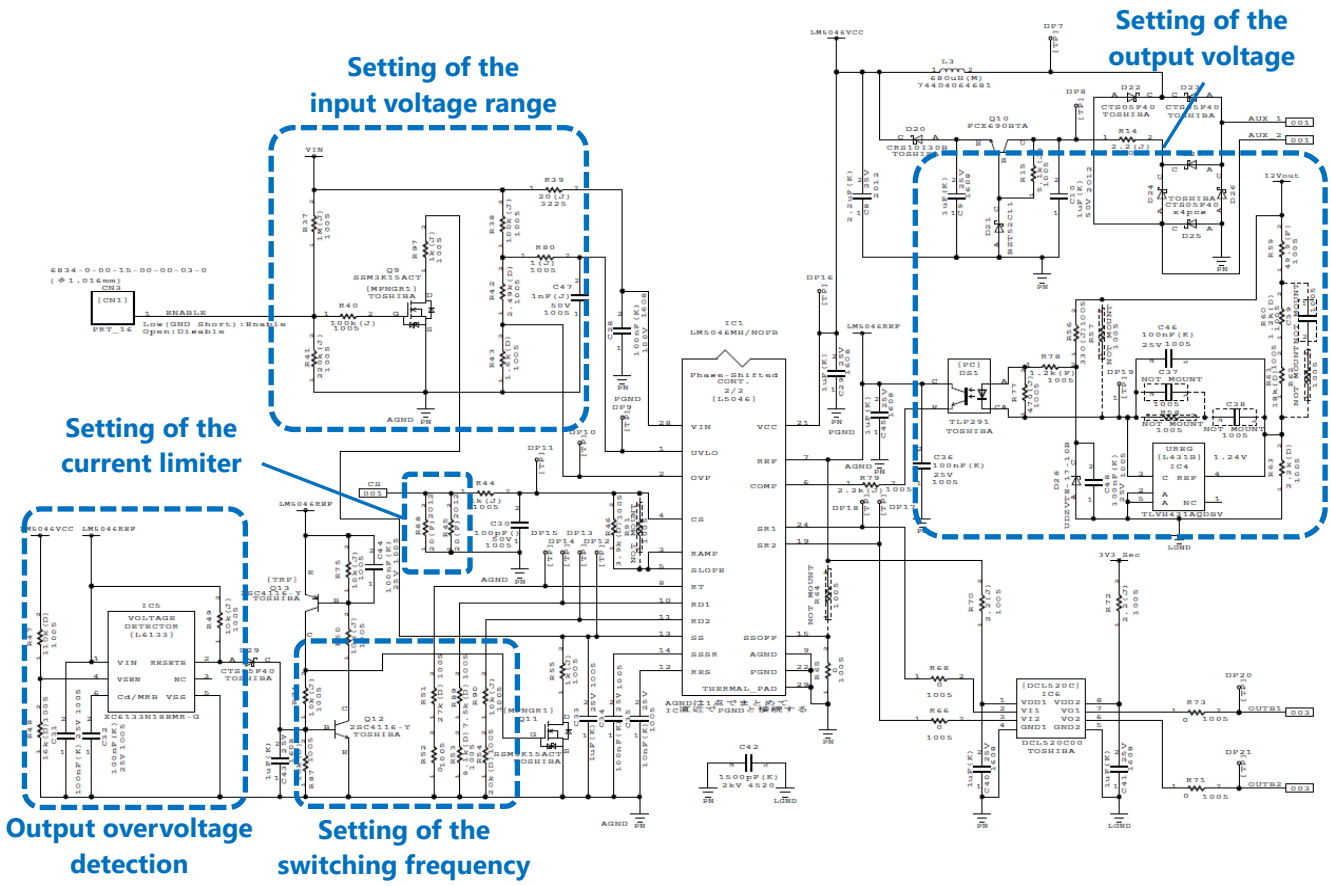

Fig 3.1 PSFB Circuit (Around the Controller)

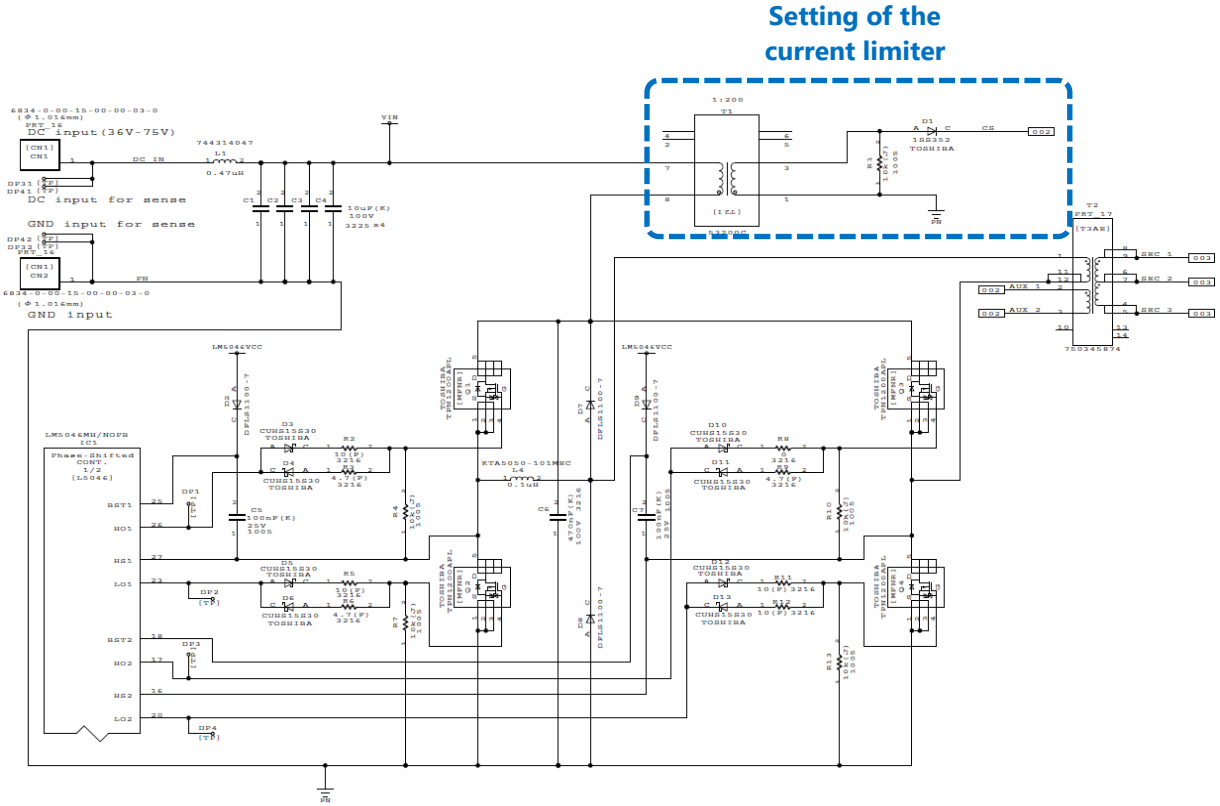

Fig 3.2 PSFB Circuit (Around the Primary-side MOSFETs)

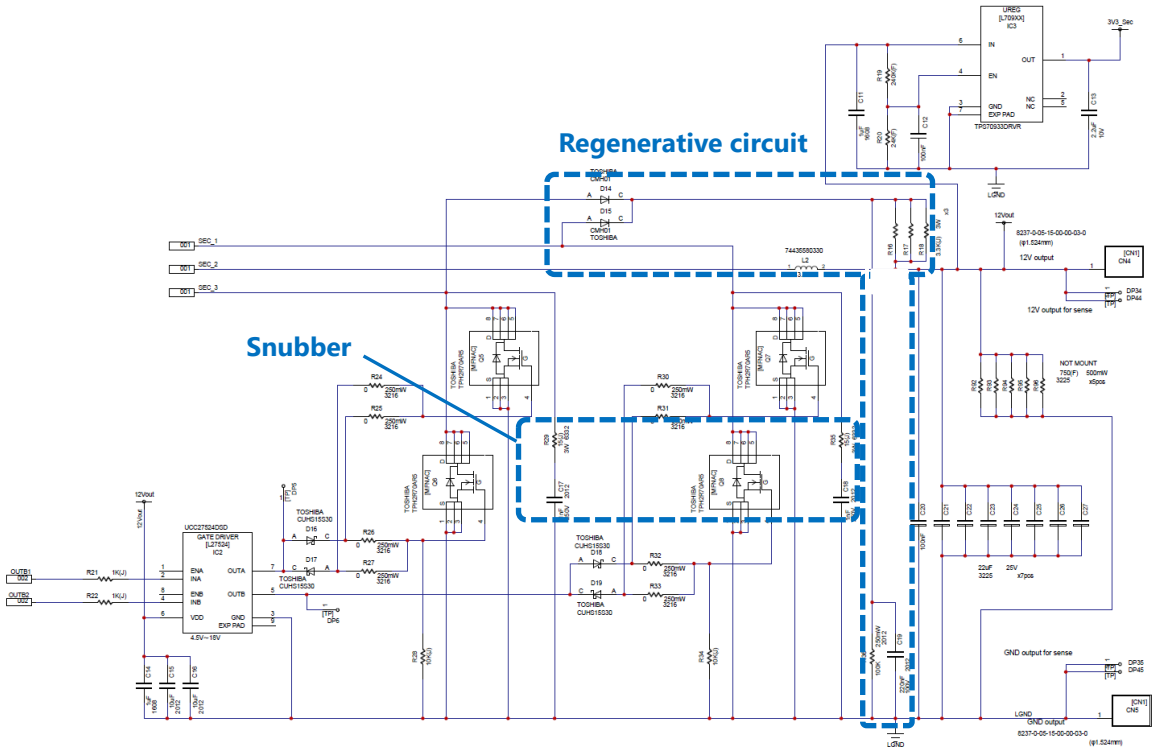

Fig 3.3 PSFB Circuit (Around the Secondary-side Synchronous Rectification MOSFETs)

3.1. Setting the Input Voltage Operating Range (Lower Limit)

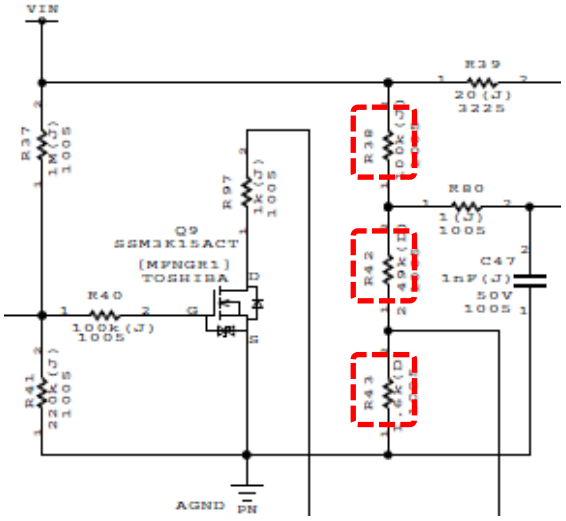

Fig 3.4 Setting the Input Voltage Range

This design sets the input voltage operating range using the resistance values of external resistors (R38, R42, R43). The input voltage V_{in} is divided by resistors (R38, R42, R43) and fed to the UVLO pin of the PSFB PWM controller, thereby setting the lower operating voltage thresholds ($V_{in\_min\_on}$, $V_{in\_min\_off}$). The PSFB PWM controller starts switching when the UVLO pin voltage-generated by the resistor divider and the internal hysteresis current (20µA)-exceeds 1.25V. After operation starts, the controller stops the internal hysteresis current and halts switching when the UVLO pin falls below 1.25V. The lower operating thresholds ($V_{in\_min\_on}$, $V_{in\_min\_off}$) are calculated by the corresponding equations.

$$V_{in\_min\_on}(V) = 1.25(V) \times \frac{(R38 + R42 + R43)}{(R42 + R43)} + 20(\mu A) \times R38$$

$$V_{in\_min\_off}(V) = 1.25(V) \times \frac{(R38 + R42 + R43)}{(R42 + R43)}$$

In this design, $V_{in\_min\_on}$ is set to 33.81V and $V_{in\_min\_off}$ is set to 31.81V. As shown in Fig 3.4, resistor values are selected as R38 = 100kΩ, R42 = 2.49kΩ, and R43 = 1.6kΩ. The relationship between input voltage (V_{in}), UVLO pin voltage, and switching operation status is shown in Fig 3.5.

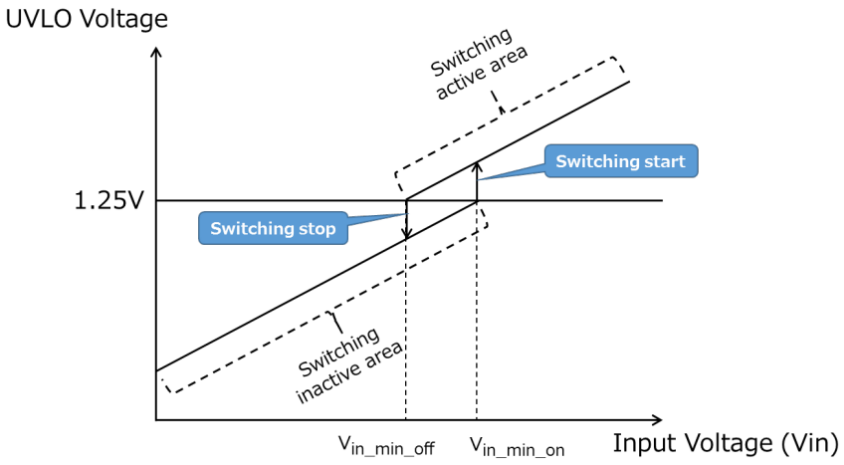

Fig 3.5 Input Voltage vs. UVLO Pin Voltage and Switching Operation Status

3.2. Setting the Input Voltage Operating Range (Upper Limit)

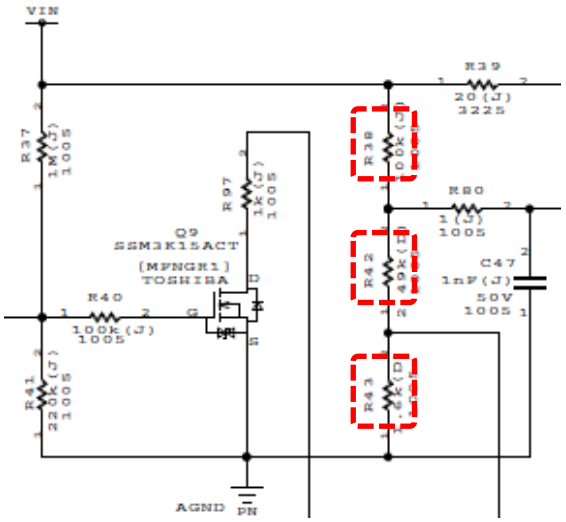

Fig 3.6 Setting the Input Voltage Range

This design sets the input voltage upper limit using the resistance values of external resistors (R38, R42, R43). The input voltage V_{in} is divided by resistors (R38, R42, R43) and fed to the OVP pin of the PSFB PWM controller, thereby setting the upper operating voltage thresholds ($V_{in\_max\_off}$, $V_{in\_max\_on}$). The PSFB PWM controller stops switching when the OVP pin voltage generated by the resistor divider exceeds 1.25V. After shutdown, the controller enables the internal hysteresis current, and switching restarts when the UVLO pin voltage exceeds 1.25V (while remaining within the OVP threshold). The upper operating thresholds ($V_{in\_max\_on}$, $V_{in\_max\_off}$) are calculated by the corresponding equations.

$$V_{in\_max\_off}(V) = 1.25(V) \times \frac{(R38 + R42 + R43)}{(R43)}$$

$$V_{in\_max\_on}(V) = 1.25(V) \times \frac{(R38 + R42 + R43)}{(R43)} - 20(\mu A) \times (R38 + R42)$$

In this design, $V_{in\_max\_off}$ is set to 81.32V and $V_{in\_max\_on}$ is set to 79.27V. As shown in Fig 3.6, resistor values are selected as R38 = 100kΩ, R42 = 2.49kΩ, and R43 = 1.6kΩ. The relationship between input voltage (V_{in}), OVP pin voltage, and switching operation status is shown in Fig 3.7.

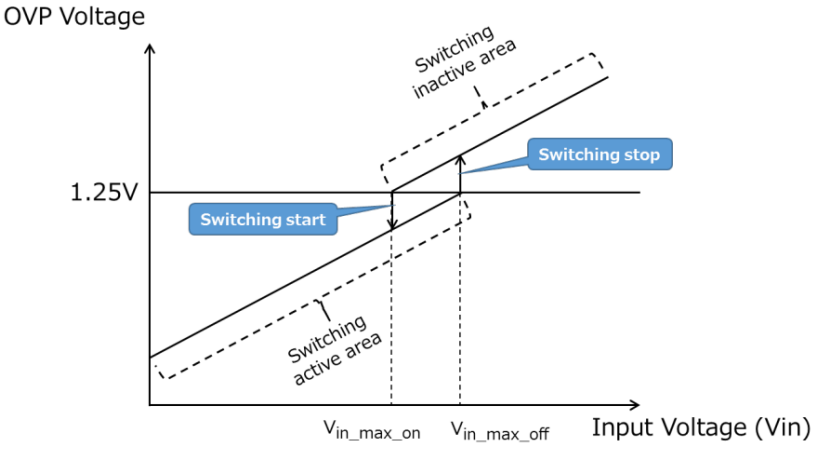

Fig 3.7 Input Voltage vs. OVP Pin Voltage and Switching Operation Status

3.3. Setting the Output Voltage

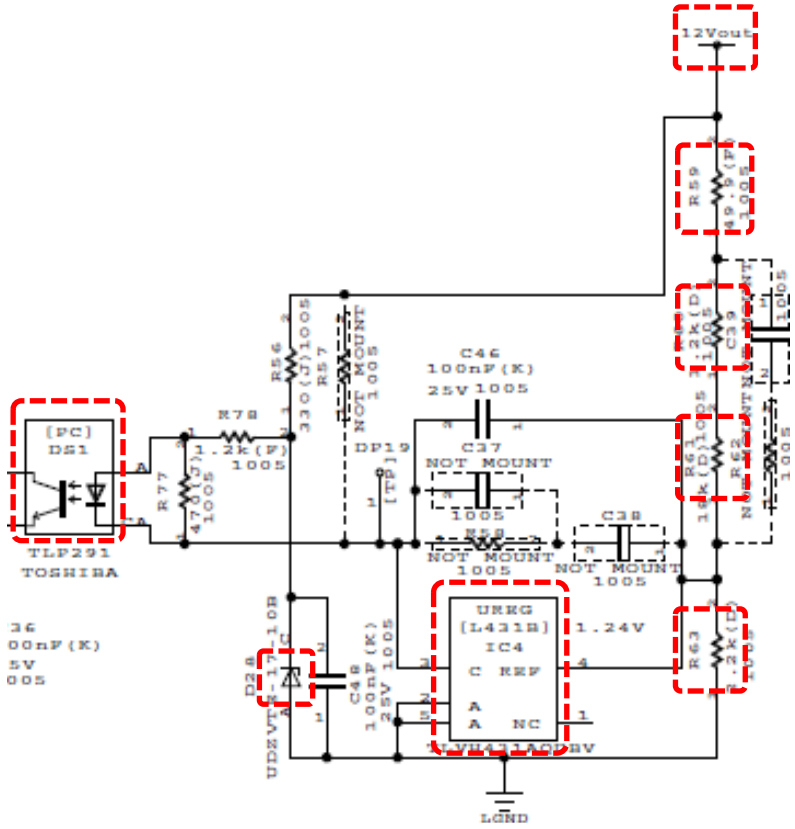

Fig 3.8 Setting the Output Voltage

This design sets the PSFB output voltage (V_{out}) using the resistance values of external resistors (R59, R60, R61, R63) and a shunt regulator (IC4). The shunt regulator (TLVH431AQDBV) controls the optocoupler (DS1) current such that the divided output voltage via resistors (R59, R60, R61, R63) matches the reference voltage (V_{REF}). The PSFB PWM controller regulates V_{out} in response to the feedback current from the optocoupler (DS1). The output voltage (V_{out}) is calculated by the corresponding equation.

$$V_{out}\ \ (V) = \frac{V_{REF}(V) \times (R59 + R60 + R61 + R63)}{R63}$$

In this design, V_{out} is set to 12.09V. As shown in Fig 3.8, resistor values are selected as R59 = 49.9Ω, R60 = 1.2kΩ, R61 = 18kΩ, and R63 = 2.2kΩ. To help prevent output oscillation, a Zener diode (D28) is used to stabilize the optocoupler (DS1) supply.

3.4. Setting the Switching Frequency

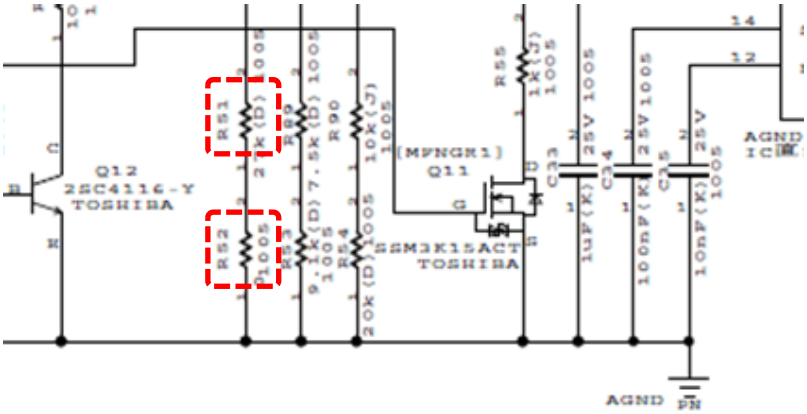

Fig 3.9 Setting the Switching Frequency

This design sets the PSFB PWM controller internal operation frequency (f_{PWM}) using the resistance values of external resistors (R51, R52). The switching frequency (f_{PWM}) is calculated by the corresponding equation.

$$f_{PWM}(Hz) = \frac{1}{\left(R51(\Omega) + R52(\Omega)\right) \times 1 \times 10^{-10}}$$

In this design, f_{PWM} is set to 370kHz. As shown in Fig 3.9, resistor values are selected as R51 = 27kΩ and R52 = 0Ω. The PSFB PWM controller switches the MOSFETs of the left and right legs of the primary full bridge (Q1–Q2 and Q3–Q4) at one-half of f_{PWM}. The output voltage has a ripple at the f_{PWM}.

3.5. Current Limiter

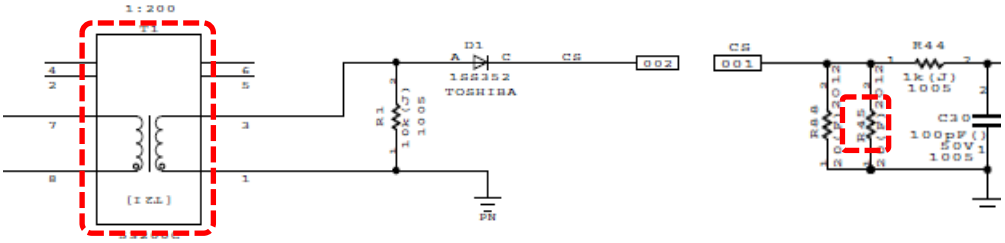

Fig 3.10 Current Limiter

When the CS pin of the PSFB PWM controller reaches the current-limit threshold (0.75V), the controller limits current by controlling the primary bridge MOSFETs. Fig 3.2 shows the PSFB circuit (around the input bridge MOSFETs). The current-limit level (I_limit) is set using the current-limit threshold (0.75V), the current-sense resistor value (R45), and the current transformer (T1) turns ratio. The current-limit level is calculated by the corresponding equation.

$$I\_limit = \frac{0.75}{(R45/R88) \times (transformer\ turns\ ratio)}$$

In this design, I_limit is set to 13.7A. As shown in Fig 3.10, resistor R45 = 8.2Ω and current transformer T1 turns ratio = 1:200 are selected.

3.6. Gate Drive Circuit

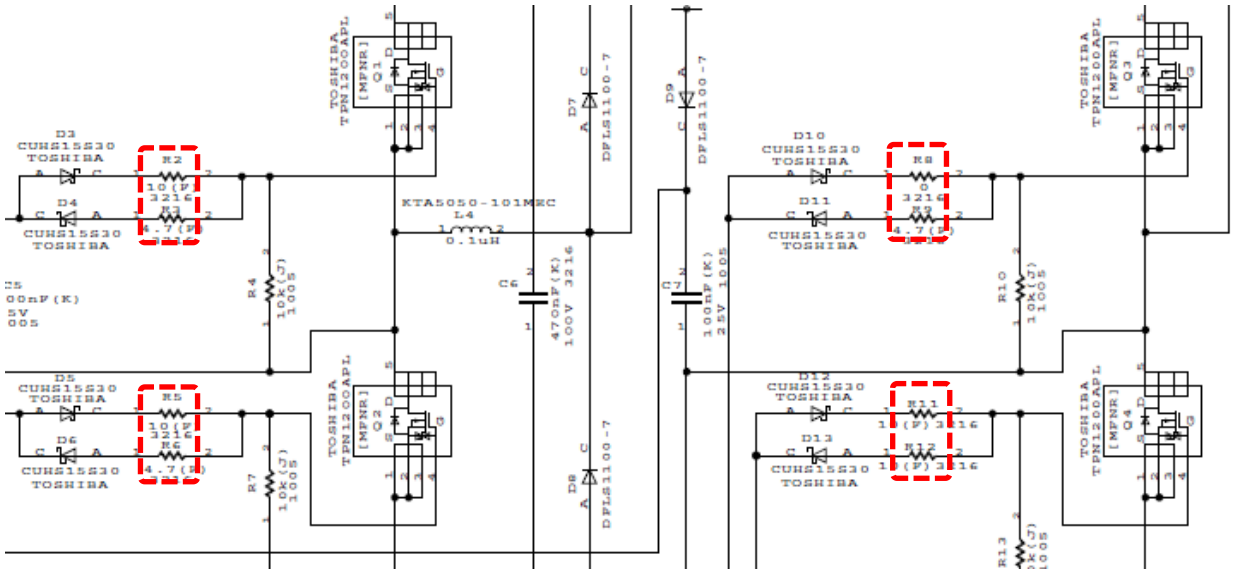

Fig 3.11 Gate Drive Circuit

Gate drive circuit design affects both power efficiency and EMI. In general, efficiency and EMI are in a trade-off relationship; a balanced design is required. While the PSFB circuit exhibits low EMI due to ZVS operation, if a hard-switching region is suspected to be the source of EMI, increase the gate series resistor values of the MOSFETs (Q1–Q4) (R2, R3, R5, R6, R8, R9, R11, R12) and verify EMI. Turn-on and turn-off can be adjusted individually.

In this design, as shown in Fig 3.11, resistors are selected as follows: R2, R5, R11, R12 = 10Ω; R3, R6, R9 = 4.7Ω; R8 = 0Ω.

3.7. Transformer

If the secondary-side synchronous rectification on-duty is set to 60% under steady-state PSFB operation and the output voltage is 12V, approximately a 20V square wave is required on the secondary side. With a nominal input voltage of 48V, this design selects transformer (T2) turns ratio 5:2:2:2 (center-tap method, with auxiliary winding). This yields a 19.2V square wave on the secondary side. In addition, primary-to-secondary isolation withstand voltage, winding temperature rise, flux saturation, core loss, etc., must be sufficiently considered.

Additionally, in this design, ZVS is achieved over a wide load range by utilizing the transformer leakage inductance together with the inductance of an external inductor (L4).

3.8. Output Capacitors

Set the output capacitor total capacitance (C_{out}) so that the output voltage ripple (V_{ripple}) meets the required specification. The combined ripple voltage contributed by the following mechanisms constitutes V_{ripple}:

- Ripple due to ripple current (ΔI) and output capacitor equivalent series resistance (ESR): V_{ripple_ESR}
- Ripple due to ripple current (ΔI), output capacitance (C_{out}), and switching frequency (f_{PWM}): V_{ripple_Cap}
- Ripple due to switching voltage (V_{sw}), output capacitor equivalent series inductance (ESL), and inductor (L): V_{ripple_ESL}

Each ripple component is calculated by the corresponding equation.

$$V_{ripple\_ESR} = \Delta I \times ESR$$

$$V_{ripple\_Cap} = \frac{\Delta I}{8 \times C_{out} \times f_{PWM}}$$

$$V_{ripple\_ESL} = \frac{V_{sw} \times ESL}{L}$$

$$\Delta I = \frac{(V_{SW} - V_{out}) \times V_{out}}{V_{SW} \times f_{PWM} \times L}$$

Given V_{sw} = 19.2V, V_{out} = 12.09V, f_{PWM} = 370kHz, and L = 3.5µH, the ripple current is ΔI = 3.45A.

With ESR = 0.29mΩ (2mΩ / 7pcs @ 500kHz), C_{out} = 50.4µF (7.2µF × 7pcs @ DC 12V & AC 0.01V), ESL = 0.14nH (1nH / 7pcs), and L = 3.5µH, the ripple voltages are V_{ripple_ESR} = 0.99mV, V_{ripple_Cap} = 23.1mV, and V_{ripple_ESL} = 1.2mV. Because the ripple due to V_{ripple_Cap} is phase-shifted relative to V_{ripple_ESR} and V_{ripple_ESL}, these cannot be simply added; however, since V_{ripple_Cap} is relatively small, a simple sum can be used as a rough estimate of output ripple.

Adjust C_{out}, ESR, and ESL so that V_{ripple} meets the required specification. Also confirm the following:

- Output undershoot/overshoot during load transients is within the specified voltage range
- The allowable ripple current rating of the output capacitors is sufficient
- Component tolerances and aging of the output capacitors are considered

3.9. Surge Voltage Reduction Circuits for Synchronous Rectification MOSFETs

To reduce surge voltage generated across the drain–source of the secondary-side synchronous rectification MOSFETs (Q5-Q8), this design employs a regenerative circuit. Snubber component footprints are provided for optional use if needed.

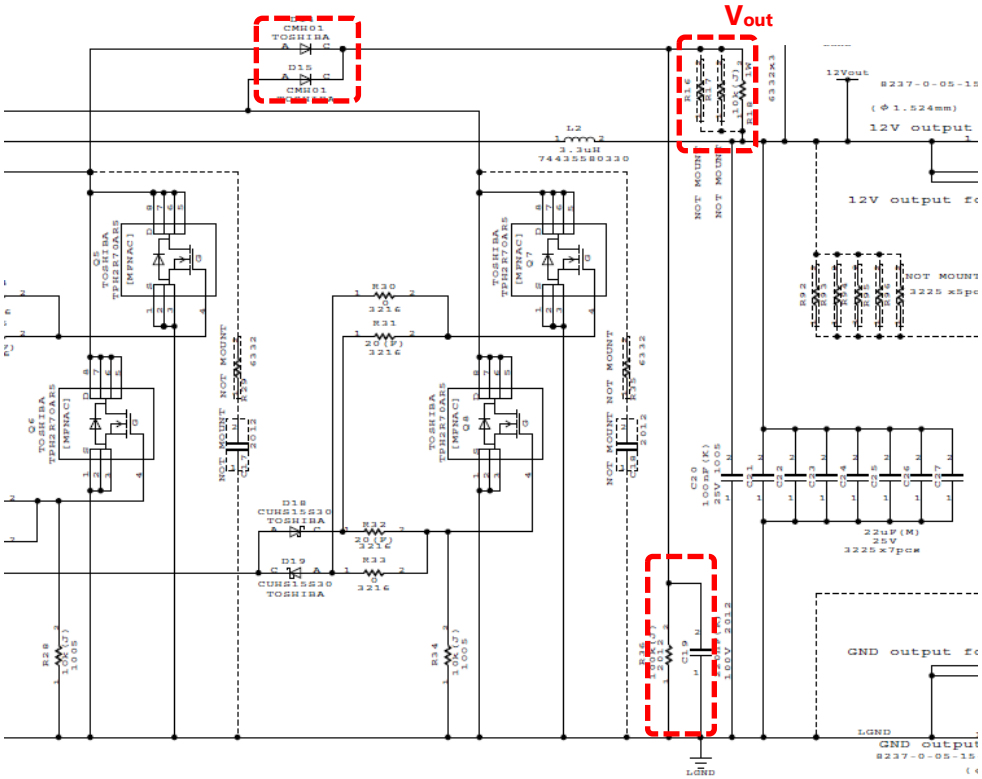

Fig 3.12 Regenerative Circuit

As shown in Fig 3.12, the regenerative circuit is composed of D14, D15, R18, R36, and C19. The surge voltage (V_{srg}) generated on Q5–Q8 is absorbed by C19 and regenerated to the output through R18. The loss generated in resistors R18 (P_{d_Rreg}) is given by the corresponding equation.

$$P_{d\_Rreg} = \frac{(V_{srg} - V_{out})^2}{R18}$$

With V_{out} = 12.09V, V_{srg} = 60V, and R18 = 10kΩ, the power loss P_{d_Rreg} dissipated in each resistor is 230mW. Adjust component values and ratings according to the actual surge voltage level.

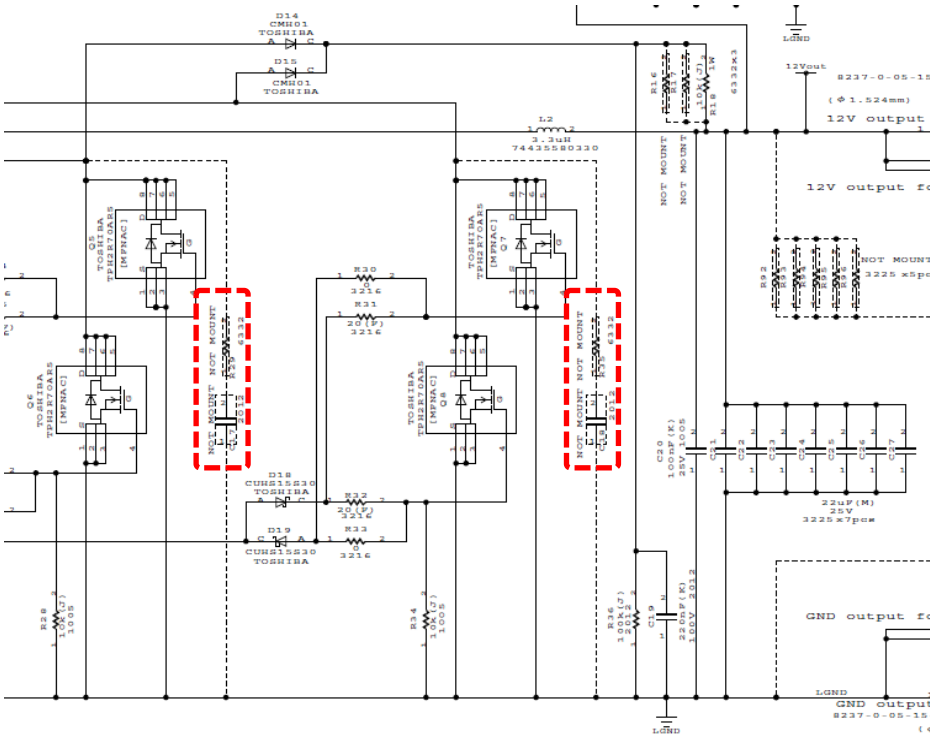

Fig 3.13 Snubber Circuit

This design does not employ a snubber circuit; however, as shown in Fig 3.13, land patterns for snubber circuit components (R29, R35, C17, and C18) are provided.

When a snubber circuit is implemented, appropriate components should be selected according to the actual surge voltage levels.

3.10. Output Overvoltage Detection Circuit

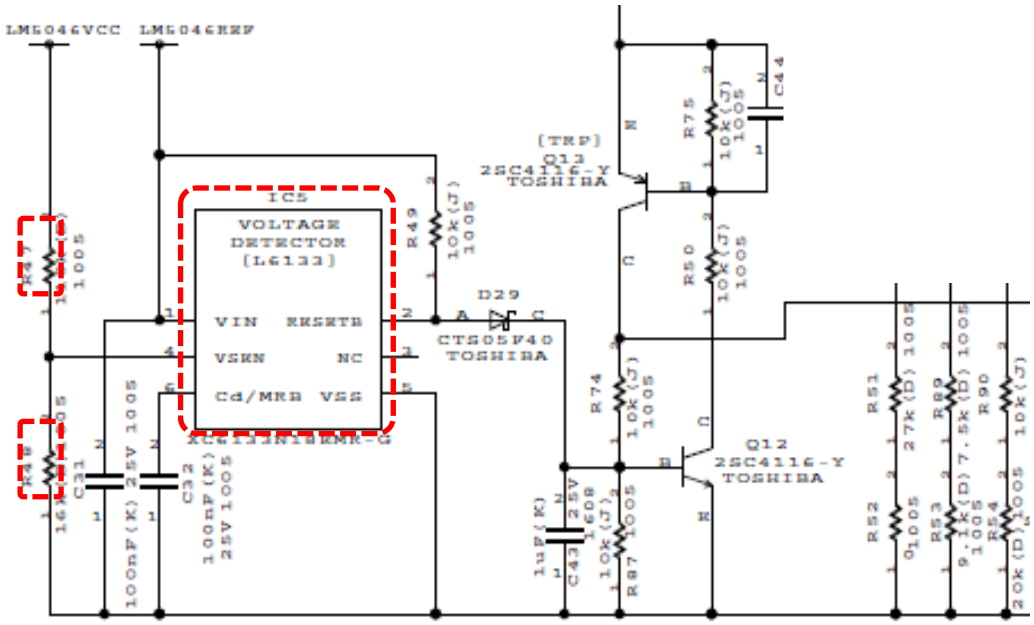

Fig 3.14 Output Overvoltage Detection Circuit

Set the output overvoltage detection value (V_{ovp}) using the detector (XC6133N18EMR-G) detection voltage (V_{det} = 1.8V) and the resistance values of external resistors (R47, R48). Output voltage monitoring is performed indirectly using the auxiliary supply voltage (V_{aux}). When the auxiliary supply voltage reaches V_{ovp}, the detector operates and latches the PSFB PWM controller SS pin low to stop switching. V_{ovp} is calculated by the corresponding equation.

$$V_{ovp} = \frac{(V_{det} + 90mV) \times (R47 + R48)}{R48}$$

In this design, V_{ovp} is set to 14.9V. As shown in Fig 3.14, resistor values are selected as R47 = 110kΩ and R48 = 16kΩ. To resume switching after overvoltage shutdown, one of the following conditions must be satisfied:

- Reset the Enable pin (open it and reconnect to GND)
- Turn off the external regulated DC supply output, then re-apply
-

If direct monitoring of the output voltage is required, implement an overvoltage detection circuit on the output side.

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