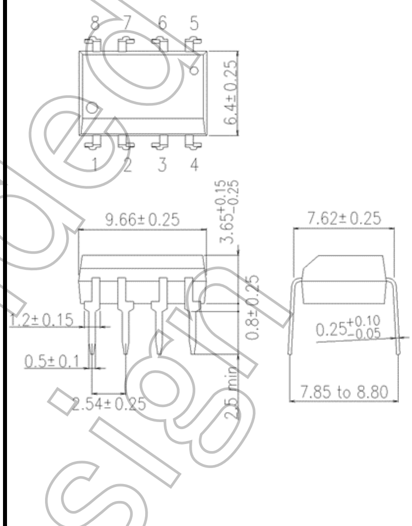
TOSHIBA Photocoupler IRED & Photo−IC

TLP651

Digital Logic Ground Isolation
Line Receiver
Microprocessor System Interfaces
Switching Power Supply Feedback Control
Analog Signal Isolation

Unit: mm



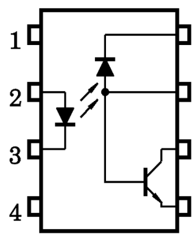
TOSHIBA 11−10C4S

Weight: 0.54 g (typ.)

The TOSHIBA TLP651 consists of a high−output infrared emitting diode and a high speed detector of one chip photo diode−transistor.
This unit is 8−lead DIP.
TLP651 has internal base connection. This base pin should be used for analog application or enable operation. If base pin is open, output signal will be noisy by environmental condition. For this case, TLP650 is suitable.

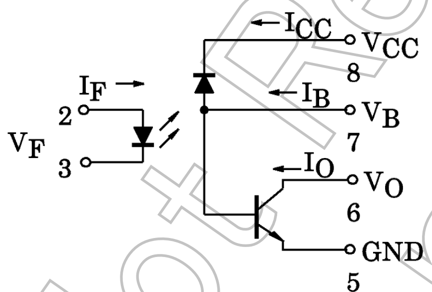
- Isolation voltage: $5000V_{rms}$ (min)
- Switching speed: t_{pHL} = 0.3μs (typ.)
  t_{pLH} = 0.5μs (typ.) (R_L = 1.9kΩ)
- TTL compatible
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A
  File No.E67349

Pin Configuration (top view)



1 : N.C.
2 : ANODE
3 : CATHODE
4 : N.C.
5 : EMITTER
6 : COLLECTOR
7 : BASE
8 : V_{CC}

Schematic



Start of commercial production
1983-12

Absolute Maximum Ratings (Ta = 25°C)

Characteristic			Symbol	Rating	Unit
LED	Forward current	(Note 1)	I_F	25	mA
	Pulse forward current	(Note 2)	I_{FP}	50	mA
	Peak transient forward current	(Note 3)	I_{FPT}	1	A
	Reverse voltage		V_R	5	V
	Diode power dissipation	(Note 4)	P_D	45	mW
Detector	Output current		I_O	8	mA
	Peak output current		I_{OP}	16	mA
	Output voltage		V_O	−0.5 to 15	V
	Supply voltage		V_{CC}	−0.5 to 15	V
	Base current		I_B	5	mA
	Emitter−base reverse voltage		V_{EB}	5	V
	Output power dissipation	(Note 5)	P_O	100	mW
Operating temperature range			T_{opr}	−55 to 100	°C
Storage temperature range			T_{stg}	−55 to 125	°C
Lead solder temperature (10 s)		(Note 6)	T_{sol}	260	°C
Isolation voltage (AC, 60 s, R.H.≤ 60 %)		(Note 7)	BV_S	5000	V_{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

(Note 1) Derate 0.8 mA above 70 °C.

(Note 2) 50 % duty cycle, 1 ms pulse width.
Derate 1.6 mA / °C above 70 °C.

(Note 3) Pulse width ≤ 1 μs, 300 pps.

(Note 4) Derate 0.9 mW / °C above 70 °C.

(Note 5) Derate 2 mW / °C above 70 °C.

(Note 6) Soldering portion of lead: Up to 2 mm from the body of the device.

(Note 7) Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

Electrical Characteristics (Ta = 25°C)

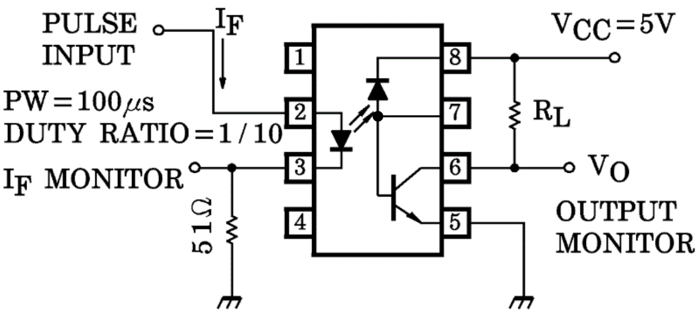
	Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
LED	Forward voltage	V_F	I_F = 16 mA	—	1.65	1.85	V
	Forward voltage temperature coefficient	$\Delta V_F / \Delta Ta$	I_F = 16 mA	—	−2	—	mV / °C
	Reverse current	I_R	V_R = 5 V	—	—	10	μA
	Capacitance between terminal	C_T	V_F = 0 V, f = 1 MHz	—	45	—	pF
Detector	High level output current	$I_{OH\ (1)}$	I_F = 0 mA, V_{CC} = V_O = 5.5 V	—	3	500	nA
		$I_{OH\ (2)}$	I_F = 0 mA, V_{CC} = V_O = 15 V	—	—	5	μA
		I_{OH}	I_F = 0 mA, V_{CC} = V_O = 15 V Ta = 70 °C	—	—	250	μA
	High level supply voltage	I_{CCH}	I_F = 0 mA, V_{CC} = 15 V	—	0.01	1	μA
Coupled	Current transfer ratio	I_O / I_F	I_F = 16 mA, V_{CC} = 4.5 V, V_O = 0.4 V; Ta = 25 °C	10	30	—	%
			Ta = 25 °C, Rank: O	19	30	—	
			Ta = 0 to 70 °C	5	—	—	
			Ta = 0 to 70 °C, Rank: O	15	—	—	
	Low level output voltage	V_{OL}	I_F = 16 mA, V_{CC} = 4.5 V, I_O = 1.1 mA (Rank O: I_O = 2.4 mA)	—	—	0.4	V
	Isolation resistance	R_S	R.H.≤ 60 %, V_S = 500 V_{DC} (Note 7)	5×10^{10}	10^{14}	—	Ω
	Capacitance between input to output	C_S	V_S = 0 V, f = 1 MHz (Note 7)	—	0.8	—	pF

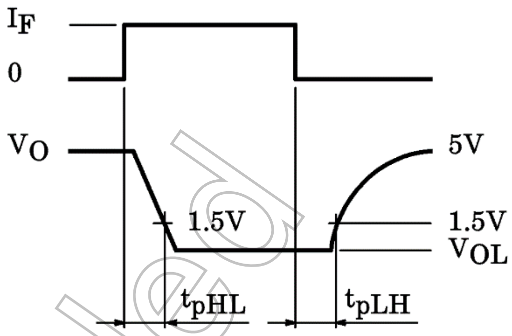
Switching Characteristics (Ta = 25°C, VCC = 5V)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (H→L)	t_{pHL}	1	I_F = 0→16 mA	—	0.2	0.8	μs
			R_L = 4.1 kΩ; Rank O: R_L = 1.9 kΩ	—	0.3	0.8	
Propagation delay time (L→H)	t_{pLH}		I_F = 16→ 0 mA	—	1.0	2.0	μs
			R_L = 4.1 kΩ; Rank O: R_L = 1.9 kΩ	—	0.5	1.2	
Common mode transient immunity at logic high output (Note 8)	CM_H	2	I_F = 0 mA, V_{CM} = 200 V_{p-p} R_L = 4.1 kΩ (Rank O: R_L = 1.9 kΩ)	—	400	—	V / μs
Common mode transient immunity at logic low output (Note 8)	CM_L		I_F =16 mA, V_{CM} = 200 V_{p-p} R_L = 4.1 kΩ (Rank O: R_L = 1.9 kΩ)	—	−1000	—	V / μs

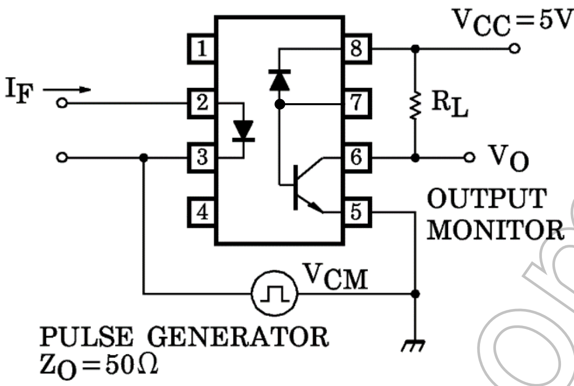
(Note 8) CM_L is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V).
CM_H is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V).

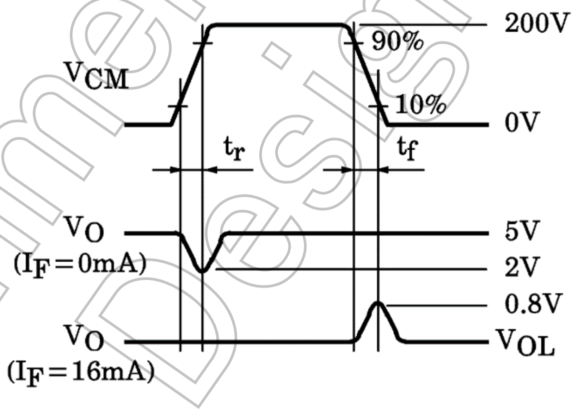
Test Circuit 1: Switching Time Test Circuit



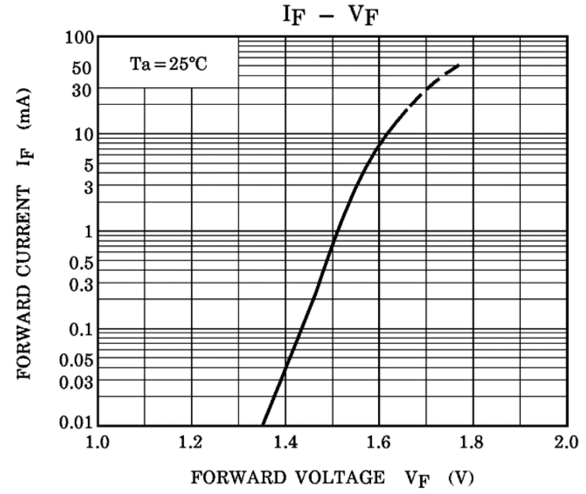


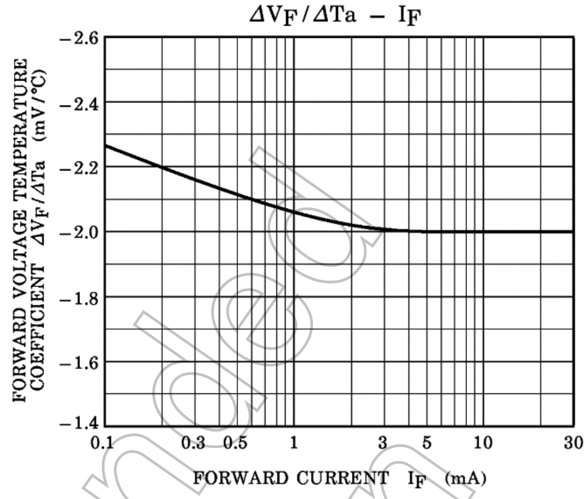
Test Circuit 2: Common Mode Noise Immunity Test Circuit

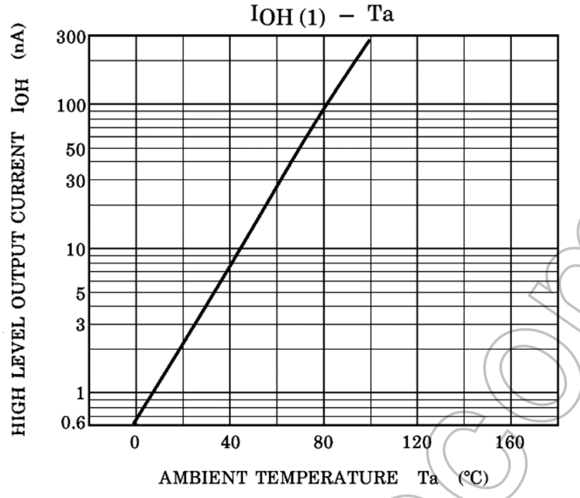


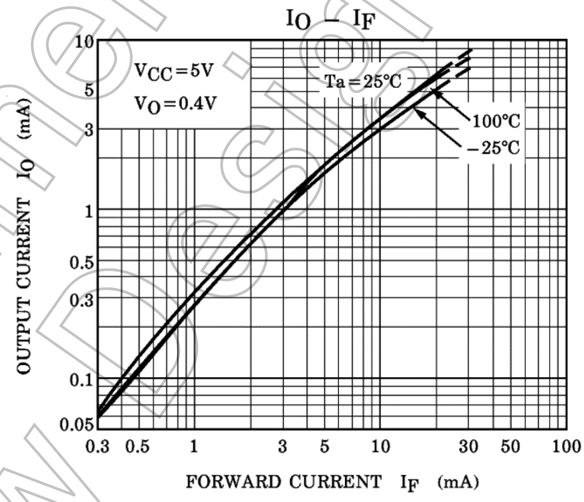


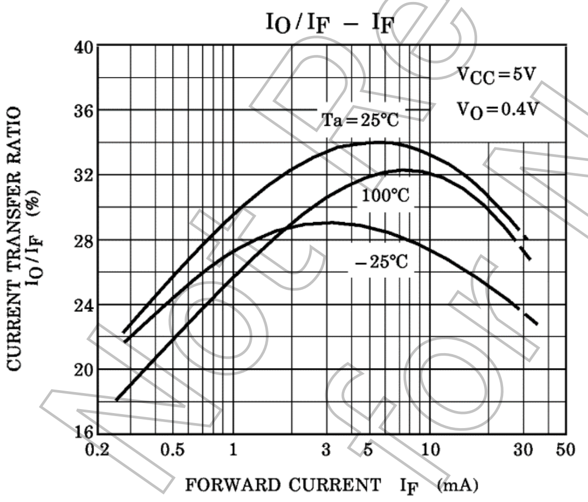
$$CM_H = \frac{160\,(V)}{t_r\,(\mu s)},\ CM_L = \frac{160\,(V)}{t_f\,(\mu s)}$$

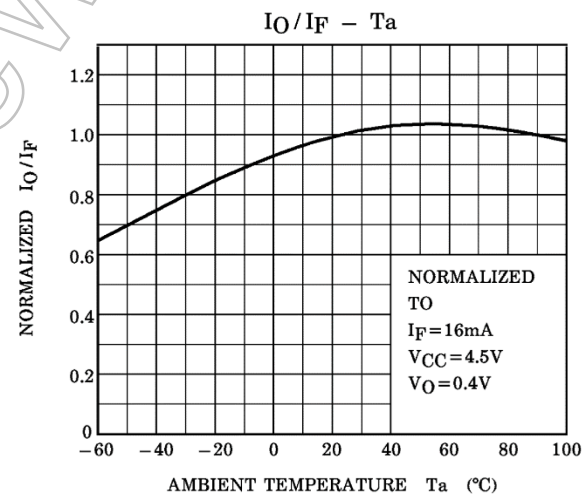




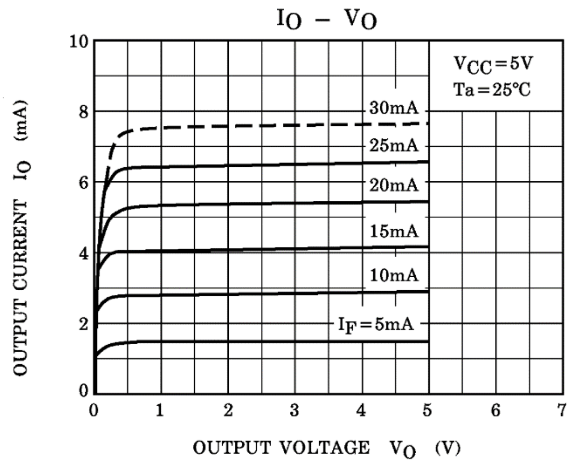


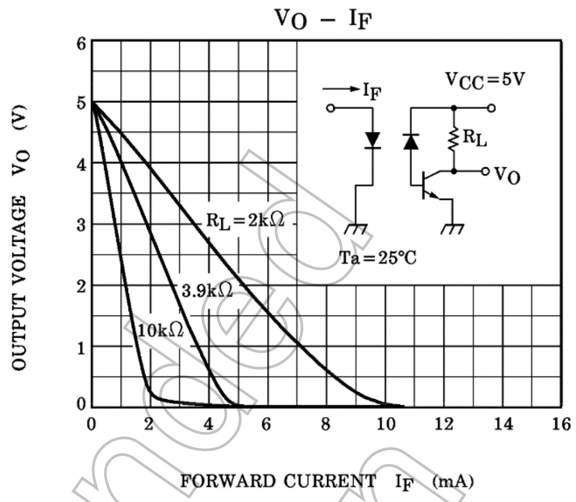


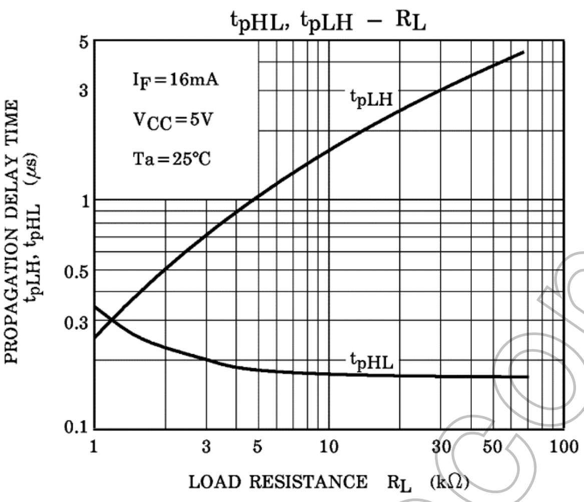




NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.







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