LOW POWER QUAD CHANNEL DIGITAL ISOLATORS

DCL34xx0B

DCL340L0B/DCL340H0B/DCL341L0B/DCL341H0B/DCL342L0B/DCL342H0B

1. Applications

- Industrial automation systems
- Motor control
- Inverter
- Switching power supply

2. Description

DCL340L0B/DCL340H0B/DCL341L0B/DCL341H0B/DCL342L0B/DCL342H0B are low power quad-channel digital isolators. Outstanding performance characteristics are achieved by Toshiba CMOS technology and the magnetic coupling structure. In addition, they comply with UL 1577 and has a 3000V_{rms} rating as an isolation voltage. These products can operate with a temperature range of -40 to 125 °C and a wide supply voltage of 2.25 to 5.5 V.

3. Features

Data rate	: Up to 25 Mbps
Supply voltage	: 2.25 V to 5.5 V
Temperature Range	: -40 °C to 125 °C
Propagation Delay	:33 ns Typ. (5.0 V operation)
Default Output	: High and Low Options
High CMTI(min.)	: ±30 kV/μs
Withstand Voltage	: 3 kV_{rms}
Package	: 16pin SSOP (16LD QSOP)
Safety-Related Certification	: UL1577, CQC, VDE DIN EN 60747-17

UL : UL1577, File No. E519997

cUL : CSA Component Acceptance Service Notice No. 5A

VDE : DIN EN IEC 60747-17 (VDE 0884-17) (Planning)

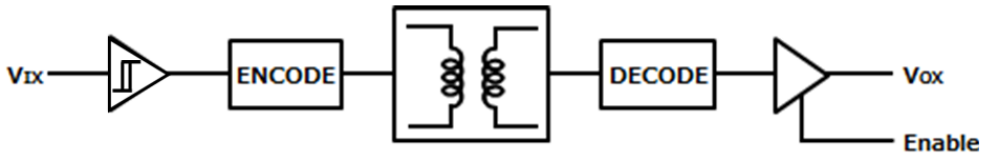
CQC : GB 4943.1-2022 (Planning)

Start of commercial production

2026-04

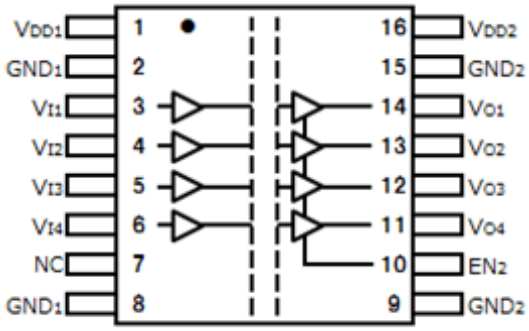
Table of Contents

4. Internal Circuit

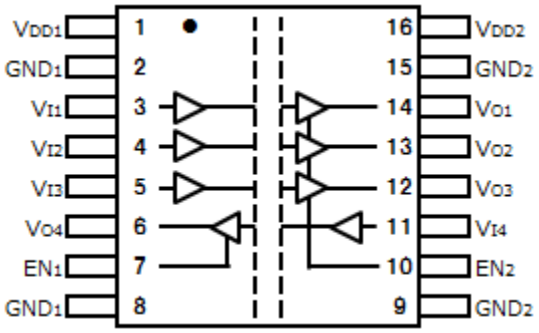


5. Pin configuration and Functions

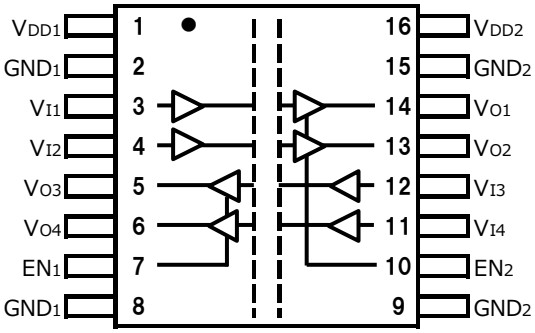
DCL340L0B / DCL340L0B



DCL341L0B / DCL341H0B



DCL342L0B / DCL342H0B



5.1. Pin Functions

PIN				I/O	DESCRIPTION
NAME	DCL340L0B DCL340H0B	DCL341L0B DCL341H0B	DCL342L0B DCL342H0B		
V_{DD1}	1	1	1	-	Power Supply, side 1
GND_1	2,8	2,8	2,8	-	GND connection for V_{DD1} , side 1
V_{I1}	3	3	3	I	Input, Channel1
V_{I2}	4	4	4	I	Input, Channel2
V_{I3}	5	5	12	I	Input, Channel3
V_{I4}	6	11	11	I	Input, Channel4
EN_1	-	7	7	I	Output enable 1. Input pins on side 1 are enabled when EN_1 is high, and in high impedance state when EN_1 is low.
GND_2	9,15	9,15	9,15	-	GND connection for V_{DD2}, side 2
EN_2	10	10	10	I	Output enable 2. Output pins on side 2 are enabled when EN_2 is high, and in high impedance state when EN_2 is low.
V_{o4}	11	6	6	O	Output, Channel4
V_{o3}	12	12	5	O	Output, Channel3
V_{o2}	13	13	13	O	Output, Channel2
V_{o1}	14	14	14	O	Output, Channel1
V_{DD2}	16	16	16	-	Power Supply, side 2
NC	7	-	-	-	Please use NC pin by open.

6. Functional Description

DCL340L0B/DCL340H0B / DCL341L0B/DCL341H0B / DCL342L0B/DCL342H0B

V_{DDI}	V_{DDO}	OUTPUT ENABLE (ENx)	INPUT (V_{IX})	OUTPUT (V_{OX})	DESCRIPTION
PU	PU	H	L	L	Normal Operation
			H	H	
		L	L or H	Z	Output Disable mode
PU	PD	X	L or H	Undetermined	When V_{DDO} is unpowered, a channel output is undetermined.
PD	PU	H	X	Default	Default mode DCL34xL0B=L , DCL34xH0B=H
		L		Z	Output Disable mode
PD	PD	X	X	Undetermined	When V_{DDO} is unpowered, a channel output is undetermined.

PU= Powered up ($V_{DD} \geq 2.25$ V), PD= Powered down ($V_{DD} < 2.25$ V → 0 V), H = High level, L = Low level, X = Don't Care

V_{DDI}, V_{DDO} : Supply voltages on the input and output sides of each channel.

ENx : Output enable signal on the same side as the V_{OX} output.

V_{IX}, V_{OX} : Input and output signals of each channel.

When the input pin (V_{IX}) on the power-off side is set to "H", power is supplied to the device via the ESD circuit, so use is prohibited.

Don't leave the Input pin (V_{IX}) and Enable pin (ENx) on the power ON side open because terminal circuits don't have pull-down resistor or pull-down resistor inside.

7. Absolute Maximum Ratings (Ta = 25 °C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power supply voltage	V_{DD1}, V_{DD2}	-0.5	6.0	V
Input Voltage	V_I	-0.5	V_{DDX}+0.5 (Note1)	V
Output Voltage	V_O	-0.5	V_{DDX}+0.5 (Note1)	V
Output Current	I_O	-15	15	mA
Storage Temperature	T_{stg}	-65	150	°C
Operating Temperature	T_{opr}	-40	125	°C
Soldering Temperature (10 s)	T_{sol}	-	260	°C
Maximum Withstanding Isolation Voltage (1 min.)	BV_S	-	3000	V_{rms}

Note1: Maximum voltage must not exceed 6 V. X = 1 or 2.

8. Recommended Operating Conditions (Note)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power supply voltage	V_{DD1}, V_{DD2}	2.25	5.5	V
Junction Temperature	T_J	-40	150	°C
Operating Temperature	T_{opr}	-40	125	°C

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this data sheet should also be considered.

Note: A ceramic capacitor (0.1 μF) should be connected between pin 1 (V_{DD1}) and pin 2 (GND_1) for V_{DD1} and between pin 16 (V_{DD2}) and pin 15 (GND2) for V_{DD2} and should be the layout on the IC as close as possible (less than 10 mm). Otherwise, the IC may not switch properly.

9. Electrical Characteristics

9.1. Electrical Characteristics – 5 V Supply

All typical specifications are at T_a = 25 °C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operating range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and -40 °C ≤ T_a ≤ 125 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Output Voltage Logic High	V_{IX} = H , I_{OH} = -20 μA	-	V_{OH}	V_{DDO}(Note1)-0.1	V_{DDO}(Note1)	-	V
	V_{IX} = H , I_{OH} = -4 mA			V_{DDO}(Note1)-0.4	V_{DDO}(Note1)-0.2	-	
Output Voltage Logic Low	V_{IX} = L , I_{OL} = 20 μA	-	V_{OL}	-	0.0	0.1	V
	V_{IX} = L , I_{OL} = 4 mA			-	0.2	0.4	
Output impedance	-	-	Z_O	-	50	-	Ω
High-level input voltage	-	-	V_{IH}	0.7*V_{DDI}(Note1)	-	-	V
Low-level input voltage	-	-	VIL	-	-	0.3*V_{DDI}(Note1)	V
Input Voltage Hysteresis	-	-	V_{HYS}	-	0.44	-	V
Input Current	V_I = V_{DDI}(Note1) or 0 V	-	I_I	-	-	±1	μA
SWITCHING SPECIFICATIONS							
Data Rate	-	-	t_{bps}	DC	-	25	Mbps
Pulse Width	-	-	PW	40	-	-	ns
Propagation Delay	50 kHz, Duty = 50 %, t_r = t_f = 2 ns, C_L = 15 pF	Fig. 12-1	t_{PHL}, t_{PLH}	-	33	46	ns
DC～10Mbps							
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$	Fig. 12-1	PWD	-	0.7	8.0	ns
Propagation Delay Skew(Note2) (Between any two units)	-	-	t_{PSK}	-	-	16	ns
Channel Matching	Same Direction	-	t_{skCD}	-	-	5.0	ns
	Opposing Direction	-	t_{skOD}	-	-	7.0	
DC～25Mbps							
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$	Fig. 12-1	PWD	-	0.7	13	ns
Propagation Delay Skew(Note2) (Between any two units)	-	-	t_{PSK}	-	-	21	ns
Channel Matching	Same Direction	-	t_{skCD}	-	-	10	ns
	Opposing Direction	-	t_{skOD}	-	-	12	
Output Rise Time	10 % - 90 %	Fig. 12-1	t_r	-	2.0	-	ns
Output Fall Time	90 % - 10 %	Fig. 12-1	t_f	-	2.0	-	ns
Enable 3-state output enable time(Note3)	50 kHz, Duty = 50 %, t_r = t_f = 2 ns, C_L = 15 pF	Fig. 12-2	t_{PZL}, t_{PZH}	-	-	10	ns
Enable 3-state output disable time		Fig. 12-2	t_{pLZ}, t_{pHZ}	-	-	15	ns
Default output delay time from input power loss	V_{DDI} < 2.25 V → 0 V		t_{DO}	-	-	25	μs
Time from PU(4) to valid output data			t_{PU}	-	-	30	μs
Common mode transient immunity	V_I = V_{DDI} or 0 V , V_{CM} = 400 V , T_a = 25°C	Fig. 12-3	|CMTI|	30	-	-	kV/μs

Note1: V_{DDI} = Input-side V_{DDX} , V_{DDO} = Output-side V_{DDX}

Note2: Propagation delay difference (between parts) is applied under the same operating conditions (power supply voltage. input current, temperature conditions, etc.).

Note3: When ENx signal is changed from Low to High, the output signal (V_{OX}) is valid after the output enable time. The output signal (V_{OX}) within the output enable time is undefined.

Note4: PU = Powered up (V_{DD} ≥ 2.25 V) , After VDD is set powered up, normal operation become valid 30μs later.

9.2. Electrical Characteristics – 3.3 V Supply

All typical specifications are at T_a = 25 °C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operating range of 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and -40 °C ≤ T_a ≤ 125 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Output Voltage Logic High	V_{IX} = H , I_{OH} = -20 μA	-	V_{OH}	V_{DDO}(Note1)-0.1	V_{DDO}(Note1)	-	V
	V_{IX} = H , I_{OH} = -4 mA			V_{DDO}(Note1)-0.4	V_{DDO}(Note1)-0.2	-	
Output Voltage Logic Low	V_{IX} = L , I_{OL} = 20 μA	-	V_{OL}	-	0.0	0.1	V
	V_{IX} = L , I_{OL} = 4 mA			-	0.2	0.4	
Output impedance	-	-	Z_O	-	50	-	Ω
High-level input voltage	-	-	V_{IH}	0.7*V_{DDI}(Note1)	-	-	V
Low-level input voltage	-	-	V_{IL}	-	-	0.3*V_{DDI}(Note1)	V
Input Voltage Hysteresis	-	-	V_{HYS}	-	0.25	-	V
Input Current	V_I = V_{DDI}(Note1) or 0 V	-	I_I	-	-	±1	μA
SWITCHING SPECIFICATIONS							
Data Rate	-	-	t_{bps}	DC	-	25	Mbps
Pulse Width	-	-	PW	40	-	-	ns
Propagation Delay	50 kHz, Duty = 50 %, t_r = t_f = 2 ns, C_L = 15 pF	Fig. 12-1	t_{PHL} , t_{PLH}	-	38	52	ns
DC～10Mbps							
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$	Fig. 12-1	PWD	-	0.7	8.0	ns
Propagation Delay Skew(Note2) (Between any two units)	-	-	t_{PSK}	-	-	19	ns
Channel Matching	Same Direction	-	t_{skCD}	-	-	5.0	ns
	Opposing Direction	-	t_{skOD}	-	-	9.0	
DC～25Mbps							
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$	Fig. 12-1	PWD	-	0.7	13	ns
Propagation Delay Skew(Note2) (Between any two units)	-	-	t_{PSK}	-	-	24	ns
Channel Matching	Same Direction	-	t_{skCD}	-	-	10	ns
	Opposing Direction	-	t_{skOD}	-	-	14	
Output Rise Time	10 % - 90 %	Fig. 12-1	t_r	-	2.0	-	ns
Output Fall Time	90 % - 10 %	Fig. 12-1	t_f	-	2.0	-	ns
Enable 3-state output enable time(Note3)	50 kHz, Duty = 50 %, t_r = t_f = 2 ns, C_L = 15 pF	Fig. 12-2	t_{PZL} , t_{PZH}	-	-	15	ns
Enable 3-state output disable time		Fig. 12-2	t_{pLZ} , t_{pHZ}	-	-	20	ns
Default output delay time from input power loss	V_{DDI} < 2.25 V → 0 V		t_{DO}	-	-	30	μs
Time from PU(Note4) to valid output data			t_{PU}	-	-	30	μs
Common mode transient immunity	V_I = V_{DDI} or 0 V , V_{CM} = 400 V, T_a = 25°C	Fig. 12-3	|CMTI|	30	-	-	kV/μs

Note1: V_{DDI} = Input-side V_{DDX} , V_{DDO} = Output-side V_{DDX}

Note2: Propagation delay difference (between parts) is applied under the same operating conditions (power supply voltage. input current, temperature conditions, etc.).

Note3: When ENx signal is changed from Low to High, the output signal (V_{OX}) is valid after the output enable time. The output signal (V_{OX}) within the output enable time is undefined.

Note4: PU = Powered up (V_{DD} ≥ 2.25 V) , After VDD is set powered up, normal operation become valid 30μs later.

9.3. Electrical Characteristics – 2.5 V Supply

All typical specifications are at T_a = 25 °C, V_{DD1} = V_{DD2} = 2.5 V. Minimum/maximum specifications apply over the entire recommended operating range of 2.25 V ≤ V_{DD1} ≤ 2.75 V, 2.25 V ≤ V_{DD2} ≤ 2.75 V, and -40 °C ≤ T_a ≤ 125 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Output Voltage Logic High	V_{IX} = H , I_{OH} = -20 μA	-	V_{OH}	V_{DDO}(Note1)-0.1	V_{DDO}(Note1)	-	V
	V_{IX} = H , I_{OH} = -4 mA			V_{DDO}(Note1)-0.4	V_{DDO}(Note1)-0.2	-	
Output Voltage Logic Low	V_{IX} = L , I_{OL} = 20 μA	-	V_{OL}	-	0.0	0.1	V
	V_{IX} = L , I_{OL} = 4 mA			-	0.2	0.4	
Output impedance	-	-	Z_O	-	50	-	Ω
High-level input voltage	-	-	V_{IH}	0.7*V_{DDI}(Note1)	-	-	V
Low-level input voltage	-	-	V_{IL}	-	-	0.3*V_{DDI}(Note1)	V
Input Voltage Hysteresis	-	-	V_{HYS}	-	0.22	-	V
Input Current	V_I= V_{DDI}(Note1) or 0 V	-	I_I	-	-	±1	μA
SWITCHING SPECIFICATIONS							
Data Rate	-	-	t_{bps}	DC	-	25	Mbps
Pulse Width	-	-	PW	40	-	-	ns
Propagation Delay	50 kHz, Duty = 50 %, t_r =t_f = 2 ns, C_L = 15 pF	Fig. 12-1	t_{PHL} , t_{PLH}	-	45	63	ns
DC～10Mbps							
Pulse Width Distortion	|t_{PHL} – t_{PLH}|	Fig. 12-1	PWD	-	0.1	8.0	ns
Propagation Delay Skew(Note2) (Between any two units)	-	-	t_{PSK}	-	-	24	ns
Channel Matching	Same Direction	-	t_{skCD}	-	-	7.0	ns
	Opposing Direction	-	t_{skOD}	-	-	11	
DC～25Mbps							
Pulse Width Distortion	|t_{PHL} – t_{PLH}|	Fig. 12-1	PWD	-	0.1	13	ns
Propagation Delay Skew(Note2) (Between any two units)	-	-	t_{PSK}	-	-	29	ns
Channel Matching	Same Direction	-	t_{skCD}	-	-	12	ns
	Opposing Direction	-	t_{skOD}	-	-	16	
Output Rise Time	10 % - 90 %	Fig. 12-1	t_r	-	2.0	-	ns
Output Fall Time	90 % - 10 %	Fig. 12-1	t_f	-	2.0	-	ns
Enable 3-state output enable time(Note3)	50 kHz, Duty = 50 %, t_r = t_f = 2 ns, C_L = 15 pF	Fig. 12-2	t_{PZL} , t_{PZH}	-	-	20	ns
Enable 3-state output disable time		Fig. 12-2	t_{pLZ} , t_{pHZ}	-	-	25	ns
Default output delay time from input power loss	V_{DDI} < 2.25 V → 0 V		t_{DO}	-	-	40	μs
Time from PU(Note4) to valid output data			t_{PU}	-	-	30	μs
Common mode transient immunity	V_I = V_{DDI} or 0 V , V_{CM} = 400 V , T_a = 25 °C	Fig. 12-3	|CMTI|	30	-	-	kV/μs

Note1: V_{DDI} = Input-side V_{DDX} , V_{DDO} = Output-side V_{DDX}

Note2: Propagation delay difference (between parts) is applied under the same operating conditions (power supply voltage. input current, temperature conditions, etc.).

Note3: When ENx signal is changed from Low to High, the output signal (V_{OX}) is valid after the output enable time. The output signal (V_{OX}) within the output enable time is undefined.

Note4: PU = Powered up (V_{DD} ≥ 2.25 V) , After VDD is set powered up, normal operation become valid 30μs later.

9.4. Supply Current Characteristics – 5 V Supply

All typical specifications are at T_a = 25 °C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operating range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and -40 °C ≤ T_a ≤ 125 °C, unless otherwise noted.

(1) DCL340x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	$I_{DD1(Q)}$	-	280	530	μA
		$I_{DD2(Q)}$	-	370	1110	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	415	630	μA
		$I_{DD2(1)}$	-	520	1280	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(1)}$	-	420	630	μA
		$I_{DD2(1)}$	-	680	1440	μA
25 Mbps	f_{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(25)}$	-	9.3	13.2	mA
		$I_{DD2(25)}$	-	8.1	10.6	mA

(2) DCL341x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	$I_{DD1(Q)}$	-	305	645	μA
		$I_{DD2(Q)}$	-	340	940	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	440	790	μA
		$I_{DD2(1)}$	-	495	1105	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(1)}$	-	490	845	μA
		$I_{DD2(1)}$	-	625	1240	μA
25 Mbps	f_{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(25)}$	-	9.1	12.7	mA
		$I_{DD2(25)}$	-	8.8	11.4	mA

(3) DCL342x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	$I_{DD1(Q)}$	-	330	795	μA
		$I_{DD2(Q)}$	-	310	780	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	465	935	μA
		$I_{DD2(1)}$	-	465	935	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(1)}$	-	560	1030	μA
		$I_{DD2(1)}$	-	560	1030	μA
25 Mbps	f_{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(25)}$	-	9.0	12.1	mA
		$I_{DD2(25)}$	-	9.0	12.1	mA

9.5. Supply Current Characteristics – 3.3 V Supply

All typical specifications are at T_a = 25 °C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operating range of 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and -40 °C ≤ T_a ≤ 125 °C, unless otherwise noted.

(1) DCL340x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	$I_{DD1(Q)}$	-	210	395	μA
		$I_{DD2(Q)}$	-	290	890	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	295	460	μA
		$I_{DD2(1)}$	-	385	995	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(1)}$	-	300	460	μA
		$I_{DD2(1)}$	-	495	1130	μA
25 Mbps	f_{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(25)}$	-	6.7	10.5	mA
		$I_{DD2(25)}$	-	5.4	7.3	mA

(2) DCL341x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	$I_{DD1(Q)}$	-	235	505	μA
		$I_{DD2(Q)}$	-	260	745	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	320	580	μA
		$I_{DD2(1)}$	-	360	845	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(1)}$	-	350	620	μA
		$I_{DD2(1)}$	-	445	950	μA
25 Mbps	f_{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(25)}$	-	6.5	9.6	mA
		$I_{DD2(25)}$	-	5.8	7.8	mA

(3) DCL342x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	$I_{DD1(Q)}$	-	250	620	μA
		$I_{DD2(Q)}$	-	240	610	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	340	710	μA
		$I_{DD2(1)}$	-	340	710	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(1)}$	-	395	780	μA
		$I_{DD2(1)}$	-	395	780	μA
25 Mbps	f_{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(25)}$	-	6.1	8.6	mA
		$I_{DD2(25)}$	-	6.1	8.6	mA

9.6. Supply Current Characteristics – 2.5 V Supply

All typical specifications are at T_a = 25 °C, V_{DD1} = V_{DD2} = 2.5 V. Minimum/maximum specifications apply over the entire recommended operating range of 2.25 V ≤ V_{DD1} ≤ 2.75 V, 2.25 V ≤ V_{DD2} ≤ 2.75 V, and -40 °C ≤ T_a ≤ 125 °C, unless otherwise noted

(1) DCL340x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	$I_{DD1(Q)}$	-	190	355	μA
		$I_{DD2(Q)}$	-	260	825	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	270	405	μA
		$I_{DD2(1)}$	-	330	905	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(1)}$	-	270	405	μA
		$I_{DD2(1)}$	-	415	1010	μA
25 Mbps	f_{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(25)}$	-	6.4	9.7	mA
		$I_{DD2(25)}$	-	4.3	6.3	mA

(2) DCL341x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	$I_{DD1(Q)}$	-	210	455	μA
		$I_{DD2(Q)}$	-	240	690	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	280	520	μA
		$I_{DD2(1)}$	-	310	765	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(1)}$	-	305	545	μA
		$I_{DD2(1)}$	-	375	845	μA
25 Mbps	f_{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(25)}$	-	5.7	8.4	mA
		$I_{DD2(25)}$	-	4.6	6.3	mA

(3) DCL342x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	$I_{DD1(Q)}$	-	230	570	μA
		$I_{DD2(Q)}$	-	220	570	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	290	635	μA
		$I_{DD2(1)}$	-	290	635	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(1)}$	-	335	690	μA
		$I_{DD2(1)}$	-	335	690	μA
25 Mbps	f_{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(25)}$	-	5.2	7.3	mA
		$I_{DD2(25)}$	-	5.2	7.3	mA

10. Insulation Specifications

PARAMETER	Symbol	TEST CONDITIONS	VALUE	UNIT
Minimum External Clearance	CLR	Shortest terminal-to-terminal distance through air	3.7	mm
Minimum External Creepage	CPG	Shortest terminal-to-terminal distance across the package surface	3.4	mm
Distance Through The Insulation	DTI	Minimum internal gap	8.5	μm
Comparative Tracking Index	CTI		400	V
Material Group	-	According to IEC 60664-1	II	-
Overvoltage Category Per IEC 60664-1	-	Rated main voltage ≤ 300 V_{RMS}	I-III	-
DIN EN IEC 60747-17; (VDE 0884-17)				
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	AC voltage (bipolar)	566	V_{PK}
Maximum Transient Isolation Voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification) , V_{TEST}= 1.2 x V_{IOTM}, t = 1 s (100 % production)	4243	V_{PK}
Maximum Impulse Voltage	V_{IMP}	IEC 62368-1 1.2/50 μs waveform	4000	V_{PK}
Maximum surge isolation voltage	V_{IOSM}	Test method per IEC 61000-4-5, 1.2/50 μs waveform, V_{IOSM} ≥ 1.3 × V_{IMP} (qualification)	5200	V_{PK}
Apparent charge measuring voltage	$V_{pd(m)}$	Method A, After Input/Output safety test subgroup2&3, $V_{ini,a}$ = V_{IOTM}, $V_{pd(m)}$ = 1.2 x V_{IORM} t_{ini} = 60 s, t_m = 10 s, partial discharge < 5 pC	680	V_{PK}
		Method A, After environmental tests subgroup 1, $V_{ini,a}$ = V_{IOTM}, $V_{pd(m)}$ = 1.3 x V_{IORM} t_{ini} = 60 s, t_m = 10 s, partial discharge < 5 pC	736	
		Method B1; At routine test (100 % production) and preconditioning (type test) $V_{ini,b}$ ≥ 1.2 x V_{IOTM}, $V_{pd(m)}$ = 1.5 x V_{IORM} $t_{ini,b}$ = 1 s, t_m = 1 s partial discharge < 5 pC	849	
Barrier capacitance, input to output	C_{IO}	f = 1 MHz	1.7	pF
DCL340x0B				
Input Capacitance	C_I	input : V_{I1}～V_{I3}	1.8	pF
		input : V_{I4}	2.3	pF
DCL341x0B				
Input Capacitance	C_I	input : V_{I1}～V_{I3}	1.8	pF
		input : V_{I4}	4.2	pF
DCL342x0B				
Input Capacitance	C_I	input : V_{I1},V_{I2}	1.8	pF
		input : V_{I3}	3.6	pF
		input : V_{I4}	4.2	pF
Isolation Resistance	R_{IO}	V_{IO} = 500 V, T_A = 25 °C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100 °C ≤ T_A ≤ 125 °C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150 °C	$>10^{9}$	
Pollution Degree	-	-	2	-
Climatic Category	-	-	40/125/21	-
UL 1577				
Maximum Withstanding Isolation Voltage	V_{ISO}	V_{TEST} = V_{ISO} , t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO} , t = 1 s (100 % production)	3000	V_{rms}

11. Safety Limiting Values

PARAMETER	Symbol	TEST CONDITIONS	Value	Unit
Safety Input, Output or Supply Current	I_S	V_{DD1} = V_{DD2} = 5.5 V, Tj = 150 ℃, Ta = 25 ℃	287	mA
		V_{DD1} = V_{DD2} = 3.6 V, Tj = 150 ℃, Ta = 25 ℃	439	mA
		V_{DD1} = V_{DD2} = 2.75 V, Tj = 150 ℃, Ta = 25 ℃	575	mA
Safety Input, Output or Total Power	P_S	Tj = 150℃, Ta = 25℃	1580	W
Maximum Safety Temperature	T_S	-	150	°C

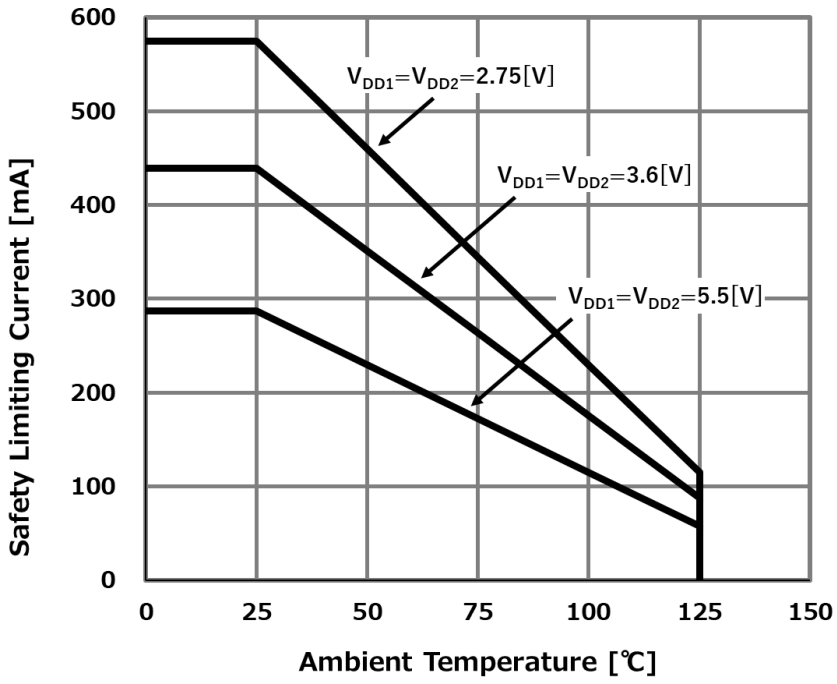


Fig. 11.1 Thermal Derating Curve for Safety Limiting Current-Ta

12. Test Circuit

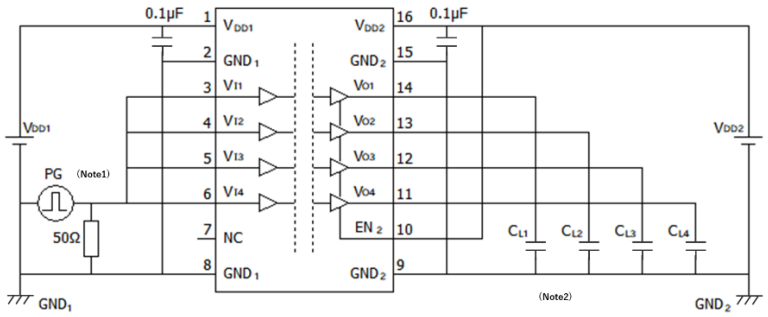


Fig. 12-1-1: DCL340L0B/DCL340H0B Switching Test Circuit

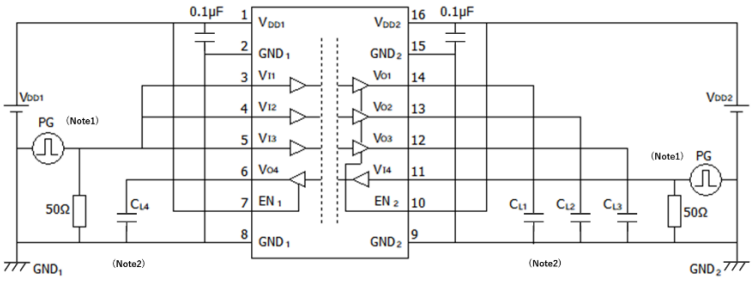


Fig. 12-1-2: DCL341L0B/DCL341H0B Switching Test Circuit

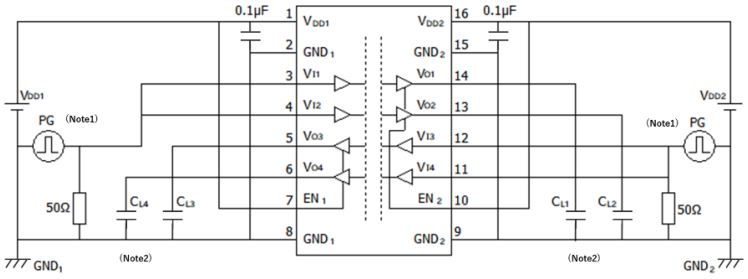


Fig. 12-1-3: DCL342L0B/DCL342H0B Switching Test Circuit

Note1: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50 % duty cycle, tr ≤ 2 ns, tf ≤ 2 ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is needed not in actual application.

Note2: C_{LX} = 15 pF includes instrumentation and fixture capacitance.

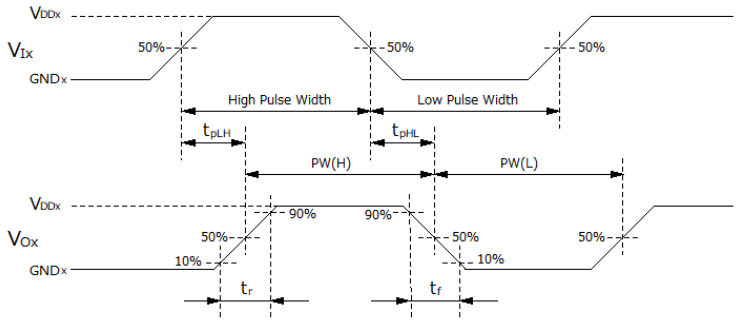


Fig. 12-1-4: DCL34xx0B Switching Waveforms

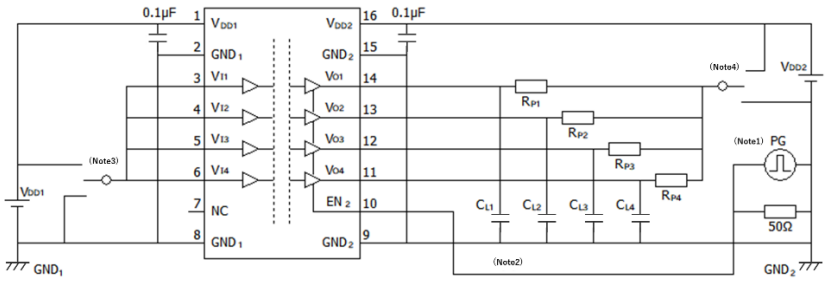


Fig. 12-2-1: DCL340L0B/DCL340H0B Enable Propagation Delay Time Test Circuit

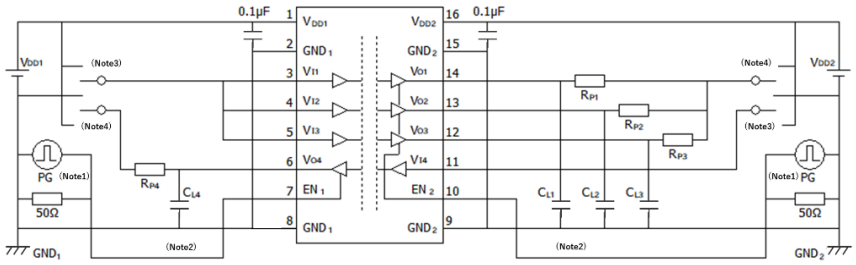


Fig. 12-2-2: DCL341L0B/DCL341H0B Enable Propagation Delay Time Test Circuit

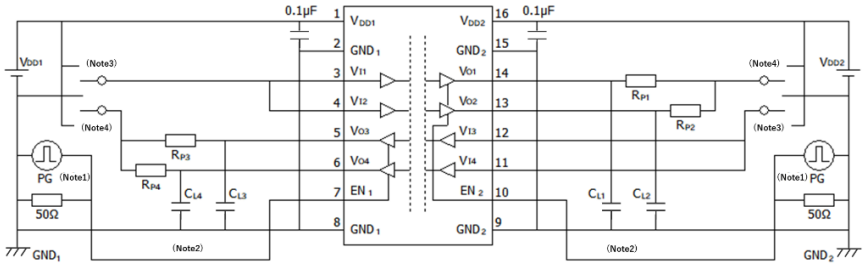


Fig. 12-2-3: DCL342L0B/DCL342H0B Enable Propagation Delay Time Test Circuit

Note1: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50 % duty cycle, tr ≤ 2 ns, tf ≤ 2 ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is needed not in actual application.

Note2: C_{LX} = 15 pF includes instrumentation and fixture capacitance.

Note3: GND for t_{PZL}, t_{PLZ}, V_{DD} for t_{PZH}, t_{PHZ}

Note4: V_{DD} for t_{PZL}, t_{PLZ}, GND for t_{PZH}, t_{PHZ}.

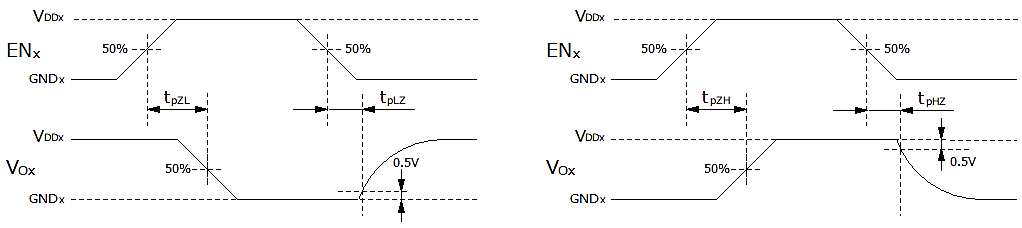


Fig. 12-2-4: DCL34xL0B/DCL34xH0B Enable Propagation Delay Time Waveforms

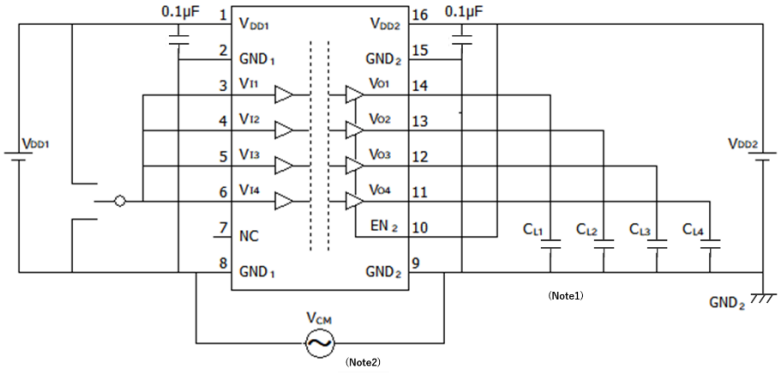


Fig. 12-3-1: DCL340L0B/DCL340H0B Common-Mode Transient Immunity Test Circuit

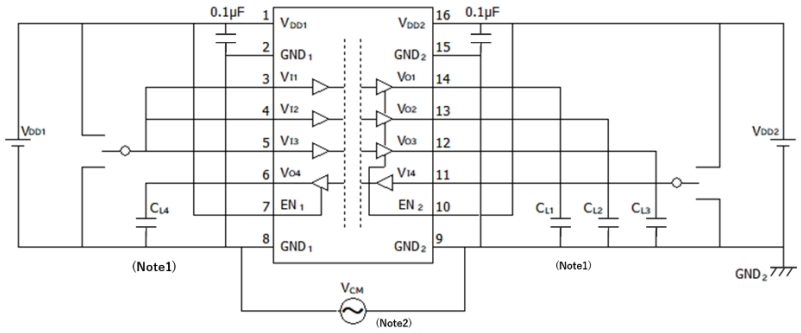


Fig. 12-3-2: DCL341L0B/DCL341H0B Common-Mode Transient Immunity Test Circuit

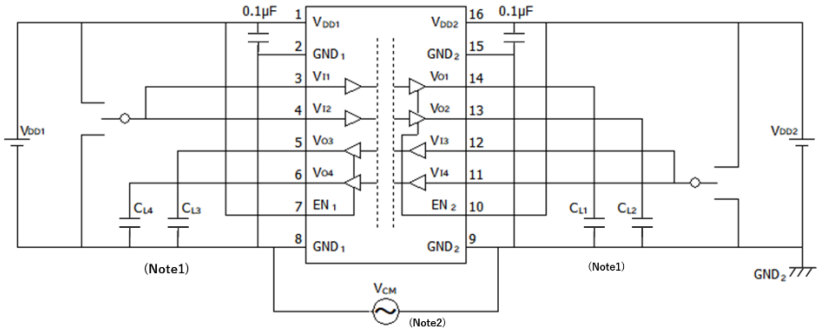


Fig. 12-3-3: DCL342L0B/DCL342H0B Common-Mode Transient Immunity Test Circuit

Note1: C_{LX} = 15 pF includes instrumentation and fixture capacitance.

Note2: Apply V_{CM} with reference to the GND terminal on the output terminal side of the IC. The GND on the IC input terminal side is isolated from the output terminal side. Depending on which channel is being measured, V_{CM} may be applied with reference to GND_1 or with reference to GND_2.

13. Characteristics Curves (Note)

Note: The following characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

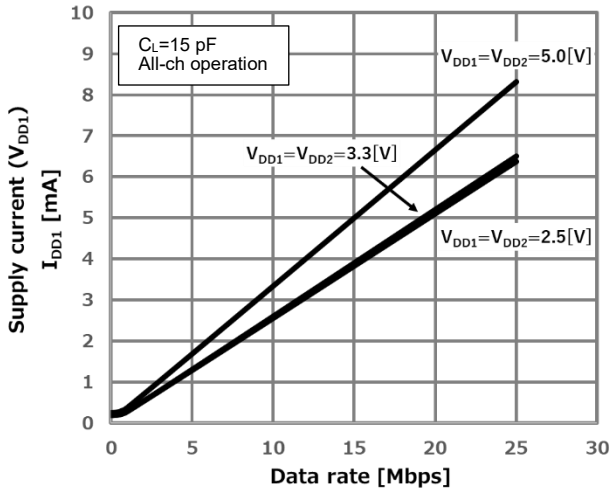


Fig.13.1. DCL340x0B I_{DD1} Supply Current - Data rate

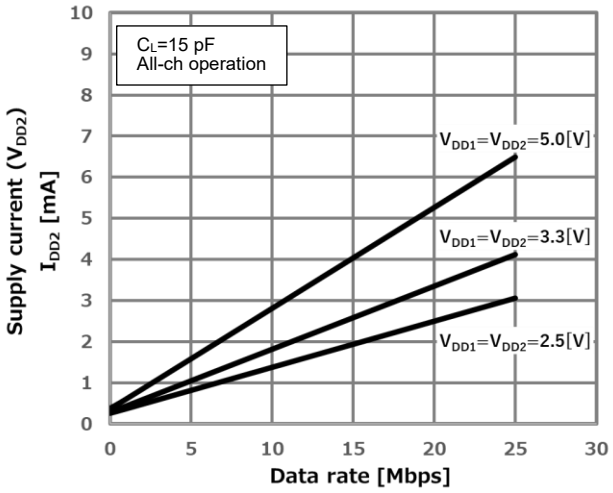


Fig.13.2. DCL340x0B I_{DD2} Supply Current - Data rate

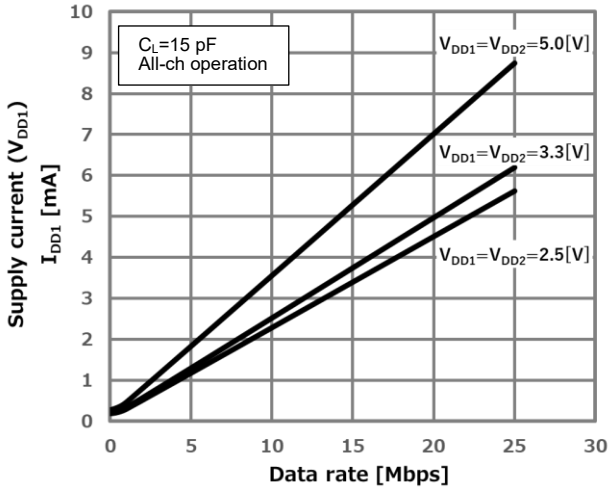


Fig.13.3. DCL341x0B I_{DD1} Supply Current - Data rate

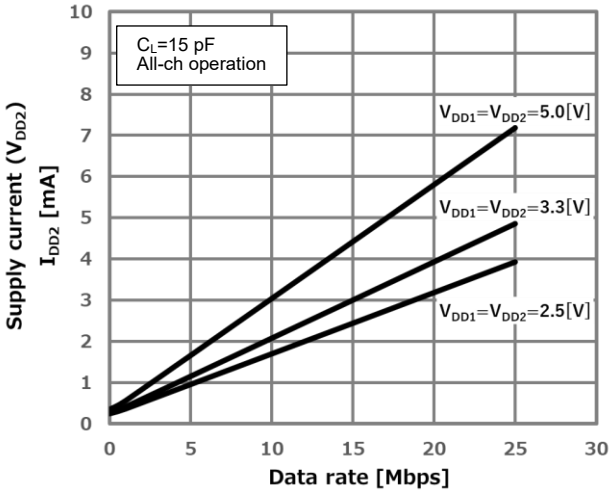


Fig.13.4. DCL341x0B I_{DD2} Supply Current - Data rate

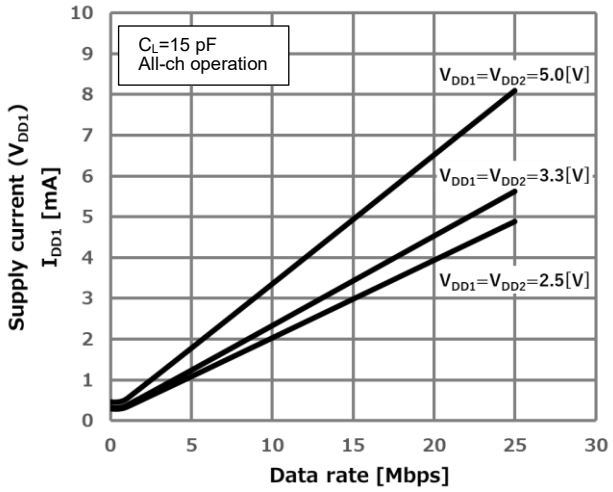


Fig.13.5. DCL342x0B I_{DD1} Supply Current - Data rate

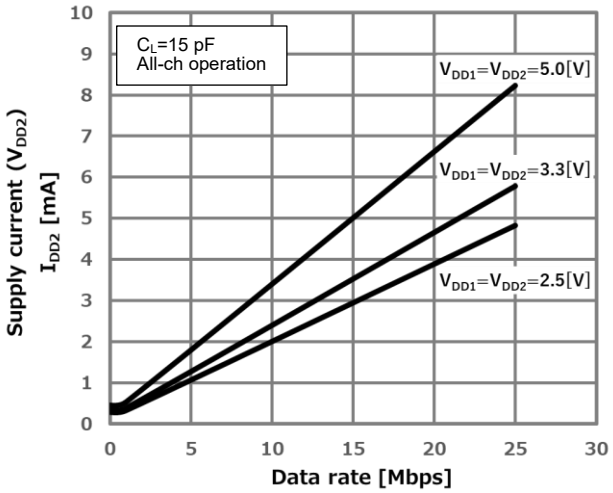


Fig.13.6. DCL342x0B I_{DD2} Supply Current - Data rate

Note: The following characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

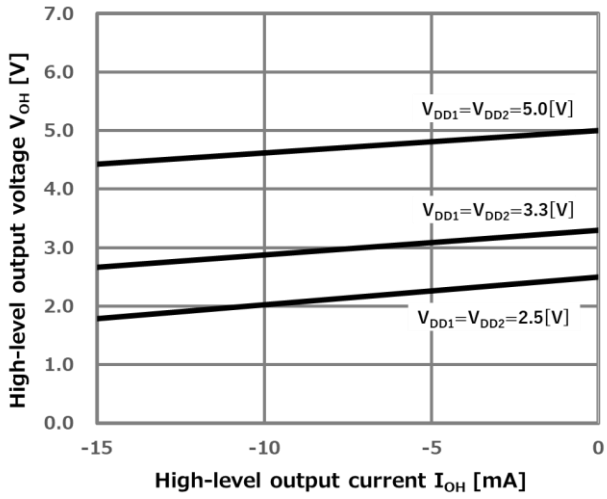


Fig.13.3. VOH—IOH

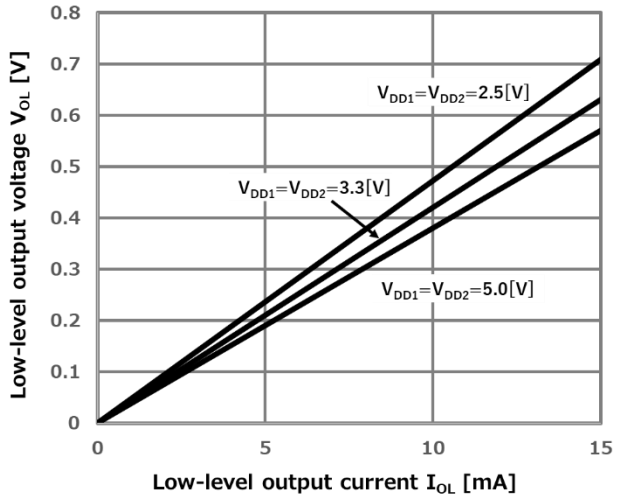


Fig.13.4. VOL—IOL

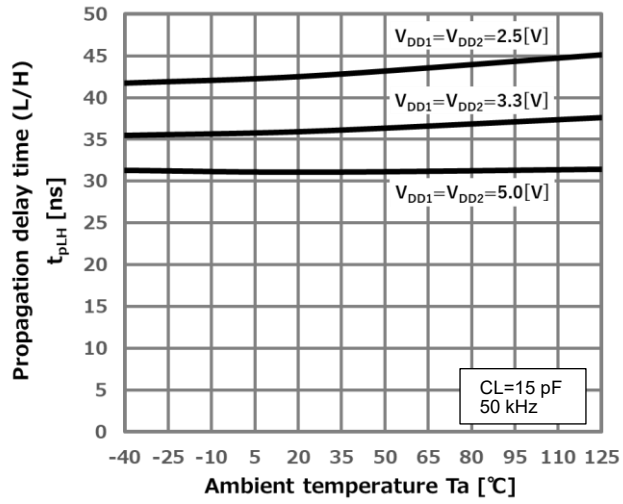


Fig.13.5. Propagation Delay Time t_{PHL}—Ta

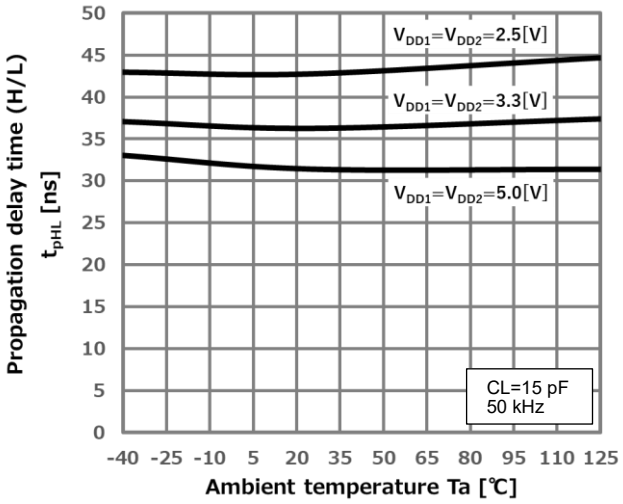
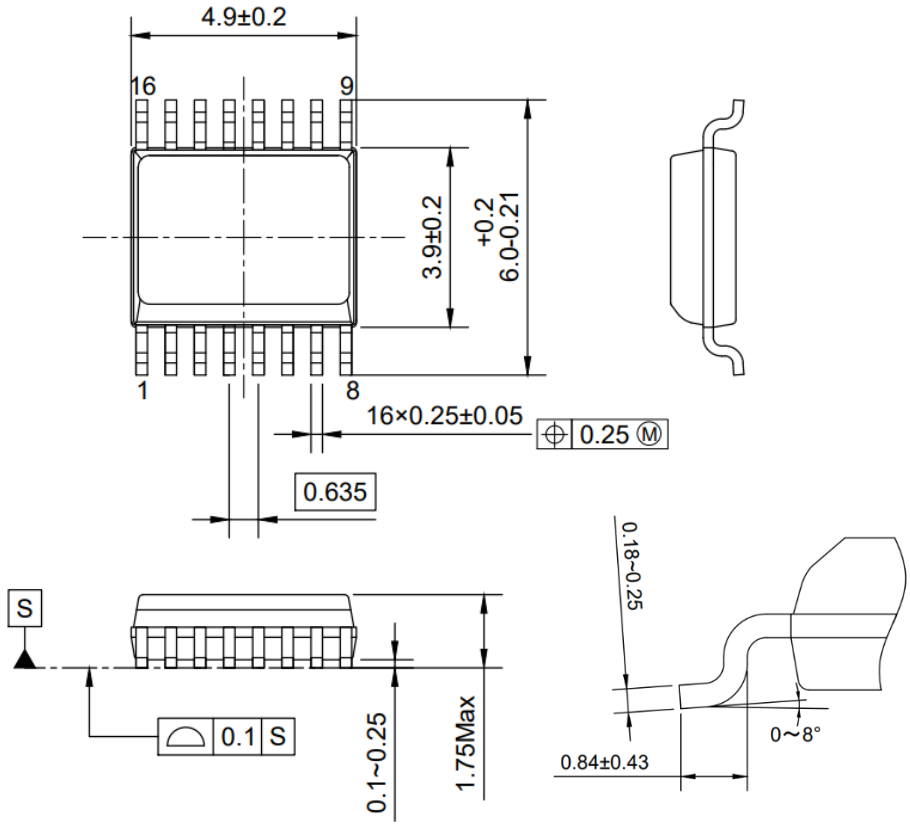


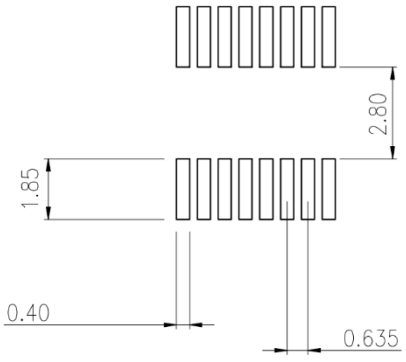
Fig.13.6. Propagation Delay Time t_{PLH}—Ta

14. Package Information

Package Name	SSOP16 (P-SSOP16-0405-0.64-001)
Implementation category	Surface Mount
Pin Number	16
Package Dimension Width × Length × Height (mm)	3.9 (Typ.) x 4.9 (Typ.) x 1.75 (Max)
Package Dimension(mm) / Land Pattern Example (mm)	Package Dimension



Land Pattern Dimensions (for reference only)



Notes : Land Pattern Dimensions

- All linear dimensions are given in millimeters unless otherwise specified.
- This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only. TOSHIBA is not responsible for any incorrect or incomplete drawings and information.
- You are solely responsible for all aspects of your own land pattern, including but not limited to soldering processes.
- The drawing shown may not accurately represent the actual shape or dimensions.
- Before creating and producing designs and using, customers must also refer to and comply with the latest versions of all relevant TOSHIBA information and the instructions for the application that Product will be used with or for.

15. Ordering guide

Model	V_{DD1} end Number of inputs	V_{DD2} end Number of inputs	Default Output	Data rate [Mbps]	Control signal	Temperature range [°C]	Package
DCL340L0B	4	0	L	25	Output Enable	-40~125	SSOP16
DCL340H0B	4	0	H	25	Output Enable	-40~125	SSOP16
DCL341L0B	3	1	L	25	Output Enable	-40~125	SSOP16
DCL341H0B	3	1	H	25	Output Enable	-40~125	SSOP16
DCL342L0B	2	2	L	25	Output Enable	-40~125	SSOP16
DCL342H0B	2	2	H	25	Output Enable	-40~125	SSOP16

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, Class 3 medical devices, equipment used for automobiles, and military vehicles and munitions. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**