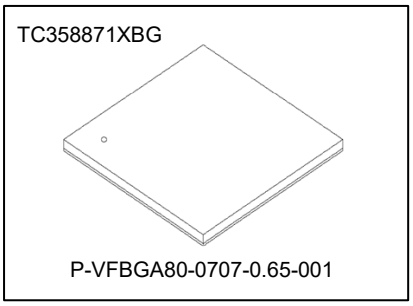
CMOS Digital Integrated Circuit Silicon Monolithic

TC358871XBG

Mobile Peripheral Devices



Weight: 67 mg (typ.)

Overview

TC358871XBG, Ultra HD to DSI, bridge converts high resolution HDMI® stream to MIPI® DSI® Tx video. The HDMI-RX runs at 297 MHz to carry up to 7.2 Gbps video stream. It requires dual link MIPI DSI Tx, 1 Gbps/data lane, to transmit out a maximum 7.2 Gbps video data.

The bridge chip is necessary for current and next generation Application Processors to drive a (dual) DSI link display by using its HDMI Tx output port.

Features

- **HDMI-RX Interface**
  - HDMI-RX
    - Video Formats Support (Up to 4K×2K / 30fps), maximum 24 bps (bit-per-pixel) no deep color support
      - RGB, YCbCr444: 24-bpp

      YCbCr422: 24-bpp
    - Color Conversion

      4:2:2 to 4:4:4 is supported

      4:4:4: to 4:2:2 is supported

      RGB888 to YCbCr (4:4:4 / 4:2:2) is supported

      YCbCr (4:4:4 / 4:2:2) to RGB888/666 is supported
      - Note: for RGB666 (R=R[5:0],2'b00, G=G[5:0],2'b00, B=G[5:0],2'b00)
    - Maximum HDMI clock speed: 297 MHz
    - Audio Supports

      Internal Audio PLL to track N/CTS value transmitted by the ACR packet.
    - 3D Support
    - Support HDCP®1.4 decryptions (optional)
    - EDID Support, Release A, Revision 1 (Feb 9, 2000)

      First 128 byte (EDID 1.3 structure)

      First E-EDID Extension: 128 bytes of CEA Extension version 3 (specified in CEA-861-D)

      Embedded 1K-byte SRAM (EDID_SRAM)
  - Does not support Audio Return Path and HDMI Ethernet Channels

- **DSI TX Interface**
  - MIPI DSI compliant
  - Dual links DSI (DSI0 and DSI1), each link supports 4 data lanes @1 Gbps/ data lane
    - DSI0 carries the left half data of HDMI Rx video stream and DSI1 carries the right one at the default configuration.
    - Left or right data can be assigned/programmed to either DSI Tx link
    - The maximum length of each half is limited to 2048-pixel plus up to full length overlap, DSI0 data length could be different from that of DSI1's
    - The maximum Hsync skew between DSI0 and DSI1 can be less than 10 ByteClk
  - Single link DSI, maximum horizontal pixel width
    - 2558 pixels (24-bit per pixel)
    - 3411 pixels (16-bit per pixel)
  - Supports video data formats
    - RGB666, RGB888, YCbCr444, YCbCr 422 16-bit and YCbCr 422 24-bit
    - YCbCr inputs can be converted into RGB before outputting

- **I²C Interface**
  - Support for normal (100 kHz), fast mode (400 kHz) and ultrafast mode (2 MHz)
  - Target Mode
    - To be used by an external Controller to configure all TC358871XBG internal registers, including EDID_SRAM and panel control
    - Support 2 I²C Target Addresses (0x0F & 0x1F) selected through boot-strap pin (INT)

- **Audio Output Interface**
  - Up to four I²S data lines for supporting multi-Channel audio data (5.1 and 7.1)
  - Maximum audio sample frequency supported is 192 kHz @8 CH
  - Support 16, 18, 20 or 24-bit data (depend on HDMI input stream)
  - Support Controller Clock output only
  - Support 32 bit-wide time-slot only
  - Output Audio Over Sampling clock (256fs)
  - Either I²S or TDM Audio interface available (pins are multiplexed)
  - I²S Audio Interface
    - Support Left or Right-justify with MSB first
  - TDM (Time Division Multiplexed) Audio

Interface
  - Fixed to 8 channels (depend on HDMI input stream)
- Digital Audio Interface
  - Supports HBR audio stream split across 4 I^2S lines if bandwidth higher than 12 MHz

- **InfraRed (IR)**
  - Support NEC InfraRed protocol.

- **Power supply inputs**
  - Core: 1.15 V
  - MIPI D-PHY^{SM}: 1.2 V
  - I/O: 1.8 V, 3.3 V
  - HDMI-RX: 3.3 V
  - APLL: 3.3 V

- **Power Consumption during typical operations**
  - 1920×1080 @60 fps: 420 mW (Dual D-PHY link)
  - 2560×1600 @60 fps: 504 mW (Dual D-PHY link)
  - 3840×2160 @30 fps: 520 mW (Dual D-PHY link)

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REFERENCES

1. MIPI D-PHY, “MIPI_D-PHY_specification_v01-00-00, May 14, 2009”
2. MIPI DSI, “MIPI Alliance Specification for Display Serial Interface (DSI) Version 1.1 Revision 22 Nov 2011”
3. HDMI, “High-Definition Multimedia Interface Specification Version 1.4b October 11, 2011”
4. I^2C bus specification, version 2.1, January 2000, Philips Semiconductor

1. Overview

TC358871XBG, Ultra HD to DSI, bridge converts high resolution HDMI stream to MIPI® DSI Tx video.

The HDMI-RX runs at 297 MHz to carry up to 7.2 Gbps video stream. It requires dual link MIPI DSI Tx, 1 Gbps/data lane, to transmit out a maximum 7.2 Gbps video data.

The bridge chip is necessary for current and next generation Application Processors to drive a (dual) DSI link display directly via its HDMI Tx output port.

TC358871XBG system view block diagrams is shown in Figure 1.1.

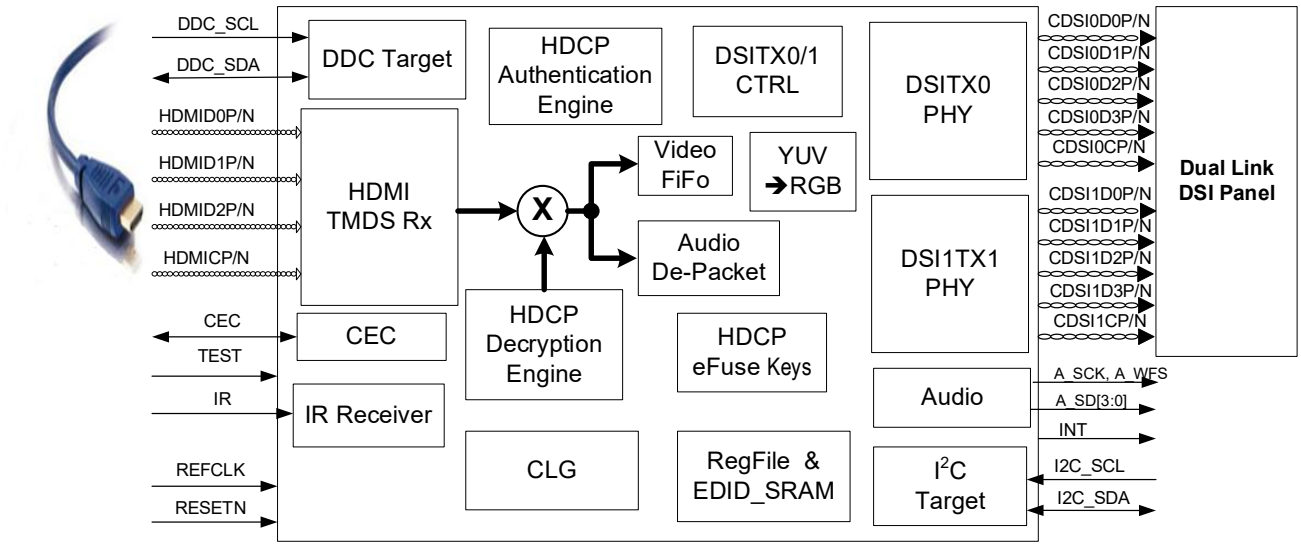


Figure 1.1 TC358871XBG System Overview

2. External Pins

TC358871XBG resides in BGA80 pin packages. The following table gives the signals of TC358871XBG and their function.

Table 2.1 TC358871XBG Functional Signal List

Group	Pin Name	Ball	I/O	Init (O)	Type (Note 1)	Function	Voltage Supply
SYSTEM (4)	RESETN	K8	I	-	Sch	System reset input (active low)	VDDIO18
	REFCLK	K9	I	-	Sch	Reference clock input (40 to 50 MHz)	VDDIO18
	TEST	G5	I	-	N	Internal test terminal (Always must be fixed low externally)	VDDIO18
	INT	J3	O	L	N	Interrupt Output signal (active high) (Note 2)	VDDIO18
CDSI TX0 (10)	CDSI0CP	F10	O	H	MIPI-PHY	MIPI-DSI0 clock positive	VDD12_MIPI0
	CDSI0CN	F9	O	H	MIPI–PHY	MIPI-DSI0 clock negative	VDD12_MIPI0
	CDSI0D0P	H10	O	H	MIPI–PHY	MIPI-DSI0 data 0 positive	VDD12_MIPI0
	CDSI0D0N	H9	O	H	MIPI–PHY	MIPI-DSI0 data 0 negative	VDD12_MIPI0
	CDSI0D1P	G10	O	H	MIPI–PHY	MIPI-DSI0 data 1 positive	VDD12_MIPI0
	CDSI0D1N	G9	O	H	MIPI–PHY	MIPI-DSI0 data 1 negative	VDD12_MIPI0
	CDSI0D2P	E10	O	H	MIPI–PHY	MIPI-DSI0 data 2 positive	VDD12_MIPI0
	CDSI0D2N	E9	O	H	MIPI–PHY	MIPI-DSI0 data 2 negative	VDD12_MIPI0
	CDSI0D3P	D10	O	H	MIPI–PHY	MIPI-DSI0 data 3 positive	VDD12_MIPI0
	CDSI0D3N	D9	O	H	MIPI–PHY	MIPI-DSI0 data 3 negative	VDD12_MIPI0
CDSI TX1 (10)	CDSI1CP	A7	O	H	MIPI-PHY	MIPI-DSI1 clock positive	VDD12_MIPI0
	CDSI1CN	B7	O	H	MIPI–PHY	MIPI-DSI1 clock negative	VDD12_MIPI1
	CDSI1D0P	A9	O	H	MIPI–PHY	MIPI-DSI1 data 0 positive	VDD12_MIPI1
	CDSI1D0N	B9	O	H	MIPI–PHY	MIPI-DSI1 data 0 negative	VDD12_MIPI1
	CDSI1D1P	A8	O	H	MIPI–PHY	MIPI-DSI1 data 1 positive	VDD12_MIPI1
	CDSI1D1N	B8	O	H	MIPI–PHY	MIPI-DSI1 data 1 negative	VDD12_MIPI1
	CDSI1D2P	A6	O	H	MIPI–PHY	MIPI-DSI1 data 2 positive	VDD12_MIPI1
	CDSI1D2N	B6	O	H	MIPI–PHY	MIPI-DSI1 data 2 negative	VDD12_MIPI1
	CDSI1D3P	A5	O	H	MIPI–PHY	MIPI-DSI1 data 3 positive	VDD12_MIPI1
	CDSI1D3N	B5	O	H	MIPI–PHY	MIPI-DSI1 data 3 negative	VDD12_MIPI1
HDMI-RX (9)	HDMICP	C1	I	-	HDMI-PHY	HDMI clock channel positive	VDD33_HDMI
	HDMICN	C2	I	-	HDMI-PHY	HDMI clock channel negative	VDD33_HDMI
	HDMID0P	D1	I	-	HDMI-PHY	HDMI data 0 channel positive	VDD33_HDMI
	HDMID0N	D2	I	-	HDMI-PHY	HDMI data 0 channel negative	VDD33_HDMI
	HDMID1P	E1	I	-	HDMI-PHY	HDMI data 1 channel positive	VDD33_HDMI
	HDMID1N	E2	I	-	HDMI-PHY	HDMI data 1 channel negative	VDD33_HDMI
	HDMID2P	F1	I	-	HDMI-PHY	HDMI data 2 channel positive	VDD33_HDMI
	HDMID2N	F2	I	-	HDMI-PHY	HDMI data 2 channel negative	VDD33_HDMI
	REXT	A1	I	-	HDMI-PHY	External reference resistor (Connect with 2 kΩ to VDD33HDMI)	VDD33_HDMI
DDC (2)	DDC_SCL	A3	IO	-	Sch/5V/OD	DDC I^2C target clock	VDDIO33
	DDC_SDA	B3	IO	-	Sch/5V/OD	DDC I^2C target data	VDDIO33
CEC(1)	CEC	A2	IO	-	Sch/OD	CEC signal	VDDIO33
HPD(2)	HPDI	A4	I	-	5 V	5 V power input	VDDIO33
	HPDO	B4	O	L	N	Hot plug detect output	VDDIO33
Audio (7)	A_SCK	K7	O	L	N	I^2S/TDM bit clock signal	VDDIO18
	A_WFS	K5	O	L	N	I^2S word clock TDM frame sync signal	VDDIO18
	A_SD3	J5	O	L	N	I^2S data signal bit3	VDDIO18
	A_SD2	J6	O	L	N	I^2S data signal bit2	VDDIO18
	A_SD1	J8	O	L	N	I^2S data signal bit1	VDDIO18
	A_SD0	J9	O	L	N	I^2S data signal bit0 TDM data signal	VDDIO18
	A_OSCK	J4	O	L	N	Audio Over Sampling Clock	VDDIO18
IR(1)	IR	G6	I	-	N	InfraRed signal (Fix low externally, if not used)	VDDIO18
I^2C(2)	I2C_SCL	K4	IO	-	Sch/OD	I^2C target clock	VDDIO18
	I2C_SDA	K3	IO	-	Sch/OD	I^2C target data	VDDIO18

Group	Pin Name	Ball	I/O	Init (O)	Type (Note 1)	Function	Voltage Supply
Audio PLL (4)	BIASDA	J1	O	L	PLL	Audio PLL BIAS signal Connect to AVSS through 0.1 µF when not used	VDDIO33
	DAOUT	J2	O	H	PLL	Audio PLL Clock Reference output clock Please leave open when not used	VDDIO33
	PCKIN	K1	I	-	PLL	Audio PLL Reference Input clock Connect to AVSS through 0.1 µF when not used	VDDIO33
	PFIL	K2	O	L	PLL	Audio PLL Low Pass Filter signal Connect to AVSS through 0.1 µF when not used	VDDIO33
POWER (10)	VDDC11	C10 K6	-	-	Power	1.1 V Internal core power supply	-
	VDDIO18	J7	-	-	Power	1.8 V IO power supply	-
	VDDIO33	H2	-	-	Power	3.3 V IO power supply	-
	VDD33_HDMI	B1 G1	-	-	Power	HDMI Phy 3.3 V power supply	-
	VDD11_HDMI	B2 G2	-	-	Power	HDMI Phy 1.1 V power supply	-
	VDD12_MIPI0	J10	-	-	Power	MIPI DSI 1.2 V power supply for link0	-
	VDD12_MIPI1	B10	-	-	Power	MIPI DSI 1.2 V power supply for link1	-
GROUND (18)	VSS	A10 C9 D4 D5 D6 D7 E4 E5 E6 E7 F4 F5 F6 F7 G4 G7 H1 K10	-	-	-	Ground	-

Total 80 pins

Note 1: Descriptions mean below.

N: Normal digital I/O

Sch: Schmitt trigger input

5 V: 5 V tolerant input

OD: Open drain

Note 2: Pull-Up to select 0x1F for I^2C Target address

Pull-Down to select 0x0F for I^2C Target address

Please consult a technical support representative before board design to determine whether pull-up or pull-down with external resistors.

2.1. TC358871XBG 80-Pin Count Summary

Table 2.2 BGA80 Pin Count Summary

Group Name	Pin Count	Notes
SYSTEM	4	-
CDSI TX0	10	-
CDSI TX1	10	-
HDMI-RX	9	-
DDC	2	-
CEC	1	-
Audio	7	-
I^2C	2	-
IR	1	-
HPD	2	-
Audio PLL	4	-
POWER	10	IO, Core
GROUND	18	IO, Core, Analog
TOTAL Pin Count	80	Func 52 + (10+18)

2.2. Pin Layout

Top view

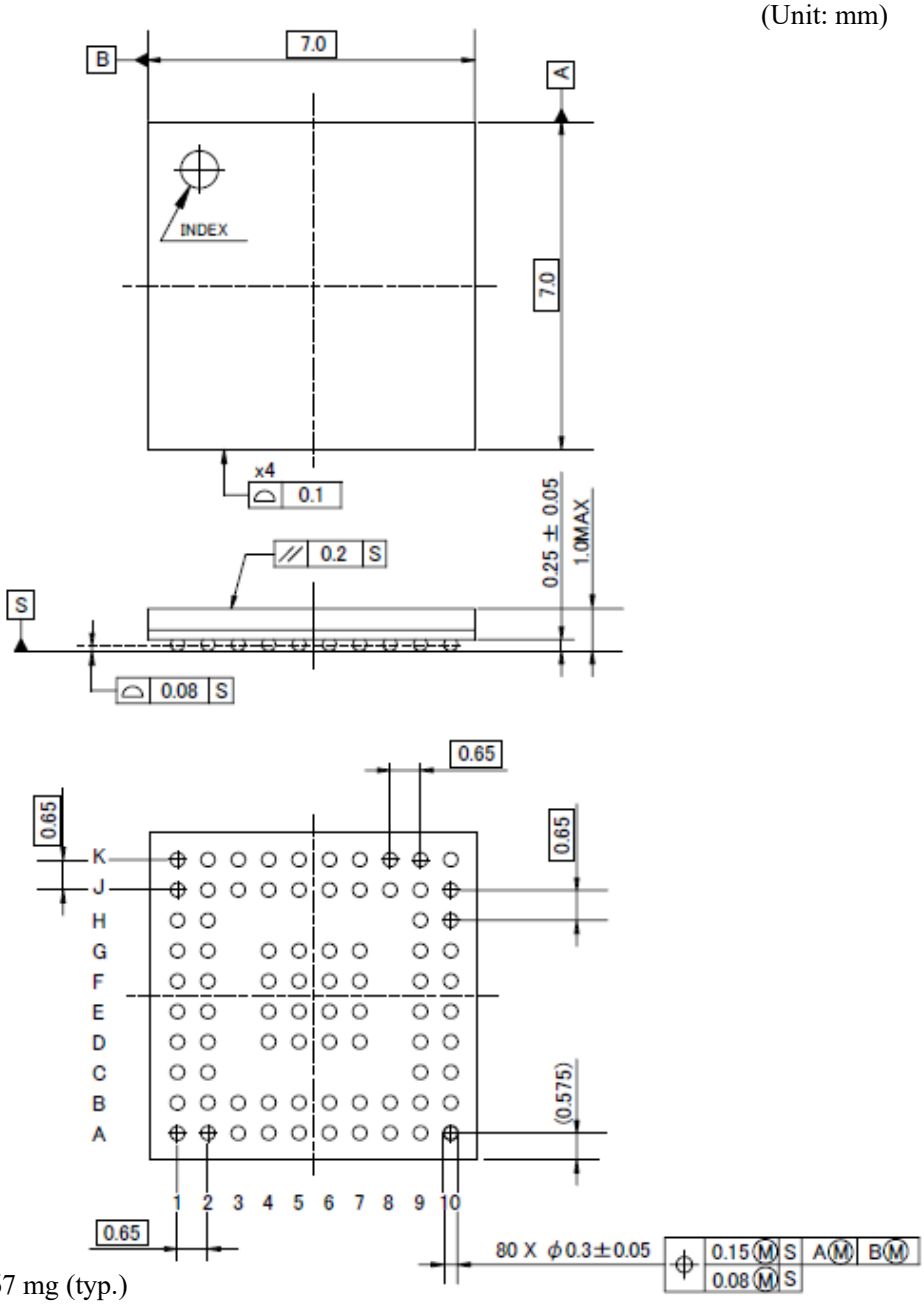
	1	2	3	4	5	6	7	8	9	10
A	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
	REXT	CEC	DDC_SCL	HPDI	CDSI1D3P	CDSI1D2P	CDSI1CP	CDSI1D1P	CDSI1D0P	VSS
B	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
	VDD33_HDMI	VDD11_HDMI	DDC_SDA	HPDO	CDSI1D3N	CDSI1D2N	CDSI1CN	CDSI1D1N	CDSI1D0N	VDD12_MIPI1
C	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
	HDMICP	HDMICN	No ball	No ball	No ball	No ball	No ball	No ball	VSS	VDDC11
D	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
	HDMID0P	HDMID0N	No ball	VSS	VSS	VSS	VSS	No ball	CDSI0D3N	CDSI0D3P
E	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
	HDMID1P	HDMID1N	No ball	VSS	VSS	VSS	VSS	No ball	CDSI0D2N	CDSI0D2P
F	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
	HDMID2P	HDMID2N	No ball	VSS	VSS	VSS	VSS	No ball	CDSI0CN	CDSI0CP
G	G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
	VDD33_HDMI	VDD11_HDMI	No ball	VSS	TEST	IR	VSS	No ball	CDSI0D1N	CDSI0D1P
H	H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
	VSS	VDDIO33	No ball	No ball	No ball	No ball	No ball	No ball	CDSI0D0N	CDSI0D0P
J	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
	BIASDA	DAOUT	INT	A_OSCK	A_SD3	A_SD2	VDDIO18	A_SD1	A_SD0	VDD12_MIPI0
K	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
	PCKIN	PFIL	I2C_SDA	I2C_SCL	A_WFS	VDDC11	A_SCK	RESETN	REFCLK	VSS

Figure 2.1 TC358871XBG 80-Pin Layout (Top View)

3. Package

The 80-pin package for TC358871XBG is described in the figures below.

(Unit: mm)



Weight: 67 mg (typ.)

Figure 3.1 TC358871XBG package (P-VFBGA80-0707-0.65-001)

The mechanical dimension of BGA80 package is listed below.

Table 3.1 Mechanical Dimension

Package	Solder Ball Pitch	Solder Ball Height	Package Dimension	Package Height
80-Pin	0.65 mm	0.25 mm	7.0 × 7.0 mm^2	1.0 mm

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

VSS= 0 V reference

Item	Symbol	Rating	Unit
Supply voltage (1.8 V - Digital IO)	VDDIO18	-0.3 to +3.9	V
Supply voltage (3.3 V - Digital IO)	VDDIO33	-0.3 to +3.9	V
Supply voltage (1.1 V – Digital Core)	VDDC11	-0.3 to +1.8	V
Supply voltage (1.2 V – MIPI DSI PHY)	VDD12_MIPI	-0.3 to +1.8	V
Supply voltage (3.3 V – HDMIRX Phy)	VDD33_HDMI	-0.3 to +3.9	V
Supply voltage (1.1 V – HDMIRX Phy)	VDD11_HDMI	-0.3 to +1.8	V
Input voltage (DSI IO)	V_{IN_DSI}	-0.3 to VDD12_MIPI+0.3	V
Output voltage (DSI IO)	V_{OUT_DSI}	-0.3 to VDD12_MIPI+0.3	V
Input voltage (Digital IO)	V_{IN_IO}	-0.3 to VDDIO18+0.3 -0.3 to VDDIO33+0.3	V
Output voltage (Digital IO)	V_{OUT_IO}	-0.3 to VDDIO18+0.3	V
DDC Input / Output voltage	DDC_SDA DDC_SCL HPDI	-0.3 to 6	V
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	-40 to +125	°C

4.2. Operating Condition

VSS= 0 V reference

Item	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8 V – Digital IO)	VDDIO18 (Note)	1.65	1.8	1.95	V
Supply voltage (3.3 V – Digital IO)	VDDIO33	3.0	3.3	3.6	V
Supply voltage (1.1 V – Digital Core)	VDDC11	1.1	1.15	1.2	V
Supply voltage (3.3 V – HDMIRX PHY)	VDD33_HDMI	3.135	3.3	3.465	V
Supply voltage (1.1 V – HDMIRX PHY)	VDD11_HDMI	1.1	1.15	1.2	V
Supply voltage (1.2 V – MIPI DSI PHY)	VDD12_MIPI0 VDD12_MIPI1	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied)	T_a	-30	+25	+70	°C

Note: VDDIO18 can be used at 1.8 V or 3.3 V.

4.3. DC Electrical Specification

Standard IO

Item	Symbol	Min	Max	Unit
Input voltage, High level input (Note 1)	V_{IH}	0.70 VDDIO18 (Note 2)	VDDIO18 (Note 2)	V
		0.70 VDDIO18 (Note 3)	VDDIO18 (Note 3)	
		0.70 VDDIO33 (Note 4)	VDDIO33 (Note 4)	
Input voltage, Low level input (Note 1)	V_{IL}	0	0.30 VDDIO18 (Note 2)	V
			0.25 VDDIO18 (Note 3)	
			0.25 VDDIO33 (Note 4)	
Input voltage High level CMOS Schmitt Trigger (Note 1)	V_{IHS}	0.70 VDDIO18 (Note 2)	VDDIO18 (Note 2)	V
		0.70 VDDIO18 (Note 3)	VDDIO18 (Note 3)	
		0.70 VDDIO33 (Note 4)	VDDIO33 (Note 4)	
Input voltage Low level CMOS Schmitt Trigger (Note 1)	V_{ILS}	0	0.30 VDDIO18 (Note 2)	V
			0.25 VDDIO18 (Note 3)	
			0.25 VDDIO33 (Note 4)	
Input leak current, High level (Condition: V_{IN} = +VDDIO, VDDIO = 3.6 V)	I_{ILH1}	-10	10	μA
Input leak current, Low level (Condition: V_{IN} = 0 V, VDDIO = 3.6 V)	I_{ILL1}	-10	10	μA

Note 1: Each power source is operating within recommended operation condition.
Note 2: For IOs related to VDDIO18 and operated at 1.8 V range.
Note 3: For IOs related to VDDIO18 and operated at 3.3 V range.
Note 4: For IOs related toVDDIO33.

HDMI DDC Target IO (DDC_SDA, DDC_SCL terminal)

Item	Symbol	Min	Max	Unit
Input voltage, High level input	V_{IH}	3.1	5.25	V
Input voltage, Low level input	V_{IL}	0	1.7	V
Output voltage Low level (I_{OL} = 8 mA)	V_{OL}	-	0.4	V
Input leak current, High level (V_{IN} = VDDIO33)	I_{IH}	-10	10	μA
Input leak current, Low level (V_{IN} = VSS)	I_{IL}	-10	10	μA

HDMI DDC 5 V input (HPDI terminal)

Item	Symbol	Min	Max	Unit
Input voltage, High level input	V_{IH}	0.8 VDDIO33	5.25	V
Input voltage, Low level input	V_{IL}	0	0.3 VDDIO33	V
Input leak current, High level (V_{IN} = VDDIO33)	I_{IH}	-10	10	μA
Input leak current, Low level (V_{IN} = VSS)	I_{IL}	-10	10	μA

HDMI HPD output (HPDO terminal)

Item	Symbol	Min	Max	Unit
Output voltage High level (I_{OH} = -4 mA)	V_{OH}	VDDIO33-0.6	-	V
Output voltage Low level (I_{OL} = 4 mA)	V_{OL}	-	0.4	V

HDMI CEC IO (CEC terminal)

Item	Symbol	Min	Max	Unit
Input voltage, High level input	V_{IH}	2	VDDIO33	V
Input voltage, Low level input	V_{IL}	0	0.8	V
Output voltage Low level (I_{OL} = 8 mA)	V_{OL}	-	0.4	V
Input leak current, High level (V_{IN} = VDDIO33)	I_{IH}	-10	10	μA
Input leak current, Low level (V_{IN} = VSS)	I_{IL}	-10	10	μA

I^2C IO (I2C_SDA, I2C_SCL terminal)

Item	Symbol	Min	Max	Unit
Input voltage, High level input	V_{IH}	0.7 VDDIO18	VDDIO18	V
Input voltage, Low level input	V_{IL}	0	0.3 VDDIO18	V
Output voltage Low level (VDDIO18 used at 1.8 V range, I_{OL} = 3 mA)	V_{OL}	-	0.2 VDDIO18	V
Output voltage Low level (VDDIO18 used at 3.3 V range, I_{OL} = 3 mA)		-	0.4	V

Audio output (A_SCK, A_WFS, A_SD3, A_SD2, A_SD1, A_SD0, A_OSCK terminal)

Item	Symbol	Min	Max	Unit
Output voltage High level (VDDIO18 used at 1.8 V range, I_{OH} = -4 mA)	V_{OH}	VDDIO18-0.45	-	V
Output voltage High level (VDDIO18 used at 3.3 V range, I_{OH} = -4 mA)		VDDIO18-0.6	-	V
Output voltage Low level (VDDIO18 used at 1.8 V range, I_{OL} = 4 mA)	V_{OL}	-	0.45	V
Output voltage Low level (VDDIO18 used at 3.3 V range, I_{OL} = 4 mA)		-	0.4	V

INT output (INT terminal)

Item	Symbol	Min	Max	Unit
Output voltage High level (VDDIO18 used at 1.8 V range, I_{OH} = -2 mA)	V_{OH}	VDDIO18-0.45	-	V
Output voltage High level (VDDIO18 used at 3.3 V range, I_{OH} = -2 mA)		VDDIO18-0.6	-	V
Output voltage Low level (VDDIO18 used at 1.8 V range, I_{OL} = 2 mA)	V_{OL}	-	0.45	V
Output voltage Low level (VDDIO18 used at 3.3 V range, I_{OL} = 2 mA)		-	0.4	V

5. External Circuit Suggestion

5.1. I²C Target address definition

INT terminal is multiplexed with configuring function of I²C Target address. During **RESETN** asserted, **INT** becomes input and detects the polarity. After **RESETN** deasserted it becomes **INT** function (output) automatically. Pull up or pull down this terminal by 10 kΩ resister externally.

If pulled up, then I²C Target address becomes 0x1F
If pulled down then I²C Target address becomes 0x0F

5.2. DDC_SDA/DDC_SCL

DDC_SDA and **DDC_SCL** are pulled up to +5 V power line and +5 V power line is also pulled down for **DDC_SDA** and **DDC_SDL** to be fixed low when +5 V power is disabled.

Below figure illustrates example DDC interface connections.

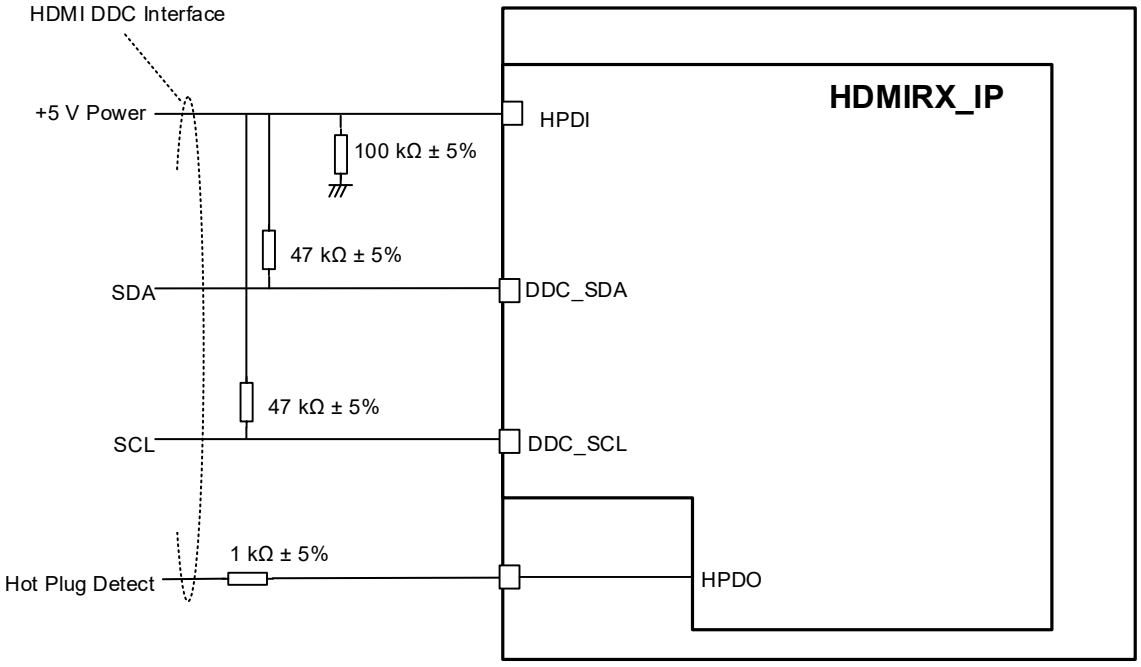


Figure 5.1 Example of DDC I/F Connection

The automatic adjustment function of terminus resistance is attached to HDMI-Rx.

Therefore, connect 2 kΩ±1% of reference resistance between **VDD33_HDMI** and **REXT**.

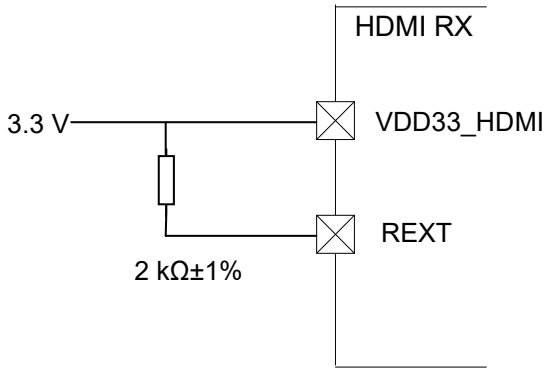


Figure 5.2 Connection of REXT resistance

5.3. Audio PLL

The Audio PLL external terminal connections used in the Audio clock generation are shown in the Figure below.

In **DAOUT** output (PLL input), a low pass filter is installed in the LSI external area.

In addition, a low pass filter for cutting unnecessary components in phase comparator output in the PLL is also installed in the LSI external area.

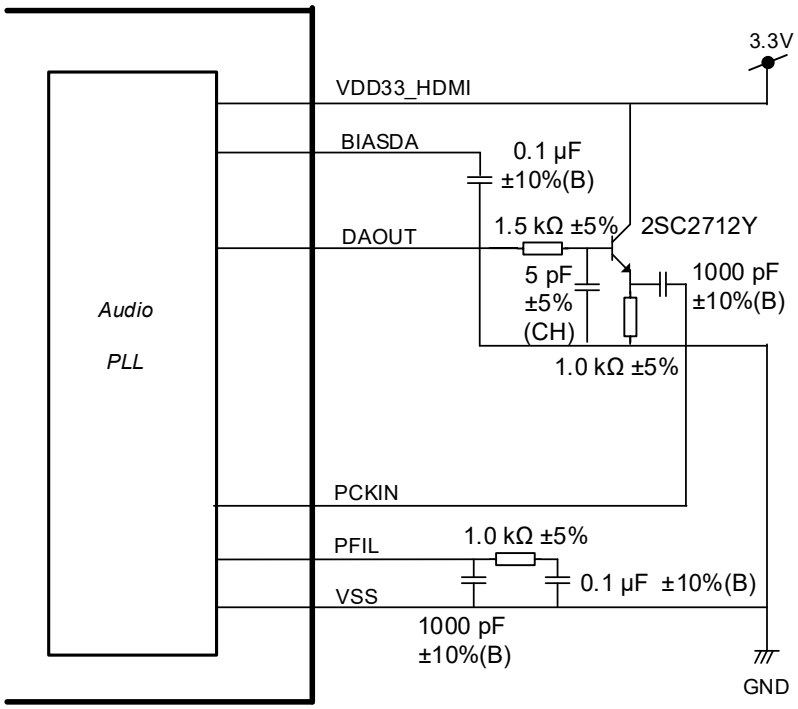


Figure 5.3 Audio Clock External LPF circuit block diagram

5.4. Suggestion of Power supply circuit

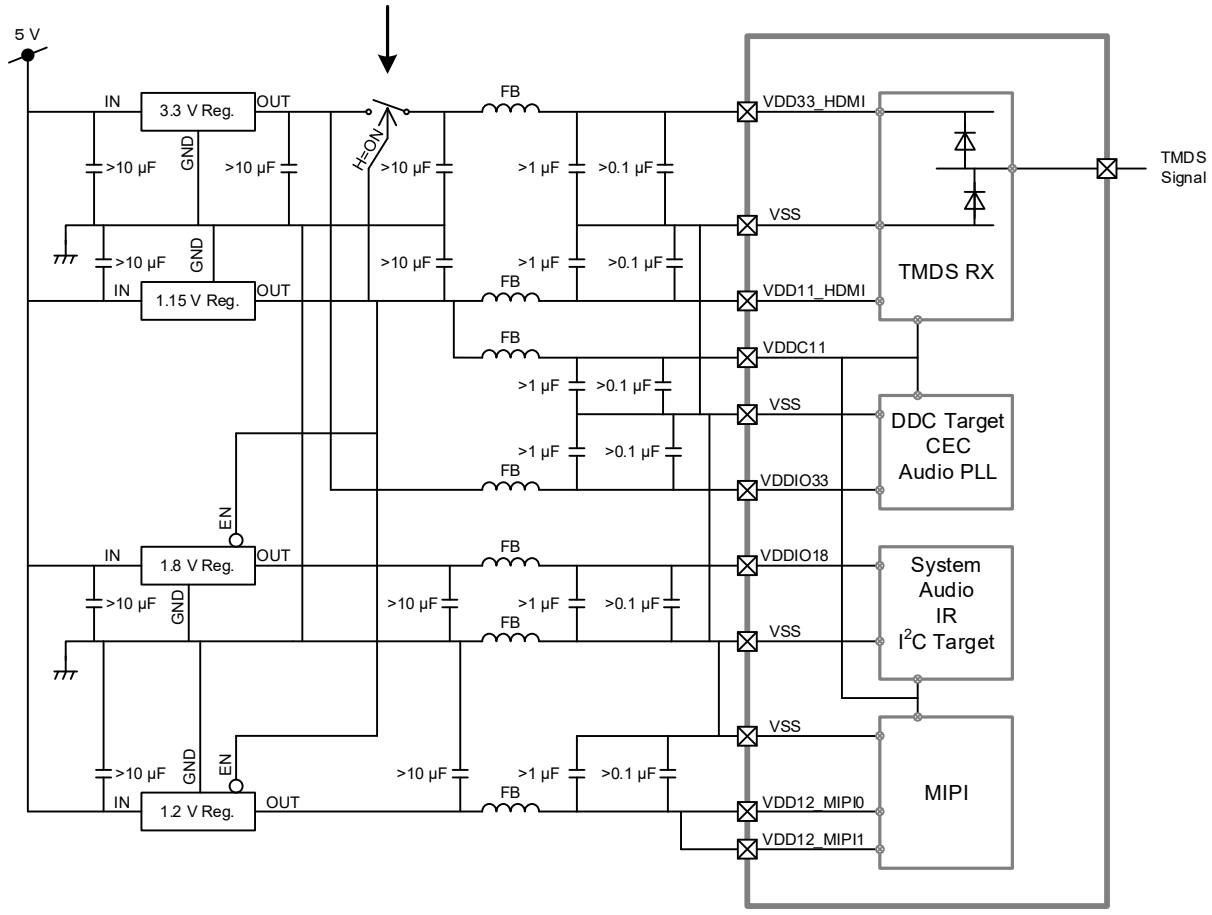
Since the ESD protection diode is attached to the TMDS input pin between a power supply/GND, current may flow backwards HDMI-Rx from source apparatus at the time of power supply OFF.

And also VDD33_HDMI power supply should be isolated from another 3.3 V power supplies because this backward current also damages them. Below figure is recommend attaching a back flow prevention circuit.

Case (1) External switch circuit

Attach the adverse current prevention switch from a TMDS differential signal.

Since reverse current also gives damage to VDDIO33, this switch shall separate VDD33_HDMI and VDDIO33.

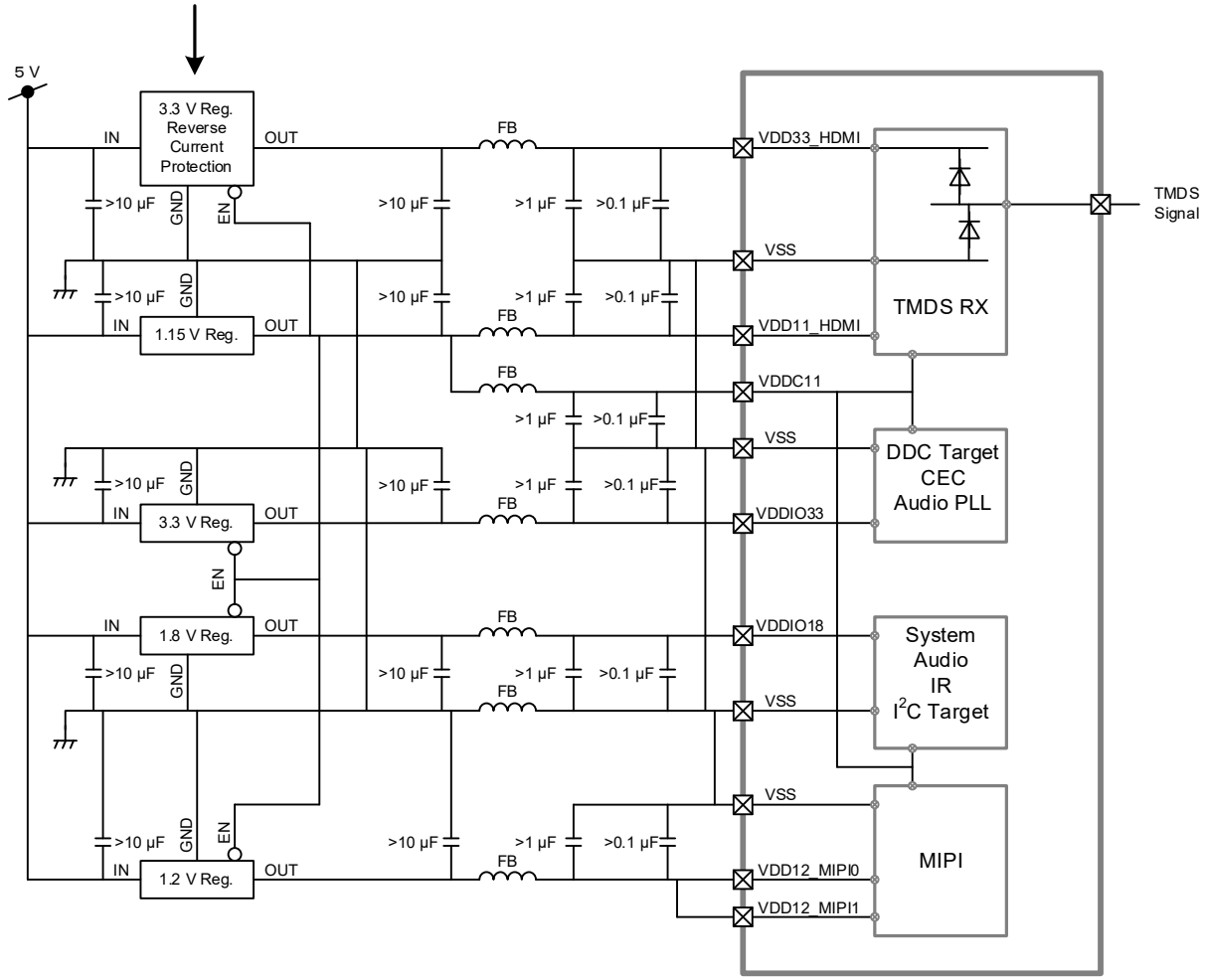


All TC358871 VSSs should be separated at AC level from regulators' VSS with FB(ferrite bead) or another method to attenuate EMI.

Figure 5.4 Suggestion of power supply circuit with external switch

Case (2) Regulator with reverse current protection

Apply a current protection regulator to VDD33_HDMI.



All TC358871 VSSs should be separated at AC level from regulators' VSS with FB(ferrite bead) or another method to attenuate EMI.

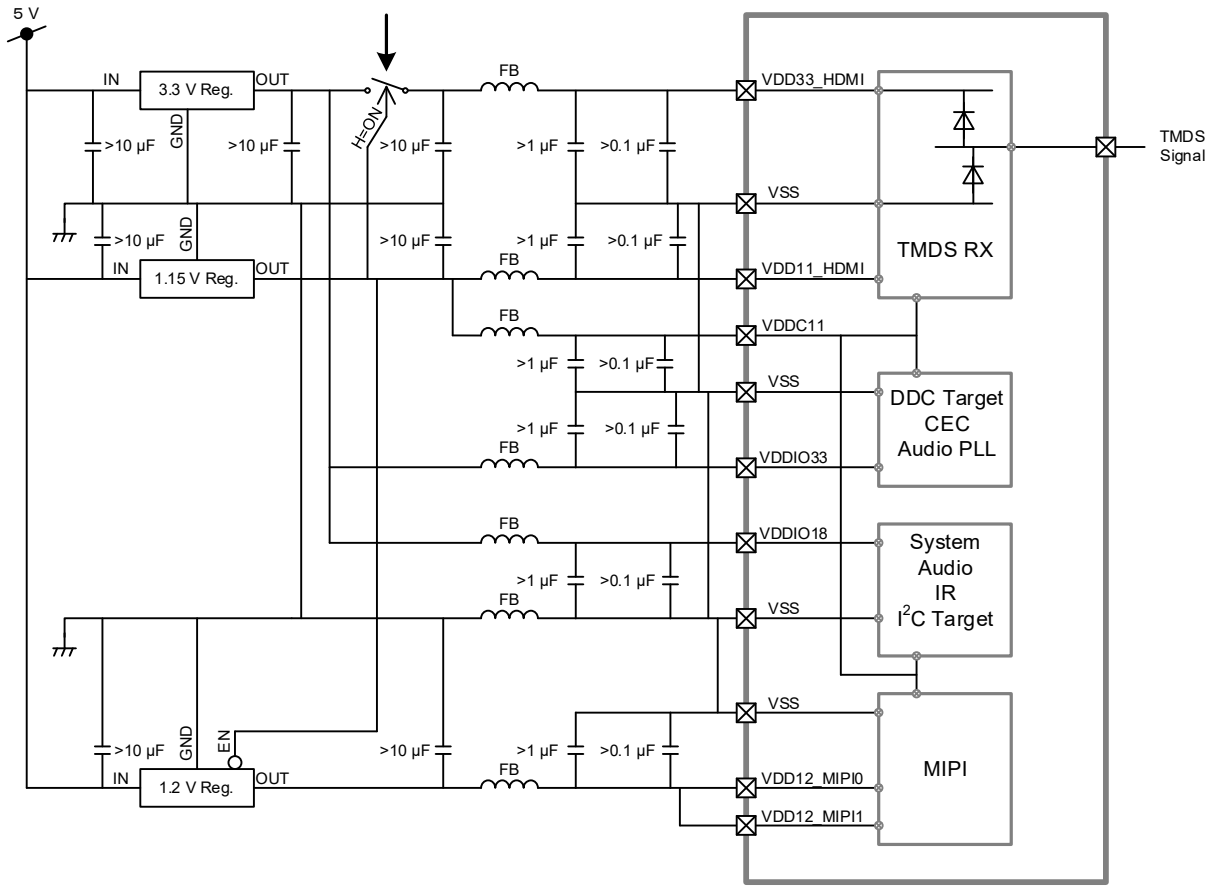
Figure 5.5 Suggestion of power supply circuit with current protection regulator

Case (3) Use of VDDIO18 at 3.3 V range

If VDDIO is applied at 3.3 V range, Common regulation is available among VDD33_HDMI, VDIO33 and VDDIO18.

Attach the adverse current prevention switch from a TMDS differential signal.

Since reverse current also gives damage to VDDIO33 and VDDIO18, this switch shall separate VDD33_HDMI and VDDIO33/VDDIO18.



All TC358871 VSSs should be separated at AC level from regulators' VSS with FB(ferrite bead) or another method to attenuate EMI.

Figure 5.6 Suggestion of power supply circuit at VDDIO18 = 3.3 V

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.0	2023-06-07	New
1.10	2026-04-14	Updated the terms "Master/Slave" to "Controller/Target". Corrected typos. Revised the last page “RESTRICTIONS ON PRODUCT USE”.

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