Full SiC MOSFET 10kW Isolated Bidirectional DC-DC Converter

Design Guide

RD264-DGUIDE-01

Toshiba Electronic Devices & Storage Corporation

Table of Contents

1. Introduction

This design guide describes how to design various circuitry for the Full SiC MOSFET 10kW Isolated Bidirectional DC-DC Converter (hereafter referred to as this design).

This design is a bidirectional DC-DC converter capable of supplying up to 10kW of power. It takes power from the high-voltage side (750V) and outputs power to the low-voltage side (400V), or takes power from the low-voltage side (400V) and outputs power to the high-voltage side (750V). This design adopts the DAB (Dual Active Bridge) topology with emphasis on efficiency. The DAB topology has a full-bridge configuration on both the high-voltage side and low-voltage side, and can handle higher power compared to the half-bridge topology. In addition, soft switching is possible due to power transfer by phase shifting, and a highly efficient DC-DC converter can be realized. It can be applied to various industrial equipment such as charging systems for electric vehicles (xEV) and inverters for photovoltaic power generation.

The high-voltage side is assumed to operate at 750V input/output. The required switching voltage rating of the device exceeds 1000V, and therefore IGBTs are generally selected. However, when IGBTs are used, switching losses are large, and significant efficiency improvement cannot be expected. In this design, a 1200V SiC MOSFET TW060N120C is used to achieve both high-power conversion and high efficiency. In addition, the low-voltage side is assumed to operate at 400V input/output. A 650V SiC MOSFET TW048N65C is used to achieve high efficiency on the low-voltage side as well.

The gate driver uses a smart gate driver coupler TLP5214A, which has a 4A sink-source current capability sufficient to drive the gate charging and discharging current during SiC MOSFET switching, and is equipped with an overcurrent protection function and a UVLO function. In addition, an optically coupled isolation amplifier TLP7920, which provides high linearity accuracy and high common-mode transient immunity, is used for the voltage sensor circuitry requiring isolation.

2. Main Components

This chapter describes the components used in this design.

2.1. SiC MOSFET TW060N120C

This design uses the 1200V SiC MOSFET TW060N120C as the switching device on the high-voltage side. The main features of TW060N120C are as follows.

- Chip design of 3rd generation (Built-in SiC schottky barrier diode)
- Low diode forward voltage: V_{DSF} = -1.35V (Typ.)
- High voltage: V_{DSS} = 1200V
- Low drain-source on-resistance: $R_{DS(ON)}$ = 60mΩ (Typ.)
- Less susceptible to malfunction due to high threshold voltage: V_{th} = 3.0 to 5.0V (V_{DS} = 10V, I_D = 4.2mA)
- Recommended gate - source drive voltage: V_{GS_on} = 18V, V_{GS_off} = 0V
- Enhancement mode

Appearance and Terminal Layout

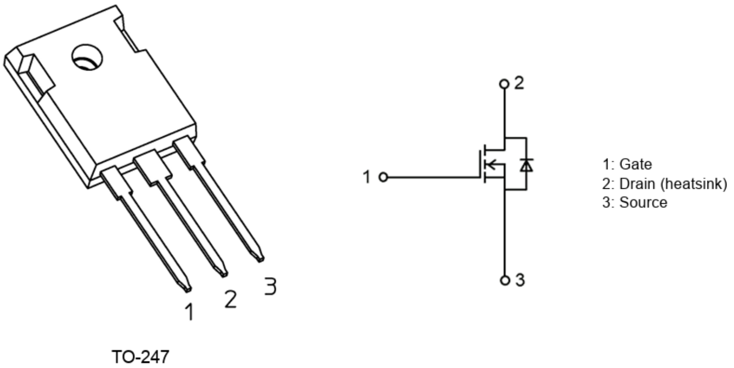


Figure 2.1 Appearance and Terminal Layout of TW060N120C

2.2. SiC MOSFET TW048N65C

This design uses the 650V SiC MOSFET TW048N65C as the switching device on the low-voltage side. The main features of TW048N65C are as follows.

- Chip design of 3rd generation (Built-in SiC schottky barrier diode)
- Low diode forward voltage: V_{DSF} = -1.35V (Typ.)
- High voltage: V_{DSS} = 650V
- Low drain-source on-resistance: $R_{DS(ON)}$ = 48mΩ (Typ.)
- Less susceptible to malfunction due to high threshold voltage: V_{th} = 3.0 to 5.0V (V_{DS} = 10V, I_D = 1.6mA)
- Recommended gate - source drive voltage: V_{GS_on} = 18V, V_{GS_off} = 0V
- Enhancement mode

Appearance and Terminal Layout

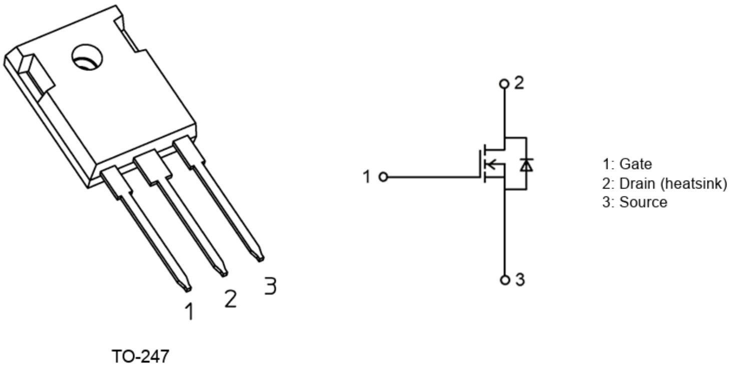


Figure 2.2 Appearance and Terminal Layout of TW048N65C

2.3. Gate Driver Photocoupler TLP5214A

This design uses the TLP5214A for isolated gate driving of the MOSFET.
The main features of the TLP5214A are as follows:

- Peak output current: ±4.0A (Max)
- Guaranteed performance over temperature: -40 to 110°C
- Supply current: 3.8mA (Max)
- Power supply voltage: 15V to 30V
- Threshold input current: 6mA (Max)
- Propagation delay time: 150ns (Max)
- DESAT leading edge blanking time: 1.1µs (Typ.)
- Common-mode transient immunity: ±35kV/µs (Min)
- Isolation voltage: 5000Vrms (Min)
- Safety standards
  UL-recognized: UL 1577, File No.E67349
  cUL-recognized: CSA Component Acceptance Service
  No. 5A, File No.E67349
  VDE approved: EN 60747-5-5, EN 62368-1

Appearance and Block Diagram

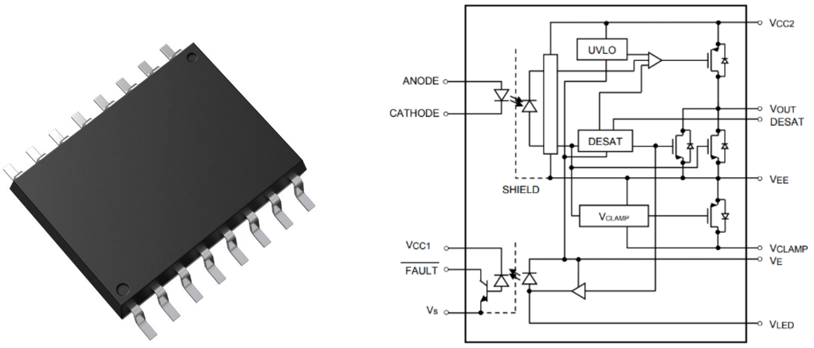


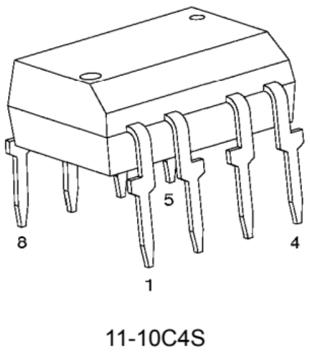
Figure 2.3 Appearance and Block Diagram of TLP5214A

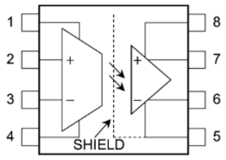
2.4. Optically Isolation Amplifier TLP7920

This design uses the optically isolation amplifier TLP7920 for isolated sensing of input and output voltages. The main features of the TLP7920 are as follows:

- Output side supply voltage: 3.0 to 5.5V
- Output side supply current: 6.2mA (Typ.)
- Operating temperature range: -40 to 105℃
- Common-mode transient immunity: 15kV/μs (Min)
- Safety standards
  UL-recognized: UL 1577, File No.E67349
  cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349
  VDE-approved: EN IEC 60747-5-5

Appearance and Pin Configuration Diagram





Pin No.	Symbol	Description
1	V_{DD1}	Input side supply voltage
2	V_{IN+}	Positive input
3	V_{IN-}	Negative input
4	GND1	Input side ground
5	GND2	Output side ground
6	V_{OUT-}	Negative output
7	V_{OUT+}	Positive output
8	V_{DD2}	Output side supply voltage

Figure 2.4 Appearance and Pin Configuration Diagram of TLP7920

3. Circuit design

This chapter describes the key circuit design considerations.

3.1. High-voltage Side Circuit Design

This section describes the design of the high-voltage side circuit of this design.

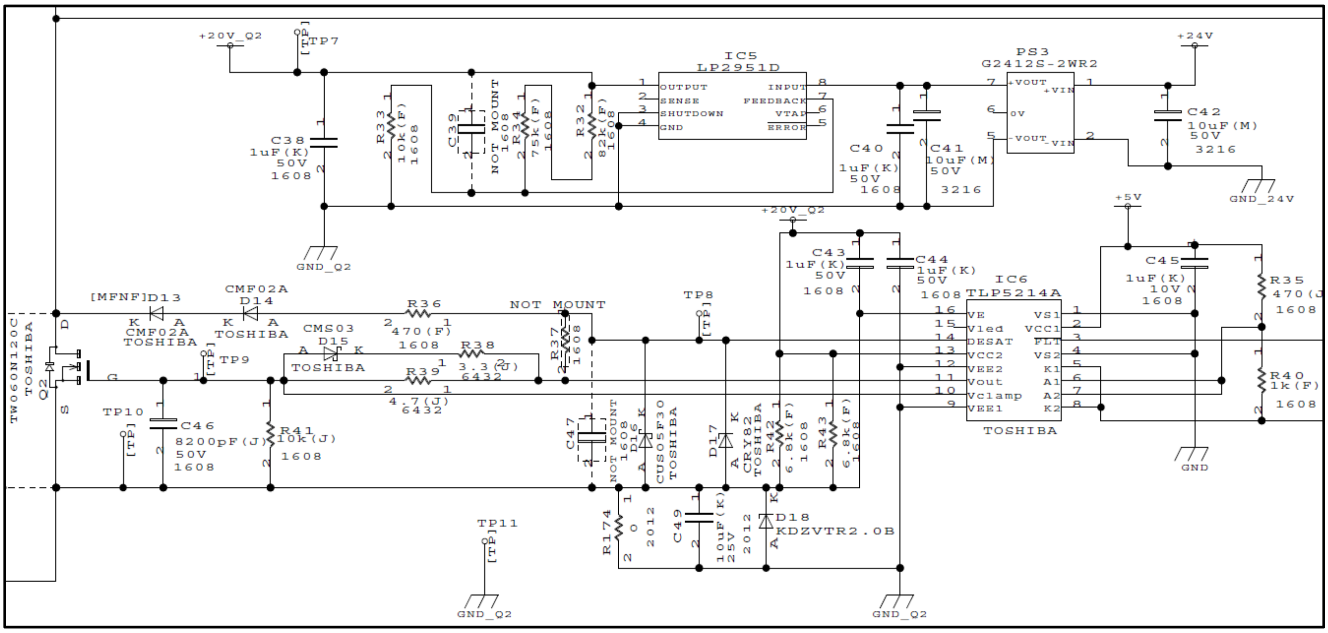


Figure 3.1 Gate Drive Circuit (High-voltage Side Lower-arm)

Gate Drive Circuit

As a representative example, this section describes the gate drive circuits of high voltage-side. The gate drive circuit of the lower arm side MOSFET Q2 is shown in Figure 3.1. The design of the gate drive circuit affects power supply efficiency and EMI noise. Generally, power supply efficiency and EMI noise have a trade-off relationship, so it is necessary to design both in a balanced manner. The gate-drive circuit of this design has a circuit configuration that can adjust the switching speed of MOSFET. If it is necessary to reduce turn-on noise, changing the gate series resistor (R39) to a large value may reduce EMI noise. Note that if the gate-series resistor is changed to a large value, not only the turn-on speed of MOSFET but also the turn-off speed will be reduced, which may result in worsening of the power supply efficiency. In this situation, in order to reduce power-efficiency degradation only the turn-off speed of MOSFET should be increased. Changing the gate-series resistor (R38) to a small value may only increase the turn-off speed of MOSFET and reduce the power-efficiency degradation of the system. When changing the gate series resistance, it is necessary to confirm that the EMI noise, power efficiency performance, and heat dissipation performance required for the system are satisfied.

Negative Bias Circuit

Negative-bias circuit is used if there is a risk of malfunction due to the parasitic mirror capacitance between the drain and gate of MOSFET. Figure 3.1 shows the gate drive circuit used on the lower arm side. When the lower arm is turned off and the upper arm is turned on, the intermediate potential rises steeply and displacement current is generated through the mirror capacitance between the drain and gate of the lower arm, and flows toward VOUT terminal of the smart gate driver coupler (IC6). When this displacement current passes through the gate resistor of the circuit, a voltage drop occurs, and when the gate voltage rises, the lower arm may be erroneously turned on, resulting in a short circuit of the upper and lower arms. Such erroneous ON occurrence was not confirmed with this design. However, measures must be taken when erroneous ON occurs due to the board layout or wiring in actual applications.

Generally, as a countermeasure against erroneous ON, it is effective to bias the voltage during gate-off to a negative voltage. Although this design does not bias the gate to a negative voltage, a negative bias circuit using a zener diode (D18) can be easily realized. By removing the 0Ω resistor (R174) placed in parallel with the D18 and placing a capacitor of about 1μF, a negative bias equivalent to the zener voltage is applied to the gate during gate-off. Although a 2V zener diode is used for this design, select an appropriate element according to the actual operation.

Output Capacitor

When the power supply is operating with high-voltage side as power supply output, the capacitance value of the output capacitors (C62 to C69) is calculated based on the hold-up time requirement. The hold-up time $Thold_{high}$ is calculated by the following equation, where the combined capacitance value of the output capacitors is $Cout_{high}$, the output voltage is $Vout_{high}$, the minimum output voltage is $Vout_{high\_min}$, and the maximum output power is Pout.

$$Thold_{high} = Cout_{high} \times \frac{(Vout_{high}^2 - Vout_{high\_min}^2)}{2 \times Pout}$$

The initial setting is $Cout_{high}$ = 705μF (3 parallel of (2 serial 470μF)), $Vout_{high}$ = 750V, $Vout_{high\_min}$ = 700V, Pout = 10kW, and the hold-up time is 2.55ms. Adjust the capacitance value of the output capacitor to satisfy the hold-up time required for the system in practical applications. In addition, when the output ripple specification is defined, the capacitance value required to satisfy the output ripple specification must be calculated and compared with the capacitance value that satisfies the hold-up time, and the larger capacitance value must be used. In addition, tolerances and aging degradation must be considered when selecting a capacitor.

3.2. Selection of Transformer and Inductors

Transformer Selection

Set the ratio n = n1/n2 of high-voltage side winding n1 and low-voltage side winding n2 to be equal to the ratio of high-voltage side voltage 750V and low-voltage side voltage 400V (750/400 = 1.875). For this design, a transformer with n1/n2 = 28/15 (= 1.87) was selected.

Inductor Selection

This section explains how to select inductors (L1 and L2). Although the maximum output power of this design is 10kW, an inductor capable of outputting up to 15kW was adopted for expandability. Since the inductor is located on the low-voltage side, the approximate number of required inductance values (L) can be calculated using the following items, assuming that the low-voltage side is the input (V_{in}) and the high-voltage side is the output (V_{out}).

- Input voltage: V_{in} (V)
- Output Voltage: V_{out} (V)
- Output Power: P_{out} (W)
- Winding ratio: n
- Switching frequency: F_c (Hz)
- Phase difference between input and output sides (overlap angle): θ (degree)

The current I_L applied to the inductor is expressed by the following equation.

$$I_L = \frac{2 \times P_{out}}{V_{out}}$$

Assuming that P_{out} is 15kW and V_{out} is 750V, I_L is 40A.

The inductance value L for outputting this I_L = 40A when the phase difference θ is calculated by the following equation.

$$L = \left(V_{in} + V_{out} \times \frac{1}{n}\right) \times \frac{\theta}{180} \times \frac{1}{F_c \times 2} \times \frac{1}{4I_L}$$

Here, assuming that F_c is 50kHz and θ is 25 degrees for controllability, the above inductance value L is calculated as 6.96μH, so an inductor of 6μH is selected for this design.

In the actual design, the inductance value of the inductor varies depending on the DC superimposition characteristics. Select a component that can secure the above calculated value while the inductance value is decreased due to DC superimposition characteristics.

3.3. Low-voltage Side Circuit Design

This section describes the design of the low-voltage side circuit of this design.

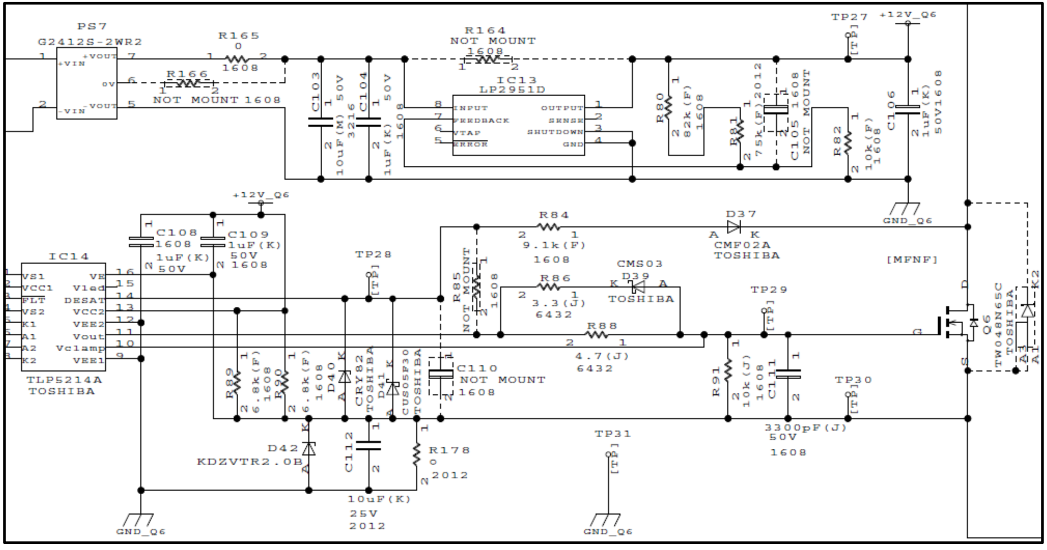


Figure 3.2 Gate Drive Circuit (Low-voltage Side Lower-arm)

Gate Drive Circuit

As a representative example, this section describes the gate drive circuits of low-voltage side. The gate drive circuit of the lower arm side MOSFET Q6 is shown in Figure 3.2. The design of the gate drive circuit affects power supply efficiency and EMI noise. Generally, power supply efficiency and EMI noise have a trade-off relationship, so it is necessary to design both in a balanced manner. The gate-drive circuit of this design has a circuit configuration that can adjust the switching speed of MOSFET. If it is necessary to reduce turn-on noise, changing the gate series resistor (R88) to a large value may reduce EMI noise. Note that if the gate-series resistor is changed to a large value, not only the turn-on speed of MOSFET but also the turn-off speed will be reduced, which may result in worsening of the power supply efficiency. In this situation, in order to reduce power-efficiency degradation only MOSFET turn-off speed should be increased. Changing the gate-series resistor (R86) to a small value may only increase the turn-off speed of MOSFET and reduce the power-efficiency degradation of the system. When changing the gate series resistance, it is necessary to confirm that the EMI noise, power efficiency performance, and heat dissipation performance required for the system are satisfied.

Negative Bias Circuit

Use a negative-bias circuit if there is a risk of malfunction due to the parasitic mirror capacitance between the drain-gate of MOSFET. Figure 3.2 shows the gate drive circuit used on the lower arm side. When the lower arm is turned off and the upper arm is turned on, the intermediate potential rises steeply and displacement current is generated through the mirror capacitance between the drain and gate of the lower arm, and flows toward VOUT terminal of the smart gate driver coupler (IC14). When this displacement current passes through the gate resistor of the circuit, a voltage drop occurs, and when the gate voltage rises, the lower arm may be erroneously turned on, resulting in a short circuit of the upper and lower arms. This design did not confirm such erroneous ON. However, measures must be taken when erroneous ON occurs due to the board layout and wiring in actual applications.

Generally, as a countermeasure against erroneous ON, it is effective to bias the voltage at gate-off to the negative voltage. Although this design does not bias the gate to a negative voltage, a negative bias circuit using a zener diode (D42) is easily realized. By removing the 0Ω resistor (R178) placed in parallel with the D42 and placing a capacitor of about 1μF, a negative bias equivalent to the zener voltage is applied to the gate during gate-off. Although a 2V zener diode is used for this design, select an appropriate element according to the actual operation.

Output Capacitor

When the power supply is operating with low-voltage side as power supply output, the capacitance value of the output capacitors (C146 to C152) is calculated based on the hold-up time requirement. The hold-up time $Thold_{low}$ is calculated by the following equation, where the combined capacitance value of the output capacitors is $Cout_{low}$, the output voltage is $Vout_{low}$, the minimum output voltage is $Vout_{low\_min}$, and the maximum output power is Pout.

$$Thold_{low} = Cout_{low} \times \frac{(Vout_{low}^2 - Vout_{low\_min}^2)}{2 \times Pout}$$

The initial setting is $Cout_{low}$ = 2820µF (6 parallel of 470µF), $Vout_{low}$ = 400V, $Vout_{low\_min}$ = 370V, Pout = 10kW, and the hold-up time is 3.25ms. Adjust the capacitance value of the output capacitor to satisfy the hold-up time required for the system in practical applications. In addition, when the output ripple specification is defined, the capacitance value required to satisfy the output ripple specification must be calculated and compared with the capacitance value that satisfies the hold-up time, and the larger capacitance value must be used. In addition, tolerances and aging degradation must be considered when selecting a capacitor.

Terms of Use

This terms of use is made between Toshiba Electronic Devices and Storage Corporation ("We") and Customer who downloads or uses this Reference Design. Customer shall comply with this terms of use. This Reference Design means all documents and data in order to design electronics applications on which our semiconductor device is embedded.

Section 1. Restrictions on usage

1. This Reference Design is provided solely as reference data for designing electronics applications. Customer shall not use this Reference Design for any other purpose, including without limitation, verification of reliability.
2. Customer shall not use this Reference Design for sale, lease or other transfer.
3. Customer shall not use this Reference Design for evaluation in high or low temperature, high humidity, or high electromagnetic environments.
4. This Reference Design shall not be used for or incorporated into any product or system whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
5. This Reference Design shall not be used in any manner that is contrary to the precautions specified by us.

Section 2. Limitations

1. We reserve the right to make changes to this Reference Design without notice.
2. This Reference Design should be treated as a reference only. WE ARE NOT RESPONSIBLE FOR ANY INCORRECT OR INCOMPLETE DATA AND INFORMATION.
3. Semiconductor devices can malfunction or fail. When designing electronics applications by referring to this Reference Design, Customer is responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of semiconductor devices could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Customer must also refer to and comply with the latest versions of all relevant our information, including without limitation, specifications, data sheets and application notes for semiconductor devices, as well as the precautions and conditions set forth in the "Semiconductor Reliability Handbook".
4. Designing electronics applications by referring to this Reference Design, Customer must evaluate the whole system sufficiently. Customer is solely responsible for applying this Reference Design to Customer's own product design or applications. WE ASSUME NO LIABILITY FOR CUSTOMER'S PRODUCT DESIGN OR APPLICATIONS.
5. WE SHALL NOT BE RESPONSIBLE FOR ANY INFRINGEMENT OF PATENTS OR ANY OTHER INTELLECTUAL PROPERTY RIGHTS OF THIRD PARTIES THAT MAY RESULT FROM THE USE OF THIS REFERENCE DESIGN. NO LICENSE TO ANY INTELLECTUAL PROPERTY RIGHT IS GRANTED BY THIS TERMS OF USE, WHETHER EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE.
6. THIS REFERENCE DESIGN IS PROVIDED "AS IS". WE (a) ASSUME NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (b) DISCLAIM ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO THIS REFERENCE DESIGN, INCLUDING WITHOUT LIMITATION, WARRANTIES OR CONDITIONS OF FUNCTION AND WORKING, WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.

Section 3. Terms and Termination

It is assumed that Customer agrees to any and all this terms of use if Customer downloads or uses this Reference Design. We may, at its sole and exclusive discretion, change, alter, modify, add, and/or remove any part of this terms of use at any time without any prior notice. We may terminate this terms of use at any time and without any cause. Upon termination of this terms of use, Customer shall eliminate this Reference Design. Furthermore, upon our request, Customer shall submit to us a written confirmation to prove elimination of this Reference Design.

Section 4. Export Control

Customer shall not use or otherwise make available this Reference Design for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). This Reference Design may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Act and the U.S. Export Administration Regulations. Export and re-export of this Reference Design is strictly prohibited except in compliance with all applicable export laws and regulations.

Section 5. Governing Laws

This terms of use shall be governed and construed by laws of Japan, without reference to conflict of law principle.

Section 6. Jurisdiction

Unless otherwise specified, Tokyo District Court in Tokyo, Japan shall be exclusively the court of first jurisdiction for all disputes under this terms of use.