32-bit RISC Microcontroller

TXZ+ Family TMPM4V Group(1)

Reference Manual Product Information (PINFO-M4V(1))

Revision 1.0

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-PMD2	Advanced Programmable Motor Control Circuit 2
CRC	Cyclic Redundancy Check
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
EHOSC	External High-speed Oscillator
EI2C	I^2C Interface Version A
IHOSC	Internal High-speed Oscillator
INT	Interrupt
LVD	Voltage Detection Circuit
OFD	Oscillation Frequency Detector
RAMP	RAM Parity
SIWDT	Clock Selective Watchdog Timer
SMIF	Serial Memory Interface
TRGSEL	Trigger Selection Circuit
TRM	Trimming Circuit
TSPI	Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Asynchronous Serial Communication Circuit

1. Outlines

Refer to this reference manual when using peripheral functions.

- Base addresses of peripheral functions
- Signal connections between peripheral functions
- Product-specific specifications for peripheral functions
- Product-specific restrictions for peripheral functions
- Registers with specific values for each product
- Registers that require specific values to be set for each product

Observe the product-specific restrictions.
If there are no signal connections between peripheral functions, do not use the corresponding function.
Be sure to set any registers that require setting of specific values.

2. Register Base Address

The following table shows the base addresses of each peripheral.

Table 2.1 Register Base Address (1/2)

Peripheral function			Base address
Clock Control and Operation Mode	CG	-	0x40083000
Interrupt Control A	IA	-	0x4003E000
Low-speed Oscillation/Power Control/Reset	RLM	-	0x4003E400
Interrupt Control B	IB	-	0x40083200
Interrupt Monitor	IMN	-	0x40083300
Port A	PORT A	-	0x40080000
Port B	PORT B	-	0x40080100
Port C	PORT C	-	0x40080200
Port D	PORT D	-	0x40080300
Port E	PORT E	-	0x40080400
Port F	PORT F	-	0x40080500
Port G	PORT G	-	0x40080600
Port H	PORT H	-	0x40080700
Port J	PORT J	-	0x40080800
Drive Capacity Control	DRV	-	0x40090000
Trigger Selector	TRGSEL	-	0x40040400
Trimming Circuit	TRM	-	0x40083100
Oscillation Frequency Detector	OFD	-	0x40084000
Voltage Detection Circuit	LVD	-	0x4003EC00
Digital Noise Filter Circuit	DNF	unit A	0x40040200
		unit B	0x40040300
Direct Memory Access Controller	DMAC	unit A	0x40044000
Asynchronous Serial Communication Circuit	UART	ch0	0x4006E000
		ch1	0x4006E400
		ch2	0x4006E800
		ch3	0x4006EC00
		ch4	0x4006F000
		ch5	0x4006F400

Table 2.2 Register Base Address (2/2)

Peripheral function			Base address
Serial Peripheral Interface	TSPI	ch0	0x4006A000
		ch1	0x4006A400
		ch2	0x4006A800
Serial Memory Interface	SMIF	ch0	0x4003C000
I^2C Interface Version A	EI2C	ch0	0x40071000
		ch1	0x40072000
12-bit Analog to Digital Converter	ADC	unit A	0x4005A000
Advanced Programmable Motor Control Circuit 2	A-PMD2	ch0	0x40068C00
32-bit Timer Event Counter	T32A	ch0	0x40061000
		ch1	0x40061400
		ch2	0x40061800
		ch3	0x40061C00
		ch4	0x40062000
Clock Selective Watchdog Timer	SIWDT	ch0	0x40040600
Flash Memory	Flash	-	0x5DFF0000
Secure Access Memory	SAM	-	0x40043400
CRC Calculation Circuit	CRC	-	0x40043100
RAM Parity	RAMP	ch0	0x40043000

3. Trigger Selector (TRGSEL)

The trigger selector is the circuit which chooses the one trigger and outputs the trigger signal to the peripheral function from maximum eight triggers inputted from the peripheral function, the port, etc.

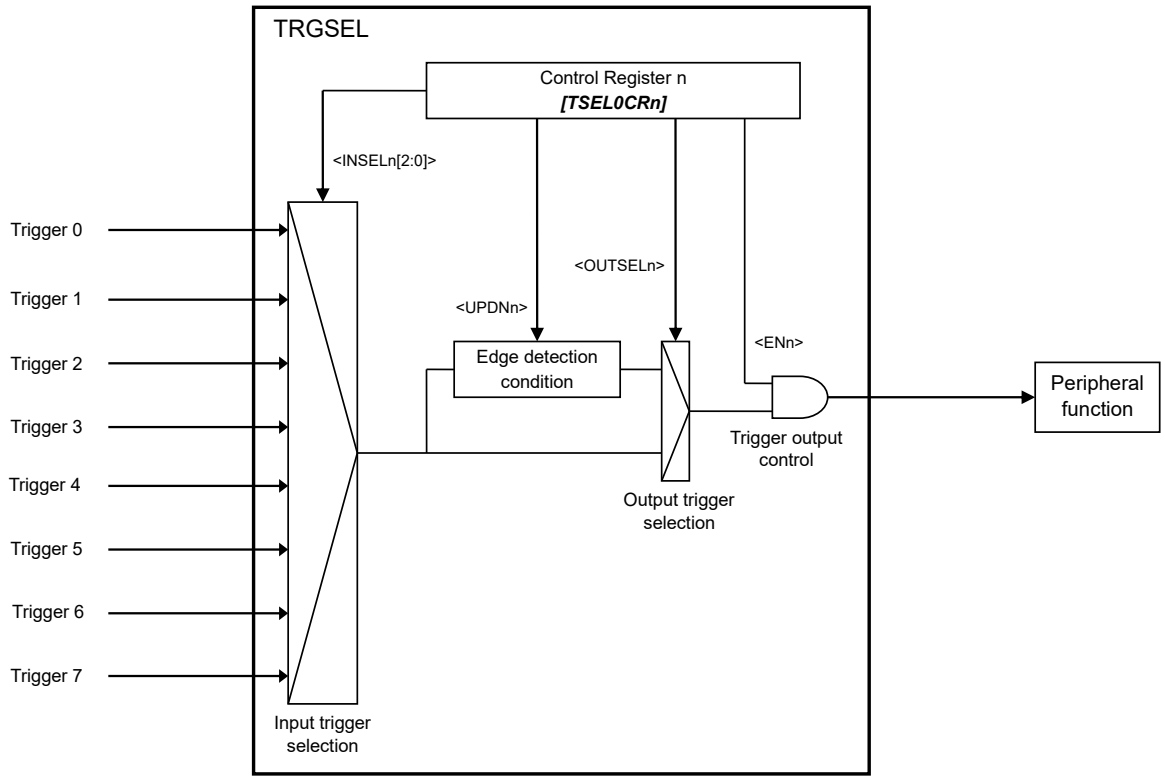

Figure 3.1 Trigger Selector Connection

3.1. Operation and Setting

When using TRGSEL, please set an applicable clock enable bit to "1" (clock supply) in fsys supply stop register A (***[CGFSYSENA]***), fsys supply stop register B (***[CGFSYSENB]***), and fc supply stop registers (***[CGFCEN]***).
An applicable register and the bit position vary according to a product. Therefore, the register may not exist with the product. Please refer to "Clock Control and Operation Mode" of the reference manual for the details.

Setting procedure of Trigger selector is as following.

(1) Selection of an input trigger (***[TSEL0CRn]*** <INSELm>)

Selection of the input trigger used for the trigger source is performed.

Please set up selection of the input trigger by the input trigger subdevice bit (***[TSEL0CRn]*** <INSELm>) of the control register. (n: register number, m: trigger number)

(2) Selection of edge detection conditions (***[TSEL0CRn]*** <UPDNm>)

For the input trigger signal which needs edge detection, selection of rising edge or falling edge detection is performed.

Please set up selection of edge detection conditions in the selection bit (***[TSEL0CRn]***<UPDNm>) of a control register.

The following shows the trigger signal which needs edge detection.

- External trigger input (TRGIN0, TRGIN1, and TRGIN2)

(3) Selection of a trigger output (***[TSEL0CRn]***<OUTSELm>)

Selection of an output without or with edge detection is performed.

Please set up selection of a trigger output in the selection bit (***[TSEL0CRn]***<OUTSELm>) of a control register.

(4) Output enable (***[TSEL0CRn]***<ENm>)

The output (enable/disable) of the selected trigger signal is chosen.

Please set up selection of output (enable/disable) in the setting bit (***[TSEL0CRn]***<ENm>) of a control register. A trigger output will be enabled if ***[TSEL0CRn]***<ENm> is set as "1".

3.2. Register

3.2.1. List of Registers

The table below shows control registers and their addresses.

Peripheral function		Channel/unit	Base address
Trigger Selector	TRGSEL	ch0	0x40040400

Register name		Address (Base+)
Control Register 0	***[TSELxCR0]***	0x0000
Control Register 1	***[TSELxCR1]***	0x0004
Control Register 2	***[TSELxCR2]***	0x0008
Control Register 3	***[TSELxCR3]***	0x000C
Control Register 4	***[TSELxCR4]***	0x0010
Control Register 5	***[TSELxCR5]***	0x0014
Control Register 6	***[TSELxCR6]***	0x0018
Control Register 7	***[TSELxCR7]***	0x001C
Control Register 8	***[TSELxCR8]***	0x0020
Control Register 9	***[TSELxCR9]***	0x0024
Control Register 10	***[TSELxCR10]***	0x0028

3.2.2. Details of Registers

The details of the register are as follows:

One register (***[TSELxCRn]***) can control four trigger selectors (INSEL0 to 3). For input trigger assignments, refer to "3.3. Trigger Selector List". Settings without input trigger assignments cannot be used.

3.2.2.1. *[TSELxCRn]* (Control Register n) (n = 0 to 10)

Bit	Bit symbol	After reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL3[2:0]	000	R/W	Select the input trigger 000: Trigger 30 001: Trigger 31 010: Trigger 32 011: Trigger 33 100: Trigger 34 101: Trigger 35 110: Trigger 36 111: Trigger 37
27	-	0	R	Read as 0
26	UPDN3	0	R/W	Edge detection 0: Rising edge detection 1: falling edge detection
25	OUTSEL3	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN3	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL2[2:0]	000	R/W	Select the input trigger 000: Trigger 20 001: Trigger 21 010: Trigger 22 011: Trigger 23 100: Trigger 24 101: Trigger 25 110: Trigger 26 111: Trigger 27
19	-	0	R	Read as 0
18	UPDN2	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL2	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN2	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0

Bit	Bit symbol	After reset	Type	Function
14:12	INSEL1[2:0]	000	R/W	Select the input trigger 000: Trigger 10 001: Trigger 11 010: Trigger 12 011: Trigger 13 100: Trigger 14 101: Trigger 15 110: Trigger 16 111: Trigger 17
11	-	0	R	Read as 0
10	UPDN1	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL1	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN1	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL0[2:0]	000	R/W	Select the input trigger 000: Trigger 00 001: Trigger 01 010: Trigger 02 011: Trigger 03 100: Trigger 04 101: Trigger 05 110: Trigger 06 111: Trigger 07
3	-	0	R	Read as 0
2	UPDN0	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL0	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN0	0	R/W	Trigger output control 0: Disable 1: Enable

3.3. Trigger Selector List

The table below shows the control registers, their connections points, and the corresponding products.

Table 3.1 Trigger Selector List for Each Product (1/6)

Register	Bit symbol	Destination	Trigger source		Product (✓:Available, -:N/A)		
					M4V4	M4V2	M4V1
[TSEL0CR0]	INSEL0	DMA ch0	Trigger 00	TSPI ch0 receive DMA request	✓	-	-
			Trigger 01	EI2C ch0 receive DMA request	✓	✓	✓
			Trigger 02	EI2C ch1 receive DMA request	✓	-	-
	INSEL1	DMA ch1	Trigger 10	TSPI ch0 transmit DMA request	✓	-	-
			Trigger 11	EI2C ch0 transmit DMA request	✓	✓	✓
			Trigger 12	EI2C ch1 transmit DMA request	✓	-	-
	INSEL2	DMA ch8	Trigger 20	UART ch1 reception DMA request	✓	✓	✓
			Trigger 21	EI2C ch0 receive DMA request	✓	✓	✓
			Trigger 22	EI2C ch1 receive DMA request	✓	-	-
	INSEL3	DMA ch9	Trigger 30	UART ch1 transmission DMA request	✓	✓	✓
			Trigger 31	EI2C ch0 transmit DMA request	✓	✓	✓
			Trigger 32	EI2C ch1 transmit DMA request	✓	-	-
[TSEL0CR1]	INSEL0	DMA ch18	Trigger 00	ADC unit A general purpose trigger DMA request	✓	✓	✓
			Trigger 01	ADC unit A single conversion DMA request			
			Trigger 02	ADC unit A continuous conversion DMA request			
	INSEL1	-	-	-	-	-	-
	INSEL2	DMA ch20	Trigger 20	T32A ch0 DMA request at match A1 register	✓	✓	✓
			Trigger 21	T32A ch0 DMA request at match C1 register			
			Trigger 22	T32A ch1 DMA request at match A1 register			
			Trigger 23	T32A ch1 DMA request at match C1 register			
			Trigger 24	SMIF interrupt			
	INSEL3	DMA ch21	Trigger 30	T32A ch2 DMA request at match A1 register	✓	✓	✓
			Trigger 31	T32A ch2 DMA request at match C1 register			
			Trigger 32	T32A ch3 DMA request at match A1 register			
			Trigger 33	T32A ch3 DMA request at match C1 register			
			Trigger 34	A-PMD2 ch0 PWM interrupt			

Table 3.2 Trigger Selector List for Each Product (2/6)

Register	Bit symbol	Destination	Trigger source		Product (✓:Available, -:N/A)		
					M4V4	M4V2	M4V1
[TSEL0CR2]	INSEL0	DMA ch22	Trigger 00	T32A ch4 DMA request at match A1 register	✓	✓	✓
			Trigger 01	T32A ch4 DMA request at match C1 register			
			Trigger 02	T32A ch0 DMA request at match B1 register			
			Trigger 03	T32A ch1 DMA request at match B1 register			
			Trigger 04	T32A ch2 DMA request at match B1 register			
			Trigger 05	T32A ch3 DMA request at match B1 register			
			Trigger 06	T32A ch4 DMA request at match B1 register			
	INSEL1	DMA ch23	Trigger 10	T32A ch0 DMA request at capture A0 register	✓	✓	✓
			Trigger 11	T32A ch0 DMA request at capture A1 register			
			Trigger 12	T32A ch1 DMA request at capture A0 register			
			Trigger 13	T32A ch1 DMA request at capture A1 register			
			Trigger 14	T32A ch0 DMA request at capture C0 register			
			Trigger 15	T32A ch0 DMA request at capture C1 register			
			Trigger 16	T32A ch1 DMA request at capture C0 register			
			Trigger 17	T32A ch1 DMA request at capture C1 register			
	INSEL2	DMA ch24	Trigger 20	T32A ch2 DMA request at capture A0 register	✓	✓	✓
			Trigger 21	T32A ch2 DMA request at capture A1 register			
			Trigger 22	T32A ch3 DMA request at capture A0 register			
			Trigger 23	T32A ch3 DMA request at capture A1 register			
			Trigger 24	T32A ch2 DMA request at capture C0 register			
			Trigger 25	T32A ch2 DMA request at capture C1 register			
			Trigger 26	T32A ch3 DMA request at capture C0 register			
			Trigger 27	T32A ch3 DMA request at capture C1 register			
	INSEL3	DMA ch25	Trigger 30	T32A ch4 DMA request at capture A0 register	✓	✓	✓
			Trigger 31	T32A ch4 DMA request at capture A1 register			
			Trigger 32	T32A ch4 DMA request at capture C0 register			
			Trigger 33	T32A ch4 DMA request at capture C1 register			
[TSEL0CR3]	INSEL0	DMA ch26	Trigger 00	T32A ch0 DMA request at capture B0 register	✓	✓	✓
			Trigger 01	T32A ch0 DMA request at capture B1 register			
			Trigger 02	T32A ch1 DMA request at capture B0 register			
			Trigger 03	T32A ch1 DMA request at capture B1 register			
			Trigger 04	T32A ch2 DMA request at capture B0 register			
			Trigger 05	T32A ch2 DMA request at capture B1 register			
	INSEL1	DMA ch27	Trigger 10	T32A ch3 DMA request at capture B0 register	✓	✓	✓
			Trigger 11	T32A ch3 DMA request at capture B1 register			
			Trigger 12	T32A ch4 DMA request at capture B0 register			
			Trigger 13	T32A ch4 DMA request at capture B1 register			
	INSEL2	DMA ch28	Trigger 20	DMAC ch0 transfer completion	✓	-	-
			Trigger 21	DMAC ch1 transfer completion			
			Trigger 22	DMAC ch8 transfer completion	✓	✓	✓
			Trigger 23	DMAC ch9 transfer completion			
			Trigger 24	DMAC ch16 transfer completion	✓	✓	-
			Trigger 25	DMAC ch17 transfer completion			
			Trigger 26	DMAC ch22 transfer completion	✓	✓	✓
	INSEL3	DMA ch29	Trigger 30	DMAC ch2 transfer completion	✓	✓	✓
			Trigger 31	DMAC ch3 transfer completion			
			Trigger 32	DMAC ch10 transfer completion			
			Trigger 33	DMAC ch11 transfer completion			
			Trigger 34	DMAC ch18 transfer completion			
			Trigger 36	DMAC ch23 transfer completion			
			Trigger 37	PC0 pin (TRGIN0)	✓	✓	✓

Table 3.3 Trigger Selector List for Each Product (3/6)

Register	Bit symbol	Destination	Trigger source		Product (✓:Available, -:N/A)		
					M4V4	M4V2	M4V1
[TSEL0CR4]	INSEL0	DMA ch30	Trigger 00	DMAC ch4 transfer completion	✓	✓	✓
			Trigger 01	DMAC ch5 transfer completion			
			Trigger 02	DMAC ch12 transfer completion			
			Trigger 03	DMAC ch13 transfer completion			
			Trigger 04	DMAC ch20 transfer completion			
			Trigger 05	DMAC ch24 transfer completion			
			Trigger 06	DMAC ch26 transfer completion			
			Trigger 07	PA5 pin (TRGIN1)	✓	✓	✓
	INSEL1	DMA ch31	Trigger 10	DMAC ch6 transfer completion	✓	✓	✓
			Trigger 11	DMAC ch7 transfer completion			
			Trigger 12	DMAC ch14 transfer completion	✓	-	-
			Trigger 13	DMAC ch15 transfer completion			
			Trigger 14	DMAC ch21 transfer completion	✓	✓	✓
			Trigger 15	DMAC ch25 transfer completion			
			Trigger 16	DMAC ch27 transfer completion			
			Trigger 17	PG1 pin (TRGIN2)	✓	✓	-
	INSEL2	ADC unit A	Trigger 20	PC0 pin (TRGIN0)	✓	✓	✓
			Trigger 21	PA5 pin (TRGIN1)	✓	✓	✓
			Trigger 22	PG1 pin (TRGIN2)	✓	✓	-
			Trigger 23	T32A ch0 timer register A1 match trigger	✓	✓	✓
			Trigger 24	T32A ch0 timer register B1 match trigger			
			Trigger 25	T32A ch0 timer register C1 match trigger			
			Trigger 26	T32A ch3 timer register A0 match trigger			
			Trigger 27	T32A ch4 timer register A0 match trigger			
	INSEL3	ADC unit B	Trigger 30	PC0 pin (TRGIN0)	✓	✓	✓
			Trigger 31	PA5 pin (TRGIN1)	✓	✓	✓
			Trigger 32	PG1 pin (TRGIN2)	✓	✓	-
			Trigger 33	T32A ch1 timer register A1 match trigger	✓	✓	✓
			Trigger 34	T32A ch1 timer register B1 match trigger			
			Trigger 35	T32A ch1 timer register C1 match trigger			
			Trigger 36	T32A ch3 timer register A1 match trigger			
			Trigger 37	T32A ch4 timer register A1 match trigger			
[TSEL0CR5]	INSEL0	TSPI ch0	Trigger 00	PC0 pin (TRGIN0)	✓	✓	✓
			Trigger 01	PA5 pin (TRGIN1)	✓	✓	✓
			Trigger 02	PG1 pin (TRGIN2)	✓	✓	-
			Trigger 03	T32A ch3 timer register A1 match trigger	✓	✓	✓
			Trigger 04	T32A ch3 timer register B1 match trigger			
			Trigger 05	T32A ch3 timer register C1 match trigger			
	INSEL1	TSPI ch1	Trigger 10	PC0 pin (TRGIN0)	✓	✓	✓
			Trigger 11	PA5 pin (TRGIN1)	✓	✓	✓
			Trigger 12	PG1 pin (TRGIN2)	✓	✓	-
			Trigger 13	T32A ch3 timer register A1 match trigger	✓	✓	✓
			Trigger 14	T32A ch3 timer register B1 match trigger			
			Trigger 15	T32A ch3 timer register C1 match trigger			
	INSEL2	TSPI ch2	Trigger 20	PC0 pin (TRGIN0)	✓	✓	✓
			Trigger 21	PA5 pin (TRGIN1)	✓	✓	✓
			Trigger 22	PG1 pin (TRGIN2)	✓	✓	-
			Trigger 23	T32A ch3 timer register A1 match trigger	✓	✓	✓
			Trigger 24	T32A ch3 timer register B1 match trigger			
			Trigger 25	T32A ch3 timer register C1 match trigger			
	INSEL3	UART ch0	Trigger 30	PC0 pin (TRGIN0)	✓	✓	✓
			Trigger 31	PA5 pin (TRGIN1)	✓	✓	✓
			Trigger 32	PG1 pin (TRGIN2)	✓	✓	-
			Trigger 33	T32A ch3 timer register A1 match trigger	✓	✓	✓
			トリガー34	T32A ch3 timer register B1 match trigger			
			トリガー35	T32A ch3 timer register C1 match trigger			

Table 3.4 Trigger Selector List for Each Product (4/6)

Register	Bit symbol	Destination	Trigger source		Product (✓:Available, -:N/A)		
					M4V4	M4V2	M4V1
[TSEL0CR6]	INSEL0	UART ch1	Trigger 00	PC0 pin (TRGIN0)	✓	✓	✓
			Trigger 01	PA5 pin (TRGIN1)	✓	✓	✓
			Trigger 02	PG1 pin (TRGIN2)	✓	✓	-
			Trigger 03	T32A ch3 timer register A1 match trigger	✓	✓	✓
			Trigger 04	T32A ch3 timer register B1 match trigger			
			Trigger 05	T32A ch3 timer register C1 match trigger			
	INSEL1	UART ch2	Trigger 10	PC0 pin (TRGIN0)	✓	✓	✓
			Trigger 11	PA5 pin (TRGIN1)	✓	✓	✓
			Trigger 12	PG1 pin (TRGIN2)	✓	✓	-
			Trigger 13	T32A ch3 timer register A1 match trigger	✓	✓	✓
			Trigger 14	T32A ch3 timer register B1 match trigger			
			Trigger 15	T32A ch3 timer register C1 match trigger			
	INSEL2	UART ch3	Trigger 20	PC0 pin (TRGIN0)	✓	✓	✓
			Trigger 21	PA5 pin (TRGIN1)	✓	✓	✓
			Trigger 22	PG1 pin (TRGIN2)	✓	✓	-
			Trigger 23	T32A ch3 timer register A1 match trigger	✓	✓	✓
			Trigger 24	T32A ch3 timer register B1 match trigger			
			Trigger 25	T32A ch3 timer register C1 match trigger			
	INSEL3	UART ch4	Trigger 30	PC0 pin (TRGIN0)	✓	✓	✓
			Trigger 31	PA5 pin (TRGIN1)	✓	✓	✓
			Trigger 32	PG1 pin (TRGIN2)	✓	✓	-
			Trigger 33	T32A ch3 timer register A1 match trigger	✓	-	-
			Trigger 34	T32A ch3 timer register B1 match trigger			
			Trigger 35	T32A ch3 timer register C1 match trigger			
[TSEL0CR7]	INSEL0	UART ch5	Trigger 00	PC0 pin (TRGIN0)	✓	✓	✓
			Trigger 01	PA5 pin (TRGIN1)	✓	✓	✓
			Trigger 02	PG1 pin (TRGIN2)	✓	✓	-
			Trigger 03	T32A ch3 timer register A1 match trigger	✓	✓	-
			Trigger 04	T32A ch3 timer register B1 match trigger			
			Trigger 05	T32A ch3 timer register C1 match trigger			
	INSEL1	TRGSEL *[TSEL0CR8]* <INSEL2> input *[TSEL0CR9]* <INSEL2> input *[TSEL0CR10]* <INSEL0> input <INSEL2> input	Trigger 10	PC0 pin (TRGIN0)	✓	✓	✓
			Trigger 11	PA5 pin (TRGIN1)	✓	✓	✓
			Trigger 12	PG1 pin TRGIN2)	✓	✓	-
			Trigger 13	UART ch4 transmission completion trigger	✓	-	-
			Trigger 14	UART ch4 reception completion trigger			
			Trigger 15	TSPI ch1 transmit completion trigger	✓	✓	✓
			Trigger 16	TSPI ch1 receive completion trigger			
			Trigger 17	EI2C ch0 status interrupt			
	INSEL2	TRGSEL *[TSEL0CR8]* <INSEL2> input *[TSEL0CR9]* <INSEL0> input *[TSEL0CR10]* <INSEL0> input <INSEL2> input	Trigger 20	PC0 pin (TRGIN0)	✓	✓	✓
			Trigger 21	PA5 pin (TRGIN1)	✓	✓	✓
			Trigger 22	PG1 pin (TRGIN2)	✓	✓	-
			Trigger 23	UART ch1 transmission completion trigger	✓	✓	✓
			Trigger 24	UART ch1 reception completion trigger			
			Trigger 25	TSPI ch0 transmit completion trigger	✓	-	-
			Trigger 26	TSPI ch0 receive completion trigger			
			Trigger 27	EI2C ch1 status interrupt	✓	✓	-
	INSEL3	TRGSEL *[TSEL0CR8]* <INSEL2> input *[TSEL0CR9]* <INSEL0> input <INSEL2> input *[TSEL0CR10]* <INSEL2> input	Trigger 30	PC0 pin (TRGIN0)	✓	✓	✓
			Trigger 31	PA5 pin (TRGIN1)	✓	✓	✓
			Trigger 32	PG1 pin (TRGIN2)	✓	✓	-
			Trigger 33	UART ch2 transmission completion trigger	✓	✓	✓
			Trigger 34	UART ch2 reception completion trigger			
			Trigger 35	TSPI ch2 transmit completion trigger			
			Trigger 36	TSPI ch2 receive completion trigger			

Table 3.5 Trigger Selector List for Each Product (5/6)

Register	Bit symbol	Destination	Trigger source		Product (✓:Available, -:N/A)		
					M4V4	M4V2	M4V1
[TSEL0CR8]	INSEL0	TRGSEL ***[TSEL0CR8]*** <INSEL2> input ***[TSEL0CR9]*** <INSEL0> input <INSEL2> input ***[TSEL0CR10]*** <INSEL0> input	Trigger 00	PC0 pin (TRGIN0)	✓	✓	✓
			Trigger 01	UART ch3 transmission completion trigger	✓	✓	✓
			Trigger 02	UART ch3 reception completion trigger			
			Trigger 03	ADC unit A general purpose trigger interrupt			
			Trigger 04	ADC unit A single conversion interrupt			
			Trigger 05	ADC unit A continuous conversion interrupt			
			Trigger 06	ADC unit A monitor function 0 Interrupt			
			Trigger 07	ADC unit A monitor function 1 Interrupt			
	INSEL1	TRGSEL ***[TSEL0CR9]*** <INSEL0> input <INSEL2> input ***[TSEL0CR10]*** <INSEL0> input <INSEL2> input	Trigger 10	UART ch0 transmission completion trigger	✓	✓	✓
			Trigger 11	UART ch0 reception completion trigger			
			Trigger 12	UART ch5 transmission completion trigger	✓	✓	-
			Trigger 13	UART ch5 reception completion trigger			
	INSEL2	T32A ch0 timer A	Trigger 20	T32A ch0 timer register B0 match trigger	✓	✓	✓
			Trigger 21	T32A ch0 timer register B1 match trigger			
			Trigger 22	T32A ch0 timer B overflow trigger			
			Trigger 23	T32A ch0 timer B underflow trigger			
			Trigger 24	***[TSEL0CR7]***<INSEL1> output			
			Trigger 25	***[TSEL0CR7]***<INSEL2> output			
			Trigger 26	***[TSEL0CR7]***<INSEL3> output			
			Trigger 27	***[TSEL0CR8]***<INSEL0> output			
	INSEL3	T32A ch0 timer B	Trigger 30	T32A ch0 timer register A0 match trigger	✓	✓	✓
			Trigger 31	T32A ch0 timer register A1 match trigger			
			Trigger 32	T32A ch0 timer A overflow trigger			
			Trigger 33	T32A ch0 timer A underflow trigger			
[TSEL0CR9]	INSEL0	T32A ch1 timer A	Trigger 00	T32A ch1 timer register B0 match trigger	✓	✓	✓
			Trigger 01	T32A ch1 timer register B1 match trigger			
			Trigger 02	T32A ch1 timer B overflow trigger			
			Trigger 03	T32A ch1 timer B underflow trigger			
			Trigger 04	***[TSEL0CR7]***<INSEL2> output			
			Trigger 05	***[TSEL0CR7]***<INSEL3> output			
			Trigger 06	***[TSEL0CR8]*** INSEL0> output			
			Trigger 07	***[TSEL0CR8]***<INSEL1> output			
	INSEL1	T32A ch1 timer B	Trigger 10	T32A ch1 timer register A0 match trigger	✓	✓	✓
			Trigger 11	T32A ch1 timer register A1 match trigger			
			Trigger 12	T32A ch1 timer A overflow trigger			
			Trigger 13	T32A ch1 timer A underflow trigger			
	INSEL2	T32A ch2 timer A	Trigger 20	T32A ch2 timer register B0 match trigger	✓	✓	✓
			Trigger 21	T32A ch2 timer register B1 match trigger			
			Trigger 22	T32A ch2 timer B overflow trigger			
			Trigger 23	T32A ch2 timer B underflow trigger			
			Trigger 24	***[TSEL0CR7]***<INSEL3> output			
			Trigger 25	***[TSEL0CR8]***<INSEL0> output			
			Trigger 26	***[TSEL0CR8]***<INSEL1> output			
			Trigger 27	***[TSEL0CR7]***<INSEL1> output			
	INSEL3	T32A ch2 timer B	Trigger 30	T32A ch2 timer register A0 match trigger	✓	✓	✓
			Trigger 31	T32A ch2 timer register A1 match trigger			
			Trigger 32	T32A ch2 timer A overflow trigger			
			Trigger 33	T32A ch2 timer A underflow trigger			

Table 3.6 Trigger Selector List for Each Product (6/6)

Register	Bit symbol	Destination	Trigger source		Product (✓:Available, -:N/A)		
					M4V4	M4V2	M4V1
[TSEL0CR10]	INSEL0	T32A ch3 timer A	Trigger 00	T32A ch3 timer register B0 match trigger	✓	✓	✓
			Trigger 01	T32A ch3 timer register B1 match trigger			
			Trigger 02	T32A ch3 timer B overflow trigger			
			Trigger 03	T32A ch3 timer B underflow trigger			
			Trigger 04	***[TSEL0CR8]***<INSEL0> output			
			Trigger 05	***[TSEL0CR8]***<INSEL1> output			
			Trigger 06	***[TSEL0CR7]***<INSEL1> output			
			Trigger 07	***[TSEL0CR7]***<INSEL2> output			
	INSEL1	T32A ch3 timer B	Trigger 10	T32A ch3 timer register A0 match trigger	✓	✓	✓
			Trigger 11	T32A ch3 timer register A1 match trigger			
			Trigger 12	T32A ch3 timer A overflow trigger			
			Trigger 13	T32A ch3 timer A underflow trigger			
	INSEL2	T32A ch4 timer A	Trigger 20	T32A ch4 timer register B0 match trigger	✓	✓	✓
			Trigger 21	T32A ch4 timer register B1 match trigger			
			Trigger 22	T32A ch4 timer B overflow trigger			
			Trigger 23	T32A ch4 timer B underflow trigger			
			Trigger 24	***[TSEL0CR8]***<INSEL1> output			
			Trigger 25	***[TSEL0CR7]***<INSEL1> output			
			Trigger 26	***[TSEL0CR7]***<INSEL2> output			
			Trigger 27	***[TSEL0CR7]***<INSEL3> output			
	INSEL3	T32A ch4 timer B	Trigger 30	T32A ch4 timer register A0 match trigger	✓	✓	✓
			Trigger 31	T32A ch4 timer register A1 match trigger			
			Trigger 32	T32A ch4 timer A overflow trigger			
			Trigger 33	T32A ch4 timer A underflow trigger			

4. Direct Memory Access Controller (DMAC)

4.1. DMA Request List

Following table shows the DMA request List.

The channel which has a register name in the trigger selector column of a table should choose the request used by a trigger selector.

Each EI2C DMA requests are connected to two channels, but one of the channels should be selected for use.

"-" in the table does not have an applicable function.

Table 4.1 DMA Request List (1/4)

Channel	Single transfer		Burst transfer		
		Signal name	Trigger selector		Signal name
0	TSPI ch0 receive DMA request	TSPI0RX_DMA	***[TSEL0CR0]*** <INSEL0>	TSPI ch0 receive DMA request	TSPI0RX_DMA
				EI2C ch0 receive DMA request	I2C0ARXDMAREQ
				EI2C ch1 receive DMA request	I2C1ARXDMAREQ
1	TSPI ch0 transmit DMA request	TSPI0TX_DMA	***[TSEL0CR0]*** <INSEL1>	TSPI ch0 transmit DMA request	TSPI0TX_DMA
				EI2C ch0 transmit DMA request	I2C0ATXDMAREQ
				EI2C ch1 transmit DMA request	I2C1ATXDMAREQ
2	TSPI ch1 receive DMA request	TSPI1RX_DMA	-	TSPI ch1 receive DMA request	TSPI1RX_DMA
3	TSPI ch1 transmit DMA request	TSPI1TX_DMA	-	TSPI ch1 transmit DMA request	TSPI1TX_DMA
4	TSPI ch2 receive DMA request	TSPI2RX_DMA	-	TSPI ch2 receive DMA request	TSPI2RX_DMA
5	TSPI ch2 transmit DMA request	TSPI2TX_DMA	-	TSPI ch2 transmit DMA request	TSPI2TX_DMA
6	UART ch0 reception DMA request	UART0RX_DMAREQ	-	UART ch0 reception DMA request	UART0RX_DMAREQ
7	UART ch0 transmission DMA request	UART0TX_DMAREQ	-	UART ch0 transmission DMA request	UART0TX_DMAREQ
8	UART ch1 reception DMA request	UART1RX_DMAREQ	***[TSEL0CR0]*** <INSEL2>	UART ch1 reception DMA request	UART1RX_DMAREQ
				EI2C ch0 receive DMA request	I2C0ARXDMAREQ
				EI2C ch1 receive DMA request	I2C1ARXDMAREQ
9	UART ch1 transmission DMA request	UART1TX_DMAREQ	***[TSEL0CR0]*** <INSEL3>	UART ch1 transmission DMA request	UART1TX_DMAREQ
				EI2C ch0 transmit DMA request	I2C0ATXDMAREQ
				EI2C ch1 transmit DMA request	I2C1ATXDMAREQ
10	UART ch2 reception DMA request	UART2RX_DMAREQ	-	UART ch2 reception DMA request	UART2RX_DMAREQ
11	UART ch2 transmission DMA request	UART2TX_DMAREQ	-	UART ch2 transmission DMA request	UART2TX_DMAREQ
12	UART ch3 reception DMA request	UART3RX_DMAREQ	-	UART ch3 reception DMA request	UART3RX_DMAREQ
13	UART ch3 transmission DMA request	UART3TX_DMAREQ	-	UART ch3 transmission DMA request	UART3TX_DMAREQ
14	UART ch4 reception DMA request	UART4RX_DMAREQ	-	UART ch4 reception DMA request	UART4RX_DMAREQ
15	UART ch4 transmission DMA request	UART4TX_DMAREQ	-	UART ch4 transmission DMA request	UART4TX_DMAREQ
16	UART ch5 reception DMA request	UART5RX_DMAREQ	-	UART ch5 reception DMA request	UART5RX_DMAREQ
17	UART ch5 transmission DMA request	UART5TX_DMAREQ	-	UART ch5 transmission DMA request	UART5TX_DMAREQ

Note: The ch0, 1, 8 and 9 are set by trigger source of DMA request. For the detail of connection, refer to the "3. Trigger Selector (TRGSEL)".

Table 4.2 DMA Request List (2/4)

Channel	Single transfer		Burst transfer		
		Signal name	Trigger selector		Signal name
18	-	-	*[TSEL0CR1]* <INSEL0>	ADC unit A general purpose trigger	ADATRG_DMAREQ
				ADC unit A single conversion	ADASGL_DMAREQ
				ADC unit A continuous conversion	ADACNT_DMAREQ
19	-	-	-	-	-
20	-	-	*[TSEL0CR1]* <INSEL2>	T32A ch0 DMA request at match A1 register	T32A00DMAREQCMPA1
				T32A ch0 DMA request at match C1 register	T32A00DMAREQCMPC1
				T32A ch1 DMA request at match A1 register	T32A01DMAREQCMPA1
				T32A ch1 DMA request at match C1 register	T32A01DMAREQCMPC1
				SMIF interrupt	INTSMI0
21	-	-	*[TSEL0CR1]* <INSEL3>	T32A ch2 DMA request at match A1 register	T32A02DMAREQCMPA1
				T32A ch2 DMA request at match C1 register	T32A02DMAREQCMPC1
				T32A ch3 DMA request at match A1 register	T32A03DMAREQCMPA1
				T32A ch3 DMA request at match C1 register	T32A03DMAREQCMPC1
				A-PMD2 ch0 PWM interrupt	INTPWM0
22	-	-	*[TSEL0CR2]* <INSEL0>	T32A ch4 DMA request at match A1 register	T32A04DMAREQCMPA1
				T32A ch4 DMA request at match C1 register	T32A04DMAREQCMPC1
				T32A ch0 DMA request at match B1 register	T32A00DMAREQCMPB1
				T32A ch1 DMA request at match B1 register	T32A01DMAREQCMPB1
				T32A ch2 DMA request at match B1 register	T32A02DMAREQCMPB1
				T32A ch3 DMA request at match B1 register	T32A03DMAREQCMPB1
				T32A ch4 DMA request at match B1 register	T32A04DMAREQCMPB1
23	-	-	*[TSEL0CR2]* <INSEL1>	T32A ch0 DMA request at capture A0 register	T32A00DMAREQCAPA0
				T32A ch0 DMA request at capture A1 register	T32A00DMAREQCAPA1
				T32A ch1 DMA request at capture A0 register	T32A01DMAREQCAPA0
				T32A ch1 DMA request at capture A1 register	T32A01DMAREQCAPA1
				T32A ch0 DMA request at capture C0 register	T32A00DMAREQCAPC0
				T32A ch0 DMA request at capture C1 register	T32A00DMAREQCAPC1
				T32A ch1 DMA request at capture C0 register	T32A01DMAREQCAPC0
				T32A ch1 DMA request at capture C1 register	T32A01DMAREQCAPC1
24	-	-	*[TSEL0CR2]* <INSEL2>	T32A ch2 DMA request at capture A0 register	T32A02DMAREQCAPA0
				T32A ch2 DMA request at capture A1 register	T32A02DMAREQCAPA1
				T32A ch3 DMA request at capture A0 register	T32A03DMAREQCAPA0
				T32A ch3 DMA request at capture A1 register	T32A03DMAREQCAPA1
				T32A ch2 DMA request at capture C0 register	T32A02DMAREQCAPC0
				T32A ch2 DMA request at capture C1 register	T32A02DMAREQCAPC1
				T32A ch3 DMA request at capture C0 register	T32A03DMAREQCAPC0
				T32A ch3 DMA request at capture C1 register	T32A03DMAREQCAPC1

Note: The ch18 and 20 to 24 are set by trigger source of DMA request. For the detail of connection, refer to the "3. Trigger Selector (TRGSEL)".

Table 4.3 DMA Request List (3/4)

Channel	Single transfer		Burst transfer		
		Signal name	Trigger selector		Signal name
25	-	-	*[TSEL0CR2]* <INSEL3>	T32A ch4 DMA request at capture A0 register	T32A04DMAREQCAPA0
				T32A ch4 DMA request at capture A1 register	T32A04DMAREQCAPA1
				T32A ch4 DMA request at capture C0 register	T32A04DMAREQCAPC0
				T32A ch4 DMA request at capture C1 register	T32A04DMAREQCAPC1
26	-	-	*[TSEL0CR3]* <INSEL0>	T32A ch0 DMA request at capture B0 register	T32A00DMAREQCAPB0
				T32A ch0 DMA request at capture B1 register	T32A00DMAREQCAPB1
				T32A ch1 DMA request at capture B0 register	T32A01DMAREQCAPB0
				T32A ch1 DMA request at capture B1 register	T32A01DMAREQCAPB1
				T32A ch2 DMA request at capture B0 register	T32A02DMAREQCAPB0
				T32A ch2 DMA request at capture B1 register	T32A02DMAREQCAPB1
27	-	-	*[TSEL0CR3]* <INSEL1>	T32A ch3 DMA request at capture B0 register	T32A03DMAREQCAPB0
				T32A ch3 DMA request at capture B1 register	T32A03DMAREQCAPB1
				T32A ch4 DMA request at capture B0 register	T32A04DMAREQCAPB0
				T32A ch4 DMA request at capture B1 register	T32A04DMAREQCAPB1
28	-	-	*[TSEL0CR3]* <INSEL2>	DMAC ch0 transfer completion	INTDMAATC0
				DMAC ch1 transfer completion	INTDMAATC1
				DMAC ch8 transfer completion	INTDMAATC8
				DMAC ch9 transfer completion	INTDMAATC9
				DMAC ch16 transfer completion	INTDMAATC16
				DMAC ch17 transfer completion	INTDMAATC17
				DMAC ch22 transfer completion	INTDMAATC22
29	-	-	*[TSEL0CR3]* <INSEL3>	DMAC ch2 transfer completion	INTDMAATC2
				DMAC ch3 transfer completion	INTDMAATC3
				DMAC ch10 transfer completion	INTDMAATC10
				DMAC ch11 transfer completion	INTDMAATC11
				DMAC ch18 transfer completion	INTDMAATC18
				DMAC ch23 transfer completion	INTDMAATC23
				TRGIN0 (PC0 pin)	TRGIN0

Note: The ch25 to 29 are set by trigger source of DMA request. For the detail of connection, refer to the "3. Trigger Selector (TRGSEL)".

Table 4.4 DMA Request List (4/4)

Channel	Single transfer		Burst transfer		
		Signal name	Trigger selector		Signal name
30	-	-	*[TSEL0CR4]* <INSEL0>	DMAC ch4 transfer completion	INTDMAATC4
				DMAC ch5 transfer completion	INTDMAATC5
				DMAC ch12 transfer completion	INTDMAATC12
				DMAC ch13 transfer completion	INTDMAATC13
				DMAC ch20 transfer completion	INTDMAATC20
				DMAC ch24 transfer completion	INTDMAATC24
				DMAC ch26 transfer completion	INTDMAATC26
				TRGIN1 (PA5 pin)	TRGIN1
31	-	-	*[TSEL0CR4]* <INSEL1>	DMAC ch6 transfer completion	INTDMAATC6
				DMAC ch7 transfer completion	INTDMAATC7
				DMAC ch14 transfer completion	INTDMAATC14
				DMAC ch15 transfer completion	INTDMAATC15
				DMAC ch21 transfer completion	INTDMAATC21
				DMAC ch25 transfer completion	INTDMAATC25
				DMAC ch27 transfer completion	INTDMAATC27
				TRGIN2 (PG1 pin)	TRGIN2

Note: The ch30 and ch31 are set by trigger source of DMA request. For the detail of connection, refer to the "3. Trigger Selector (TRGSEL)".

5. Communication Function

5.1. Asynchronous Serial Communication Circuit (UART)

5.1.1. Half Clock Mode Support

Half clock mode of the UART corresponds to 1-pin mode only.

5.1.2. Internal Signal Connection Specification

5.1.2.1. Trigger Transfer Signal Connection

Transfer function of the UART has a trigger signal control.
A trigger control signal is selected with the trigger source and use it as the following table.

Table 5.1 UART Trigger Transfer Signal Connection (1/2)

Channel		Trigger source		
	Signal name	Trigger selector	Input trigger signal	Signal name
ch0	UART0TRGIN	***[TSEL0CR5]*** <INSEL3>	PC0 (TRGIN0)	TRGIN0
			PA5 (TRGIN1)	TRGIN1
			PG1 (TRGIN2)	TRGIN2
			T32A ch3 timer register A1 match trigger	T32A03TRGOUTCMPA1
			T32A ch3 timer register B1 match trigger	T32A03TRGOUTCMPB1
			T32A ch3 timer register C1 match trigger	T32A03TRGOUTCMPC1
ch1	UART1TRGIN	***[TSEL0CR6]*** <INSEL0>	PC0 (TRGIN0)	TRGIN0
			PA5 (TRGIN1)	TRGIN1
			PG1 (TRGIN2)	TRGIN2
			T32A ch3 timer register A1 match trigger	T32A03TRGOUTCMPA1
			T32A ch3 timer register B1 match trigger	T32A03TRGOUTCMPB1
			T32A ch3 timer register C1 match trigger	T32A03TRGOUTCMPC1
ch2	UART2TRGIN	***[TSEL0CR6]*** <INSEL1>	PC0 (TRGIN0)	TRGIN0
			PA5 (TRGIN1)	TRGIN1
			PG1 (TRGIN2)	TRGIN2
			T32A ch3 timer register A1 match trigger	T32A03TRGOUTCMPA1
			T32A ch3 timer register B1 match trigger	T32A03TRGOUTCMPB1
			T32A ch3 timer register C1 match trigger	T32A03TRGOUTCMPC1
ch3	UART3TRGIN	***[TSEL0CR6]*** <INSEL2>	PC0 (TRGIN0)	TRGIN0
			PA5 (TRGIN1)	TRGIN1
			PG1 (TRGIN2)	TRGIN2
			T32A ch3 timer register A1 match trigger	T32A03TRGOUTCMPA1
			T32A ch3 timer register B1 match trigger	T32A03TRGOUTCMPB1
			T32A ch3 timer register C1 match trigger	T32A03TRGOUTCMPC1

Table 5.2 UART Trigger Transfer Signal Connection (2/2)

Channel		Trigger source		
	Signal name	Trigger selector	Input trigger signal	Signal name
ch4	UART4TRGIN	***[TSEL0CR6]*** <INSEL3>	PC0 (TRGIN0)	TRGIN0
			PA5 (TRGIN1)	TRGIN1
			PG1 (TRGIN2)	TRGIN2
			T32A ch3 timer register A1 match trigger	T32A03TRGOUTCMPA1
			T32A ch3 timer register B1 match trigger	T32A03TRGOUTCMPB1
			T32A ch3 timer register C1 match trigger	T32A03TRGOUTCMPC1
ch5	UART5TRGIN	***[TSEL0CR7]*** <INSEL0>	PC0 (TRGIN0)	TRGIN0
			PA5 (TRGIN1)	TRGIN1
			PG1 (TRGIN2)	TRGIN2
			T32A ch3 timer register A1 match trigger	T32A03TRGOUTCMPA1
			T32A ch3 timer register B1 match trigger	T32A03TRGOUTCMPB1
			T32A ch3 timer register C1 match trigger	T32A03TRGOUTCMPC1

5.1.2.2. T32A Connection

In the UART, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

Table 5.3 UART Inside Connection List: Output

Channel	Function output		Trigger selector	Output destination	
		Signal name			Signal name
ch0	UART ch0 transmission completion trigger output	UART0TXTRG	***[TSEL0CR8]*** <INSEL1>	TRGSEL ***[TSEL0CR9]***<INSEL0> input ***[TSEL0CR9]***<INSEL2> input ***[TSEL0CR10]***<INSEL0> input ***[TSEL0CR10]***<INSEL2> input	-
	UART ch0 reception completion trigger output	UART0RXTRG			
ch1	UART ch1 transmission completion trigger output	UART1TXTRG	***[TSEL0CR7]*** <INSEL2>	TRGSEL ***[TSEL0CR8]***<INSEL2> input ***[TSEL0CR9]***<INSEL0> input ***[TSEL0CR10]***<INSEL0> input ***[TSEL0CR10]***<INSEL2> input	-
	UART ch1 reception completion trigger output	UART1RXTRG			
ch2	UART ch2 transmission completion trigger output	UART2TXTRG	***[TSEL0CR7]*** <INSEL3>	TRGSEL ***[TSEL0CR8]***<INSEL2> input ***[TSEL0CR9]***<INSEL0> input ***[TSEL0CR9]***<INSEL2> input ***[TSEL0CR10]***<INSEL2> input	-
	UART ch2 reception completion trigger output	UART2RXTRG			
ch3	UART ch3 transmission completion trigger output	UART3TXTRG	***[TSEL0CR8]*** <INSEL0>	TRGSEL ***[TSEL0CR8]***<INSEL2> input ***[TSEL0CR9]***<INSEL0> input ***[TSEL0CR9]***<INSEL2> input ***[TSEL0CR10]***<INSEL0> input	-
	UART ch3 reception completion trigger output	UART3RXTRG			
ch4	UART ch4 transmission completion trigger output	UART4TXTRG	***[TSEL0CR7]*** <INSEL1>	TRGSEL ***[TSEL0CR8]***<INSEL2> input ***[TSEL0CR9]***<INSEL2> input ***[TSEL0CR10]***<INSEL0> input ***[TSEL0CR10]***<INSEL2> input	-
	UART ch4 reception completion trigger output	UART4RXTRG			
ch5	UART ch5 transmission completion trigger output	UART5TXTRG	***[TSEL0CR8]*** <INSEL1>	TRGSEL ***[TSEL0CR9]***<INSEL0> input ***[TSEL0CR9]***<INSEL2> input [TSEL0CR10]<INSEL0> input [TSEL0CR10]<INSEL2> input	-
	UART ch5 reception completion trigger output	UART5RXTRG			

5.2. Serial Peripheral Interface (TSPI)

5.2.1. Transfer Mode

The serial peripheral interface can use SPI mode and SIO mode.

5.2.2. *[TSPIxCR2]*<RXDLY> Set Value

TMPM4V Group(1) products setting value of TSPI control register 2 (***[TSPIxCR2]***<RXDLY[2:0]>) is as follows:

Table 5.4 *[TSPIxCR2]*<RXDLY[2:0]> Set Value

Bit	Bit Symbol	After Reset	Function
18:16	<RXDLY[2:0]>	001	000: fsys ≤ 40MHz 001: fsys > 40MHz

5.2.3. Internal Signal Connection Specification

5.2.3.1. Trigger Transfer Signal Connection

Transfer function of the TSPI has a trigger signal control.
A trigger control signal is selected with the trigger source and use it as the following table.

Table 5.5 TSPI Trigger Transfer Signal Connection Specification

Channel		Trigger source		
	Signal name	Trigger selector	Input trigger signal	Signal name
ch0	TSPI0TRG (input)	***[TSEL0CR5]*** <INSEL0>	PC0 (TRGIN0)	TRGIN0
			PA5 (TRGIN1)	TRGIN1
			PG1 (TRGIN2)	TRGIN2
			T32A ch3 timer register A1 match trigger	T32A03TRGOUTCMPA1
			T32A ch3 timer register B1 match trigger	T32A03TRGOUTCMPB1
			T32A ch3 timer register C1 match trigger	T32A03TRGOUTCMPC1
ch1	TSPI1TRG (input)	***[TSEL0CR5]*** <INSEL1>	PC0 (TRGIN0)	TRGIN0
			PA5 (TRGIN1)	TRGIN1
			PG1 (TRGIN2)	TRGIN2
			T32A ch3 timer register A1 match trigger	T32A03TRGOUTCMPA1
			T32A ch3 timer register B1 match trigger	T32A03TRGOUTCMPB1
			T32A ch3 timer register C1 match trigger	T32A03TRGOUTCMPC1
ch2	TSPI2TRG (input)	***[TSEL0CR5]*** <INSEL2>	PC0 (TRGIN0)	TRGIN0
			PA5 (TRGIN1)	TRGIN1
			PG1 (TRGIN2)	TRGIN2
			T32A ch3 timer register A1 match trigger	T32A03TRGOUTCMPA1
			T32A ch3 timer register B1 match trigger	T32A03TRGOUTCMPB1
			T32A ch3 timer register C1 match trigger	T32A03TRGOUTCMPC1

5.2.3.2. T32A Connection

In the TSPI, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

Table 5.6 TSPI Inside Connection: Output

Channel	Function output		Trigger selector	Output destination	
		Signal name			Signal name
ch0	TSPI ch0 transmit completion signal	TSPI0TXEND	***[TSEL0CR7]*** <INSEL2>	TRGSEL ***[TSEL0CR8]***<INSEL2> input ***[TSEL0CR9]***<INSEL0> input ***[TSEL0CR10]***<INSEL0> input ***[TSEL0CR10]***<INSEL2> input	-
	TSPI ch0 receive completion signal	TSPI0RXEND			
ch1	TSPI ch1 transmit completion signal	TSPI1TXEND	***[TSEL0CR7]*** <INSEL1>	TRGSEL ***[TSEL0CR8]***<INSEL2> input ***[TSEL0CR9]***<INSEL2> input ***[TSEL0CR10]***<INSEL0> input ***[TSEL0CR10]***<INSEL2> input	-
	TSPI ch1 receive completion signal	TSPI1RXEND			
ch2	TSPI ch2 transmit completion signal	TSPI2TXEND	***[TSEL0CR7]*** <INSEL3>	TRGSEL ***[TSEL0CR8]***<INSEL2> input ***[TSEL0CR9]***<INSEL0> input ***[TSEL0CR9]***<INSEL2> input ***[TSEL0CR10]***<INSEL2> input	-
	TSPI ch2 receive completion signal	TSPI2RXEND			

5.3. Serial Memory Interface (SMIF)

5.3.1. Capacity of Primary and Secondary Buffer

The table below shows the primary/secondary buffer capacities of SMIF in the TMPM4V Group(1).

Table 5.7 SMIF Capacity of Buffer

Channel	Primary buffer	Secondary buffer
ch0	32 bytes	256 bytes

6. Timer Function

6.1. 32-bit Timer Event Counter (T32A)

6.1.1. Internal Signal Connection Specification

6.1.1.1. Capture Trigger Signal Connection

In the 32-bit timer event counter, capture trigger signal is connected to signals of the following table.
The input trigger signal which has a register name in the trigger selector column of the following table should choose the input trigger used by a trigger selector.

Table 6.1 T32A Capture Trigger Connection (1/3)

Channel	Timer	Input signal name of capture trigger	Trigger source		
			Trigger selector	Input trigger signal	Signal name
ch0	Timer A	T32A00TRGINAPHCK (Other timer output)	-	T32A ch0 timer B output	T32A00OUTB
		T32A00TRGINAPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL2>	T32A ch0 timer register B0 match trigger	T32A00TRGOUTCMPB0
				T32A ch0 timer register B1 match trigger	T32A00TRGOUTCMPB1
				T32A ch0 timer B overflow trigger	T32A00TRGOUTOFB
				T32A ch0 timer B underflow trigger	T32A00TRGOUTUFB
				[TSEL0CR7]<INSEL1> output	-
				[TSEL0CR7]<INSEL2> output	-
				[TSEL0CR7]<INSEL3> output	-
				[TSEL0CR8]<INSEL0> output	-
	Timer B	T32A00TRGINBPHCK (Other timer output)	-	T32A ch0 timer A output	T32A00OUTA
		T32A00TRGINBPCK (other timer input)	***[TSEL0CR8]*** <INSEL3>	T32A ch0 timer register A0 match trigger	T32A00TRGOUTCMPA0
				T32A ch0 timer register A1 match trigger	T32A00TRGOUTCMPA1
				T32A ch0 timer A overflow trigger	T32A00TRGOUTOFA
				T32A ch0 timer A underflow trigger	T32A00TRGOUTUFA
	Timer C	T32A00TRGINCPHCK (Other timer output)	-	-	-
		T32A00TRGINCPCK (Internal trigger input)	-	-	-
ch1	Timer A	T32A01TRGINAPHCK (Other timer output)	-	T32A ch1 timer B output	T32A01OUTB
		T32A01TRGINAPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL0>	T32A ch1 timer register B0 match trigger	T32A01TRGOUTCMPB0
				T32A ch1 timer register B1 match trigger	T32A01TRGOUTCMPB1
				T32A ch1 timer B overflow trigger	T32A01TRGOUTOFB
				T32A ch1 timer B underflow trigger	T32A01TRGOUTUFB
				[TSEL0CR7]<INSEL2> output	-
				[TSEL0CR7]<INSEL3> output	-
				[TSEL0CR8] INSEL0> output	-
				[TSEL0CR8]<INSEL1> output	-
	Timer B	T32A01TRGINBPHCK (Other timer output)	-	T32A ch1 timer A output	T32A01OUTA
		T32A01TRGINBPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL1>	T32A ch1 timer register A0 match trigger	T32A01TRGOUTCMPA0
				T32A ch1 timer register A1 match trigger	T32A01TRGOUTCMPA1
				T32A ch1 timer A overflow trigger	T32A01TRGOUTOFA
				T32A ch1 timer A underflow trigger	T32A01TRGOUTUFA
	Timer C	T32A01TRGINCPHCK (Other timer output)	-	-	-
		T32A00TRGINCPCK (Internal trigger input)	-	-	-

Table 6.2 T32A Capture Trigger Connection (2/3)

Channel	Timer	Input signal name of capture trigger	Trigger source		
			Trigger selector	Input trigger signal	Signal name
ch2	Timer A	T32A02TRGINAPHCK (Other timer output)	-	T32A ch2 timer B output	T32A02OUTB
		T32A02TRGINAPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL2>	T32A ch2 timer register B0 match trigger	T32A02TRGOUTCMPB0
				T32A ch2 timer register B1 match trigger	T32A02TRGOUTCMPB1
				T32A ch2 timer B overflow trigger	T32A02TRGOUTOFB
				T32A ch2 timer B underflow trigger	T32A02TRGOUTUFB
				[TSEL0CR7]<INSEL3> output	-
				[TSEL0CR8]<INSEL0> output	-
				[TSEL0CR8]<INSEL1> output	-
				[TSEL0CR7]<INSEL1> output	-
	Timer B	T32A02TRGINBPHCK (Other timer output)	-	T32A ch2 timer A output	T32A02OUTA
		T32A02TRGINBPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL3>	T32A ch2 timer register A0 match trigger	T32A02TRGOUTCMPA0
				T32A ch2 timer register A1 match trigger	T32A02TRGOUTCMPA1
				T32A ch2 timer A overflow trigger	T32A02TRGOUTOFA
				T32A ch2 timer A underflow trigger	T32A02TRGOUTUFA
	Timer C	T32A02TRGINCPHCK (Other timer output)	-	-	-
		T32A02TRGINCPCK (Internal trigger input)	-	-	-
ch3	Timer A	T32A03TRGINAPHCK (Other timer output)	-	T32A ch3 timer B output	T32A03OUTB
		T32A03TRGINAPCK (Internal trigger input)	***[TSEL0CR10]*** <INSEL0>	T32A ch3 timer register B0 match trigger	T32A03TRGOUTCMPB0
				T32A ch3 timer register B1 match trigger	T32A03TRGOUTCMPB1
				T32A ch3 timer B overflow trigger	T32A03TRGOUTOFB
				T32A ch3 timer B underflow trigger	T32A03TRGOUTUFB
				[TSEL0CR8]<INSEL0> output	-
				[TSEL0CR8]<INSEL1> output	-
				[TSEL0CR7]<INSEL1> output	-
				[TSEL0CR7]<INSEL2> output	-
	Timer B	T32A03TRGINBPHCK (Other timer output)	-	T32A ch3 timer A output	T32A03OUTA
		T32A03TRGINBPCK (Internal trigger input)	***[TSEL0CR10]*** <INSEL1>	T32A ch3 timer register A0 match trigger	T32A03TRGOUTCMPA0
				T32A ch3 timer register A1 match trigger	T32A03TRGOUTCMPA1
				T32A ch3 timer A overflow trigger	T32A03TRGOUTOFA
				T32A ch3 timer A underflow trigger	T32A03TRGOUTUFA
	Timer C	T32A03TRGINCPHCK (Other timer output)	-	-	-
		T32A03TRGINCPCK (Internal trigger input)	-	-	-

Table 6.3 T32A Capture Trigger Connection (3/3)

Channel		Input signal name of capture trigger	Trigger source		
	Timer		Trigger selector	Input trigger signal	Signal name
ch4	Timer A	T32A04TRGINAPHCK (Other timer output)	-	T32A ch4 timer B output	T32A04OUTB
		T32A04TRGINAPCK (Internal trigger input)	***[TSEL0CR10]*** <INSEL2>	T32A ch4 timer register B0 match trigger	T32A04TRGOUTCMPB0
				T32A ch4 timer register B1 match trigger	T32A04TRGOUTCMPB1
				T32A ch4 timer B overflow trigger	T32A04TRGOUTOFB
				T32A ch4 timer B underflow trigger	T32A04TRGOUTUFB
				[TSEL0CR8]<INSEL1> output	-
				[TSEL0CR7]<INSEL1> output	-
				[TSEL0CR7]<INSEL2> output	-
				[TSEL0CR7]<INSEL3> output	-
	Timer B	T32A04TRGINBPHCK (Other timer output)	-	T32A ch4 timer A output	T32A04OUTA
		T32A04TRGINBPCK (Internal trigger input)	***[TSEL0CR10]*** <INSEL3>	T32A ch4 timer register A0 match trigger	T32A04TRGOUTCMPA0
				T32A ch4 timer register A1 match trigger	T32A04TRGOUTCMPA1
				T32A ch4 timer A overflow trigger	T32A04TRGOUTOFA
				T32A ch4 timer A underflow trigger	T32A04TRGOUTUFA
	Timer C	T32A04TRGINCPHCK (Other timer output)	-	-	-
		T32A04TRGINCPCK (Internal trigger input)	-	-	-

6.1.1.2. Synchronous Control Connection

In the 32-bit timer event counter, as shown in the following tables, synchronous connection of the timer is carried out within the same channel.

Table 6.4 T32A Synchronous Control Connection Specifications

Channel	Timer	Output		Timer	Input	
		Function	Signal name		Function	Signal name
ch0	Timer A	Synchronous start output A	T32A00SYNCSTARTOUTA	Timer B	Synchronous start B	T32A00SYNCSTARTB
		Synchronous stop output A	T32A00SYNCSTOPOUTA		Synchronous stop B	T32A00SYNCSTOPB
		Synchronous reload output A	T32A00SYNCRELOADOUTA		Synchronous reload B	T32A00SYNCRELOADB
ch1	Timer A	Synchronous start output A	T32A01SYNCSTARTOUTA	Timer B	Synchronous start B	T32A01SYNCSTARTB
		Synchronous stop output A	T32A01SYNCSTOPOUTA		Synchronous stop B	T32A01SYNCSTOPB
		Synchronous reload output A	T32A01SYNCRELOADOUTA		Synchronous reload B	T32A01SYNCRELOADB
ch2	Timer A	Synchronous start output A	T32A02SYNCSTARTOUTA	Timer B	Synchronous start B	T32A02SYNCSTARTB
		Synchronous stop output A	T32A02SYNCSTOPOUTA		Synchronous stop B	T32A02SYNCSTOPB
		Synchronous reload output A	T32A02SYNCRELOADOUTA		Synchronous reload B	T32A02SYNCRELOADB
ch3	Timer A	Synchronous start output A	T32A03SYNCSTARTOUTA	Timer B	Synchronous start B	T32A03SYNCSTARTB
		Synchronous stop output A	T32A03SYNCSTOPOUTA		Synchronous stop B	T32A03SYNCSTOPB
		Synchronous reload output A	T32A03SYNCRELOADOUTA		Synchronous reload B	T32A03SYNCRELOADB
ch4	Timer A	Synchronous start output A	T32A04SYNCSTARTOUTA	Timer B	Synchronous start B	T32A04SYNCSTARTB
		Synchronous stop output A	T32A04SYNCSTOPOUTA		Synchronous stop B	T32A04SYNCSTOPB
		Synchronous reload output A	T32A04SYNCRELOADOUTA		Synchronous reload B	T32A04SYNCRELOADB

6.1.2. Pulse Counter

The 32-bit timer event counter is the one phase pulse counter only.

7. Motor Control Function

7.1. Motor Control Function Connection

The motor control functions are connected as shown in Figure 7.1 and work together to control the motor. For details on each function, refer to the reference manual.

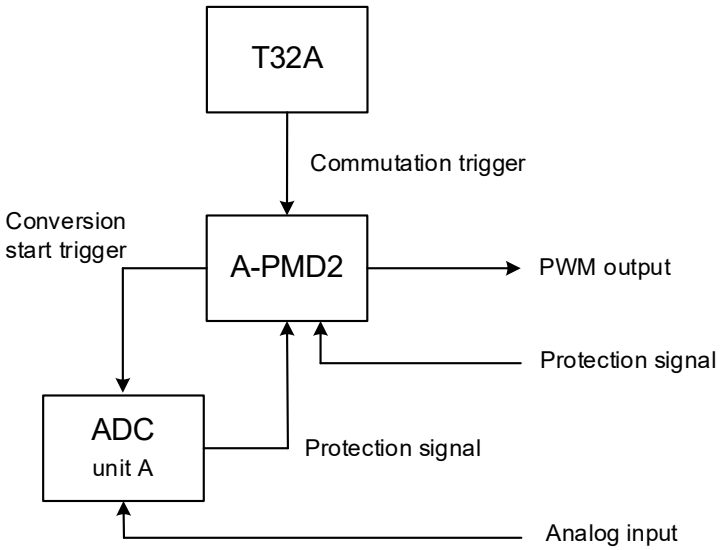

Figure 7.1 Motor Control Function Connection (Outline)

7.2. Advanced Programmable Motor Control Circuit 2 (A-PMD2)

7.2.1. Internal Signal Connection Specification

Table 7.1 and Table 7.2 show the internal connection specifications.

Table 7.1 A-PMD2 Inside Connection Specification: Input

Channel	Function input		Input source	
		Signal name		Signal name
ch0	ADC conversion completion interrupt A	INTADAPDA	ADC unit A	INTADAPDA
	ADC conversion completion interrupt B	INTADAPDB		INTADAPDB
	ADC conversion completion interrupt C	INTADxPDC	-	-
	ADC conversion completion interrupt D	INTADxPDD		
	ADC conversion priority interrupt	INTADxPFLG		
	ADC monitor function 0 (OVV detection)	ADACMP0L_N	ADC unit A	ADACP0L_N
	ADC monitor function 1 (OVV detection)	ADACMP1L_N		ADACP1L_N
	ADC conversion signal	ADABUSY		ADABUSY
	Commutation trigger (General purpose timer synchronous)	PMD0TMR	T32A ch2	T32A02TRGOUTCMPB0
	Commutation trigger (MCMP synchronous)	ENC0CTRGO	-	-
	Commutation trigger (Position detect synchronous) ENC interrupt 0 (debug output)	INTENC00		
	ENC interrupt 1 (debug output)	INTENC01		
	ENC debug output	ENC0DBG		
	COMP EMG protection synchronous input	COMP0EMG	-	-
		COMP1EMG	-	-
		COMP2EMG	-	-
		COMP3EMG	-	-
		COMP4EMG	-	-
		COMP5EMG	-	-
	COMP OVV protection synchronous input	COMP0OVV	-	-
		COMP1OVV	-	-
		COMP2OVV	-	-
		COMP3OVV	-	-
		COMP4OVV	-	-
		COMP5OVV	-	-
	VE U-phase PWM duty	VE0CMPU	-	-
	VE V-phase PWM duty	VE0CMPV		
	VE W-phase PWM duty	VE0CMPW		
	VE trigger comparison 0	VE0TRGCMP0		
	VE trigger comparison 1	VE0TRGCMP1		
	VE synchronous trigger output selection	VE0TRGSEL		
	VE Conduction control / Output control	VE0OUTCR		
	VE Task transition signal	VE0TASKP		
	VE interrupt	INTVCN0		
	VE EMG release	VExEMGRS	-	-

Table 7.2 A-PMD2 Inside Connection Specification: Output

Channel	Function output		Output destination	
		Signal name		Signal name
ch0	ADC synchronous trigger output 0	PMD0TRG0	ADC unit A	PMDTRG0
	ADC synchronous trigger output 1	PMD0TRG1	ADC unit A	PMDTRG1
	ADC synchronous trigger output 2	PMD0TRG2	ADC unit A	PMDTRG2
	ADC synchronous trigger output 3	PMD0TRG3	ADC unit A	PMDTRG3
	ADC synchronous trigger output 4	PMD0TRG4	ADC unit A	PMDTRG4
	ADC synchronous trigger output 5	PMD0TRG5	ADC unit A	PMDTRG5
	ADC synchronous trigger output 6	PMD0TRG6	ADC unit A	PMDTRG6
	PWM signal for encoder	PMD0PWMON	-	-
	PWM output control	PMD0MDOUT		
	PWM interrupt	INTPWM0	-	-

8. Analog Function

8.1. 12-bit Analog to Digital Converter (ADC)

8.1.1. Corresponding Registers

The following table shows the correspondence registers of TMPM4V Group(1).

Table 8.1 ADC Corresponding Registers

Unit	General purpose start-up factor program register	Conversion result storage register
A	***[ADATSET0]*** to ***[ADATSET23]***	***[ADAREG0]*** to ***[ADAREG23]***

8.1.2. Function Pin and Port

The functional pins are assigned to the port of the following tables.
There is also a channel which does not have functional pins depending on a product.

Table 8.2 ADC Function Pin and Port

Unit	Signal input	Function pin/ signal name	Port	Product list (✓: Available, - : N/A)		
				M4V4	M4V2	M4V1
A	AINA00	AINA00	PE0	✓	✓	✓
	AINA01	AINA01	PE1	✓	✓	✓
	AINA02	AINA02	PE2	✓	✓	✓
	AINA03	AINA03	PE3	✓	✓	✓
	AINA04	AINA04	PE4	✓	-	-
	AINA05	AINA05	PE5	✓	-	-
	AINA06	AINA06	PE6	✓	-	-
	AINA07	AINA07	PE7	✓	-	-
	AINA08	AINA08	PF0	✓	-	-
	AINA09	AINA09	PF1	✓	✓	✓
	AINA10	AINA10	PF2	✓	✓	✓
	AINA11	AINA11	PF3	✓	✓	✓
	AINA12	AINA12	PF4	✓	✓	✓
	AINA13	AINA13	PF5	✓	✓	-
	AINA14	VREFH	-	✓	✓	✓
	AINA15	VREFL	-	✓	✓	✓
	AINA16	Reference power supply (Note2)	-	✓	✓	✓

Note1: AINA14 to AINA16 are connected internally for self-check function support.

Note2: For reference power supply, refer to the electrical characteristics of "TMPM4V Group(1) Data Sheet".

8.1.3. Setting Value of Mode Setting Register 2

For the setting value of mode setting register 2 (***[ADxMOD2]***), set the values in the table below.

Table 8.3 Setting Value of ADC Mode Setting Register 2

Register name	Value
[ADxMOD2]<MOD2[31:0]>	0x00000000

8.1.4. Trimming Setting Register Setting Value

For the trimming setting register (***[ADxTRM]***), set the values in the table below.

Table 8.4 Setting Value of Trimming Setting Register

Register name	Value
[ADxTRM]<TRM[31:0]>	0x00000000

8.1.5. Internal Signal Connection Specification

Table 8.5 and Table 8.6 show the internal connection specifications. For input trigger signals with a register name in the trigger selector column, select the input trigger to be used with the trigger selector. "-" in the table does not have an applicable function.

Table 8.5 ADC Startup Trigger Connection Specifications

Unit	Function input		Trigger selector	Input source	
		Signal name			Signal name
A	PMD trigger 0	PMDTRG0	-	A-PMD2 ch0	PMD0TRG0
	PMD trigger 1	PMDTRG1	-		PMD0TRG1
	PMD trigger 2	PMDTRG2	-		PMD0TRG2
	PMD trigger 3	PMDTRG3	-		PMD0TRG3
	PMD trigger 4	PMDTRG4	-		PMD0TRG4
	PMD trigger 5	PMDTRG5	-		PMD0TRG5
	PMD trigger 6	PMDTRG6	-		PMD0TRG6
	PMD trigger 7	PMDTRG7	-	-	-
	PMD trigger 8	PMDTRG8	-		
	PMD trigger 9	PMDTRG9	-		
	PMD trigger 10	PMDTRG10	-		
	PMD trigger 11	PMDTRG11	-		
	General purpose trigger	ADATRGIN	***[TSEL0CR4]*** <INSEL2>	PC0 (TRGIN0)	TRGIN0
				PA5 (TRGIN1)	TRGIN1
				PG1 (TRGIN2)	TRGIN2
				T32A ch0	T32A00TRGOUTCMPA1
					T32A00TRGOUTCMPB1
					T32A00TRGOUTCMPC1
				T32A ch3	T32A03TRGOUTCMPA0
				T32A ch4	T32A04TRGOUTCMPA0

Table 8.6 ADC Inside Connection: Output

Unit	Function output	Signal name	Trigger selector	Output destination	Signal name
A	General purpose trigger interrupt	INTADATRG	***[TSEL0CR8]*** <INSEL0>	TRGSEL ***[TSEL0CR8]*** <INSEL2> input ***[TSEL0CR9]*** <INSEL0> input <INSEL2> input ***[TSEL0CR10]*** <INSEL0> input	-
	Single conversion interrupt	INTADASGL			
	Continuous conversion interrupt	INTADACNT			
	Monitor function 0 interrupt	INTADACP0			
	Monitor function 1 interrupt	INTADACP1			
	Monitor function 0 output for PMD protect function	ADACP0L_N	-	A-PMD2 ch0	ADACMP0L_N
	Monitor function 1 output for PMD protect function	ADACP1L_N	-		ADACMP1L_N
	PMD trigger interrupt A	INTADAPDA	-		INTADAPDA
	PMD trigger interrupt B	INTADAPDB	-		INTADAPDB
	AD conversion flag	ADABUSY	-		ADABUSY
	Conversion result storing register	ADAREG0	-	-	-
		ADAREG1	-		
		ADAREG2	-		
		ADAREG3	-		
	Phase select information	ADAUVWIS0	-		-
		ADAUVWIS1	-		
		ADAUVWIS2	-		
		ADAUVWIS3	-		

9. System Function

9.1. Voltage Detection Circuit (LVD)

9.1.1. Detection Power Supply

A voltage detecting circuit monitors the power supply of the following tables.

Table 9.1 LVD Detection Power Supply

Detection power supply	Power supply name
Digital power source	DVDD5A/DVDD5B

9.1.2. LVD Control Register Setting

The after reset value and possible settings of LVD control register ***[LVDCR]*** <LVL[2:0]> are as follows:

Table 9.2 LVD Control Register *[LVDCR]*<LVL[2:0]> Setting

Bit	Bit symbol	After reset	Function
6:4	<LVL[2:0]>	000	Detection/release voltage setting Detection voltage Release voltage 000: 2.65V 2.7V 001: 2.7V 2.75V 010: 2.8V 2.85V 011: 2.9V 2.95V 100: 4.0V 4.05V 101: 4.2V 4.25V 110: 4.4V 4.45V 111: 4.6V 4.65V

9.2. Clock Selective Watchdog Timer (SIWDT)

9.2.1. Output Control

To select the internal high-speed oscillator 2 (f_{IHOSC2}), rewriting of the internal high-speed oscillator2 can be forbidden.

Table 9.3 SIWDT Output Control

Output control	Signal name	Remark
Protect signal of internal high-speed oscillator 2 control bit (***[CGOSCCR]***<IHOSC2EN>)	OSCPRO	Setting by ***[SIWD0OSCCR]***<OSCPRO>

9.3. Oscillation Frequency Detection Circuit (OFD)

9.3.1. Reference Clock

The oscillation frequency detection circuit operates considering the clock of the following tables as a reference clock.

Table 9.4 OFD Reference Clock

Reference clock	Signal name	Divide value
Internal high-speed oscillator 2	f_{IHOSC2}	256

10. Memory

10.1. Flash Memory

10.1.1. Access Control Register *[FCACCR]* Setting

The settings of access control register ***[FCACCR]*** is as follows:
In TMPM4V Group(1), use ***[FCACCR]*** with the value after reset.

Table 10.1 Access Control Register *[FCACCR]* Setting

Bit	Bit symbol	After reset	Function
10:8	-	011	-
1:0	<FCLC[1:0]>	11	Code flash read clock control

10.1.2. Macro Code at ID-Read

The macro code values for this product are as follows:

Table 10.2 Macro Code at ID-Read

Code	ID[15:0]
Macro code (Code Flash)	0x0504

10.1.3. Single Boot Resource

The peripheral function of the following table is used in single boot.

Table 10.3 Single Boot Resource

Peripheral function	Channel	Function	Pin name
BOOT	-	-	PG0 (BOOT_N)
UART	ch0	RXD	PD2 (UT0RXD)
		TXD	PD3 (UT0TXDA)
T32A	ch0	-	-

10.2. RAM Parity (RAMP)

10.2.1. Error Detection Block Area

The following table shows the detection RAM block area of each product.

Table 10.4 RAM Area and Address of RAMP

Register name	RAM area address	Products (✓: Available, - : N/A)		
		M4V4	M4V2	M4V1
[RPARST]<RPARFG1>	0x20004000-0x20007FFF	✓	✓	✓
[RPARST]<RPARFG0>	0x20000000-0x20003FFF	✓	✓	✓

11. Other Function

11.1. Digital Noise Filter (DNF)

11.1.1. External Interrupt Pin and Setting Register

Table 11.1 shows the external interrupt pins and the corresponding DNF setting registers.

Table 11.1 External Interrupt Pins and DNF Setting Registers

Unit	External interrupt pin (Signal name)	Setting register name
A	INT00	***[DNFAENCR]***<NFEN0>
	INT01	***[DNFAENCR]***<NFEN1>
	INT02	***[DNFAENCR]***<NFEN2>
	INT03	***[DNFAENCR]***<NFEN3>
	INT04	***[DNFAENCR]***<NFEN4>
	INT05	***[DNFAENCR]***<NFEN5>
	INT06	***[DNFAENCR]***<NFEN6>
	INT07	***[DNFAENCR]***<NFEN7>
	INT08	***[DNFAENCR]***<NFEN8>
	INT09	***[DNFAENCR]***<NFEN9>
	INT10	***[DNFAENCR]***<NFEN10>
	INT11	***[DNFAENCR]***<NFEN11>
	INT12	***[DNFAENCR]***<NFEN12>
	INT13	***[DNFAENCR]***<NFEN13>
	INT14	***[DNFAENCR]***<NFEN14>
	INT15	***[DNFAENCR]***<NFEN15>
B	INT16	***[DNFBENCR]***<NFEN0>
	INT17	***[DNFBENCR]***<NFEN1>
	INT18	***[DNFBENCR]***<NFEN2>
	INT19	***[DNFBENCR]***<NFEN3>
	INT20	***[DNFBENCR]***<NFEN4>

12. Revision History

Table 12.1 Revision History

Revision	Date	Description
1.0	2026-04-24	- First release

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