LOW POWER DUAL CHANNEL DIGITAL ISOLATORS

DCL32xx00

DCL320C00 / DCL320D00 / DCL321C00 / DCL321D00

1. Applications

- Industrial automation systems
- Motor control
- Inverter
- Switching power supply

2. Description

DCL320C00/DCL320D00/DCL321C00/DCL321D00 are low power dual-channel digital isolators. Outstanding performance characteristics are achieved by Toshiba CMOS technology and the magnetic coupling structure. In addition, they comply with UL 1577 and has a 3000Vrms rating as an isolation voltage. These products can operate with a temperature range of -40 to 125 °C and a wide supply voltage of 2.25 to 5.5 V.

3. Features

Data rate	: Up to 25 Mbps
Supply voltage	: 2.25 V to 5.5 V
Temperature Range	: -40 °C to 125 °C
Propagation Delay	: 33 ns Typ. (5.0 V operation)
Default Output	: High and Low Options
High CMTI(min.)	: ±30 kV/μs
Withstand Voltage	: 3 kVrms
Package	: 8pin SOIC Narrow body
Safety-Related Certification	: UL1577, CQC, VDE DIN EN 60747-17

UL : UL1577, File No. E519997

cUL : CSA Component Acceptance Service Notice No. 5A

VDE : DIN EN IEC 60747-17 (VDE 0884-17) (Planning)

CQC : GB 4943.1-2022 (Planning)

Start of commercial production

2026-07

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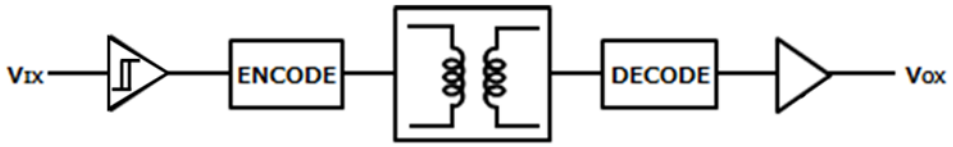
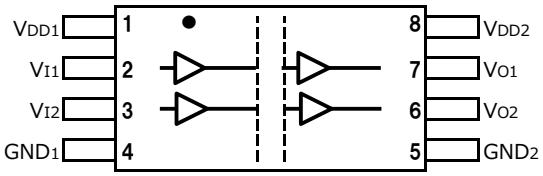
4. Internal Circuit



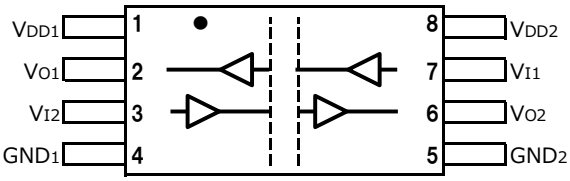
5. Pin configuration and Functions

Pin Layout

DCL320C00 / DCL320D00



DCL321C00 / DCL321D00



Pin Function

PIN			I/O	DESCRIPTION
NAME	DCL320C00 DCL320D00	DCL321C00 DCL321D00		
V_{DD1}	1	1	—	Power Supply, side 1
V_{I1}	2	7	I	Input, Channel1
V_{I2}	3	3	I	Input, Channel2
GND_1	4	4	—	GND connection for V_{DD1}, side 1
GND_2	5	5	—	GND connection for V_{DD2}, side 2
V_{O2}	6	6	O	Output, Channel2
V_{O1}	7	2	O	Output, Channel1
V_{DD2}	8	8	—	Power Supply, side 2

6. Functional Description

DCL320C00/DCL320D00 / DCL321C00/DCL321D00

V_{DDI}	V_{DDO}	INPUT (V_{Ix})	OUTPUT (V_{Ox})	COMMENTS
PU	PU	L	L	Normal Operation
		H	H	
PU	PD	L or H	Undetermined	When V_{DDO} is unpowered, a channel output is undetermined.
PD	PU	X	Default	Default mode: DCL320C00 = L, DCL320D00 = H DCL321C00 = L, DCL321D00 = H
PD	X	H	-	Don't use since a certain voltage will be output through the internal ESD circuit.

PU= Powered up ($V_{DD} \geq 2.25$ V), PD= Powered down ($V_{DD} < 2.25$ V → 0 V), H = High level, L = Low level, X = Don't Care

V_{DDI}, V_{DDO} : Supply voltages on the input and output sides of each channel.

V_{IX}, V_{OX} : Input and output signals of each channel.

When the input pin (V_{IX}) on the power-off side is set to "H", power is supplied to the device via the ESD circuit, so use is prohibited.

Don't leave the Input pin (V_{IX}) on the power ON side open because terminal circuits don't have pull-down resistor or pull-down resistor inside.

7. Absolute Maximum Ratings (T_a = 25 °C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power supply voltage	V_{DD1}, V_{DD2}	-0.5	6.0	V
Input Voltage	V_I	-0.5	V_{DDX}+0.5(Note1)	V
Output Voltage	V_O	-0.5	V_{DDX}+0.5(Note1)	V
Output Current	I_O	-15	15	mA
Storage Temperature	T_{stg}	-65	150	°C
Operating Temperature	T_{opr}	-40	125	°C
Soldering Temperature (10 s)	T_{sol}	-	260	°C
Maximum Withstanding Isolation Voltage (60 s)	BV_S	-	3000	Vrms

1: Maximum voltage must not exceed 6 V. X = 1 or 2.

8. Recommended Operating Conditions (Note)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power supply voltage	V_{DD1}, V_{DD2}	2.25	5.5	V
Junction Temperature	T_J	-40	150	°C
Ambient Temperature	T_a	-40	125	°C

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this data sheet should also be considered.

Note: A ceramic capacitor (0.1 μF) should be connected between pin 1 (V_{DD1}) and pin 2 (GND_1) for V_{DD1} and between pin 16 (V_{DD2}) and pin 15 (GND_2) for V_{DD2} and should be the layout on the IC as close as possible (less than 10 mm). Otherwise, the IC may not switch properly.

9. Electrical Characteristics

9.1. Electrical Characteristics – 5 V Supply

All typical specifications are at T_a = 25 °C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operating range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and -40 °C ≤ T_a ≤ 125 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Output Voltage Logic High	V_{IX} = H , I_{OH} = -20 μA	Fig.12.1	V_{OH}	V_{DDO}(Note1)-0.1	V_{DDO}(Note1)	-	V
	V_{IX} = H , I_{OH} = -4 mA			V_{DDO}(Note1)-0.4	V_{DDO}(Note1)-0.2	-	
Output Voltage Logic Low	V_{IX} = L , I_{OL} = 20 μA	Fig.12.1	V_{OL}	-	0.0	0.1	V
	V_{IX} = L , I_{OL} = 4 mA			-	0.2	0.4	
Output impedance	-	Fig.12.1	Z_O	-	50	-	Ω
High-level input voltage	-	Fig.12.2	V_{IH}	0.7*V_{DDI}(Note1)	-	-	V
Low-level input voltage	-	Fig.12.2	V_{IL}	-	-	0.3*V_{DDI}(Note1)	V
Input Voltage Hysteresis	-	Fig.12.2	V_{HYS}	-	0.44	-	V
Input Current	V_I = V_{DDI}(Note1) or 0 V	-	I_I	-	-	±1	μA
SWITCHING SPECIFICATIONS							
Data Rate	-	-	t_{bps}	DC	-	25	Mbps
Pulse Width	-	-	PW	40	-	-	ns
Propagation Delay	50 kHz, Duty = 50 %, t_r = t_f = 2 ns, C_L = 15 pF	Fig.12.3	t_{PHL}, t_{PLH}	-	33	46	ns
DC～10Mbps							
Pulse Width Distortion	|t_{PHL} – t_{PLH}|	Fig.12.3	PWD	-	0.7	8.0	ns
Propagation Delay Skew(Note2) (Between any two units)	-	-	t_{PSK}	-	-	16	ns
Channel Matching	Same Direction	Fig.12.3	t_{skCD}	-	-	5.0	ns
	Opposing Direction	Fig.12.3	t_{skOD}	-	-	7.0	
DC～25Mbps							
Pulse Width Distortion	|t_{PHL} – t_{PLH}|	Fig.12.3	PWD	-	0.7	13	ns
Propagation Delay Skew(Note2) (Between any two units)	-	-	t_{PSK}	-	-	21	ns
Channel Matching	Same Direction	Fig.12.3	t_{skCD}	-	-	10	ns
	Opposing Direction	Fig.12.3	t_{skOD}	-	-	12	
Output Rise Time	10 % - 90 %	Fig.12.3	t_r	-	2.0	-	ns
Output Fall Time	90 % - 10 %	Fig.12.3	t_f	-	2.0	-	ns
Default output delay time from input power loss	V_{DDI} < 2.25 V → 0 V	-	t_{DO}	-	-	25	μs
Time from PU(Note3) to valid output data	-	-	t_{PU}	-	-	30	μs
Common mode transient immunity	V_I = V_{DDI} or 0 V , V_{CM} = 400 V ,T_a = 25°C	Fig. 12.4	|CMTI|	30	-	-	kV/μs

Note1: V_{DDI} = Input-side V_{DDX} , V_{DDO} = Output-side V_{DDX}

Note2: Propagation delay difference (between parts) is applied under the same operating conditions (power supply voltage. input current, temperature conditions, etc.).

Note3: PU = Powered up (V_{DD} ≥ 2.25 V) , After V_{DD} is set powered up, normal operation become valid 30μs later.

9.2. Electrical Characteristics – 3.3 V Supply

All typical specifications are at T_a = 25 °C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operating range of 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and -40 °C ≤ T_a ≤ 125 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Output Voltage Logic High	V_{IX} = H , I_{OH} = -20 μA	Fig.12.1	V_{OH}	V_{DDO}(Note1)-0.1	V_{DDO}(Note1)	-	V
	V_{IX} = H , I_{OH} = -4 mA			V_{DDO}(Note1)-0.4	V_{DDO}(Note1)-0.2	-	
Output Voltage Logic Low	V_{IX} = L , I_{OL} = 20 μA	Fig.12.1	V_{OL}	-	0.0	0.1	V
	V_{IX} = L , I_{OL} = 4 mA			-	0.2	0.4	
Output impedance	-	Fig.12.1	Z_O	-	50	-	Ω
High-level input voltage	-	Fig.12.2	V_{IH}	0.7*V_{DDI}(Note1)	-	-	V
Low-level input voltage	-	Fig.12.2	V_{IL}	-	-	0.3*V_{DDI}(Note1)	V
Input Voltage Hysteresis	-	Fig.12.2	V_{HYS}	-	0.25	-	V
Input Current	V_I = V_{DDI}(Note1) or 0 V	-	I_I	-	-	±1	μA
SWITCHING SPECIFICATIONS							
Data Rate	-	-	t_{bps}	DC	-	25	Mbps
Pulse Width	-	-	PW	40	-	-	ns
Propagation Delay	50 kHz, Duty = 50 %, t_r = t_f = 2 ns, C_L = 15 pF	Fig.12.3	t_{PHL} , t_{PLH}	-	38	52	ns
DC～10Mbps							
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$	Fig.12.3	PWD	-	0.7	8.0	ns
Propagation Delay Skew(Note2) (Between any two units)	-	-	t_{PSK}	-	-	19	ns
Channel Matching	Same Direction	Fig.12.3	t_{skCD}	-	-	5.0	ns
	Opposing Direction	Fig.12.3	t_{skOD}	-	-	9.0	
DC～25Mbps							
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$	Fig.12.3	PWD	-	0.7	13	ns
Propagation Delay Skew(Note2) (Between any two units)	-	-	t_{PSK}	-	-	24	ns
Channel Matching	Same Direction	Fig.12.3	t_{skCD}	-	-	10	ns
	Opposing Direction	Fig.12.3	t_{skOD}	-	-	14	
Output Rise Time	10 % - 90 %	Fig.12.3	t_r	-	2.0	-	ns
Output Fall Time	90 % - 10 %	Fig.12.3	t_f	-	2.0	-	ns
Default output delay time from input power loss	V_{DDI} < 2.25 V → 0 V	-	t_{DO}	-	-	30	μs
Time from PU(Note3) to valid output data	-	-	t_{PU}	-	-	30	μs
Common mode transient immunity	V_I = V_{DDI} or 0 V , V_{CM} = 400 V, T_a = 25°C	Fig. 12.4	|CMTI|	30	-	-	kV/μs

Note1: V_{DDI} = Input-side V_{DDX} , V_{DDO} = Output-side V_{DDX}

Note2: Propagation delay difference (between parts) is applied under the same operating conditions (power supply voltage. input current, temperature conditions, etc.).

Note3: PU = Powered up (V_{DD} ≥ 2.25 V) , After V_{DD} is set powered up, normal operation become valid 30μs later.

9.3. Electrical Characteristics – 2.5 V Supply

All typical specifications are at T_a = 25 °C, V_{DD1} = V_{DD2} = 2.5 V. Minimum/maximum specifications apply over the entire recommended operating range of 2.25 V ≤ V_{DD1} ≤ 2.75 V, 2.25 V ≤ V_{DD2} ≤ 2.75 V, and -40 °C ≤ T_a ≤ 125 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Output Voltage Logic High	V_{IX} = H , I_{OH} = -20 μA	Fig.12.1	V_{OH}	V_{DDO}(Note1)-0.1	V_{DDO}(Note1)	-	V
	V_{IX} = H , I_{OH} = -4 mA			V_{DDO}(Note1)-0.4	V_{DDO}(Note1)-0.2	-	
Output Voltage Logic Low	V_{IX} = L , I_{OL} = 20 μA	Fig.12.1	V_{OL}	-	0.0	0.1	V
	V_{IX} = L , I_{OL} = 4 mA			-	0.2	0.4	
Output impedance	-	Fig.12.1	Z_O	-	50	-	Ω
High-level input voltage	-	Fig.12.2	V_{IH}	0.7*V_{DDI}(Note1)	-	-	V
Low-level input voltage	-	Fig.12.2	V_{IL}	-	-	0.3*V_{DDI}(Note1)	V
Input Voltage Hysteresis	-	Fig.12.2	V_{HYS}	-	0.22	-	V
Input Current	V_I= V_{DDI}(Note1) or 0 V	-	I_I	-	-	±1	μA
SWITCHING SPECIFICATIONS							
Data Rate	-	-	t_{bps}	DC	-	25	Mbps
Pulse Width	-	-	PW	40	-	-	ns
Propagation Delay	50 kHz, Duty = 50 %, t_r =t_f = 2 ns, C_L = 15 pF	Fig.12.3	t_{PHL} , t_{PLH}	-	46	63	ns
DC～10Mbps							
Pulse Width Distortion	|t_{PHL} – t_{PLH}|	Fig.12.3	PWD	-	0.4	8.0	ns
Propagation Delay Skew(Note2) (Between any two units)	-	-	t_{PSK}	-	-	24	ns
Channel Matching	Same Direction	Fig.12.3	t_{skCD}	-	-	7.0	ns
	Opposing Direction	Fig.12.3	t_{skOD}	-	-	11	
DC～25Mbps							
Pulse Width Distortion	|t_{PHL} – t_{PLH}|	Fig.12.3	PWD	-	0.4	13	ns
Propagation Delay Skew(Note2) (Between any two units)	-	-	t_{PSK}	-	-	29	ns
Channel Matching	Same Direction	Fig.12.3	t_{skCD}	-	-	12	ns
	Opposing Direction	Fig.12.3	t_{skOD}	-	-	16	
Output Rise Time	10 % - 90 %	Fig.12.3	t_r	-	2.0	-	ns
Output Fall Time	90 % - 10 %	Fig.12.3	t_f	-	2.0	-	ns
Default output delay time from input power loss	V_{DDI} < 2.25 V → 0 V	-	t_{DO}	-	-	40	μs
Time from PU(Note3) to valid output data	-	-	t_{PU}	-	-	30	μs
Common mode transient immunity	V_I = V_{DDI} or 0 V , V_{CM} = 400 V, T_a = 25°C	Fig. 12.4	|CMTI|	30	-	-	kV/μs

Note1: V_{DDI} = Input-side V_{DDX} , V_{DDO} = Output-side V_{DDX}

Note2: Propagation delay difference (between parts) is applied under the same operating conditions (power supply voltage. input current, temperature conditions, etc.).

Note3: PU = Powered up (V_{DD} ≥ 2.25 V) , After V_{DD} is set powered up, normal operation become valid 30μs later.

9.4. Supply Current Characteristics 5 V Supply

All typical specifications are at T_a = 25 °C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operating range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and -40 °C ≤ T_a ≤ 125 °C, unless otherwise noted.

(1) DCL320x00

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current	VI = 0 or 1	$I_{DD1(Q)}$	-	155	290	μA
		$I_{DD2(Q)}$	-	210	590	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	225	345	μA
		$I_{DD2(1)}$	-	285	680	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(25)}$	-	225	350	μA
		$I_{DD2(25)}$	-	375	780	μA
25 Mbps	f_{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(100)}$	-	4.8	6.9	mA
		$I_{DD2(100)}$	-	4.4	5.7	mA

(2) DCL321x00

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current	VI = 0 or 1	$I_{DD1(Q)}$	-	180	430	μA
		$I_{DD2(Q)}$	-	180	435	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	260	515	μA
		$I_{DD2(1)}$	-	260	515	μA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(25)}$	-	305	570	μA
		$I_{DD2(25)}$	-	305	570	μA
25 Mbps	f_{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(100)}$	-	4.7	6.3	mA
		$I_{DD2(100)}$	-	4.7	6.3	mA

9.5. Supply Current Characteristics 3.3 V Supply

All typical specifications are at T_a = 25 °C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operating range of 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and -40 °C ≤ T_a ≤ 125 °C, unless otherwise noted.

(1) DCL320x00

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current	VI = 0 or 1	$I_{DD1(Q)}$	-	110	210	µA
		$I_{DD2(Q)}$	-	155	465	µA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	155	245	µA
		$I_{DD2(1)}$	-	200	525	µA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(25)}$	-	160	240	µA
		$I_{DD2(25)}$	-	260	600	µA
25 Mbps	f_{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(100)}$	-	3.4	5.4	mA
		$I_{DD2(100)}$	-	2.8	3.9	mA

(2) DCL321x00

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current	VI = 0 or 1	$I_{DD1(Q)}$	-	135	335	µA
		$I_{DD2(Q)}$	-	135	335	µA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	185	385	µA
		$I_{DD2(1)}$	-	185	385	µA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(25)}$	-	215	420	µA
		$I_{DD2(25)}$	-	215	420	µA
25 Mbps	f_{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(100)}$	-	3.2	4.7	mA
		$I_{DD2(100)}$	-	3.2	4.7	mA

9.6. Supply Current Characteristics 2.5 V Supply

All typical specifications are at T_a = 25 °C, V_{DD1} = V_{DD2} = 2.5 V. Minimum/maximum specifications apply over the entire recommended operating range of 2.25 V ≤ V_{DD1} ≤ 2.75 V, 2.25 V ≤ V_{DD2} ≤ 2.75 V, and -40 °C ≤ T_a ≤ 125 °C, unless otherwise noted

(1) DCL320x00

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current	VI = 0 or 1	$I_{DD1(Q)}$	-	100	190	µA
		$I_{DD2(Q)}$	-	140	435	µA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	140	215	µA
		$I_{DD2(1)}$	-	175	475	µA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(25)}$	-	140	220	µA
		$I_{DD2(25)}$	-	220	530	µA
25 Mbps	f_{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(100)}$	-	3.1	4.8	mA
		$I_{DD2(100)}$	-	2.1	3.0	mA

(2) DCL321x00

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current	VI = 0 or 1	$I_{DD1(Q)}$	-	125	310	µA
		$I_{DD2(Q)}$	-	125	310	µA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	160	340	µA
		$I_{DD2(1)}$	-	160	340	µA
1 Mbps	f_{CLK} = 500 kHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(25)}$	-	180	365	µA
		$I_{DD2(25)}$	-	180	365	µA
25 Mbps	f_{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C_L = 15 pF	$I_{DD1(100)}$	-	2.6	3.9	mA
		$I_{DD2(100)}$	-	2.6	3.9	mA

10. Insulation Specifications

PARAMETER	Symbol	TEST CONDITIONS	VALUE	UNIT
Minimum External Clearance	CLR	Shortest terminal-to-terminal distance through air	3.8	mm
Minimum External Creepage	CPG	Shortest terminal-to-terminal distance across the package surface	3.8	mm
Distance Through The Insulation	DTI	Minimum internal gap	8.5	µm
Comparative Tracking Index	CTI	-	400	V
Material Group	-	According to IEC 60664-1	II	-
Overvoltage Category Per IEC 60664-1	-	Related Mains Voltage ≤ 300 V_{rms}	I-III	-
DIN EN IEC 60747-17; (VDE 0884-17)				
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	AC voltage (bipolar)	566	V_{PK}
Maximum Transient Isolation Voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification) , V_{TEST}= 1.2 x V_{IOTM}, t = 1 s (100 % production)	4243	V_{PK}
Maximum Impulse Voltage	V_{IMP}	IEC 62368-1 1.2/50 µs waveform	4000	V_{PK}
Maximum surge isolation voltage	V_{IOSM}	Test method per IEC 61000-4-5, 1.2/50 µs waveform, V_{IOSM} ≥ 1.3 × V_{IMP} (qualification)	5200	V_{PK}
Apparent charge measuring voltage	$V_{pd(m)}$	Method A, After Input/Output safety test subgroup2&3, $V_{ini,a}$ = V_{IOTM}, $V_{pd(m)}$ = 1.2 x V_{IORM} t_{ini} = 60 s, t_m = 10 s, partial discharge < 5 pC	680	V_{PK}
		Method A, After environmental tests subgroup 1, $V_{ini,a}$ = V_{IOTM}, $V_{pd(m)}$ = 1.3 x V_{IORM} t_{ini} = 60 s, t_m = 10 s, partial discharge < 5 pC	736	
		Method B1; At routine test (100 % production) and preconditioning (type test) $V_{ini,b}$ ≥ 1.2 x V_{IOTM}, $V_{pd(m)}$ = 1.5 x V_{IORM} $t_{ini,b}$ = 1 s, t_m = 1 s partial discharge < 5 pC	849	
Barrier capacitance, input to output	C_{IO}	f = 1 MHz	1.2	pF
Input Capacitance	C_I	input : V_{I1}	4.4	pF
		input : V_{I2}	3.9	
Isolation Resistance	R_{IO}	V_{IO} = 500 V, T_a = 25 °C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100 °C ≤ T_a ≤ 125 °C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150 °C	$>10^{9}$	
Pollution Degree	-	-	2	-
Climatic Category	-	-	40/125/21	-
UL 1577				
Maximum Withstanding Isolation Voltage	V_{ISO}	V_{TEST} = V_{ISO} , t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO} , t = 1 s (100 % production)	3000	V_{rms}

11. Safety Limiting Values

PARAMETER	Symbol	TEST CONDITIONS	Value	Unit
Safety Input, Output or Supply Current	I_S	V_{DD1} = V_{DD2} = 5.5 V, Tj = 150 ℃, Ta = 25 ℃	255	mA
		V_{DD1} = V_{DD2} = 3.6 V, Tj = 150 ℃, Ta = 25 ℃	390	mA
		V_{DD1} = V_{DD2} = 2.75 V, Tj = 150 ℃, Ta = 25 ℃	511	mA
Safety Input, Output or Total Power	P_S	Tj = 150℃, Ta = 25℃	1404	W
Maximum Safety Temperature	T_S	-	150	°C

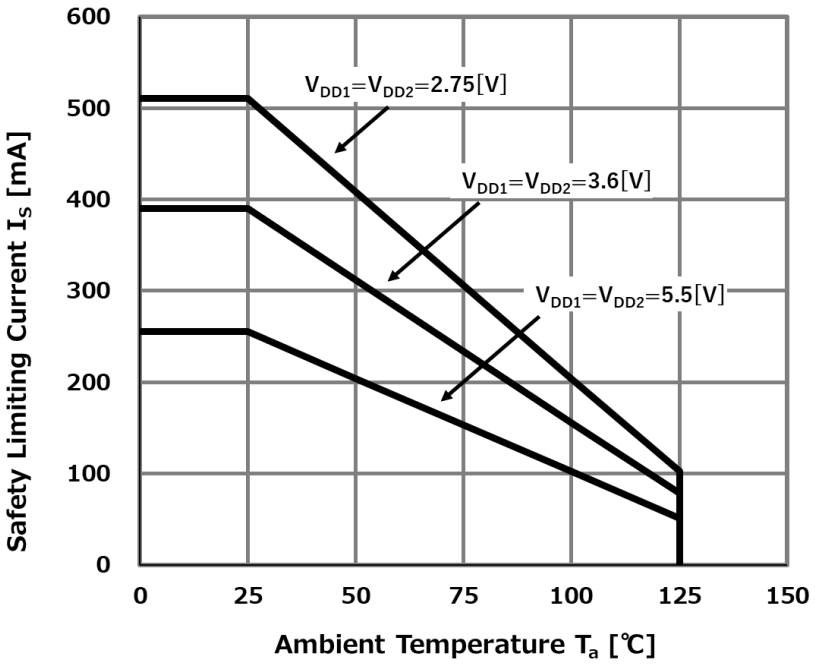


Fig. 11.1 Thermal Derating Curve for Safety Limiting Current-T_a

12. Test Circuit

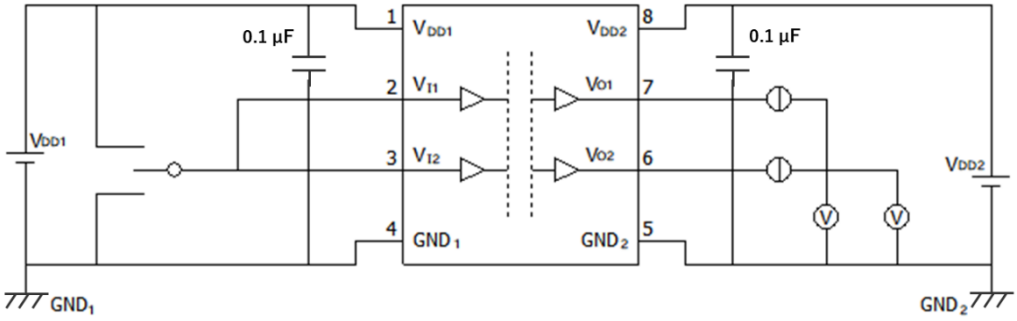


Fig. 12.1 (A) DCL320C00/DCL320D00 V_{OH}/V_{OL} Test Circuit

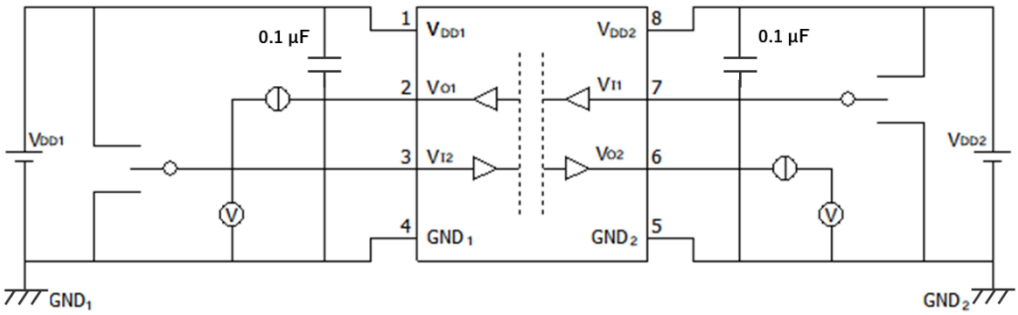


Fig. 12.1 (B) DCL321C00/DCL321D00 V_{OH}/V_{OL} Test Circuit

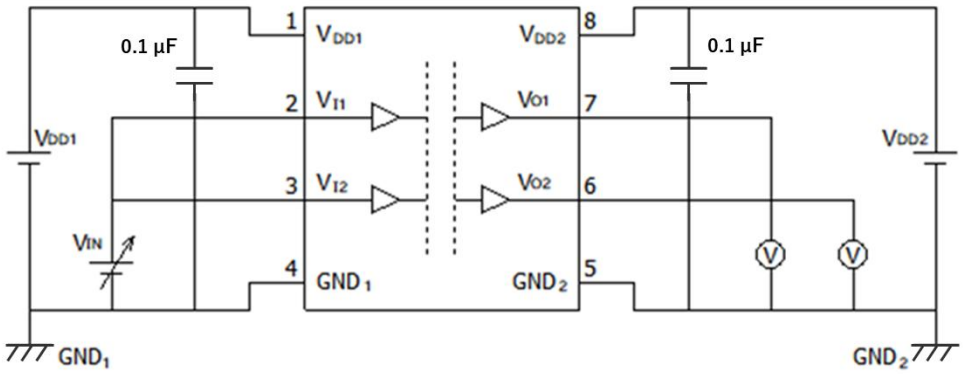


Fig. 12.2 (A) DCL320C00/DCL320D00 V_{IH}/V_{IL} Test Circuit

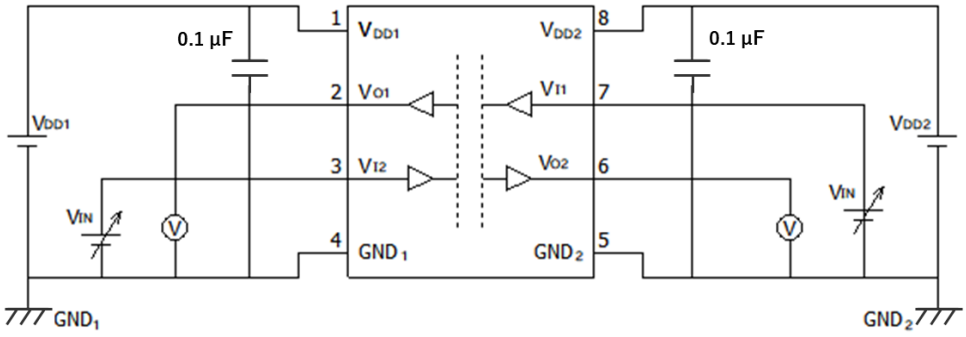


Fig. 12.2 (B) DCL321C00/DCL321D00 V_{IH}/V_{IL} Test Circuit

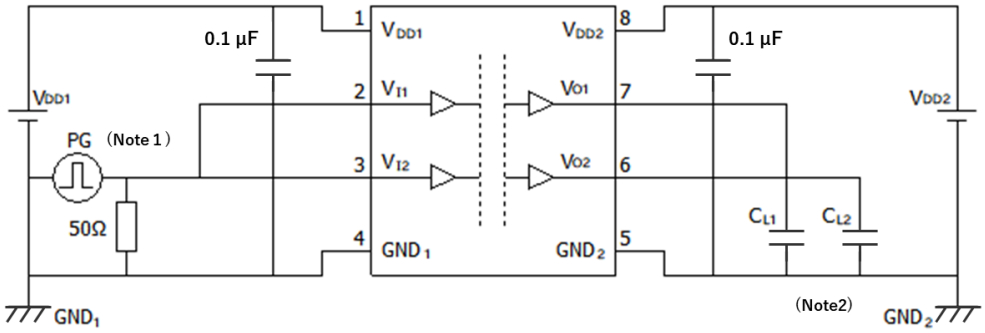


Fig.12.3 (A) DCL320C00/DCL320D00 Switching Test Circuit

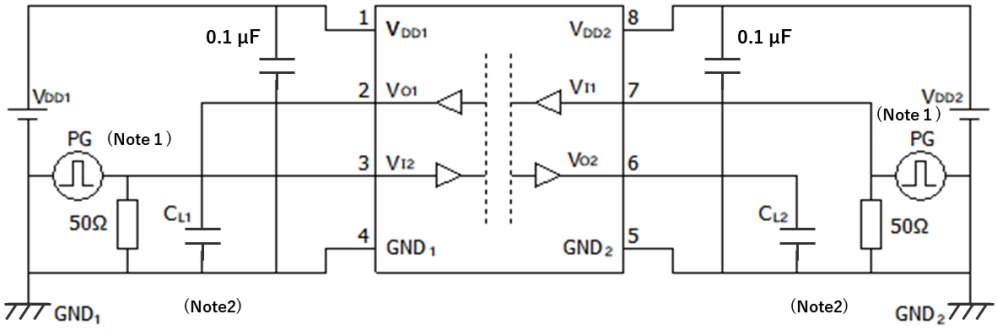


Fig.12.3 (B) DCL321C00/DCL321D00 Switching Test Circuit

Note1: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50 % duty cycle, tr ≤ 2 ns, tf ≤ 2 ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is needed not in actual application.

Note2: C_{LX} = 15 pF includes instrumentation and fixture capacitance.

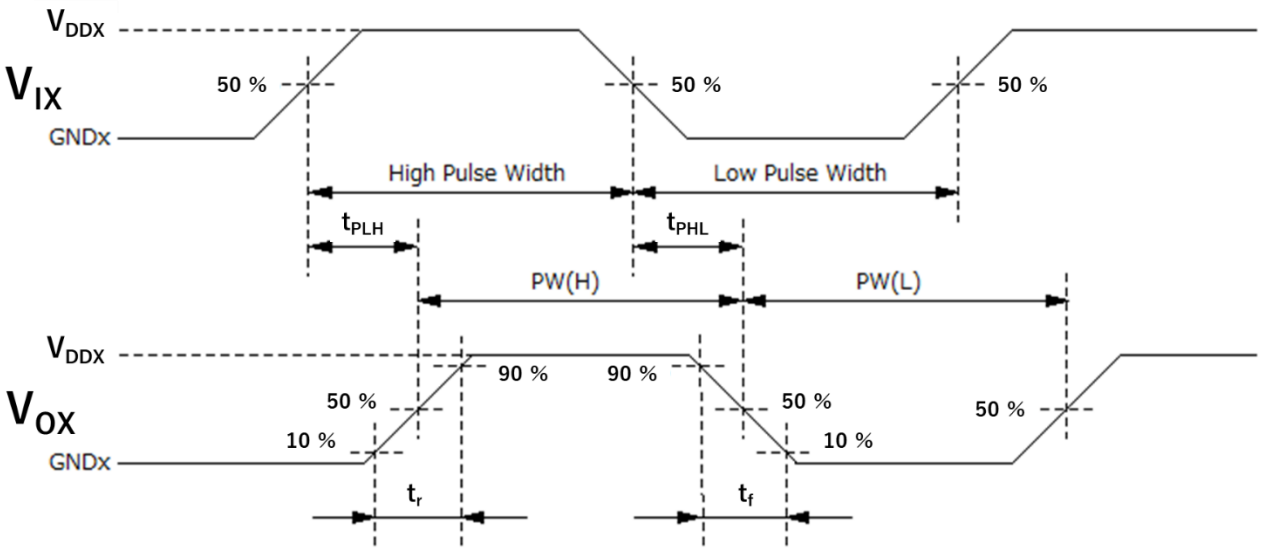


Fig.12.3 (C) Switching Test Circuit and Voltage Waveforms

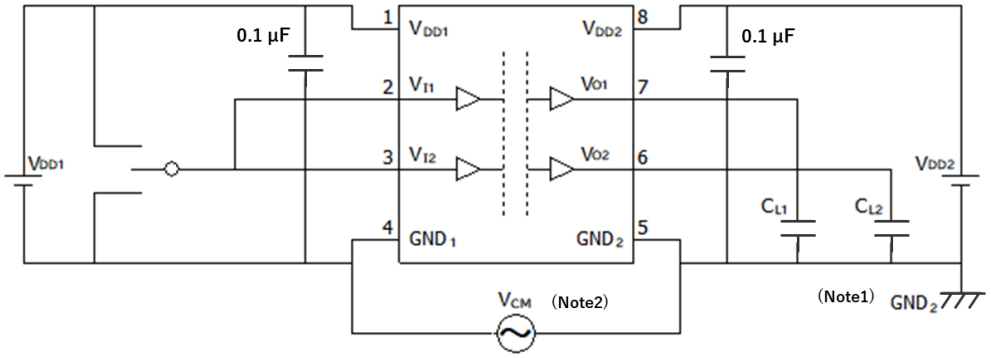


Fig.12.4 (A) DCL320C00/DCL320D00 Common-Mode Transient Immunity Test Circuit

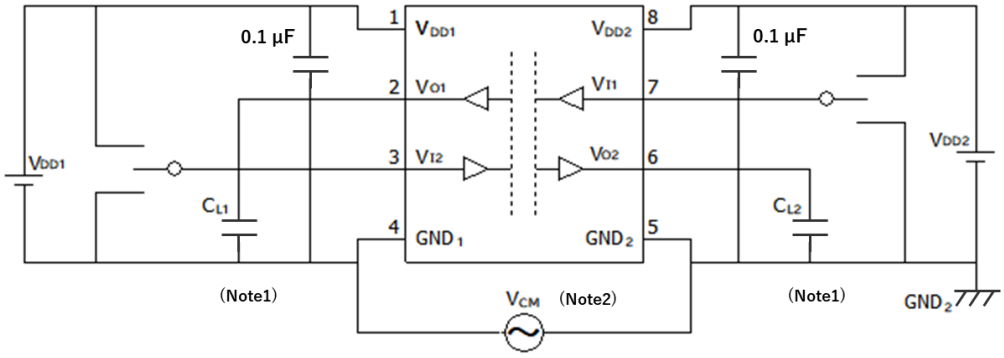


Fig.12.4 (B) DCL321C00/DCL321D00 Common-Mode Transient Immunity Test Circuit

Note1: C_{LX} = 15 pF includes instrumentation and fixture capacitance.

Note2: Apply V_{CM} with reference to the GND terminal on the output terminal side of the IC. The GND on the IC input terminal side is isolated from the output terminal side. Depending on which channel is being measured, V_{CM} may be applied with reference to GND_1 or with reference to GND_2.

13. Characteristics Curves (Note)

Note: The following characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

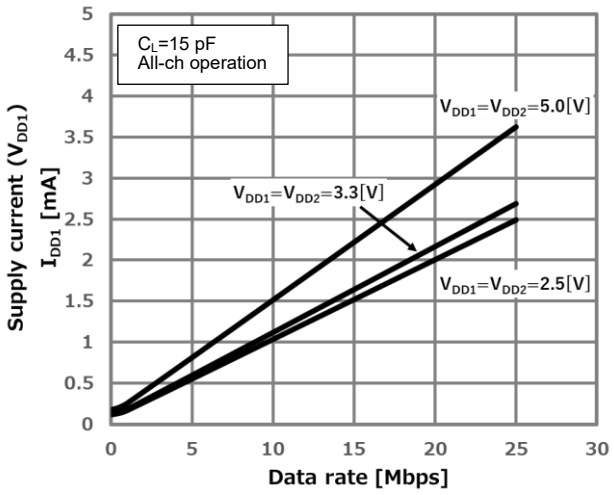


Fig.13.1. DCL321x00 I_{DD1} Supply Current - Data rate

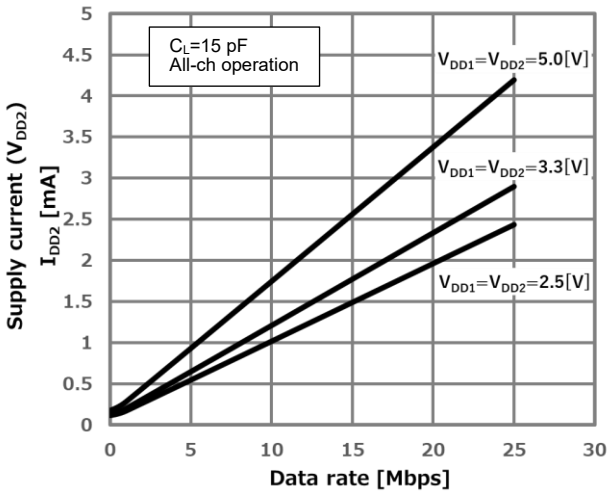


Fig.13.2. DCL321x00 I_{DD2} Supply Current - Data rate

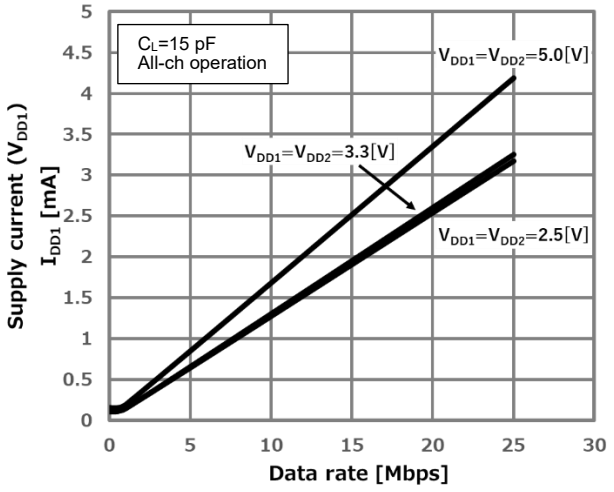


Fig.13.3. DCL320x00 I_{DD1} Supply Current - Data rate

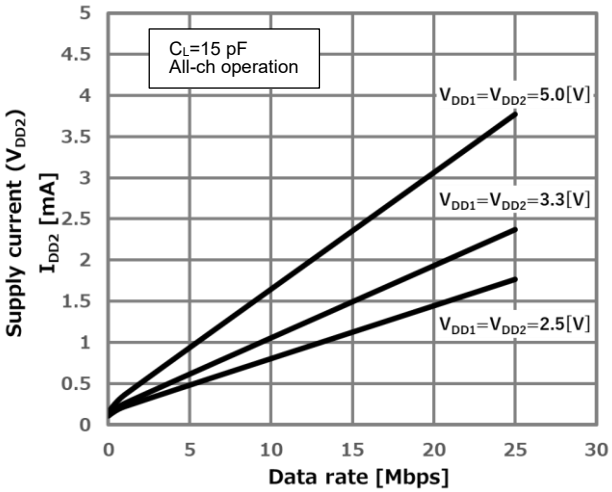


Fig.13.4. DCL320x00 I_{DD2} Supply Current - Data rate

Note: The following characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

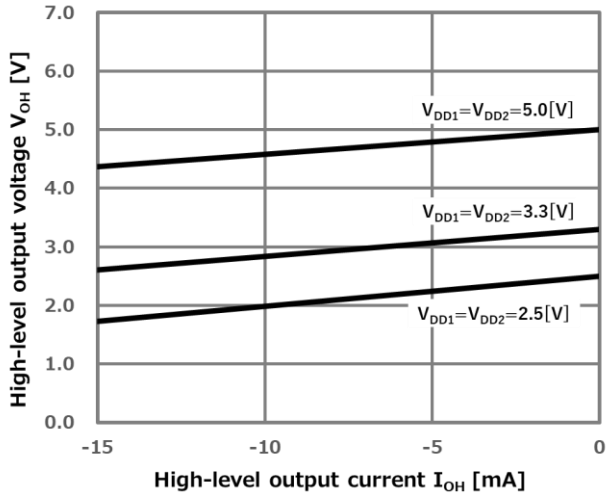


Fig.13.3. VOH－IOH

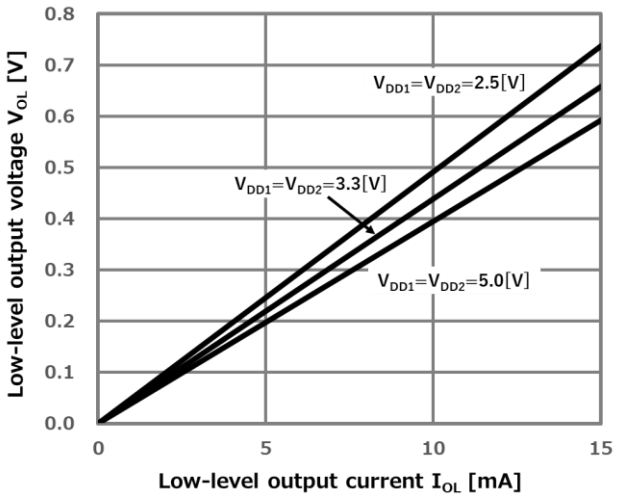


Fig.13.4. VOL－IOL

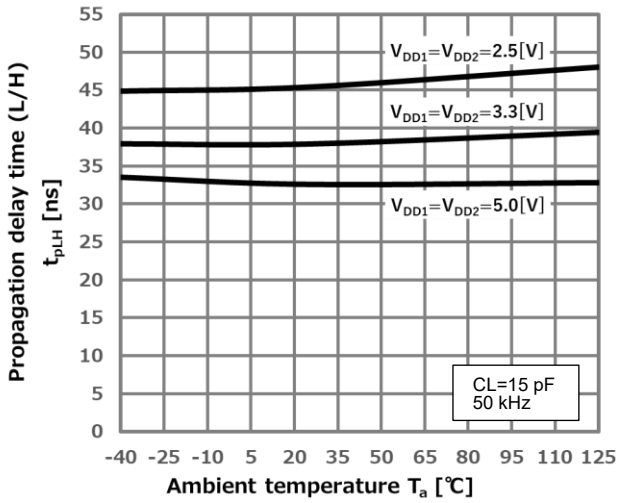


Fig.13.5. Propagation Delay Time t_{PHL}－T_a

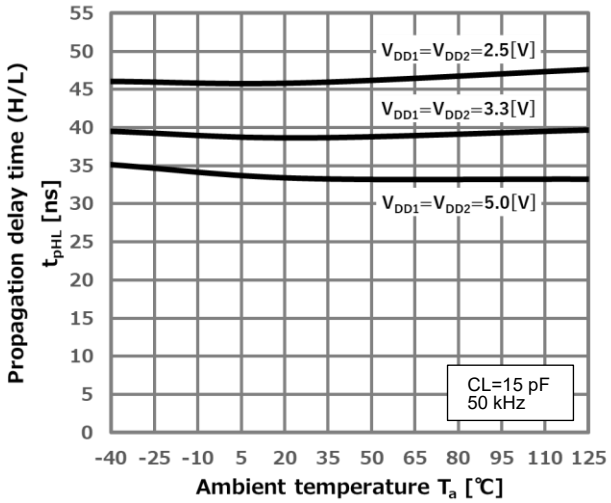
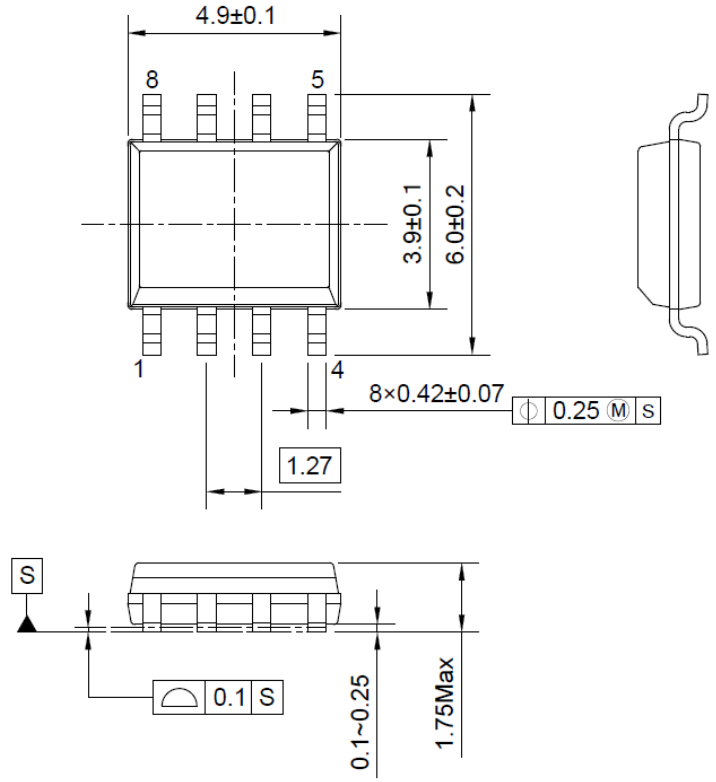
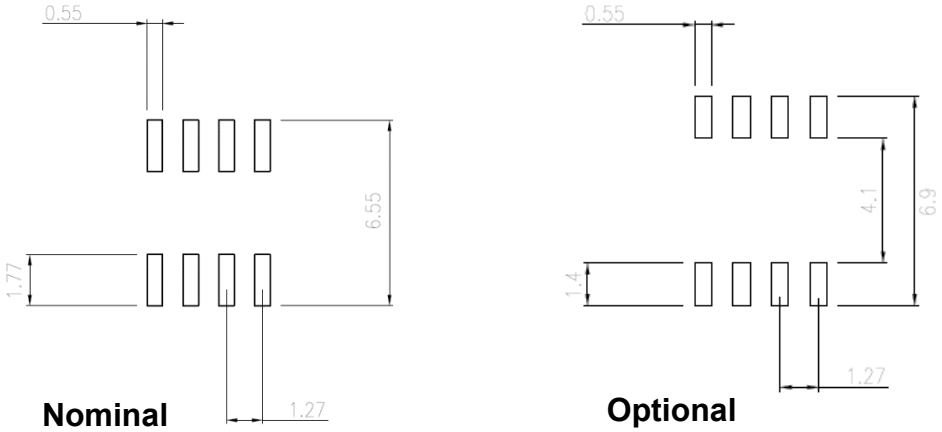


Fig.13.6. Propagation Delay Time t_{PLH}－T_a

14. Package Information

Package Name	SOIC8-N (P-SOP8-0405-1.27-002)
Implementation category	Surface Mount
Pin Number	8
Weight (g)	0.072 (Typ.)
Package Dimension (mm) Width × Length × Height	4.9 ×6.0×1.75(Max)
Package Dimension (mm)	
Land Pattern Example (mm) [for reference only]	

Notes: Land Pattern Dimensions

- All linear dimensions are given in millimeters unless otherwise specified.
- This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only.
  TOSHIBA is not responsible for any incorrect or incomplete drawings and information.
- You are solely responsible for all aspects of your own land pattern, including but not limited to soldering processes.
- The drawing shown may not accurately represent the actual shape or dimensions.
- Before creating and producing designs and using, customers must also refer to and comply with the latest versions of all relevant TOSHIBA information and the instructions for the application that Product will be used with or for.

15.Ordering guide

Model	V_{DD1} end Number of inputs	V_{DD2} end Number of inputs	Default Output	Data rate [Mbps]	Control signal	Temperature range [°C]	Package
DCL320C00	2	0	L	25	-	-40 ~ 125	SOIC8-N
DCL320D00	2	0	H	25	-	-40 ~ 125	SOIC8-N
DCL321C00	1	1	L	25	-	-40 ~ 125	SOIC8-N
DCL321D00	1	1	H	25	-	-40 ~ 125	SOIC8-N

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