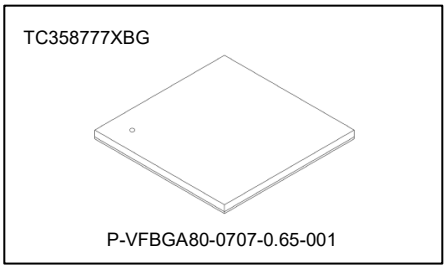
CMOS Digital Integrated Circuit Silicon Monolithic

TC358777XBG

Mobile Peripheral Devices



Weight: 66 mg (typ.)

Overview

This Functional Specification defines operation of TC358777XBG chip, which concatenates two MIPI® DSI® streams of video packets, one from each DSI link into a single VESA® DisplayPort™ video stream.

TC358777XBG housed in a 7.0 mm by 7.0 mm size package with 0.65 mm ball pitch.

TC358777XBG exhibits two independent 4-data lane DSI receivers and one 4-lane DisplayPort transmitter. Each DSI link data lane can receive data up to 1 Gbps/lane, with up to 8 Gbps total input data rate. Each DSI receiver link can activate 0-, 1-, 2-, 3- or 4-data lanes independently. DP main link can toggle bit rate at either 1.62 or 2.7 Gbps per lane, with maximum output data rate at 8.64 Gbps. DP transmitter is able to operate with 1-, 2- or 4-lanes in its main link.

The target application is for high resolution DisplayPort panels, whose bandwidth requirement cannot be met by a single 4-data lane DSI link @4 Gbps. TC358777XBG is an ideal bridge chip which enables application processors, or hosts, with dual DSI links to drive up to 2560 x 2048 x 24 (or 18) DisplayPort panels @60 fps.

Features

● DSI Receiver

- Dual 4-Data Lane DSI Link with Bi-direction support at Data Lane 0, it can be used in 1-, 2-, 3- or 4-data lane configuration.
- Maximum speed at 1 Gbps/lane.
- Video input data formats: RGB-565, RGB-666 and RGB-888.
- Interlaced video mode is not supported.
- Provide path for DSI host/transmitter to control TC358777XBG and its attached panel.
- DSI Link High Speed clock, DSIClk or an external clock, REFCLK, is required before programming TC358777XBG.

● DisplayPort Source/Transmitter

- VESA DisplayPort Rev 1.1a Standard.

  Bit Rate @ 1.62 or 2.7 Gbps, Voltage Swing @0.4, 0.6, 0.8 or 1.2 V, Pre-Emphasis Level @0, 3.5 or 6 dB.

  There are four lanes available in DP main Link, which can operate in 1-, 2- or 4-lane configuration.

  AUX channel with nominal bit rate at 1 Mbps.
- After receiving DSI link burst data, TC358777XBG retimes video data to DP panel's pixel clock for Synchronous (to DisplayPort link symbol clock, LSClk) Clock Mode operation.
- SSCG with up to 30 kHz modulation to reduce EMI.
- Built in Color Bar Generator to verify DisplayPort protocol.
- Secure ASSR (Alternate Scrambler Seed Reset) support for eDP panels

  System designer connects DISABLE_ASSR pin to GND to enable eDP panels and ASSR

  Drive DISABLE_ASSR pin with VDD_IO for using DP panels and disable ASSR

  System software read Revision ID field, 0x0500[7:0]:

  0x01 indicates eDP panels are used, DPCD register bit 0x0010A[0] of eDP panel should be set.

  0x03 assumes DP panels are connected, DPCD register bit 0x0010A[0] of DP panel should Not be set.

● I^2C Target Port

- Support for normal (100 kHz) and fast (400 kHz) modes.
- External I^2C controller can access TC358777XBG internal registers via this port.
- Address auto increment is supported.
- TC358777XBG Target Port address is 0x68, (binary 1101_000x) where x = 1 for read and x = 0 for write. The target address can be changed to 0x0F (binary 0001_111x) by tying pin SPI_SS_I2C_ADR_SEL to high.

● SPI Target Interface

- Target select pin supported.
- Transfer Frame size of 48 bits.
- Maximum clock speed is up to 30 MHz.

● **Audio Interface**
- Support either I^2S or TDM (Time Division Multiplex) mode.
- TDM mode can support 2, 4, 6 and 8 channel of audio data.
- Support 16, 18, 20 or 24-bit PCM audio data word.
- Sample frequency, fs, supported: 32, 44.1, 48, 88.2, 96, 176.4 & 192 kHz.
- 512 × fs audio oversample clock is required to generate accurate audio clock timestamps in order for the DisplayPort panel to recover audio clock correctly.
- Ability to insert IEC60958 status bits and preamble bits per channel.

● **Operation**
- Host programs TC358777XBG either by using DSI link 0 (DSI0), I^2C bus or SPI bus.
- TC358777XBG provides “mailbox registers”, 20-bit AuxAddr and 16-byte AuxData, for Host to access DisplayPort Panel's DisplayPort Configuration Data, DPCD, registers.
- Host splits a video line data into two streams of DSI video packets. Host has two options to split the video line data:

  Left-Right Side: Left (first) side video packet goes to DSI0 and Right side data to DSI1.

  Even-Odd Group: Even (first) groups of pixels are transmitted in DSI0 while Odd ones are carried by DSI1.

  The number of pixels per group is programmable; from 1 to 64.

  The number of pixels per group and/or the number of groups in each video packet can be different between the two DSI links. This feature in connection with TC358777XBG’s capability to support configurable number of data lanes.

  It is recommended that host pack the split video line data into one video packet for each DSI link before transmitting. However, TC358777XBG supports multiple DSI packets per horizontal line time as long as DSI link bandwidth is enough for the overhead.
- TC358777XBG is responsible to generate video frame timing based on the register values set by the Host. Host does not have to care/generate video horizontal timings, such as Horizontal Front/Back Porch and Horizontal Pulse width. Host is responsible to send the video data packets to TC358777XBG in time line-by-line and separated each line data by HSS.

  Host is expected to send exactly one line of video data per horizontal sync period between the two DSI links.

  Host is expected to start HSS_0, HSS packet of DSI0, and HSS_1, HSS packet of DSI1, either at “the same time” or with fixed delay/skew between them (HSS_0 earlier than that of HSS_1).

  “The same time” means within ±5 clock cycles.

  The time skew between the two DSI links' Hsync Start, HSS, packet cannot drift more than one video line time within one video frame period.

  Host is recommended to use the same clock source to generate both DSI link clocks in order to prevent these two clocks from drifting away.

  Otherwise, clock sources with 50 ppm accuracy are required.

  It is recommended that each DSI link sends HSS and video packets back-to-back. Host can insert variable length of blanking packet between HSS and video packets as long as the bandwidth is allowed.
- TC358777XBG concatenates two (streams of) video packets, one (stream) from each DSI link, into a single DisplayPort video stream before transmitting it out to the panel.

● **Clock Source:**
- An external reference clock, REFCLK, is used to drive PLLs for generating DisplayPort's stream/pixel clock, StrmClk/PixelClk, and Link Symbol Clock, LSClk.

  Support DisplayPort Synchronous (StrmClk and LSClk) Clock Mode.

  Allowed REFCLK Frequency Value: 13, 19.2, 26, 38.4 MHz.
- Optionally, DSIClk can be used/divided down to replace REFCLK and drive PLLs used to generate the required clocks.

● **Power Supply**
- MIPI D-PHY[SM] and DP PHY: 1.2 V
- Core: 1.2 V
- DP-PHY: 1.8 V
- I/O: 1.8 V (all IO pins must be same power level)

● **Power Consumption (Typical Condition)**

- Sleep State, with RESX asserted
  12 mW
- Typical Operation:
  2560 × 1440 × 24 @60 fps
  Dual DSI Rx, each link @3.7 Gbps
  31.0 mW for both Links
  Core
  186.6 mW
  DP Tx (2.7 Gbps Link speed @4 lanes, 0.4 V Swing without Pre-Emphasis)
  168.6 mW
  Total = 386.2 mW

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REFERENCES

1. MIPI D-PHY, “MIPI Alliance Specification for D-PHY Version 1.00.00 14-May-2009”
2. MIPI Alliance Standard for DSI Version 1.02.00 – 28 June 2010
3. VESA DisplayPort Standard (Version 1, Revision 1a January 11, 2008)
4. VESA Embedded DisplayPort (eDP) Standard (Version 1.1 October 23, 2009)
5. I^2C bus specification, version 2.1, January 2000, Philips Semiconductor

1. Introduction

This Functional Specification defines operation of TC358777XBG chip, which concatenates two DSI streams of video packets, one from each DSI link into a single DisplayPort video stream.

TC358777XBG housed in a 7.0 mm by 7.0 mm size package with 0.65 mm ball pitch.

TC358777XBG exhibits two independent 4-data lane DSI receivers and one 4-lane DisplayPort transmitter. Each DSI link data lane can receive data up to 1 Gbps/lane, with up to 8 Gbps total input data rate. Each DSI receiver link can activate 0-, 1-, 2-, 3- or 4-data lanes independently. DP main link can toggle bit rate at either 1.62 or 2.7 Gbps per lane, with maximum output data rate at 8.64 Gbps. DP transmitter is able to operate with 1-, 2- or 4-lanes in its main link.

The target application is for high resolution DisplayPort panels, whose bandwidth requirement cannot be met by a single 4-data lane DSI link @4 Gbps. TC358777XBG is an ideal bridge chip which enables application processors, or hosts, with dual DSI links to drive up to 2560 × 2048 × 24 (or 18) DisplayPort panels @60 fps.

DSI host controls/configures TC358777XBG chip by using DSI's Generic Long Write packets. TC358777XBG provides mailbox registers for host to control (command) DisplayPort panel's DisplayPort Configuration Data, DPCD, registers. After host writes to these mailbox registers, TC358777XBG starts Aux channel bus cycles to communicate with the DisplayPort panel. TC358777XBG supports both Aux native mode and I^2C mapped mode.

TC358777XBG supports bi-directional DSI link. Host can read TC358777XBG's registers by using DSI's Generic Short Read (2 parameter) packets. The read data is returned to host via DSI's reverse direction Low Power packets in data lane 0. Host can also access the DPCD status registers of DisplayPort panel by issuing read commands via TC358777XBG's mailbox registers. The maximum read data length is limited to 8 bytes per DSI link read.

Host can also access TC358777XBG's registers, and DP panel's DPCD registers, by using an I^2C bus by addressing TC358777XBG's target address 0x68 (1101_000x). Either an external reference clock, REFCLK, or DSI link's high speed, HS, clock needs to toggle before programming TC358777XBG. REFCLK is limited to 13, 19.2, 26 or 38.4 MHz only.

TC358777XBG exhibits a SPI target port, which provides host as third path to program its registers. Since SPI port shares the same pins as those of I^2C's, only one target port can be used by the Host. I^2C target port is active by default, asserting input pin SPI_I2C activates SPI interface. Please tie the unused input pins to ground.

Audio interface can accept I^2S or Time Domain Multiplex, TDM, type of audio data. This audio data is packed as Secondary Data Packets which are mixed with video stream before routing out to DP panel via DP's main link. Host needs to provide a 512 × fs, audio sample clock frequency, clock in order for the DisplayPort Panel to recover audio clock precisely.

This document assumes that both DSI links use the same clock source to generate DSI links timing. The unintentional clock skews due to two clock sources used to generate DSI links' timing is discussed in “2 Features”.

The target system diagram and TC358777XBG block diagram are shown in Figure 1.1 and Figure 1.2, respectively.

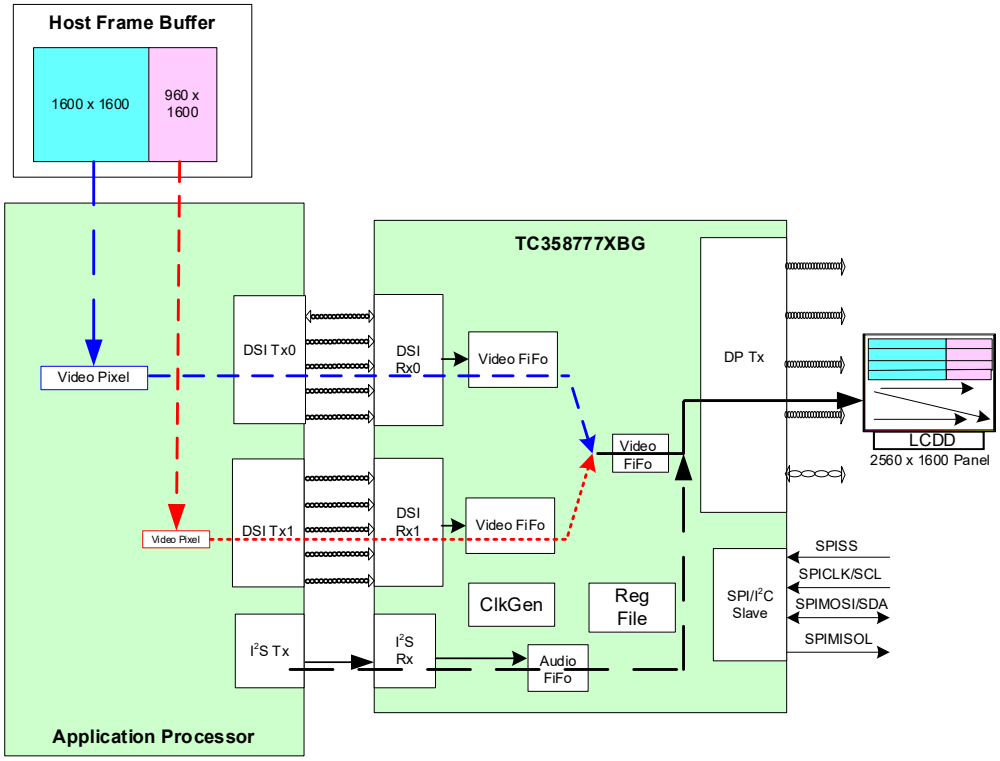


Figure 1.1 TC358777XBG in System Application

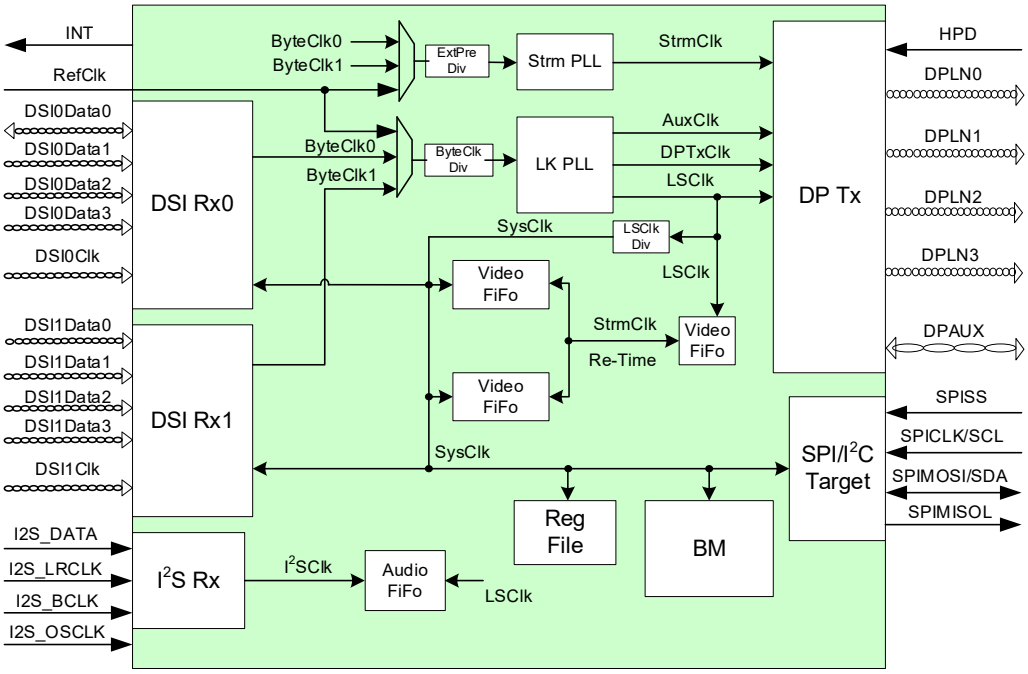


Figure 1.2 TC358777XBG Block Diagram and Functional

2. Features

- **DSI Receiver**
  - Dual 4-Data Lane DSI Link with Bi-direction support at Data Lane 0, it can be used in 1-, 2-, 3- or 4-data lane configuration.
  - Maximum speed at 1 Gbps/lane.
  - Video input data formats: RGB-565, RGB-666 and RGB-888.
  - Interlaced video mode is not supported.
  - Provide path for DSI host/transmitter to control TC358777XBG and its attached panel.
  - DSI Link High Speed clock, DSIClk or an external clock, REFCLK, is required before programming TC358777XBG.

- **DisplayPort Source/Transmitter**
  - VESA DisplayPort Rev 1.1a Standard.
    Bit Rate @ 1.62 or 2.7 Gbps, Voltage Swing @0.4, 0.6, 0.8 or 1.2 V, Pre-Emphasis Level @0, 3.5 or 6 dB.
    There are four lanes available in DP main Link, which can operate in 1-, 2- or 4-lane configuration.
    AUX channel with nominal bit rate at 1 Mbps.
  - After receiving DSI link burst data, TC358777XBG retimes video data to DP panel's pixel clock for Synchronous (to DisplayPort link symbol clock, LSClk) Clock Mode operation.
  - SSCG with up to 30 kHz modulation to reduce EMI.
  - Built in Color Bar Generator to verify DisplayPort protocol.
  - Secure ASSR (Alternate Scrambler Seed Reset) support for eDP panels
    System designer connects DISABLE_ASSR pin to GND to enable eDP panels and ASSR
    Drive DISABLE_ASSR pin with VDD_IO for using DP panels and disable ASSR
    System software read Revision ID field, 0x0500[7:0]:
    0x01 indicates eDP panels are used, DPCD register bit 0x0010A[0] of eDP panel should be set
    0x03 assumes DP panels are connected, DPCD register bit 0x0010A[0] of DP panel should Not be set

- **I^2C Target Port**
  - Support for normal (100 kHz) and fast (400 kHz) modes.
  - External I^2C controller can access TC358777XBG internal registers via this port.
  - Address auto increment is supported.
  - TC358777XBG Target Port address is 0x68, (binary 1101_000x) where x = 1 for read and x = 0 for write. The target address can be changed to 0x0F (binary 0001_111x) by tying pin SPI_SS_I2C_ADR_SEL to high.

- **SPI Target Interface**
  - Target select pin supported.
  - Transfer Frame size of 48 bits.
  - Maximum clock speed is up to 30 MHz.

- **Audio Interface**
  - Support either I^2S or TDM (Time Division Multiplex) mode.
  - TDM mode can support 2, 4, 6 and 8 channel of audio data.
  - Support 16, 18, 20 or 24-bit PCM audio data word.
  - Sample frequency, fs, supported: 32, 44.1, 48, 88.2, 96, 176.4 & 192 kHz.
  - 512 × fs audio oversample clock is required to generate accurate audio clock timestamps in order for the DisplayPort panel to recover audio clock correctly.
  - Ability to insert IEC60958 status bits and preamble bits per channel.

- **Operation**
  - Host programs TC358777XBG either by using DSI link 0 (DSI0), I^2C bus or SPI bus.
  - TC358777XBG provides “mailbox registers”, 20-bit AuxAddr and 16-byte AuxData, for Host to access DisplayPort Panel's DisplayPort Configuration Data, DPCD, registers.
  - Host splits a video line data into two streams of DSI video packets. Host has two options to split the video line data:
    Left-Right Side: Left (first) side video packet goes to DSI0 and Right side data to DSI1.
    Even-Odd Group: Even (first) groups of pixels are transmitted in DSI0 while Odd ones are carried by DSI1.
    The number of pixels per group is programmable; from 1 to 64.
    The number of pixels per group and/or the number of groups in each video packet can be different between the two DSI links. This feature in connection with TC358777XBG's capability to support configurable number of data lanes.
    It is recommended that host pack the split video line data into one video packet for each DSI link before transmitting. However, TC358777XBG supports multiple DSI packets per horizontal line time as long as DSI link bandwidth is enough for the overhead.
  - TC358777XBG is responsible to generate video frame timing based on the register values set by the Host. Host does not have to care/generate video horizontal timings, such as Horizontal Front/Back Porch and Horizontal Pulse width. Host is responsible to send the video data packets to TC358777XBG in time line-by-line and separated each line data by HSS.
    Host is expected to send exactly one line of video data per horizontal sync period between the two DSI links.
    Host is expected to start HSS0, HSS packet of DSI0, and HSS1, HSS packet of DSI1, either at “the same time” or with fixed delay/skew between them (HSS0 earlier than that of HSS1).
    “The same time” means within ±5 clock cycles.
    The time skew between the two DSI links' Hsync Start, HSS, packet cannot drift more than one video line time within one video frame period.
    Host is recommended to use the same clock source to generate both DSI link clocks in order to prevent these two clocks from drifting away.
    Otherwise, clock sources with 50 ppm accuracy are required.
    It is recommended that each DSI link sends HSS and video packets back-to-back. Host can insert variable length of blanking packet between HSS and video packets as long as the bandwidth is allowed.
  - TC358777XBG concatenates two (streams of) video packets, one (stream) from each DSI link, into a single DisplayPort video stream before transmitting it out to the panel.

- **Clock Source:**
  - An external reference clock, REFCLK, is used to drive PLLs for generating DisplayPort's stream/pixel clock, StrmClk/PixelClk, and Link Symbol Clock, LSClk.
    Support DisplayPort Synchronous (StrmClk and LSClk) Clock Mode.
    Allowed REFCLK Frequency Value: 13, 19.2, 26, 38.4 MHz.
  - Optionally, DSIClk can be used/divided down to replace REFCLK and drive PLLs used to generate the required clocks.

- **Power Supply**
  - MIPI D-PHY and DP PHY: 1.2 V
  - Core: 1.2 V
  - DP-PHY: 1.8 V
  - I/O: 1.8 V (all IO pins must be same power level)

- **Power Consumption (Typical Condition)**

  - Sleep State, with RESX asserted
    12 mW

  - Typical Operation:
    2560 × 1440 × 24 @60 fps
    Dual DSI Rx, each link @3.7 Gbps
    31.0 mW for both Links
    Core
    186.6 mW
    DP Tx (2.7 Gbps Link speed @4 lanes, 0.4 V Swing without Pre-Emphasis)
    168.6 mW
    Total = 386.2 mW
    The breakdown of each power rail is shown in the table below

	VDD_DSI12 (1.2 V)	VDDC (1.2 V)	VDD_PLL912 (1.2 V)	VDD_DP12 (1.2 V)	VDD_DP18 VDD_PLL18 (1.8 V)	VDD_IO (1.8 V)	Total Power	Unit
Typical Operation	25.8	153.2	2.3	50.9	59.7	0		mA
	31.0	183.8	2.8	61.1	107.5	0	386.2	mW
Power Down	0.1	3.8	0	2.1	2.7	0		mA
	0.1	4.6	0	2.5	4.9	0	12.1	mW

Note: Attention about ESD. This product is weak against ESD. Please handle it carefully.

3. External Pins

3.1. TC358777XBG Pin Layout

The mapping of TC358777XBG signals to the external pins is shown in the figure below.

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
DSI0DM_0	DSI0DP_0	VDD_DSI12	DSI1DM_3	DSI1DM_2	DSI1CM	VDD_DSI12	DSI1DM_1	DSI1DM_0	VDDIO
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**	**B9**	**B10**
DSI0DM_1	DSI0DP_1	VSS	DSI1DP_3	DSI1DP_2	DSI1CP	VSS	DSI1DP_1	DSI1DP_0	RESX
C1	**C2**							**C9**	**C10**
DSI0CM	DSI0CP							SPI_SCLK	SPI_MISO
D1	**D2**		**D4**	**D5**	**D6**	**D7**		**D9**	**D10**
DSI0DM_2	DSI0DP_2		TEST5	TEST6	TEST7	TEST		SPI_SS	SPI_MOSI
E1	**E2**		**E4**	**E5**	**E6**	**E7**		**E9**	**E10**
DSI0DM_3	DSI0DP_3		VSS	TEST3	TEST4	VPGM		INT	I2S_OSCLK
F1	**F2**		**F4**	**F5**	**F6**	**F7**		**F9**	**F10**
VDDC	VSS		TEST9	VSS	TEST8	Disable ASSR		I2S_BCLK	I2S_DATA
G1	**G2**		**G4**	**G5**	**G6**	**G7**		**G9**	**G10**
PREC_RES_0	PREC_RES_1		DIFF_SE	TEST2	TEST10	VSS		SPI_I2C	I2S_LRCLK
H1	**H2**							**H9**	**H10**
VDDC	VSS							HPD	VDD_PLL912
J1	**J2**	**J3**	**J4**	**J5**	**J6**	**J7**	**J8**	**J9**	**J10**
VDD_DP12	VSS_DP	DPLNP_0	VSS_DP	DPLNP_1	VSS_DP	DPLNP_2	VSS_DP	DPLNP_3	DPAUXP
K1	**K2**	**K3**	**K4**	**K5**	**K6**	**K7**	**K8**	**K9**	**K10**
VDD_PLL18	REFCLK	DPLNM_0	VDD_DP18	DPLNM_1	VDD_DP12	DPLNM_2	VDD_DP18	DPLNM_3	DPAUXM

Figure 3.1 TC358777XBG Chip Pin Layout (Top view)

3.2. TC358777XBG Pinout Description

The following table gives the signals of TC358777XBG and their function.

Table 3.1 TC358777XBG Functional Signal List

Group	Pin Name	I/O	Type	Function	Power Supply
System (6)	REFCLK	I	SCH	13, 19.2, 26 or 38.4 MHz Ref Clock	1.8 V
	DIFF_SE	I	Normal	Test Pin, please tie to GND	1.8 V
	SPI_I2C	I	Normal	1: Activate SPI Target Interface 0: Select I^2C Target Port	1.8 V
	DISABLE_ASSR	I	Normal	1: Disable ASSR, set when connecting to DP panel 0: Enable ASSR for eDP panel application	1.8 V
	RESX	I	SCH	System Reset – active Low	1.8 V
	INT	O	Normal	Interrupt Pin to Host	1.8 V
DSI0 Rx (10)	DSI0CP	I	MIPI-PHY	MIPI-DSI0 Rx Clock Lane Positive	1.2 V
	DSI0CM	I	MIPI-PHY	MIPI-DSI0 Rx Clock Lane Negative	1.2 V
	DSI0DP[0]	I/O	MIPI-PHY	MIPI-DSI0 Rx Data Lane Positive	1.2 V
	DSI0DM[0]	I/O	MIPI-PHY	MIPI-DSI0 Rx Data Lane Negative	1.2 V
	DSI0DP[3:1]	I	MIPI-PHY	MIPI-DSI0 Rx Data Lane Positive	1.2 V
	DSI0DM[3:1]	I	MIPI-PHY	MIPI-DSI0 Rx Data Lane Negative	1.2 V
DSI1 Rx (10)	DSI1CP	I	MIPI-PHY	MIPI-DSI1 Rx Clock Lane Positive	1.2 V
	DSI1CM	I	MIPI-PHY	MIPI-DSI1 Rx Clock Lane Negative	1.2 V
	DSI1DP[3:0]	I	MIPI-PHY	MIPI-DSI1 Rx Data Lane Positive	1.2 V
	DSI1DM[3:0]	I	MIPI-PHY	MIPI-DSI1 Rx Data Lane Negative	1.2 V
DP Tx (13)	HPD	I	SCH	DP Rx Interrupt/Detected	1.8 V
	DPLNP[3:0]	O	DP-PHY	DP Output Main Link Positive	1.8 V
	DPLNM[3:0]	O	DP-PHY	DP Output Main Link Negative	1.8 V
	DPAUXP	I/O	DP-PHY	DP Output AUX Channel Positive	1.8 V
	DPAUXM	I/O	DP-PHY	DP Output AUX Channel Positive	1.8 V
	PREC_RES[1:0]	I	DP-PHY	Precision Resistance (3K @1%)	1.8 V
Audio (4)	I2S_OSCLK	I	Normal	512 times Audio Sample Clock	1.8 V
	I2S_BCLK	I	Normal	Audio Clock	1.8 V
	I2S_LRCLK	I	Normal	Audio Left/Right Selector	1.8 V
	I2S_DATA	I	Normal	Audio Data	1.8 V
SPI/I^2C (4)	SPI_SCLK/I2C_SCL	I	OD	SPI Clock/I^2C Clock	1.8 V
	SPI_MOSI/I2C_SDA	I/O	OD	SPI Input data/I^2C SDA	1.8 V
	SPI_MISO	O	Normal	SPI Output data to Host	1.8 V
	SPI_SS_I2C_ADR_SEL	I	Normal	SPI Target Select, I^2C Target Address Select	1.8 V
DFT (11)	TEST	I	Normal	Test Pin, active high	1.8 V
	TEST[10:2]	I	Normal	Test Pin, please tie to GND	1.8 V
	VPGM	—	—	Test Pin, please tie to GND	1.8 V
Power (11)	VDD_IO (1)	—	—	VDD for IO power supply	1.8 V
	VDD_DP18 (2)	—	—	VDD for DP PHY/Analog PHY	1.8 V
	VDD_PLL18 (1)	—	—	VDD for DP PLL	1.8 V
	VDD_DP12 (2)	—	—	VDD for DP PHY/PLL	1.2 V
	VDD_PLL912 (1)	—	—	VDD for Stream Clock PLL	1.2 V
	VDD_DSI12 (2)	—	—	VDD for MIPI-DSI PHY	1.2 V
	VDDC (2)	—	—	VDD for Internal Core	1.2 V
Ground (11)	VSS_DP (4)	—	—	VSS for DP PHY/PLL	—
	VSS (7)	—	—	VSS for Internal Core/MIPI/IO	—

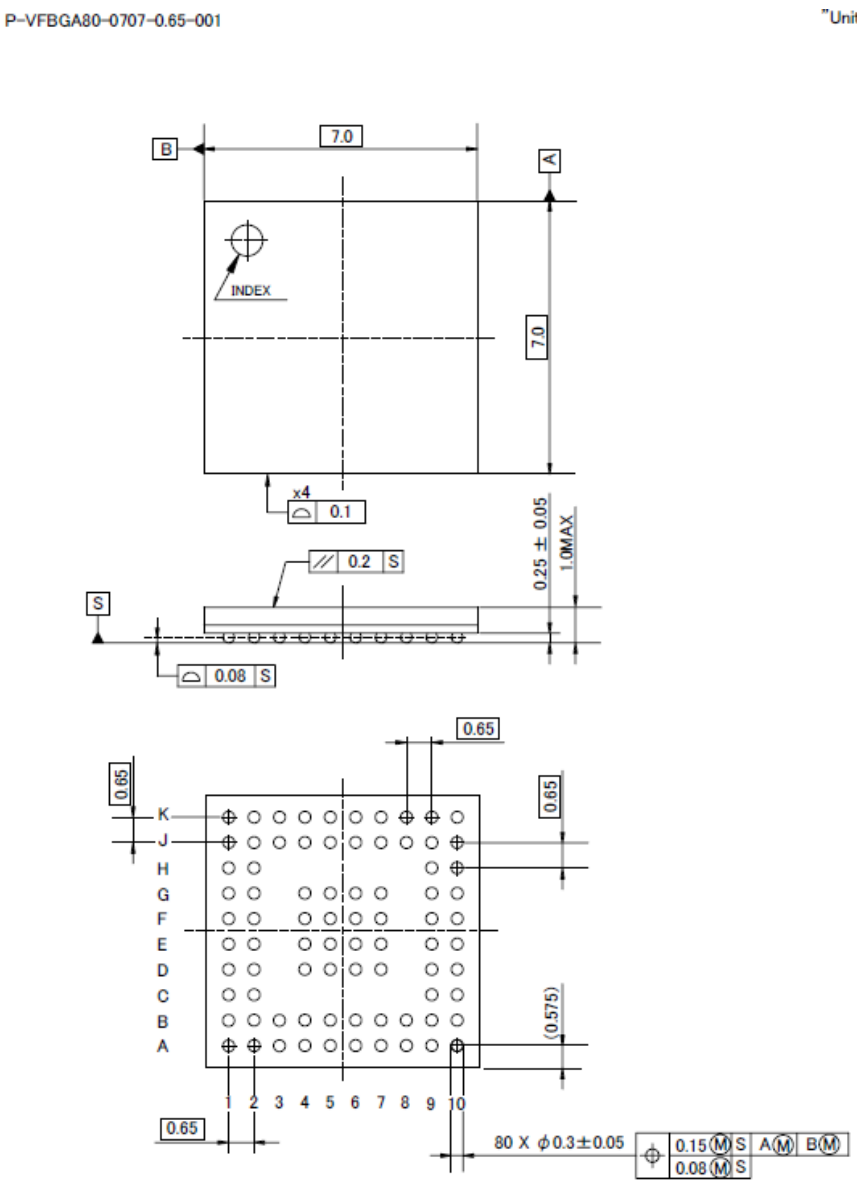
Normal: Normal IO, CMOS input or CMOS output
OD: Pseudo open-drain output, Schmitt trigger input
SCH: Schmitt trigger input buffer
MIPI-PHY: Front-end analog IO for MIPI
DP-PHY: Front-end analog IO for DisplayPort

Table 3.2 Pin Count Summary

Group Name	Pin Count
SYSTEM	6
DSI Rx	20
DisplayPort Tx	13
I^2S	4
SPI/I^2C	4
DFT	11
POWER	11
GROUND	11
Total	80

4. Package

TC358777XBG housed in a 7.0 mm by 7.0 mm size package with 0.65 mm ball pitch. The detailed package drawing is shown below.



Weight: 66 mg (typ.)

Figure 4.1 TC358777XBG Package Dimension

Table 4.1 TC358777XBG Package Details

Description	Normal
Body size (W, mm)	7
Body size (L, mm)	7
Overall thickness (t, mm)	1
Terminal pitch (mm)	0.65

5. Electrical characteristics

5.1. Absolute Maximum Ratings

VSS and VSS_DP = 0 V reference

VDD18 used for VDD_IO as well as VDD_DP18, and VDD_PLL18; VDD12 used for VDDC as well as VDD_DSI12, VDD_DP12, and VDD_PLL912

Parameter	Symbol	Rating	Unit
Supply voltage (1.8 V)	VDD18	-0.3 to +3.5	V
Supply voltage (1.2 V)	VDD12	-0.3 to +2.0	V
Supply voltage (IO)	VDD18	-0.3 to +3.5	V
	V_{REF}	-0.3 to +3.5	V
Input voltage	V_{IN}	-0.3 to VDDIO+0.3	V
Output voltage	V_{OUT}	-0.3 to VDDIO+0.3	V
Storage temperature	T_{stg}	-40 to +125	°C

5.2. Operating Condition

VSS and VSS_DP = 0 V reference

VDD18 used for VDD_IO as well as VDD_DP18, and VDD_PLL18; VDD12 used for VDDC as well as VDD_DSI12, VDD_DP12, and VDD_PLL912

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8 V)	VDD18	1.71	1.8	1.89	V
Supply voltage (1.2 V)	VDD12	1.14	1.2	1.26	V
Operating frequency (internal)	F_{op}	—	—	270	MHz
Operating temperature	T_a	-20	—	+70	°C

5.3. DC Electrical Specification

VSS = VSS_DP = 0 V reference

Parameter	Symbol	Min	Typ.	Max	Unit
Input voltage High level CMOS input (Note 1)	V_{IH}	0.7 VDDIO	—	VDDIO	V
Input voltage Low level CMOS input (Note 1)	V_{IL}	0	—	0.3 VDDIO	V
Input voltage High level Schmitt trigger input (Note 1)	V_{IHS}	0.7 VDDIO	—	VDDIO	V
Input voltage Low level Schmitt trigger input (Note 1)	V_{ILS}	0	—	0.3 VDDIO	V
Output voltage High level, I_{OH} = -4 mA (Note 1)	V_{OH}	0.8 VDDIO	—	VDDIO	V
Output voltage Low level, I_{OL} = 4 mA (Note 1)	V_{OL}	0	—	0.2 VDDIO	V
Input leak current High level	I_{IH} (Note 2)	-10	—	10	μA
Input leak current Low level	I_{IL} (Note 3)	-10	—	10	μA

Note 1: VDD_IO within operating condition.

Note 2: Normal pin, or Schmitt trigger pin applied VDD_IO supply voltage to input pin.

Note 3: Normal pin, or Schmitt trigger pin applied VSS (0 V) to input pin.

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.0	2012-11-10	1. Start from 770XBG Rev 0.99D 2. Add ASSR support 3. Add Power consumption for each voltage rail
1.1	2013-01-15	1. Update MIPI copyright Footer: Change “Toshiba America Electronic Components, Inc.” to “Toshiba Corporation and its affiliates.” 2. Update VSDelay Calculation (assume DP data lane is either 2 or 4 lanes)
1.2	2013-10-25	1. Typo correction on register Tx_Rx_TA 2. Add Audio Functionality Description
1.3	2013-11-17	1. Update register field description for 0x0644[23:18]
1.4	2014-06-20	1. Add 777XBG package
1.41	2016-07-20	1. Typo Correction on DSI1DP[3:0]/DSI1DM[3:0]
1.42	2016-09-01	1. Modified duplicate DSI1CP/DSI1CM.
1.6	2017-10-23	Corrected typo. Changed header, footer and the last page. Changed corporate name.
1.63	2019-02-07	Modified descriptions of trademark and service mark. Corrected typos. Modified descriptions of I^2C in Features. Corrected weight of TC358777XBG in cover page and chapter 4. Revised the last page “RESTRICTIONS ON PRODUCT USE” and added URL.
1.65	2024-04-10	Changed from supporting HDCP to not supporting HDCP. Corrected typos.
2.00	2026-06-12	Removed TC358770AXBG package. Updated the term “Master/Slave” to “Controller/Target”. Corrected typos. Revised the last page “RESTRICTIONS ON PRODUCT USE”.

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