

Application Note

TMPM3HQB UsersManual

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1. Preface

This application note describes a reference for the usage environment when running the sample program on TMPM3HQB10B.

If you select something other than TMPM3HQB10B the MCU, a compile error may occur due to insufficient terminal or IP channel.

In that case, please modify the program and check the operation.

2. Technical Term

Term/Abbreviation	Definition
BSP	Board Support Package
UART	Universal Asynchronous Receiver Transmitter
LED	Light-emitting diode
TSPI	Toshiba Serial Peripheral Interface
I2C	Inter-Integrated Circuit
EI2C	Enhanced Inter-Integrated Circuit

3. Reference Document

Document	Notes
TMPM3H Group (2) Data sheet	-
Reference manual	Refer to the reference manual of each IP to be used.
Application note	Refer to the application note of sample software to be used.

4. Operation Confirmation Condition

Item	Name	Version
Used Microcontroller	TMPM3HQB10BFG	-
Used Board	AdBun-M3HQB	-
Integrated Development Environment	EWARM	V9.60
Integrated Development Environment	Arm® Keil® MDK	V5.43
Integrated Development Environment	Embedded Studio	V8.24
Sample Program	TXZp_TMPM3HQB	V2.0.0

5. Used Channel and Port Assignment

5.1. User Interface

5.1.1. Push-Switch

Channel	Function	Port
BSP_PSW_1	Input	PV0
BSP_PSW_2	Input	PV1
BSP_PSW_3	Input	PV2
BSP_PSW_4	Input	PV3
BSP_PSW_5	Input	PC2

5.1.2. Slide-Switch

Channel	Function	Port
BSP_SSW_1	Input	PP6
BSP_SSW_2	Input	PP7
BSP_SSW_3	Input	-
BSP_SSW_4	Input	-

5.1.3. LED

Channel	Function	Port
BSP_LED_1	Output	PK4
BSP_LED_2	Output	PK5
BSP_LED_3	Output	PK6
BSP_LED_4	Output	PK7

5.2. Communication

5.2.1. UART Communication

Channel	Peripheral Channel	Function	Port
BSP_UART_1	ch0	BSP_UART1_TXD	PA1
		BSP_UART1_RXD	PA2
		BSP_UART1_CTS	-
		BSP_UART1_DTR	-
BSP_UART_2	-	BSP_UART2_TXD	-
		BSP_UART2_RXD	-
		BSP_UART2_CTS	-
		BSP_UART2_DTR	-

5.2.2. TSPI Communication

Channel	Peripheral Channel	Function	Port
BSP_TSPI_1	ch0	BSP_SPI1_TXD	PB3
		BSP_SPI1_RXD	PB4
		BSP_SPI1_SCK	PB2
		BSP_SPI1_CS	PB5
		BSP_SPI1_CSIN	PB5
BSP_TSPI_2	ch1	BSP_SPI2_TXD	-
		BSP_SPI2_RXD	-
		BSP_SPI2_SCK	-
		BSP_SPI2_CS	-
		BSP_SPI2_CSIN	-

5.2.3. I2C Communication

Channel	Peripheral Channel	Function	Port
BSP_I2C_1	ch1	BSP_I2C1_SCL	PA4
		BSP_I2C1_SDA	PA5
BSP_I2C_2	-	BSP_I2C2_SCL	-
		BSP_I2C2_SDA	-

5.2.4. EI2C Communication

Channel	Peripheral Channel	Function	Port
BSP_EI2C_1	ch1	BSP_EI2C1_SCL	PA4
		BSP_EI2C1_SDA	PA5
BSP_EI2C_2	-	BSP_EI2C2_SCL	-
		BSP_EI2C2_SDA	-

5.3. Timer

Channel	Peripheral Channel	Function	Port
BSP_T32A_1	BSP_T32A_TIMER_1	ch0A: 1ms Timer	-
BSP_T32A_2	BSP_T32A_PPG_1	ch3A: Pulse Output (T32A_PPG Sample)	PJ0
BSP_T32A_3	BSP_T32A_PPG_2	ch0A: Pulse Output (TRM Sample)	PA0
BSP_T32A_4	BSP_T32A_CAPT_1	ch2A: Pulse Output (TRM Sample)	PR1
BSP_T32A_5	BSP_T32A_TRM_fs	-	-
BSP_T32A_6	BSP_T32A_CAPT_2	ch3B: Pulse Input (T32A_MEASURE Sample)	-

5.4. ADC

Channel	Peripheral Channel	Function	Port
BSP_ADC_1	BSP_THERMISTOR_1	Variable resistance voltage	PE0
BSP_ADC_2	BSP_VR_1	Variable resistance voltage	PD4
BSP_ADC_3	BSP_VR_2	Variable resistance voltage	PD5

5.5. A-ENC

Channel	Peripheral Channel	Function	Port
BSP_ENC_1	BSP_ENC1_A	Encoder input	PA0
	BSP_ENC1_B	Encoder input	PA1
	BSP_ENC1_Z	Encoder input	-
BSP_ENC_2	BSP_ENC2_A	Encoder input	-
	BSP_ENC2_B	Encoder input	-
	BSP_ENC2_Z	Encoder input	-

5.6. DAC

Channel	Peripheral Channel	Function	Port
BSP_ADC_1	ch0	-	PG0
BSP_ADC_2	-	-	PG1
BSP_ADC_3	-	-	-
BSP_ADC_4	-	-	-

5.7. Remote Controller

Channel	Peripheral Channel	Function	Port
BSP_RMC_1	ch0	-	PB1

5.8. Digital LCD

Channel	Peripheral Channel	Function	Port
BSP_DLCD_1	-	-	-
DCOM	BSP_DLCD_DCOM0	DCOM0	PC3
	BSP_DLCD_DCOM1	DCOM1	PC2
	BSP_DLCD_DCOM2	DCOM2	PC1
	BSP_DLCD_DCOM3	DCOM3	PC0
SEG	BSP_DLCD_SEG00	(BSP_PSW_4dual use)	PV3
	BSP_DLCD_SEG01	(BSP_PSW_3dual use)	PV2
	BSP_DLCD_SEG02	(BSP_PSW_2dual use)	PV1
	BSP_DLCD_SEG03	(BSP_PSW_1dual use)	PV0
	BSP_DLCD_SEG04	SEG04	PP7
	BSP_DLCD_SEG05	SEG05	PP6
	BSP_DLCD_SEG06	SEG06	PP5
	BSP_DLCD_SEG07	SEG07	PP4
	BSP_DLCD_SEG08	SEG08	PP3
	BSP_DLCD_SEG09	SEG09	PK7
	BSP_DLCD_SEG10	SEG10	PK6
	BSP_DLCD_SEG11	SEG11	PK5
	BSP_DLCD_SEG12	SEG12	PK4
	BSP_DLCD_SEG13	(MBEDIF_IO1 dual use)	PK3
	BSP_DLCD_SEG14	SEG14	PK2
	BSP_DLCD_SEG15	(MBEDIF_IO0 dual use)	PK1
	BSP_DLCD_SEG16	SEG16	PK0
	BSP_DLCD_SEG17	SEG17	PJ5
	BSP_DLCD_SEG18	SEG18	PJ4
	BSP_DLCD_SEG19	SEG19	PJ3
	BSP_DLCD_SEG20	(MBEDIF_RXD dual use)	PJ2
	BSP_DLCD_SEG21	(MBEDIF_TXD dual use)	PJ1
	BSP_DLCD_SEG22	SEG22	PJ0
	BSP_DLCD_SEG23	SEG23	PN0
	BSP_DLCD_SEG24	SEG24	PN1
	BSP_DLCD_SEG25	SEG25	PN2
	BSP_DLCD_SEG26	SEG26	PN3
	BSP_DLCD_SEG27	SEG27	PN4
	BSP_DLCD_SEG28	SEG28	PN5
	BSP_DLCD_SEG29	SEG29	PR7
	BSP_DLCD_SEG30	SEG30	PR6
	BSP_DLCD_SEG31	SEG31	PR5
	BSP_DLCD_SEG32	SEG13	PR4
	BSP_DLCD_SEG33	SEG15	PR3
	BSP_DLCD_SEG34	SEG20	PR2
	BSP_DLCD_SEG35	SEG21	PR1
	BSP_DLCD_SEG36	SEG00	PR0
	BSP_DLCD_SEG37	SEG01	PC6
	BSP_DLCD_SEG38	SEG02	PC5
	BSP_DLCD_SEG39	SEG03	PC4

6. System Setting

6.1.1. Power supply voltage

V	Notes
3.3	-

6.1.2. Clock setting

Clock	Function	MHz	Notes
fEHOSC	External oscillator	12	-
fIHOSC	Internal oscillator	10	-
fs	Low-speed oscillator	0.032768	-
fc	High-speed clock	120	Uses fEHOSC, fsys, ϕ T0 base clock, ADC, DNF
fsys	High speed system clock	120	Peripheral operating clocks other than ADC and DNF
ϕ T0	-	120	-

Note: It's basic setting. Settings change depending on the sample software.

7. Communication Setting

7.1. UART Communication Setting

7.1.1. UART Setting

Item	Setting Value	Notes
Baud Rate	115200(bps)	-
Data Length	8(bit)	-
Parity	None	-
Stop Bit	1(bit)	-
Flow Control	None	-

7.1.2. Log Control line feed code

Item	Setting Value	Notes
[line feed] (Send to Terminal emulator)	LF	-
[line feed] (Receive from Terminal emulator)	LF	-

7.1.3. Log Control error

Item	Setting Value	Notes
Error Log_Command	"Command Error!![line feed]"	When an unsupported command is entered
Error Log_Parameter	"Parameter Error!![line feed]"	Command parameter is not the expected value
Error Log_Input	"Input Error!![line feed]"	When an input request other than a command is not an expected value
Error Log_Erasing	"Erasing Error!![line feed]"	Flash
Error Log_Writing	"Writing Error!![line feed]"	Flash, I2C
Error Log_Reading	"Reading Error!![line feed]"	Flash, I2C

7.1.4. Log Control and others

Item	Setting Value	Notes
MCU name	TMPM3HQB	-

7.2. I2C Communication Setting

7.2.1. I2C Setting

Item	Setting Value	Notes
I2C Clock (EI2C-A)	800kHz	In Concroller operation
I2C Clock (I2C-B)	400kHz	In Concroller operation
Data Length	8bit	-
Acknowledge	Available	-
Start/Stop Condition	Generated	-

7.2.2. Target Operating Specifications

Item	Setting Value	Notes
Target Address	0x60	Indicates 7bit that enters <7:1>
Sub Address Size	0x02	Sub Address is 2byte
Start Sub Address	0x0000	Indicates the leading Address of Sub Address
Data Size	0x10	Indicates the valid data size (byte)>>Sub Address range:0000-000F
Init Value	0x55	Initial value of Data.
Dummy Data	0xAA	This is returned when Read request is out of scope

7.3. SPI Communication Setting

Item	Setting Value	Notes
SPI Clock	10MHz	In Controller operation
Data Length	8bit	-
Parity	None	-
Data Transfer Direction	MSB	-

7.4. BSP Slave Device Specifications

Item	Specification	Notes
SPI Slave IC	ICM-20602	-

8. Flash Control range

8.1. Reference Manual

Reference manual	Notes
TXZ+ Family Reference Manual Flash Memory	FLASH10MUD32-A

8.2. Code Flash Required specification control range

Flash Area	Start	Stop	Size	Notes
Code Flash All area	0x00000000	0x000FFFFF	512kbyte	
Code Flash Block 0	0x00000000	0x00007FFF	32kbyte	
Code Flash Page 0	0x00000000	0x00000FFF	4 kbyte	
Code Flash Page 1	0x00001000	0x00001FFF	4 kbyte	
Code Flash Page 2	0x00002000	0x00002FFF	4 kbyte	
Code Flash Page 3	0x00003000	0x00003FFF	4 kbyte	
Code Flash Page 4	0x00004000	0x00004FFF	4 kbyte	
Code Flash Page 5	0x00005000	0x00005FFF	4 kbyte	
Code Flash Page 6	0x00006000	0x00006FFF	4 kbyte	
Code Flash Page 7	0x00007000	0x00007FFF	4 kbyte	
Code Flash Page SIZE	0x00001000	-	4 kbyte	
Code Flash Block 1	0x00008000	0x0000FFFF	32 kbyte	CODE areas A
Code Flash Block 2	0x00010000	0x00017FFF	32 kbyte	CODE areas B

8.3. Code Flash User Information Required specification control range

Code Area	Start	Stop	Notes	Notes
UserInformation All area	0x5E005000	0x5E005FFF	4 kbyte	

8.4. Data Flash Required specification control range

Code Area	Start	Stop	Notes	Notes
Data Flash All area	0x30000000	0x30007FFF	32 kbyte	
Data Flash Block 0	0x30000000	0x30000FFF	4 kbyte	
Data Flash Page 0	0x30000000	0x300000FF	256 byte	
Data Flash Page 1	0x30000100	0x300001FF	256 byte	
Data Flash Page SIZE	0x100	-	256 byte	

9. DLCD

9.1. DLCD Control Device

Item	Specification
DLCD_PANEL	S5038

10. Interrupt List by Sample

10.1. ADC_NTC_Monitor

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update
INTADACP0	ADC monitor. For monitoring temperature information (Temperature A)
INTADACP1	ADC monitor. For monitoring temperature information (Temperature B)
INTUART0TX	UART Transmit Interrupt for terminal emulator
INTUART0ERR	UART Error Interrupt for terminal emulator

10.2. A-ENC32

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update

10.3. CG_EXINT

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update
INT02	External interrupts when BSP_PSW_5 is pressed

10.4. CG_RTC

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update
INTRTC	RTC interrupt

10.5. CRC

Interrupt Source	Control Description
INTUART0TX	UART Transmit Interrupt
INTUART0ERR	UART Error Interrupt

10.6. DAC

Interrupt Source	Control Description
INTUART0RX	UART Receive Interrupt
INTUART0TX	UART Transmit Interrupt
INTUART0ERR	UART Error Interrupt

10.7. DLCD

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update
INTADACNT	ADC continuous conversion interrupt

10.8. DNF

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update
INT17_18_32_33	External interrupt when PSW_5 is pressed

10.9. I2C Common

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update
INTI2C1NST	I2C Interrupt
INTI2C1ATX	I2C Arbitration Lost Detection Interrupt
INTI2C1BRX	I2C Bus Free Detection Interrupt

10.10. EI2C Common

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update

10.11. FLASH Common

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update
INTUART0TX	UART Transmit Interrupt
INTUART0ERR	UART Error Interrupt

10.12. LVD

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update

10.13. OFD

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update

10.14. PORT

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update

10.15. RAMP

Interrupt Source	Control Description
INTRARIO	RAMP RAM Parity Interrupt
INTUART0RX	UART Receive Interrupt
INTUART0TX	UART Transmit Interrupt
INTUART0ERR	UART Error Interrupt

10.16. RMC

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update
INTRMC0	RMC interrupt (Leader detection interrupt, configure to end reception / trigger an interrupt when the data bit period reaches MAX)
INTUART0TX	UART Transmit Interrupt
INTUART0ERR	UART Error Interrupt

10.17. RTC

Interrupt Source	Control Description
INTRTC	RTC Interrupt
INTUART0TX	UART Transmit Interrupt
INTUART0ERR	UART Error Interrupt

10.18. SIWDT

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update
NMI	Watchdog Timer Interrupt

10.19. T32A_IntevalTimer

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update

10.20. T32A_MEASURE

Interrupt Source	Control Description
INTT32A03A	T32A Timer A, Timer counter increments every 512ms for display update. For PPG outputting
INTUART0TX	UART Transmit Interrupt
INTUART0ERR	UART Error Interrupt

10.21. T32A_PPG

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update
INTUART0TX	UART Transmit Interrupt
INTUART0ERR	UART Error Interrupt

10.22. TRM

Interrupt Source	Control Description
INTT32A02ACAP0	T32A chx Timer y Capture 0, For pulse measurement. Used to measure the external reference clock.
INTT32A02ACAP1	T32A chx Timer y Capture 1, For pulse measurement. Used to measure the external reference clock.
INTT32A06BCAP1	T32A chx Timer y Capture 1, For pulse measurement. Used to measure fs
INTUART0TX	UART Transmit Interrupt
INTUART0ERR	UART Error Interrupt

10.23. TSPI_ACCELEROMETER

Interrupt Source	Control Description
INTUART0TX	UART Transmit Interrupt
INTUART0ERR	UART Error Interrupt
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update
INTT1RX	SPI Receive Interrupt
INTT1TX	SPI Transmit Interrupt

10.24. TSPI_xxx_RECEIVE

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update
INTT1RX	SPI Receive Interrupt
INTT1ERR	SPI Error Interrupt
INTDMAATC	DMA Transmit End Interrupt
INTDMAAERR	DMA Error Interrupt

10.25. TSPI_xxx_TRANS

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update
INTT1TX	SPI Transmit Interrupt
INTT1ERR	SPI Error Interrupt
INTDMAATC	DMA Transmit End Interrupt
INTDMAAERR	DMA Err or Interrupt

10.26. UART_RECEIVE

Interrupt Source	Control Description
INTUART0RX	UART Receive Interrupt
INTUART0ERR	UART Error Interrupt
INTDMAATC	DMA Transmit End Interrupt
INTDMAAERR	DMA Error Interrupt

10.27. UART_TRANS

Interrupt Source	Control Description
INTT32A00A	T32A Timer A, Timer counter increments every 1ms for display update
INTUART0TX	UART Transmit Interrupt
INTUART0ERR	UART Error Interrupt
INTDMAATC	DMA Transmit End Interrupt
INTDMAAERR	DMA Error Interrupt

11. Precautions for Use

Please confirm the operation sufficiently if use in an environment other than the operation check environment.

12. Revision History

Revision	Data	Description
1.0	2026/06/30	First release

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