

TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

TC75W51FU, TC75W51FK

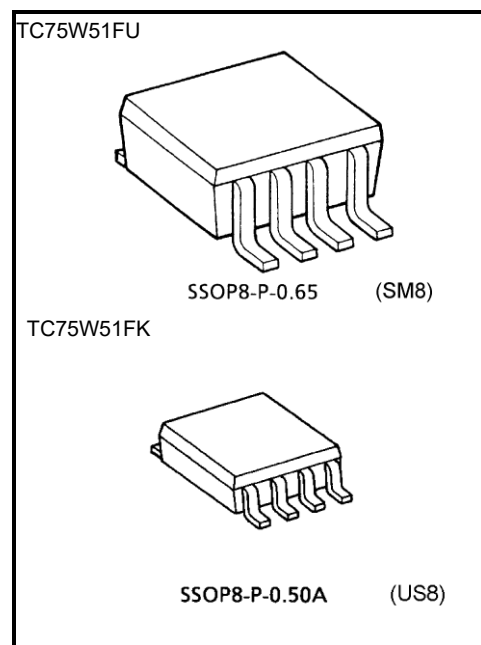
Dual Operational Amplifier

1. General

The TC75W51 is a CMOS Dual-operation amplifier which incorporates a phase compensation circuit. It is designed for use with a low voltage, low-current power supply; This differentiates this device from conventional general-purpose bipolar op-amps.

2. Features

- Low supply voltage: $V_{DD} = \pm 0.75$ to ± 3.5 V or 1.5 to 7 V
- Low supply current: $I_{DD} (V_{DD} = 3 \text{ V}) = 120 \mu\text{A}$ (typ.)
- The internally phase compensated operational amplifier.
- Small package



Weight

SSOP8-P-0.65 : 0.021 g (typ.)

SSOP8-P-0.50A : 0.01 g (typ.)

3. Absolute Maximum Ratings (Note) ($T_a = 25^\circ\text{C}$)

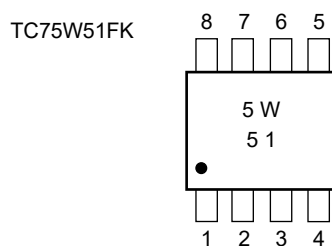
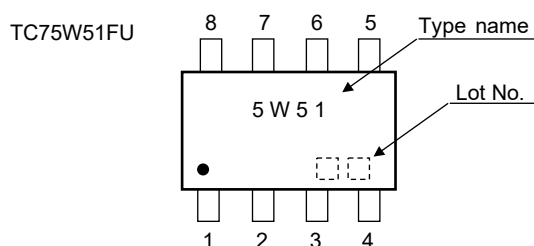
Characteristic	Symbol	製品名	Rating	Unit
Supply voltage	V_{DD}, V_{SS}		± 3.5 or 7	V
Differential input voltage	DV_{IN}		± 7	V
Input voltage	V_{IN}		V_{SS} to V_{DD}	V
Power dissipation	P_D	TC75W51FU	250	mW
		TC75W51FK	200	
Operating temperature	T_{opr}		-40 to 85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to 125	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

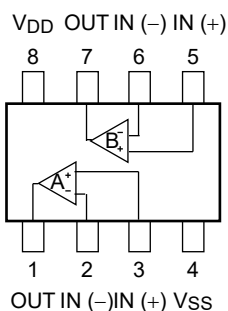
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Start of commercial production
1994-01

4. Marking (Top View)



5. Pin Connection (Top View)



6. Electrical Characteristics

6.1 DC Characteristics (Note) (V_{DD} = 3.0 V, V_{SS} = GND, T_a = 25 °C)

Characteristics	Symbol	TEST Circuit	TEST Condition	Min	typ.	Max	Unit
Input offset voltage	V _{IO}	1	R _S = 1 kΩ, R _F = 100 kΩ	—	2	10	mV
Input offset current	I _{IO}	—	—	—	1	—	pA
Input bias current	I _I	—	—	—	1	—	pA
Common mode input voltage	CMV _{IN}	2	R _S = 1 kΩ, R _F = 100 kΩ	0	—	2.5	V
Voltage gain (Open Loop)	G _V	—	—	60	70	—	dB
Maximum output Voltage	V _{OH}	3	R _L ≥ 100 kΩ	2.9	—	—	V
	V _{OL}	4	R _L ≥ 100 kΩ	—	—	0.1	
Common mode input signal rejection ratio	CMRR	2	V _{IN} = 0 to 2.5 V	55	65	—	dB
Supply voltage rejection ratio	SVRR	1	V _{DD} = 1.5 to 7.0 V	60	70	—	dB
Supply current	I _{DD}	5	—	—	120	400	μA

Note: This device should be operated at less than 70 μA source current.

6.2 DC Characteristics (Note) (V_{DD} = 1.5 V, V_{SS} = GND, T_a = 25 °C)

Characteristics	Symbol	TEST Circuit	TEST Condition	Min	typ.	Max	Unit
Input offset voltage	V _{IO}	1	R _S = 10 kΩ, R _F = 100 kΩ	—	2	10	mV
Input offset current	I _{IO}	—	—	—	1	—	pA
Input bias current	I _I	—	—	—	1	—	pA
Common mode input voltage	CMV _{IN}	2	R _S = 10 kΩ, R _F = 100 kΩ	0	—	1.0	V
Voltage gain (Open loop)	G _V	—	—	60	70	—	dB
Maximum output voltage	V _{OH}	3	R _L ≥ 100 kΩ	1.4	—	—	V
	V _{OL}	4	R _L ≥ 100 kΩ	—	—	0.1	
Supply current	I _{DD}	5	—	—	100	300	μA

Note: This device should be operated at less than 70 μA source current.

6.3 AC Characteristics ($V_{DD} = 3.0\text{ V}$, $V_{SS} = \text{GND}$, $T_a = 25\text{ }^{\circ}\text{C}$)

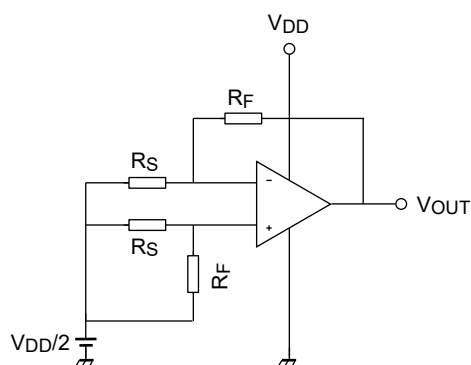
Characteristics	Symbol	TEST Circuit	TEST Condition	Min	typ.	Max	Unit
Slew rate	SR	—	$A_V = 0\text{ dB}$	—	0.5	—	$\text{V}/\mu\text{s}$
Unity gain cross frequency	f_T	—	$A_V = 40\text{ dB}$	—	0.6	—	MHz

6.4 AC Characteristics ($V_{DD} = 1.5\text{ V}$, $V_{SS} = \text{GND}$, $T_a = 25\text{ }^{\circ}\text{C}$)

Characteristics	Symbol	TEST Circuit	TEST Condition	Min	typ.	Max	Unit
Slew rate	SR	—	$A_V = 0\text{ dB}$	—	0.3	—	$\text{V}/\mu\text{s}$
Unity gain cross frequency	f_T	—	$A_V = 40\text{ dB}$	—	0.5	—	MHz

6.5 TEST Circuit

1. SVRR, V_{IO}



- SVRR**
For each of the two V_{DD} values, measure the V_{OUT} value, as indicated below, and calculate the value of SVRR using the equation shown.

When $V_{DD} = 1.5\text{ V}$: $V_{DD} = V_{DD1}$, $V_{OUT} = V_{OUT1}$,

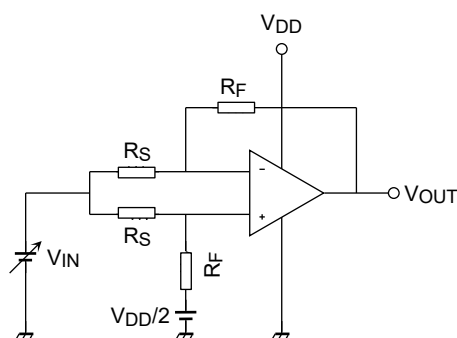
When $V_{DD} = 7.0\text{ V}$: $V_{DD} = V_{DD2}$, $V_{OUT} = V_{OUT2}$

$$SVRR = 20 \log \left(\left| \frac{V_{OUT1} - V_{OUT2}}{V_{DD1} - V_{DD2}} \right| \times \frac{R_S}{R_F + R_S} \right)$$

- V_{IO}**
Measure the value of V_{OUT} and calculate the value of V_{IO} using the following equation.

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2} \right) \times \frac{R_S}{R_F + R_S}$$

2. CMRR, CMV_{IN}



- CMRR**
Measure the V_{DD} value, as indicated below, and calculate the value of the CMRR using the equation shown.

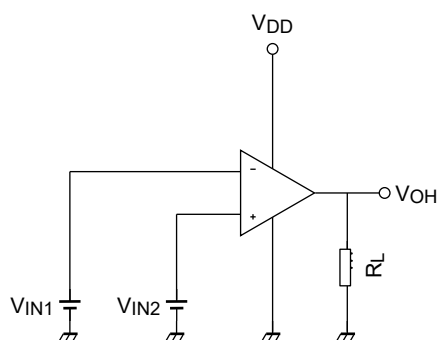
When $V_{IN} = 0\text{ V}$: $V_{IN} = V_{IN1}$, $V_{OUT} = V_{OUT1}$

When $V_{IN} = 2.5\text{ V}$: $V_{IN} = V_{IN2}$, $V_{OUT} = V_{OUT2}$

$$CMRR = 20 \log \left(\left| \frac{V_{OUT1} - V_{OUT2}}{V_{IN1} - V_{IN2}} \right| \times \frac{R_S}{R_F + R_S} \right)$$

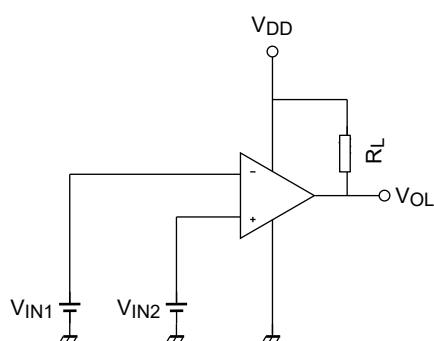
- CMV_{IN}**
Input range within which the CMRR specification guarantees V_{OUT} value (as varied by the V_{IN} value).

3. V_{OH}



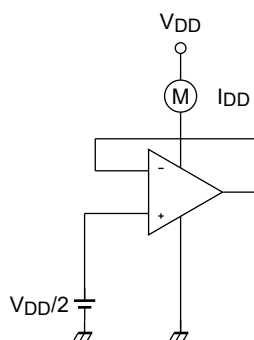
- V_{OH}
TEST Condition $V_{IN1} = \frac{V_{DD}}{2} - 0.05 \text{ V}$
 $V_{IN2} = \frac{V_{DD}}{2} + 0.05 \text{ V}$

4. V_{OL}



- V_{OL}
TEST Condition $V_{IN1} = \frac{V_{DD}}{2} + 0.05 \text{ V}$
 $V_{IN2} = \frac{V_{DD}}{2} - 0.05 \text{ V}$

5. I_{DD}



7. Characteristics Curves (Note)

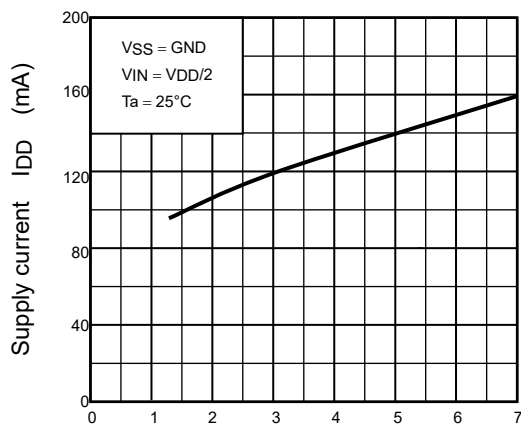


Fig 7.1 $I_{DD} - V_{DD}$

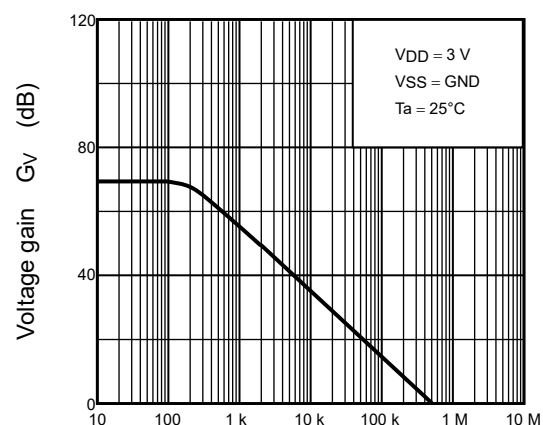


Fig 7.2 $G_v - f$

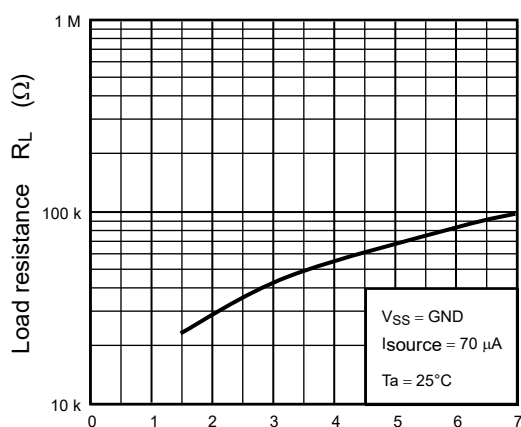


Fig 7.3 $R_L - V_{DD}$

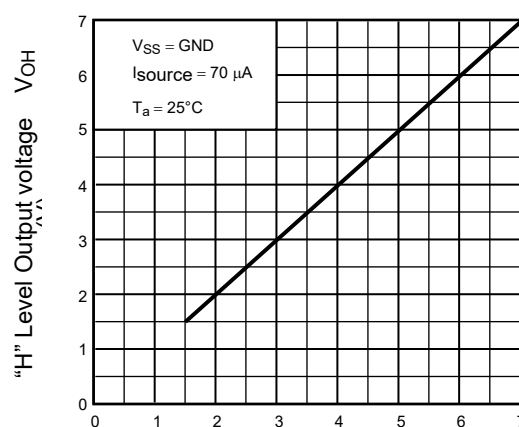


Fig 7.4 $V_{OH} - V_{DD}$

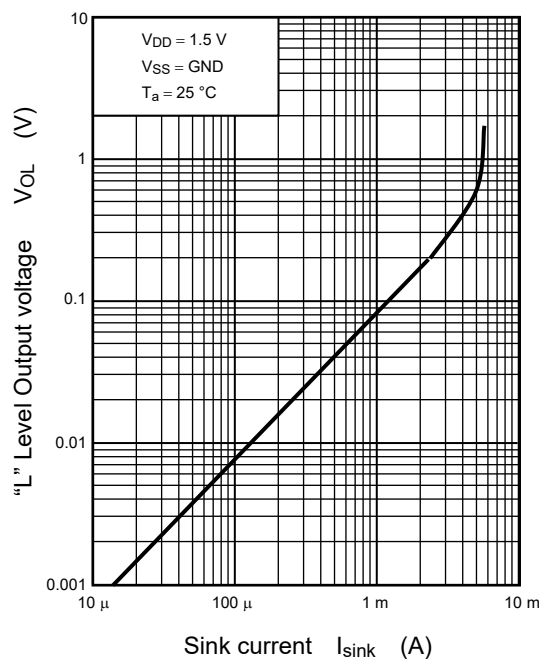


Fig 7.5 $V_{OL} - I_{sink}$

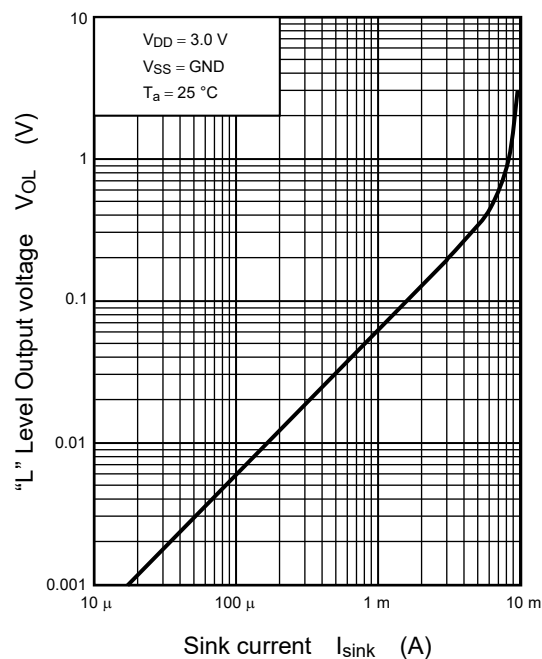


Fig 7.6 $V_{OL} - I_{sink}$

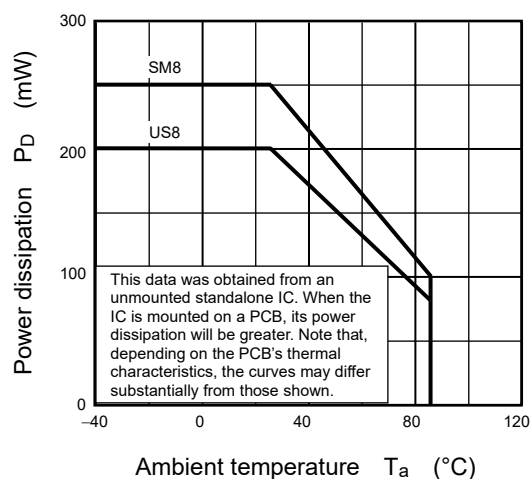


Fig 7.7 $P_D - T_a$

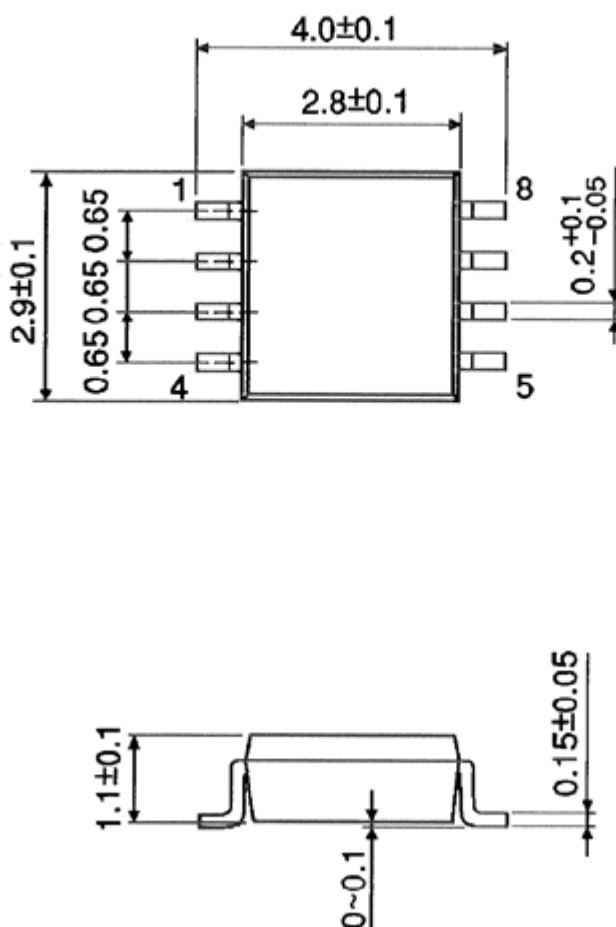
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

8 Package Dimensions

8.1 TC75W51FU

SSOP8-P-0.65

Unit : mm

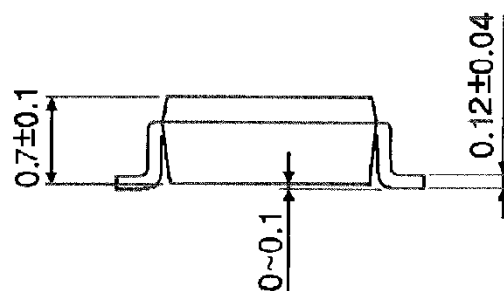
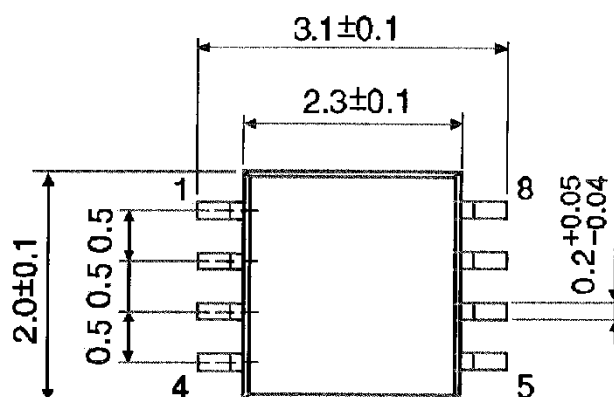


Weight: 0.021 g (typ.)

8.2 TC75W51FK

SSOP8-P-0.50A

Unit : mm



Weight: 0.01 g (typ.)

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