Application Note

TSPI_CONTROLLER_RECEIVE

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Table of Contents

Table of Contents 2
1. Preface 3
2. Technical Term 3
3. Reference Document 3
4. Target Sample Program 4
5. Configuration Diagram 4
6. Sample Program: TSPI_CONTROLLER_RECEIVE 5
6.1. Outlines of Operation 5
6.2. Function to Use 5
6.3. Interrupt to Use 5
6.4. Configuration 6
6.5. Example of Terminal Emulator Output 6
6.6. DMAC Communication Setting 6
7. Activity diagram 7
7.1. main 7
7.2. Interrupt 11
8. Revision History 13
RESTRICTIONS ON PRODUCT USE 14

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1. Preface

This application note describes the sample software TSPI_CONTROLLER_RECEIVE using Serial Peripheral Interface (TSPI).
This document helps the user check operation of a product under development and develop its program.

2. Technical Term

Term/Abbreviation	Definition
BSP	Board Support Package
CG	Clock Control and Operation Mode
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access Controller
Timer	T32A:32-bit Timer Event Counter
TSPI	Serial Peripheral Interface

3. Reference Document

Document	Notes
Data sheet	Refer to the data sheet of MCU to be used.
Reference manual	Refer to the reference manual of each IP to be used.
Application note MCU User Guide	Refer to the MCU user guide to be used.

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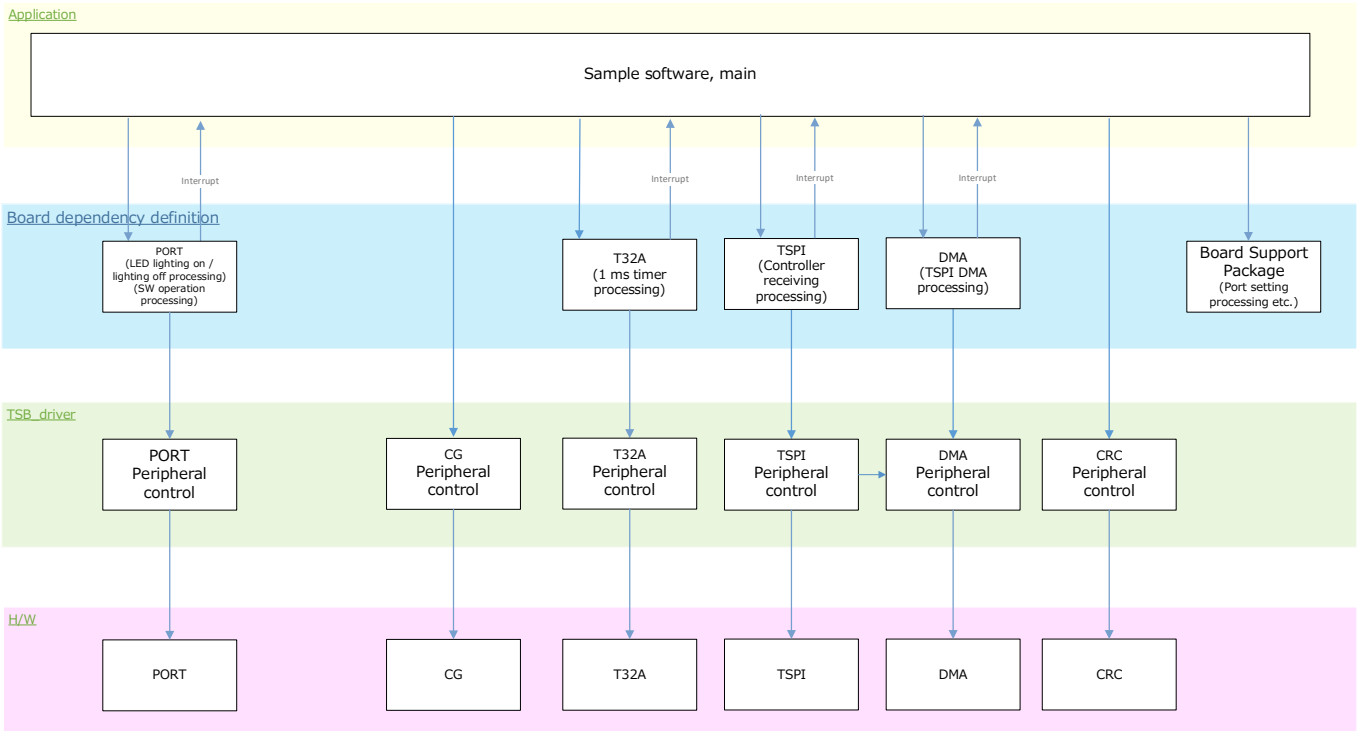
4. Target Sample Program

Sample Program	Outline
TSPI_CONTROLLER_RECEIVE	Sample program of SPI function (Controller Receive)

5. Configuration Diagram



6. Sample Program: TSPI_CONTROLLER_RECEIVE

This sample software that uses the Controller receive processing function of the SPI communication function to enter the reception waiting state when the switch is pressed, and switches the LED turn on / turn off each time data receive is completed.

6.1. Outlines of Operation

Turns off BSP_LED_1, BSP_LED_3, and BSP_LED_4.
When BSP_PSW_1 is pressed, BSP_LED_3 and BSP_LED_4 are turned off and data for the data size is received. Switches the lighting status (turn on / turn off) of BSP_LED_1.
When an SPI read error occurs, BSP_LED_3 is turn on.
When CRC does not match, BSP_LED_4 is turn on.

6.2. Function to Use

The functions to use are as follows:
For the Port assignment of each BSP channel, refer to the MCU user guide.

IP	Channel	Objective
TSPI	BSP_TSPI_1	SPI Communication
T32A	BSP_T32A_TIMER_1	Interval timer
PORT (Push-Switch)	BSP_PSW_1	Event Trigger
PORT (LED)	BSP_LED_1	For operation check
	BSP_LED_3	For operation check
	BSP_LED_4	For operation check

6.3. Interrupt to Use

For details, please refer to the “Interrupt List by Sample” in the MCU User’s Manual.

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6.4. Configuration

Configuration setting.

Configuration	Soft Definition Name	Current Value (Defaults)	Description
DATA_LENGTH	BSP_DATA_LENGTH	12	Data size (unit: byte) Compilation switch (Note1): Be switched by the BSP_CHK_CODE setting.
Check CODE	BSP_CHK_CODE	BSP_CHK_CODE_ CRC16	BSP_CHK_CODE_CRC16 and BSP_CHK_CODE_CRC32 can be switched
Communication Control	BSP_REQUEST_MODE	BSP_FIFO_MODE	BSP_FIFO_MODE and BSP_DMA_MODE can be switched.
Receive Fill Level Setting	BSP_RX_FILL_LEVEL	4	Set to RIL of TSPIxCR2

Note1: When BSP_CHK_CODE_CRC16, 12byte.
When BSP_CHK_CODE_CRC32, 14byte.

6.5. Example of Terminal Emulator Output

Nothing.

6.6. DMAC Communication Setting

Startup Factors and Transfer Mode

Configuration	Description
Startup Factors	DMA Request from TSPI Driver (Request Based on FIFO level)
Transfer Mode	Singel Transfer/Unit Normal Transfer

Channel Control Data: Transfer Mode Setting [DMAChnlCfg]

Configuration	Description
Destination Address Increment	00: [1byte]
Destination Data Size	00: [1byte]
Source Address Increment	11: [No increment]
Source Data Size	00: [1byte]
Arbitration	0000: [After 1 Rotation Transfer]
Transfer Count	0x00B: [12times (BSP_DATA_LENGTH)]
Singel Transfer Setting	0: [Not used because it is not a chain transfer]
Transfer Mode	001: [Unit Normal Transfer]

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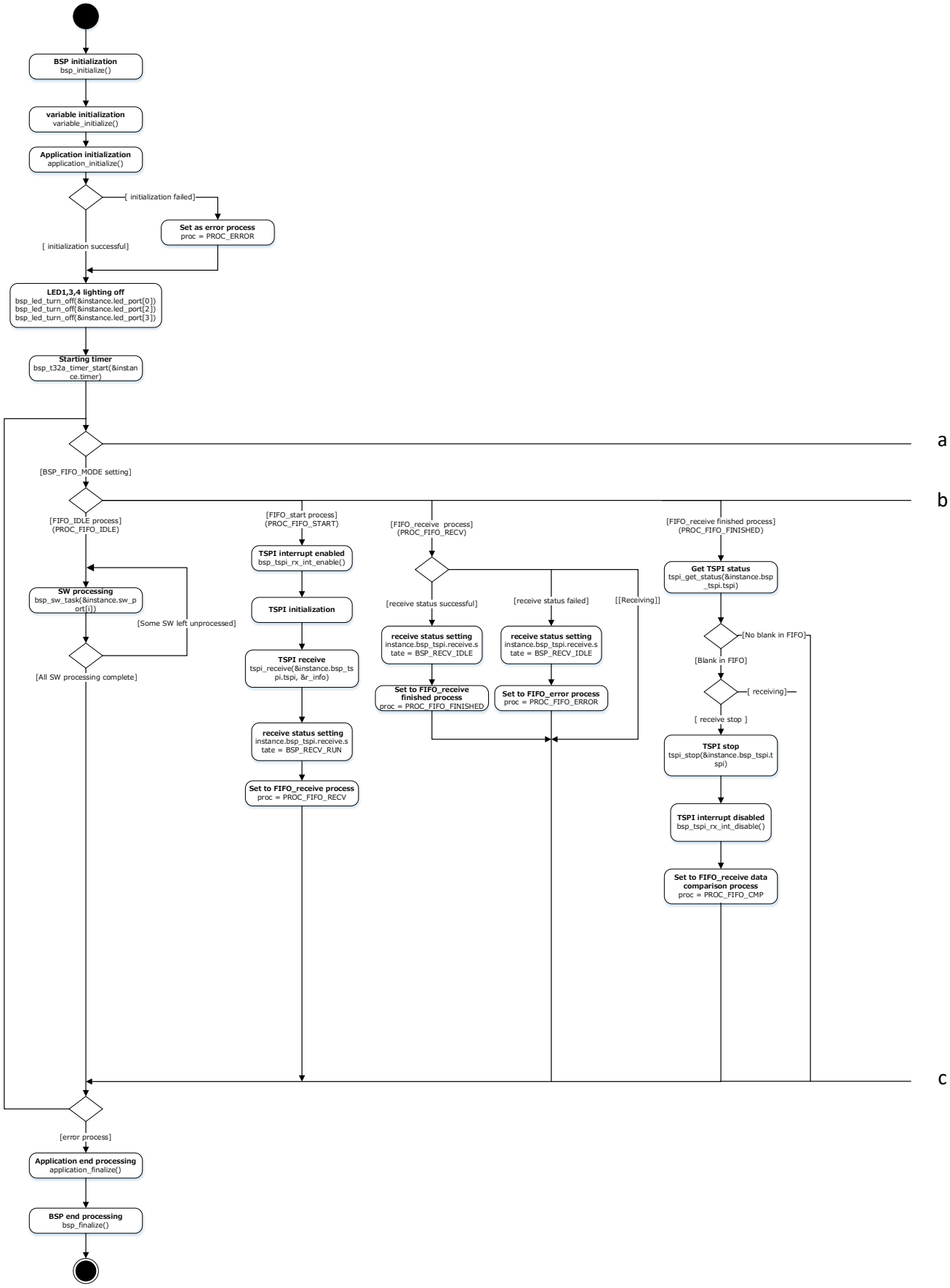
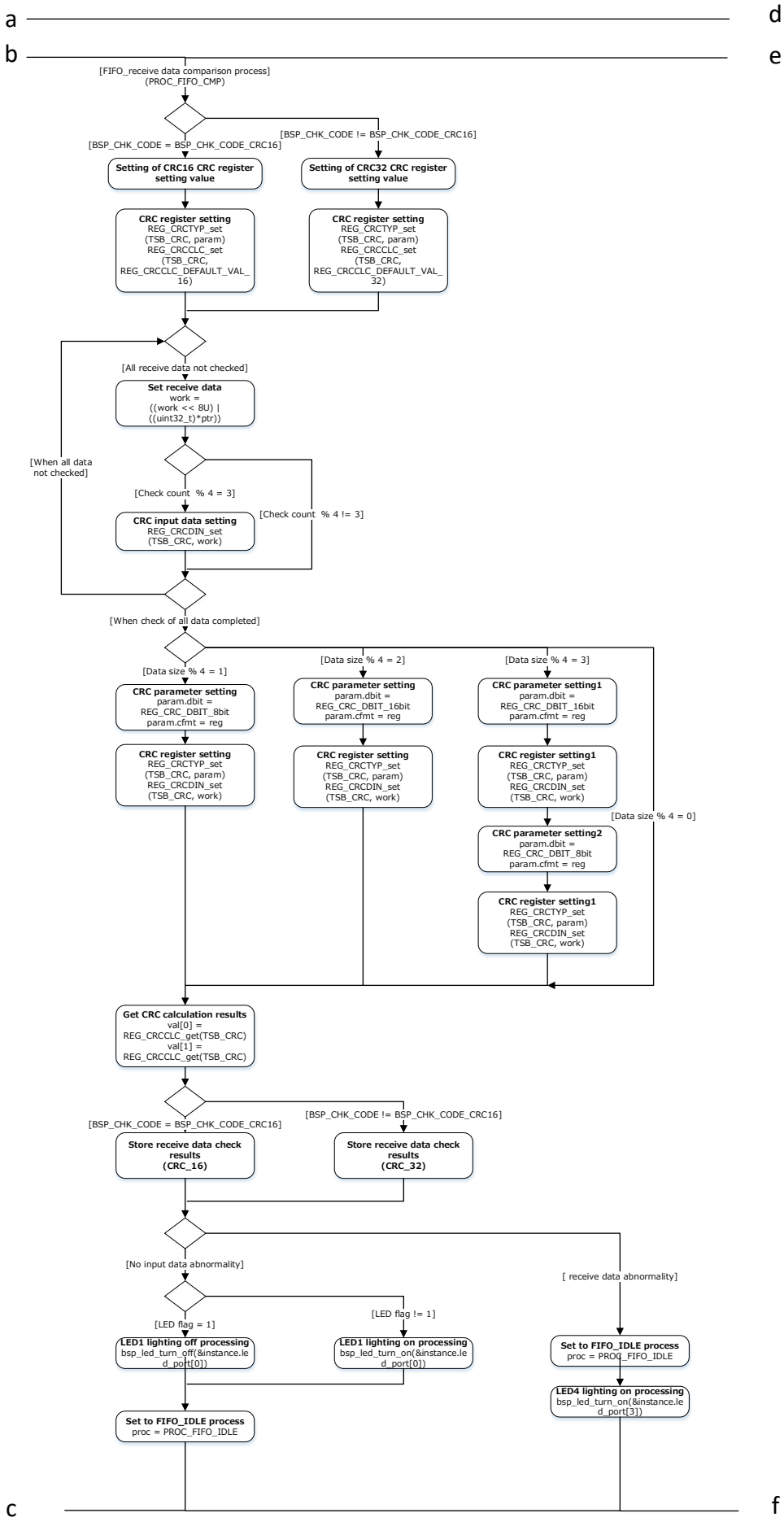
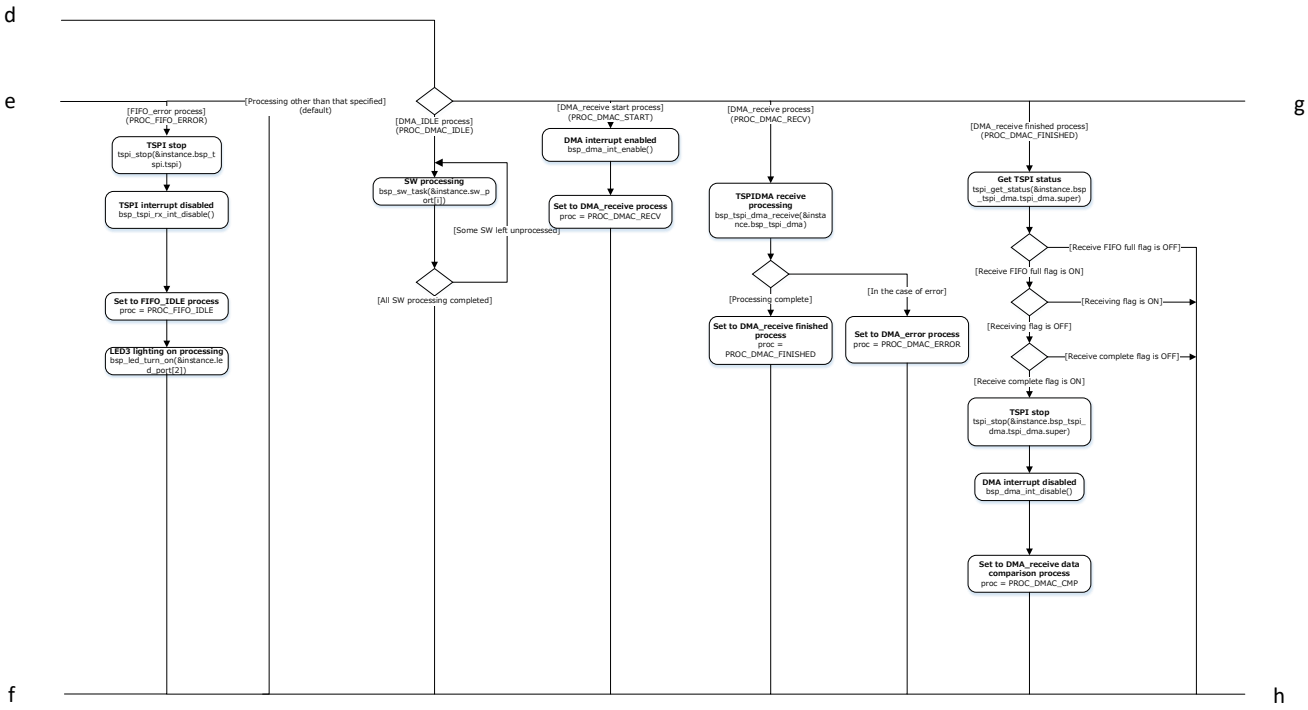
7. Activity diagram

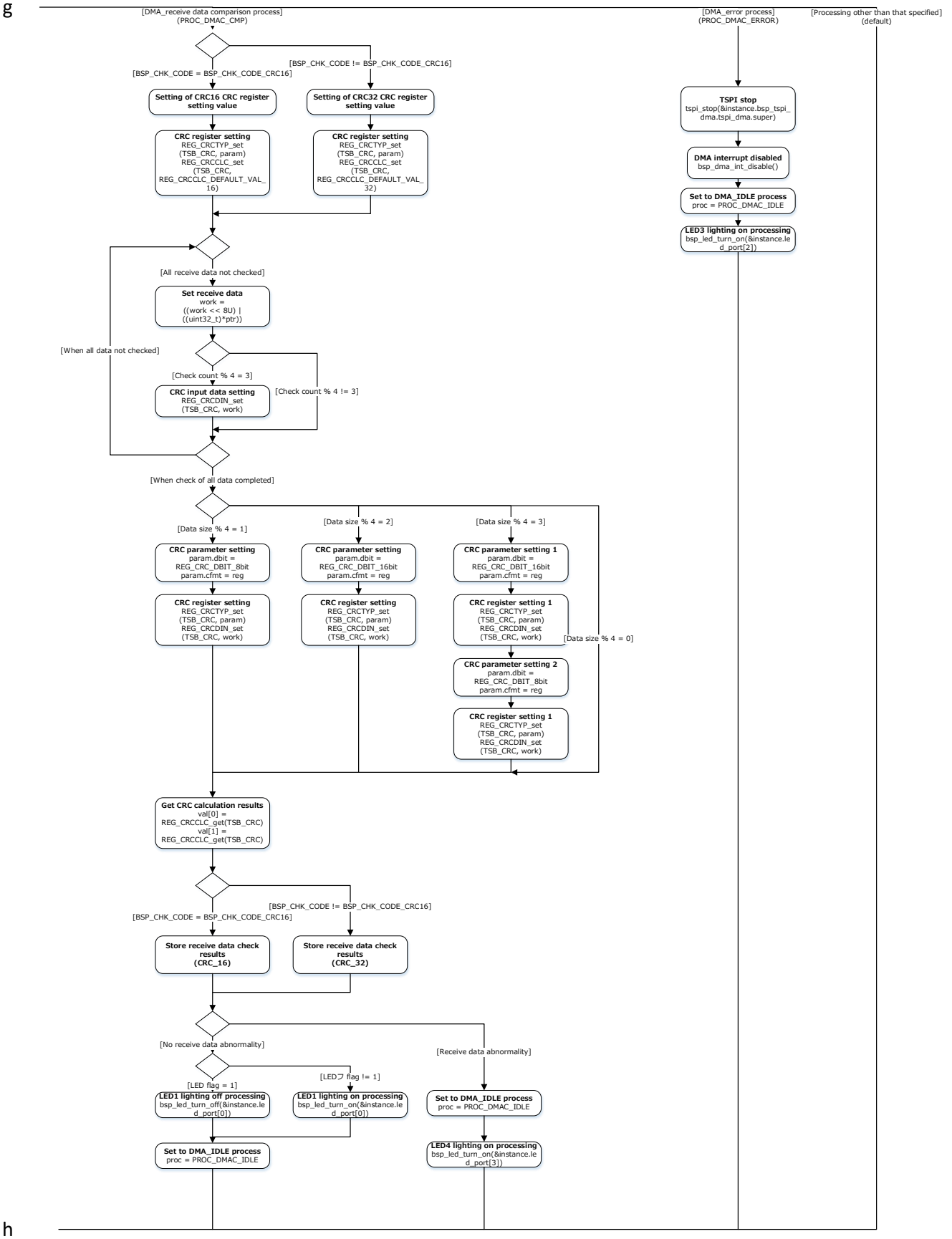
7.1. main




a
d
b
e
[FIFO_receive data comparison process]
(PROC_FIFO_CMP)
[BSP_CHK_CODE = BSP_CHK_CODE_CRC16]
[BSP_CHK_CODE != BSP_CHK_CODE_CRC16]
Setting of CRC16 CRC register setting value
Setting of CRC32 CRC register setting value
CRC register setting
REG_CRCTYP_set
(TSB_CRC, param)
REG_CRCCLC_set
(TSB_CRC,
REG_CRCCLC_DEFAULT_VAL_16)
CRC register setting
REG_CRCTYP_set
(TSB_CRC, param)
REG_CRCCLC_set
(TSB_CRC,
REG_CRCCLC_DEFAULT_VAL_32)
[All receive data not checked]
Set receive data
work =
((work << 8U) |
((uint32_t)*ptr))
[When all data not checked]
[Check count % 4 = 3]
[Check count % 4 != 3]
CRC input data setting
REG_CRCDIN_set
(TSB_CRC, work)
[When check of all data completed]
[Data size % 4 = 1]
[Data size % 4 = 2]
[Data size % 4 = 3]
[Data size % 4 = 0]
CRC parameter setting
param.dbit =
REG_CRC_DBIT_8bit
param.cfmt = reg
CRC parameter setting
param.dbit =
REG_CRC_DBIT_16bit
param.cfmt = reg
CRC parameter setting1
param.dbit =
REG_CRC_DBIT_16bit
param.cfmt = reg
CRC register setting
REG_CRCTYP_set
(TSB_CRC, param)
REG_CRCDIN_set
(TSB_CRC, work)
CRC register setting
REG_CRCTYP_set
(TSB_CRC, param)
REG_CRCDIN_set
(TSB_CRC, work)
CRC register setting1
REG_CRCTYP_set
(TSB_CRC, param)
REG_CRCDIN_set
(TSB_CRC, work)
CRC parameter setting2
param.dbit =
REG_CRC_DBIT_8bit
param.cfmt = reg
CRC register setting1
REG_CRCTYP_set
(TSB_CRC, param)
REG_CRCDIN_set
(TSB_CRC, work)
Get CRC calculation results
val[0] =
REG_CRCCLC_get(TSB_CRC)
val[1] =
REG_CRCCLC_get(TSB_CRC)
[BSP_CHK_CODE = BSP_CHK_CODE_CRC16]
[BSP_CHK_CODE != BSP_CHK_CODE_CRC16]
Store receive data check results
(CRC_16)
Store receive data check results
(CRC_32)
[No input data abnormality]
[receive data abnormality]
[LED flag = 1]
[LED flag != 1]
LED1 lighting off processing
bsp_led_turn_off(&instance.led_port[0])
LED1 lighting on processing
bsp_led_turn_on(&instance.led_port[0])
Set to FIFO_IDLE process
proc = PROC_FIFO_IDLE
LED4 lighting on processing
bsp_led_turn_on(&instance.led_port[3])
Set to FIFO_IDLE process
proc = PROC_FIFO_IDLE
c
f

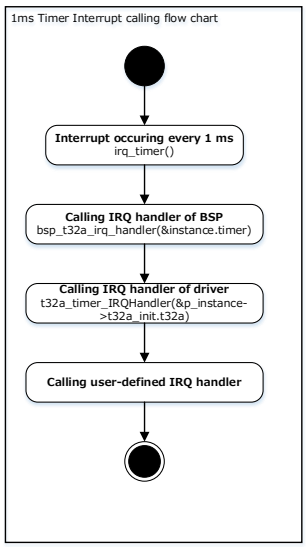

d
e
g
f
h
[FIFO_error process]
(PROC_FIFO_ERROR)
TSPI stop
tspi_stop(&instance.bsp_tspi.tspi)
TSPI interrupt disabled
bsp_tspi_rx_int_disable()
Set to FIFO_IDLE process
proc = PROC_FIFO_IDLE
LED3 lighting on processing
bsp_led_turn_on(&instance.led_port[2])
[Processing other than that specified]
(default)
[DMA_IDLE process]
(PROC_DMAC_IDLE)
SW processing
bsp_sw_task(&instance.sw_port[j])
[Some SW left unprocessed]
[All SW processing completed]
[DMA_receive start process]
(PROC_DMAC_START)
DMA interrupt enabled
bsp_dma_int_enable()
Set to DMA_receive process
proc = PROC_DMAC_RECV
[DMA_receive process]
(PROC_DMAC_RECV)
TSPIDMA receive processing
bsp_tspi_dma_receive(&instance.bsp_tspi_dma)
[Processing complete]
[In the case of error]
Set to DMA_receive finished process
proc = PROC_DMAC_FINISHED
Set to DMA_error process
proc = PROC_DMAC_ERROR
[DMA_receive finished process]
(PROC_DMAC_FINISHED)
Get TSPI status
tspi_get_status(&instance.bsp_tspi_dma.tspi_dma.super)
[Receive FIFO full flag is OFF]
[Receive FIFO full flag is ON]
[Receiving flag is ON]
[Receiving flag is OFF]
[Receive complete flag is OFF]
[Receive complete flag is ON]
TSPI stop
tspi_stop(&instance.bsp_tspi_dma.tspi_dma.super)
DMA interrupt disabled
bsp_dma_int_disable()
Set to DMA_receive data comparison process
proc = PROC_DMAC_CMP

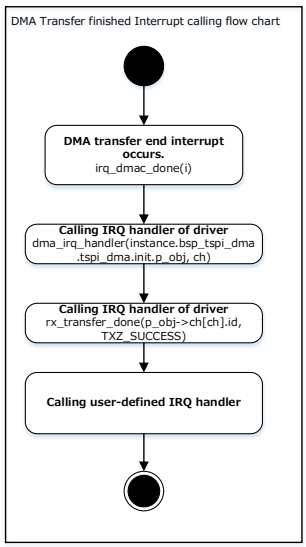
g

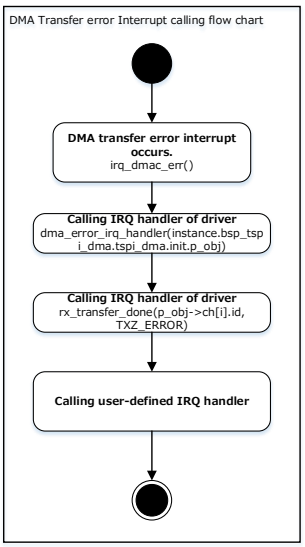

[DMA_receive data comparison process]
(PROC_DMAC_CMP)
[BSP_CHK_CODE = BSP_CHK_CODE_CRC16]
[BSP_CHK_CODE != BSP_CHK_CODE_CRC16]
Setting of CRC16 CRC register setting value
Setting of CRC32 CRC register setting value
CRC register setting
REG_CRCTYP_set
(TSB_CRC, param)
REG_CRCCLC_set
(TSB_CRC,
REG_CRCCLC_DEFAULT_VAL_16)
CRC register setting
REG_CRCTYP_set
(TSB_CRC, param)
REG_CRCCLC_set
(TSB_CRC,
REG_CRCCLC_DEFAULT_VAL_32)
[All receive data not checked]
Set receive data
work =
((work << 8U) |
((uint32_t)*ptr))
[When all data not checked]
[Check count % 4 = 3]
[Check count % 4 != 3]
CRC input data setting
REG_CRCDIN_set
(TSB_CRC, work)
[When check of all data completed]
[Data size % 4 = 1]
[Data size % 4 = 2]
[Data size % 4 = 3]
[Data size % 4 = 0]
CRC parameter setting
param.dbit =
REG_CRC_DBIT_8bit
param.cfmt = reg
CRC parameter setting
param.dbit =
REG_CRC_DBIT_16bit
param.cfmt = reg
CRC parameter setting 1
param.dbit =
REG_CRC_DBIT_16bit
param.cfmt = reg
CRC register setting
REG_CRCTYP_set
(TSB_CRC, param)
REG_CRCDIN_set
(TSB_CRC, work)
CRC register setting
REG_CRCTYP_set
(TSB_CRC, param)
REG_CRCDIN_set
(TSB_CRC, work)
CRC register setting 1
REG_CRCTYP_set
(TSB_CRC, param)
REG_CRCDIN_set
(TSB_CRC, work)
CRC parameter setting 2
param.dbit =
REG_CRC_DBIT_8bit
param.cfmt = reg
CRC register setting 1
REG_CRCTYP_set
(TSB_CRC, param)
REG_CRCDIN_set
(TSB_CRC, work)
Get CRC calculation results
val[0] =
REG_CRCCLC_get(TSB_CRC)
val[1] =
REG_CRCCLC_get(TSB_CRC)
[BSP_CHK_CODE = BSP_CHK_CODE_CRC16]
[BSP_CHK_CODE != BSP_CHK_CODE_CRC16]
Store receive data check results
(CRC_16)
Store receive data check results
(CRC_32)
[No receive data abnormality]
[Receive data abnormality]
[LED flag = 1]
[LED flag != 1]
LED1 lighting off processing
bsp_led_turn_off(&instance.led_port[0])
LED1 lighting on processing
bsp_led_turn_on(&instance.led_port[0])
Set to DMA_IDLE process
proc = PROC_DMAC_IDLE
Set to DMA_IDLE process
proc = PROC_DMAC_IDLE
LED4 lighting on processing
bsp_led_turn_on(&instance.led_port[3])
[DMA_error process]
(PROC_DMAC_ERROR)
[Processing other than that specified]
(default)
TSPI stop
tspi_stop(&instance.bsp_tspi_dma.tspi_dma.super)
DMA interrupt disabled
bsp_dma_int_disable()
Set to DMA_IDLE process
proc = PROC_DMAC_IDLE
LED3 lighting on processing
bsp_led_turn_on(&instance.led_port[2])

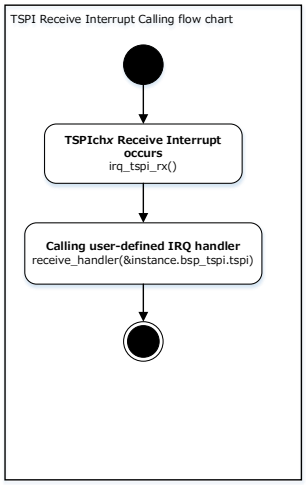
h

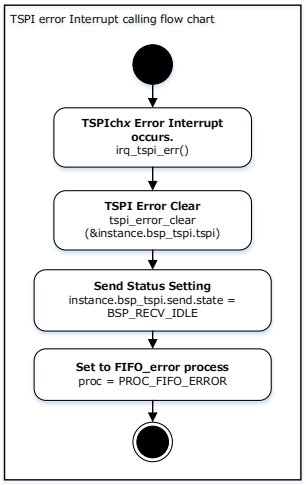
7.2. Interrupt

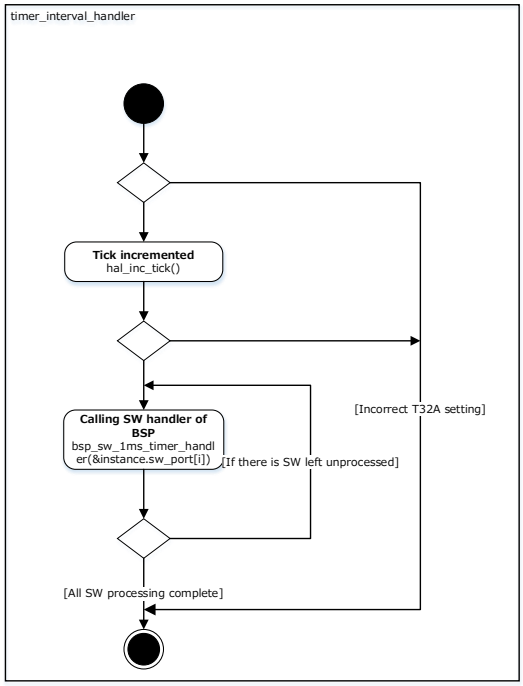




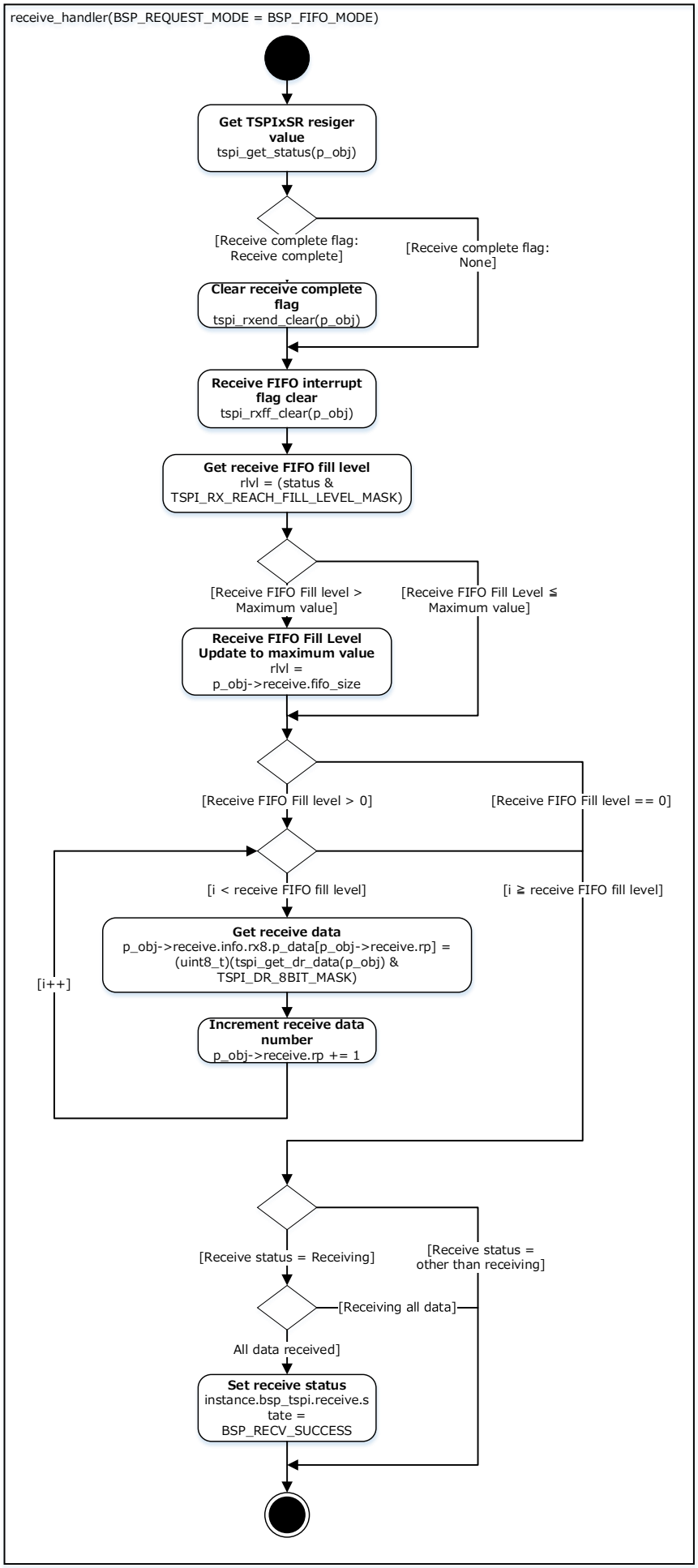








For x detail, please refer to the “Activity Diagram Symbol” in the MCU User’s Manual


receive_handler(BSP_REQUEST_MODE = BSP_FIFO_MODE)
Get TSPIxSR resiger value
tspi_get_status(p_obj)
[Receive complete flag: Receive complete]
[Receive complete flag: None]
Clear receive complete flag
tspi_rxend_clear(p_obj)
Receive FIFO interrupt flag clear
tspi_rxff_clear(p_obj)
Get receive FIFO fill level
rlvl = (status & TSPI_RX_REACH_FILL_LEVEL_MASK)
[Receive FIFO Fill level > Maximum value]
[Receive FIFO Fill Level ≦ Maximum value]
Receive FIFO Fill Level Update to maximum value
rlvl = p_obj->receive.fifo_size
[Receive FIFO Fill level > 0]
[Receive FIFO Fill level == 0]
[i < receive FIFO fill level]
[i ≧ receive FIFO fill level]
Get receive data
p_obj->receive.info.rx8.p_data[p_obj->receive.rp] = (uint8_t)(tspi_get_dr_data(p_obj) & TSPI_DR_8BIT_MASK)
[i++]
Increment receive data number
p_obj->receive.rp += 1
[Receive status = Receiving]
[Receive status = other than receiving]
[Receiving all data]
All data received]
Set receive status
instance.bsp_tspi.receive.state = BSP_RECV_SUCCESS

8. Revision History

Revision	Date	Description
1.0	2025-01-20	First release
1.1	2025-10-30	6.3 Interrupt to Use Added M3H Interrupt Name.
1.2	2026-07-30	6.3 Interrupt to Use Detailed information is transcribed into the User's Manual

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