For high-speed differential interface 64GT/s Mux/De-Mux bus switch TDS5B212MX, TDS5C212MX Application Note

Overview

This document describes the guidelines and precautions for using Mux (multiplexer) /De-Mux (demultiplexer) bus switch TDS5B212MX, TDS5C212MX for high-speed differential interfaces. Recommended transfer rates can be used for interfaces such as 1 to 64GT/s, PCIe® 6.0, PCIe® 5.0, CXL 3.0, USB4® Version2, Thunderbolt™5 and DisplayPort™ 2.0.

Table of Contents

Contents

List of Figures

List of Tables

1. Introduction

In recent years, PCIe, USB, Thunderbolt and other high-speed communication interfaces have been widely adopted in PCs, servers, and other electronic devices, and these interfaces have been used to connect and expand CPU, peripheral chips, graphics boards, peripheral devices, and servers, testers and other applications.

However, if the frequency increases as the communication speed increases, the signal loss on the transmission path tends to occur. This loss occurs even when the signal passes through the board wiring, and it is necessary to design the circuit design to reduce the loss.

Therefore, Mux/De-Mux used when expanding the differential interface also requires high-frequency and low-loss products. We have recently developed a high-frequency, low-loss 2:1 Mux/1:2 De-Mux bus-switch TDS5B212MX, TDS5C212MX that can be used in PCIe 6, PCIe 5, USB4, Thunderbolt 5 and other applications.

This document explains applications using TDS5B212MX, TDS5C212MX and precautions for designing the circuit board.

2. General

This chapter describes the basic specifications, pin configuration, and functions of the TDS5B212MX and TDS5C212MX.

It outlines the common features of both products as well as the differences in their pin assignments, providing the basic information required to choose the appropriate device when considering system configuration and board layout.

In addition, this chapter explains the differences between these products, which are passive switches, and active switches such as redrivers and retimers.

2.1. Overview

The TDS5B212MX and TDS5C212MX are high-speed differential 2:1 Mux / 1:2 De-Mux bus switches. Each device handles two differential channels, switching one lane of TX/RX differential signals. Both products share the same functional and electrical specifications, differing only in pinout and high-frequency performance.

These products achieve excellent high-frequency performance by adopting Toshiba's proprietary SOI process, "TaRF SOI™". The -3 dB bandwidth reaches 29 GHz for the TDS5B212MX and 34 GHz for the TDS5C212MX, providing low-loss and wideband differential insertion loss characteristics.

Combined with these excellent high-frequency characteristics and wide electrical operating range, the devices support many high-speed data protocols. The recommended transfer rate is 1 to 64 GT/s, including PCIe 6.0.

- PCIe® Series : PCIe 6.0 / 5.0 / 4.0 / 3.0
- CXL™ Series : CXL 3.0 / 2.0 / 1.0
- USB Series : USB4 Ver.2 / USB4 / USB3.2 Gen2×1 / Gen1×1
- Thunderbolt™ Series : Thunderbolt 5 / 4 / 3 / 2
- DisplayPort™ Series : DisplayPort 2.0 / 1.4 / 1.3 / 1.2

The compact XQFN16 package (1.6 × 2.4 mm) also helps reduce PCB footprint.

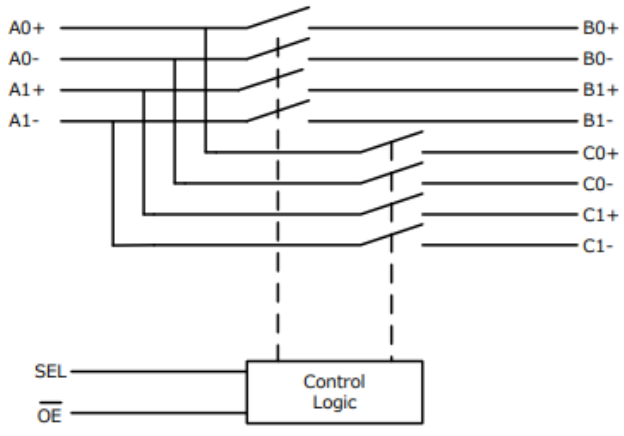


Fig. 1 Block Diagram

(Common in TDS5B212MX, TDS5C212MX)

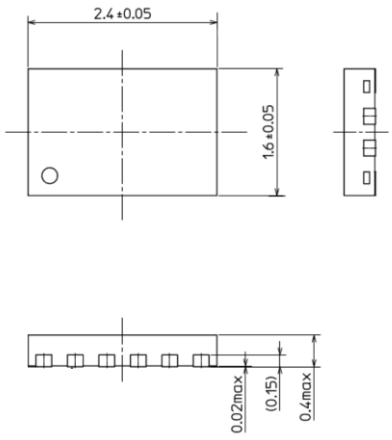


Fig. 2 Packaging Dimensions (unit:mm)

(Common in TDS5B212MX, TDS5C212MX)

2.2. Pin Layout

TDS5B212MX and TDS5C212MX have the same function but different terminal arrangements.

The TDS5B212MX adopts the same pin assignment as the TDS4B212MX, a Mux/De-Mux designed for 32 Gbps data rate.

TDS5C212MX achieves a wider bandwidth than the TDS5B212MX through a pin assignment optimized for high-frequency performance.

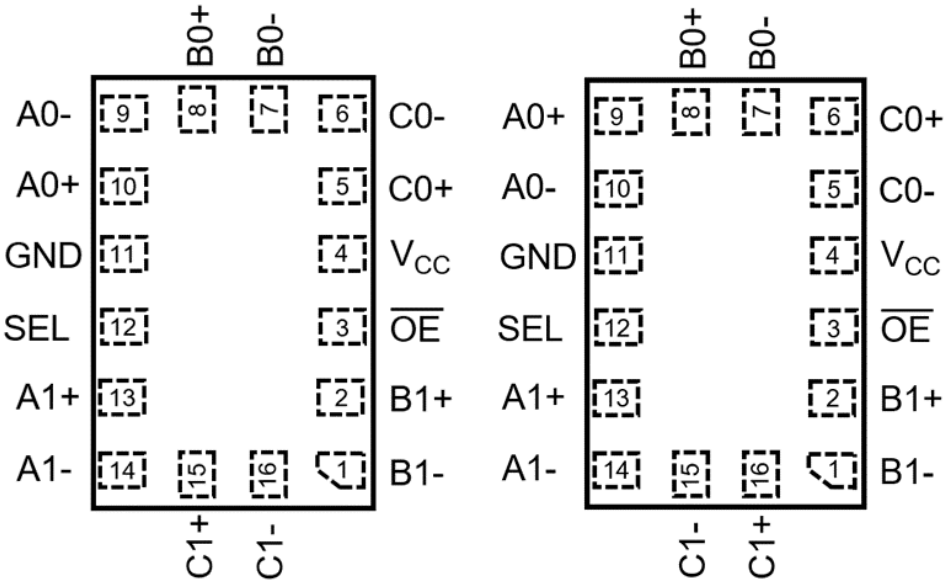


Fig. 3 Pinout Diagram (Top View) Left: TDS5B212MX Right: TDS5C212MX

Fig. 4 illustrates the use of TDS5B212MX and TDS5C212MX to switch the connection of System A between Systems B and C.

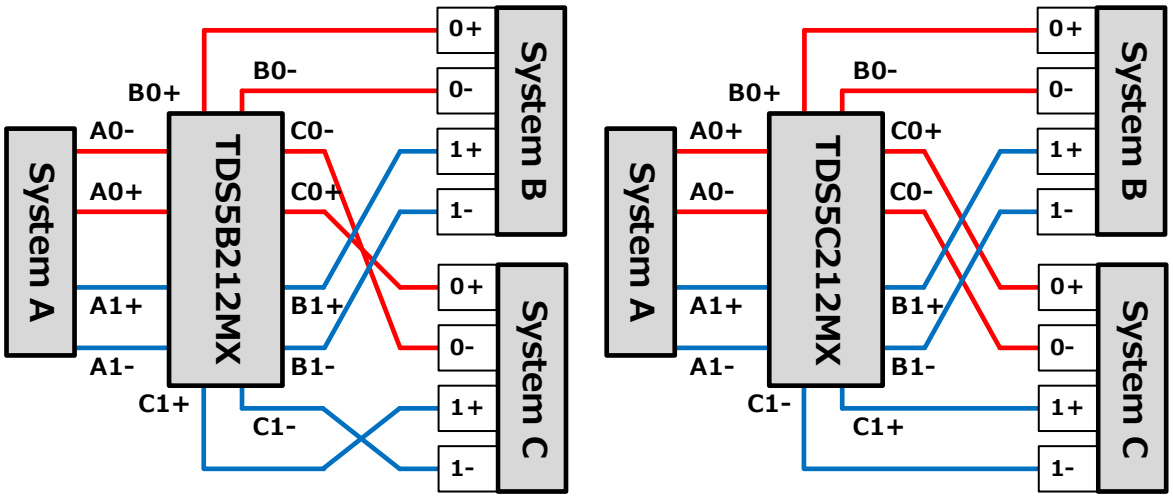


Fig. 4 Typical Wiring of TDS5B212MX, TDS5C212MX

2.3. Functions

TDS5B212MX and TDS5C212MX can be combined with a SEL to select either port B or port C as the A port connection destination, and to transmit differential signals bidirectionally between the connected ports.

Setting $\overline{OE}$ to the low level (L), the unit enters the active mode. By setting SEL to the low level (L), ports A and B are connected. By setting SEL to the high level (H), ports A and C are connected.

Setting $\overline{OE}$ to the high level (H), the unit enters the standby mode. All ports are disconnected irrespective of SEL.

Table 1 Port Connections and Control Input Logic (n = 0, 1)

Input$\overline{OE}$	Input SEL	Function (n = 0, 1)
L	L	An+ Port = Bn+ Port, An- Port = Bn- Port
L	H	An+ Port = Cn+ Port, An- Port = Cn- Port
H	Don't care	An, Bn and Cn Port Disconnect

2.4. Differences from Active Switches (Redrivers, Retimers)

Switches for high-speed differential interfaces are broadly classified into two types: active switches and passive switches.

Redrivers and retimers are categorized as active switches. They receive the signal internally, reshape and amplify it to compensate for insertion loss and jitter, and then retransmit it. This improves signal quality but introduces response delay (latency) and power consumption due to internal processing. Redrivers and retimers with built-in Mux/De-Mux functions also fall under this category.

The TDS5B212MX and TDS5C212MX, in contrast, are passive switches: they electrically connect and switch differential signals without compensation or regeneration. Since signals pass through the device without reshaping, path switching is achieved with minimal latency. Their transparent structure—independent of protocol or physical layer (signals pass through as-is, regardless of standard or condition)—also supports switching between different high-speed differential interfaces such as PCIe and USB, enabling flexible Mux/De-Mux implementation in diverse systems.

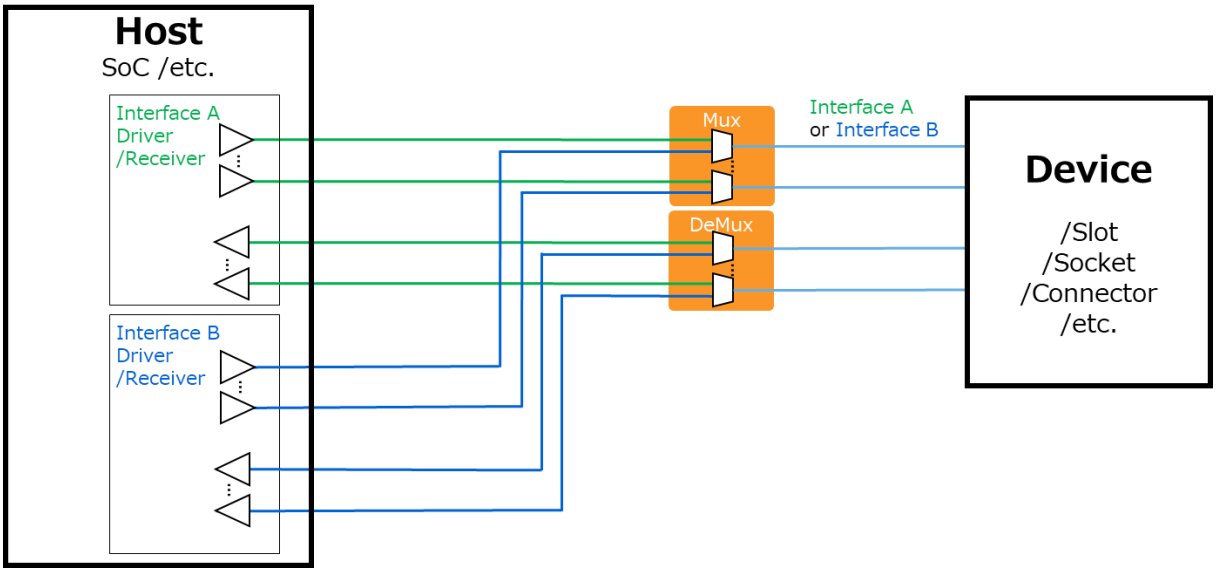


Fig. 5 Example of switching between two interfaces using a passive switch

In addition, this product features very low current consumption.

It is also suitable for short-distance Mux/De-Mux applications where redrivers or retimers are not required.

In summary, while active switches aim to correct signal quality, passive switches are suited for systems where signal quality is already ensured, providing a simple means of path selection.

3. High-frequency characteristics and eye patterns

High-frequency characteristics and eye patterns are critical parameters for high-speed differential signal bus switches. This chapter presents the evaluation results of high-frequency characteristics and eye patterns for the TDS5B212MX and TDS5C212MX.

3.1. Evaluation board used for measurement

High-frequency characteristics and eye pattern evaluations were performed using evaluation boards on which the TDS5B212MX and TDS5C212MX were respectively mounted. Signal loss in high-speed transmission occurs both along the transmission lines on the board and when passing through the TDS5B212MX or TDS5C212MX. Therefore, de-embedding was applied to the evaluation data obtained from the product-mounted evaluation board to subtract the loss components attributed to the transmission lines, thereby extracting the standalone device characteristics.

For eye patterns, to confirm the impact of the standalone device characteristics on the differential signal, de-embedding was also applied to the evaluation data of a through board, and the resulting eye pattern data is presented as the "through board" reference.

The evaluation board is fabricated using MEGTRON6 material. 1.95 mm connectors (V connectors) were used for the connection between the evaluation board and cables. Since the evaluation board is designed to minimize the trace length including the device, measurement is limited to the path between the A0± port and the C0± port.

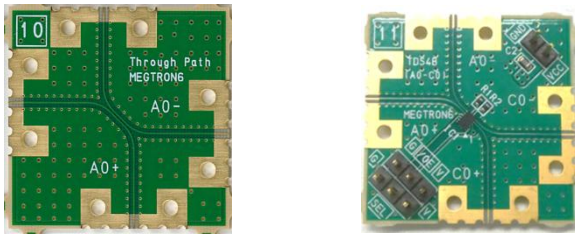


Fig. 6 Evaluation board (Left: Through board, Right: Product-mounted board)

For the cascade connection evaluation results described later, an evaluation board capable of mounting two devices on a single board, as shown in the figure below, was used.

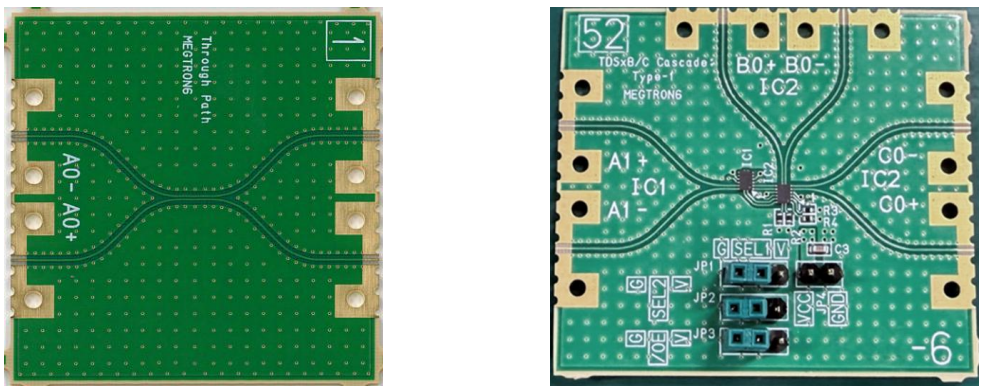


Fig. 7 Cascade evaluation board (Left: Through board, Right: Product-mounted board)

3.2. High-frequency characteristics evaluation results

The −3 dB bandwidth (Typ.) is as high as 29 GHz and 34 GHz, providing low loss even at high frequencies.

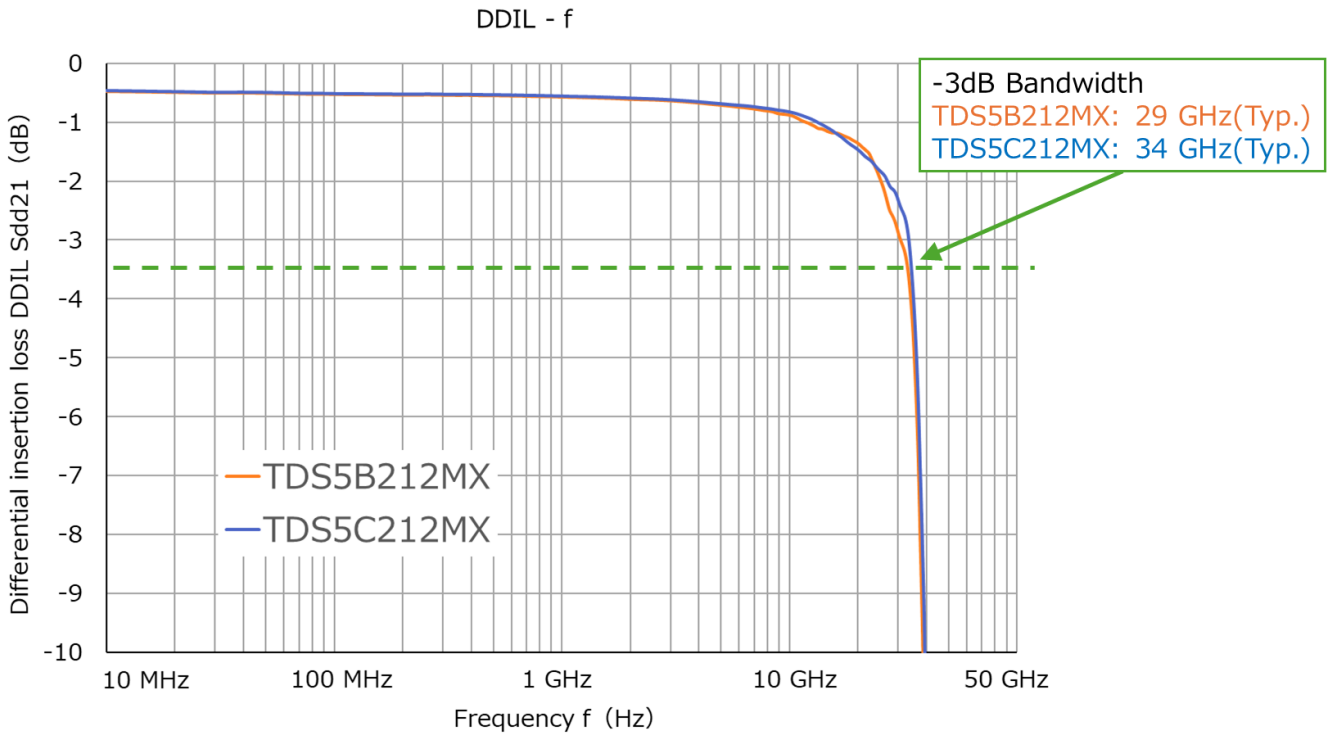


Fig. 8 TDS5B212MX, TDS5C212MX Differential insertion loss - frequency

Table 2 TDS5B212MX, TDS5C212MX -3dB Band width and Differential insertion loss

High-frequency characteristics (Typ.)		TDS5B212MX	TDS5C212MX
−3dB Bandwidth		29 GHz	34 GHz
Differential insertion loss DDIL S_{dd21}	f = 2.5 GHz	-0.6 dB	-0.6 dB
	f = 4.0 GHz	-0.7 dB	-0.7 dB
	f = 5.0 GHz	-0.7 dB	-0.7 dB
	f = 8.0 GHz	-0.8 dB	-0.8 dB
	f = 10.0 GHz	-0.9 dB	-0.9 dB
	f = 12.8 GHz	-1.1 dB	-1.1 dB
	f = 16.0 GHz	-1.2 dB	-1.2 dB

3.3. What is Eye Pattern?

An eye pattern is a method for visually assessing the transmission waveform of a differential signal. It is generated by overlaying signal waveforms for each bit, resulting in an eye-like shape.

Eye patterns are widely used to evaluate signal integrity in the design and testing of semiconductor devices, communication systems, and boards.

An ideal NRZ (Non Return to Zero) eye pattern has a wide opening with short rise and fall times, as shown in Fig. 5. In practice, however, signal attenuation and noise cause the eye opening to narrow and rise/fall times to increase, as shown in Fig. 6. This degradation becomes more pronounced as attenuation and noise increase, making eye patterns an effective indicator of differential signal waveform quality.

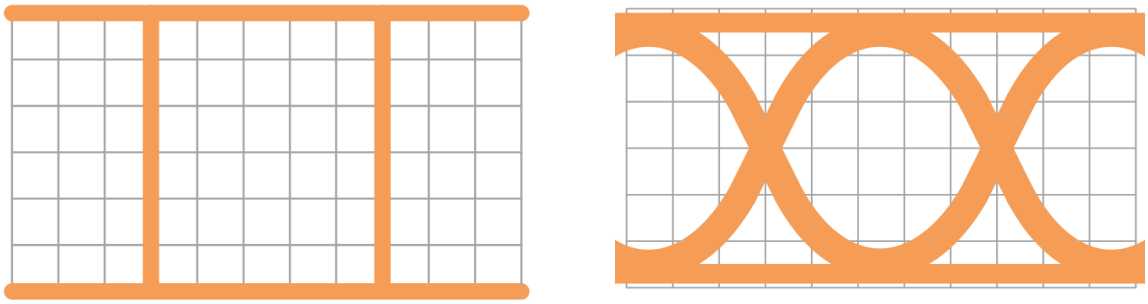


Fig. 9 Left: Ideal eye pattern　　Right: General eye pattern

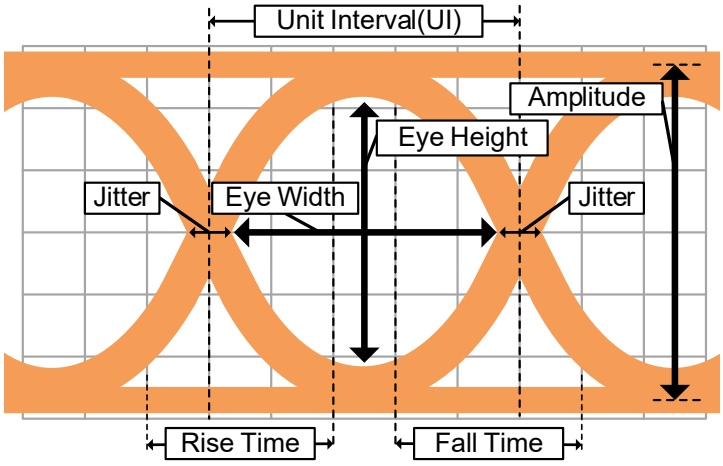


Fig. 10 Typical measured values on the eye pattern

Eye height: Eye Height indicates the vertical opening of the eye. A larger Eye Height represents a better eye pattern.

Eye width: Eye Width indicates the horizontal opening of the eye. A larger Eye Width represents a better eye pattern.

Jitter: Jitter is the time difference between the rising and falling edges at their crossing point, visually appearing as the thickness of the horizontal line at the crossing. A smaller Jitter and TJ (Total Jitter) represent a better eye pattern.

The eye pattern evaluation results for each interface are shown on the following pages.

3.4. PCIe 6.0 eye pattern evaluation results

PCIe 6.0
64GT/s PAM4
1Vp-p(Diff)
PRBS-7

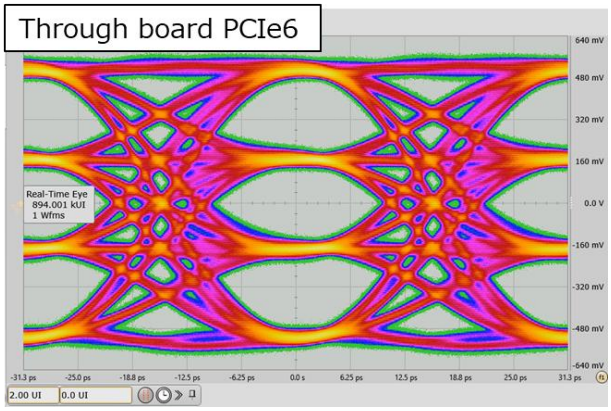


Fig. 11 PCIe 6.0 Through board result

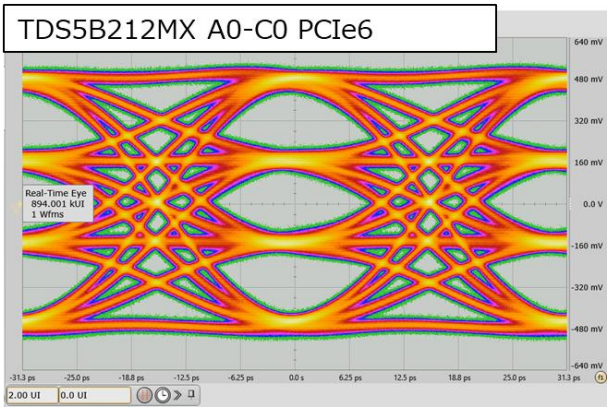


Fig. 12 PCIe 6.0 TDS5B212MX result

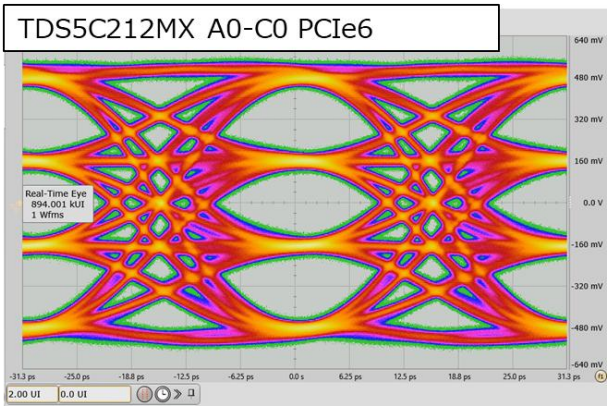


Fig. 13 PCIe 6.0 TDS5C212MX result

Table 3 PCIe 6.0 eye pattern evaluation results

Item	Eye	Eye Height (mV)	ΔEye Height (mV)	Eye Width (ps)	ΔEye Width (ps)	TJ (ps)	ΔTJ (ps)
Through board	Low	231	-	14.36	-	18.94	-
	Middle	243	-	16.99	-	14.83	-
	High	241	-	14.65	-	18.51	-
TDS5B212MX	Low	191	-40	12.74	-1.61	20.56	1.62
	Middle	205	-38	15.82	-1.17	15.96	1.13
	High	180	-61	12.26	-2.39	20.57	2.06
TDS5C212MX	Low	214	-17	12.70	-1.66	19.87	0.93
	Middle	219	-24	16.41	-0.59	15.72	0.89
	High	214	-27	13.53	-1.12	19.47	0.95

3.5. PCIe 5.0 eye pattern evaluation results

PCIe 5.0
32Gbps NRZ
1Vp-p(Diff)
PRBS-7

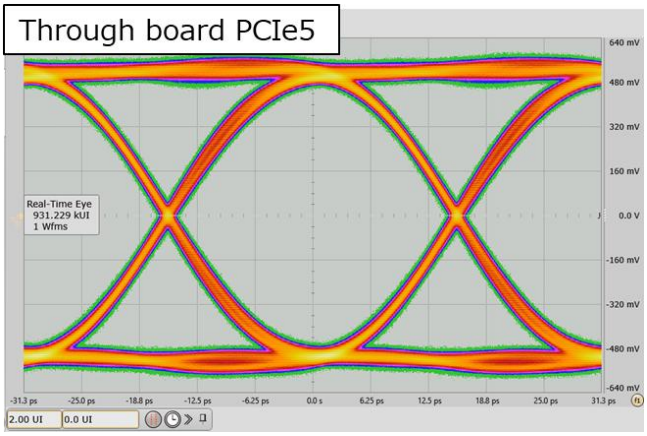


Fig. 14 PCIe 5.0 Through board result

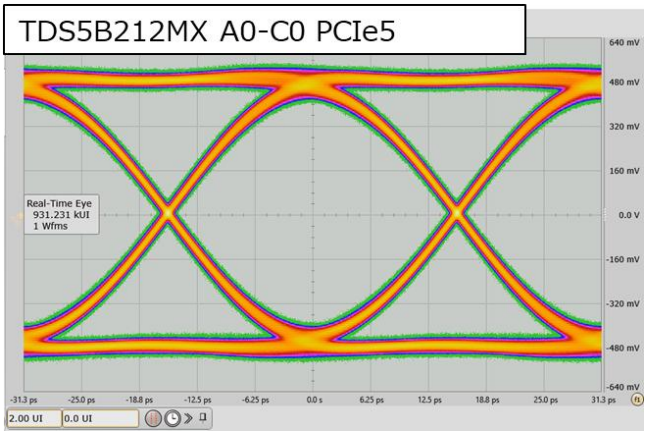


Fig. 15 PCIe 5.0 TDS5B212MX result

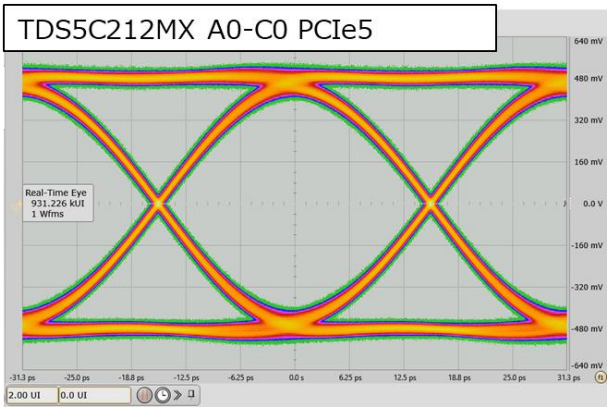


Fig. 16 PCIe 5.0 TDS5C212MX result

Table 4 PCIe 5.0 eye pattern evaluation results

Item	Eye Height (mV)	ΔEye Height (mV)	Eye Width (ps)	ΔEye Width (ps)	TJ (ps)	ΔTJ (ps)
Through board	844	-	28.42	-	4.08	-
TDS5B212MX	725	-119	29.00	-0.59	3.87	0.21
TDS5C212MX	714	-130	28.76	-0.34	3.93	0.16

3.6. USB4 Version2 eye pattern evaluation results

USB4 Version2
40Gbps PAM3
1Vp-p(Diff)
PRBS-7

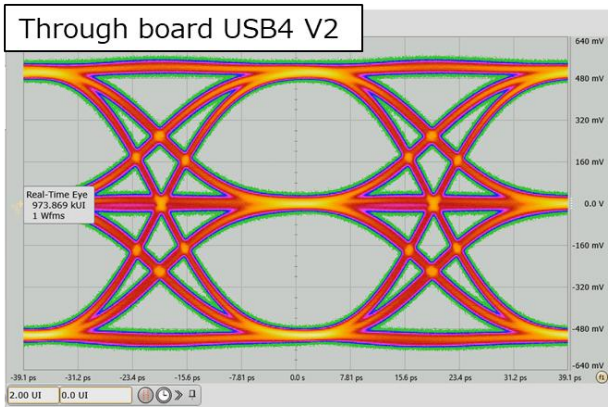


Fig. 17 USB4 Version2 Through board result

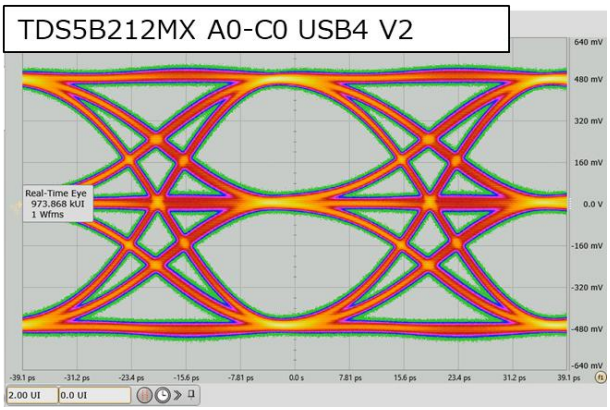


Fig. 18 USB4 Version2 TDS5B212MX result

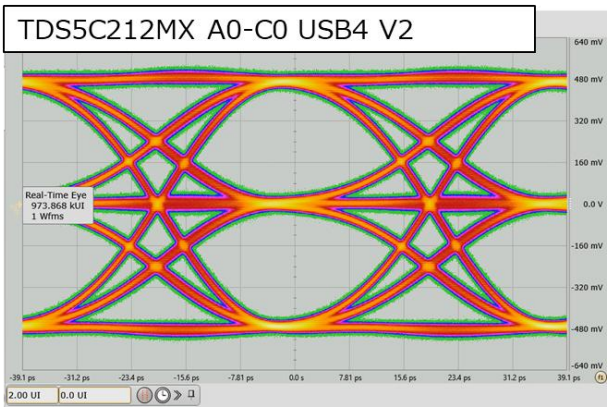


Fig. 19 USB4 Version2 TDS5C212MX result

Table 5 USB4 Version2 eye pattern evaluation results

Item	Eye	Eye Height (mV)	ΔEye Height (mV)	Eye Width (ps)	ΔEye Width (ps)	TJ (ps)	ΔTJ(ps)
Through board	High	418	-	25.39	-	14.07	-
	Low	418	-	24.96	-	14.15	-
TDS5B212MX	High	384	-34	23.19	-2.20	16.33	2.27
	Low	389	-29	23.74	-1.22	15.73	1.57
TDS5C212MX	High	386	-32	23.74	-1.65	15.76	1.69
	Low	376	-42	23.19	-1.77	16.01	1.86

3.7. USB4 eye pattern evaluation results

USB4
20Gbps NRZ
1Vp-p(Diff)
PRBS-7

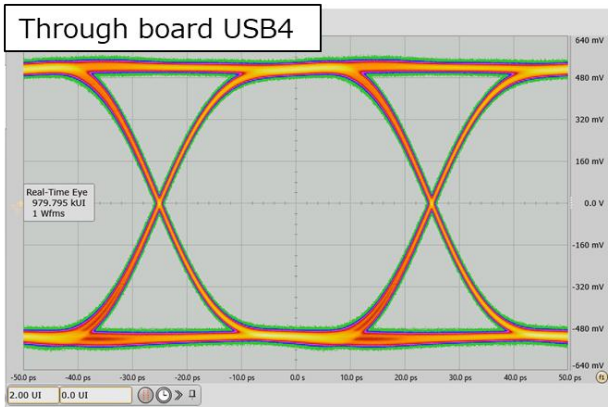


Fig. 20 USB4 Through board result

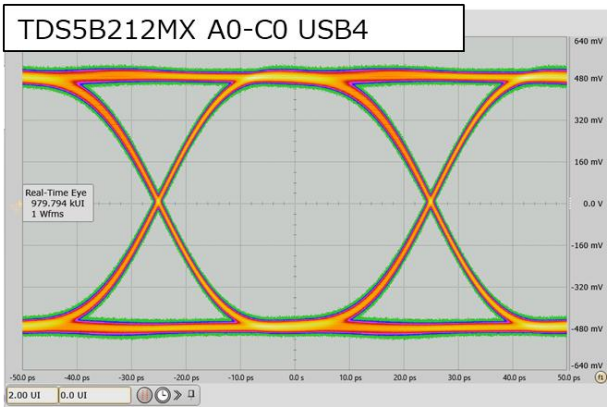


Fig. 21 USB4 TDS5B212MX result

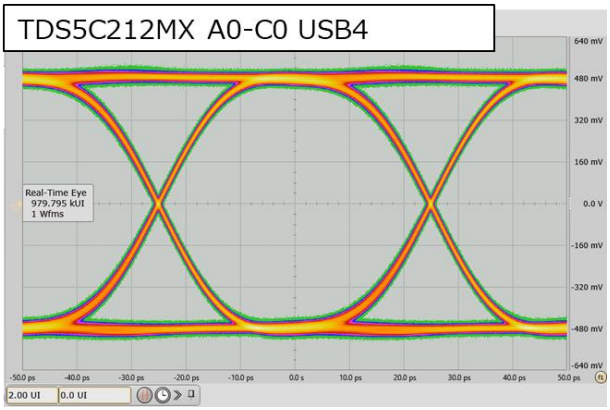


Fig. 22 USB4 TDS5C212MX result

Table 6 USB4 eye pattern evaluation results

Item	Eye Height (mV)	ΔEye Height (mV)	Eye Width (ps)	ΔEye Width (ps)	TJ (ps)	ΔTJ (ps)
Through board	930	-	48.28	-	3.17	-
TDS5B212MX	854	-76	48.05	-0.23	3.49	0.32
TDS5C212MX	859	-71	47.89	-0.39	3.47	0.30

4. Design considerations

This chapter describes key points to be noted when applying the TDS5B212MX and TDS5C212MX in circuit and board designs.

Design guidelines for achieving stable signal transmission are provided, covering topics such as switch I/O voltage conditions, internal structure, and placement examples of AC coupling capacitors.

4.1. Voltage Conditions for Switch I/O Terminals

The datasheets of the TDS5B212MX and TDS5C212MX define both absolute maximum ratings and operating ranges as the voltage conditions applicable to the switch I/O pins (An±, Bn±, Cn±). The absolute maximum ratings specify the upper and lower limits of the switch I/O voltage V_S; exceeding this range may cause device damage. The operating range, on the other hand, specifies the recommended conditions for differential signaling, defined by the differential signal voltage $V_{I/O(Diff)}$ and the common signal voltage $V_{I/O(Com)}$. The former represents the signal amplitude, and the latter its center potential.

Table 7 Switch I/O Voltage Conditions (See the datasheet for details.)

Category	Item	Symbol	Rating
Absolute Maximum Ratings	Switch I/O voltage	V_S	-0.5 ~ 2.5 V
Operating Ranges	Signal pins differential voltage	$V_{I/O(Diff)}$	0 ~1.8 V
	Signal pins common mode voltage	$V_{I/O(Com)}$	0 ~ 2.0 V

The differential signal voltage $V_{I/O(Diff)}$ of 0 to 1.8 V corresponds to a single-ended amplitude of 0 to 0.9 V. Accordingly; each signal line is allowed to swing up to ±0.45 V around the common signal voltage as it varies.

Specifically, as shown in Figure 23, when the common voltage ranges from 0 V to 2.0 V, the I/O voltage operating range including the differential component is defined as −0.45 V to 2.45 V. This also represents the I/O voltage operating range for non-differential use.

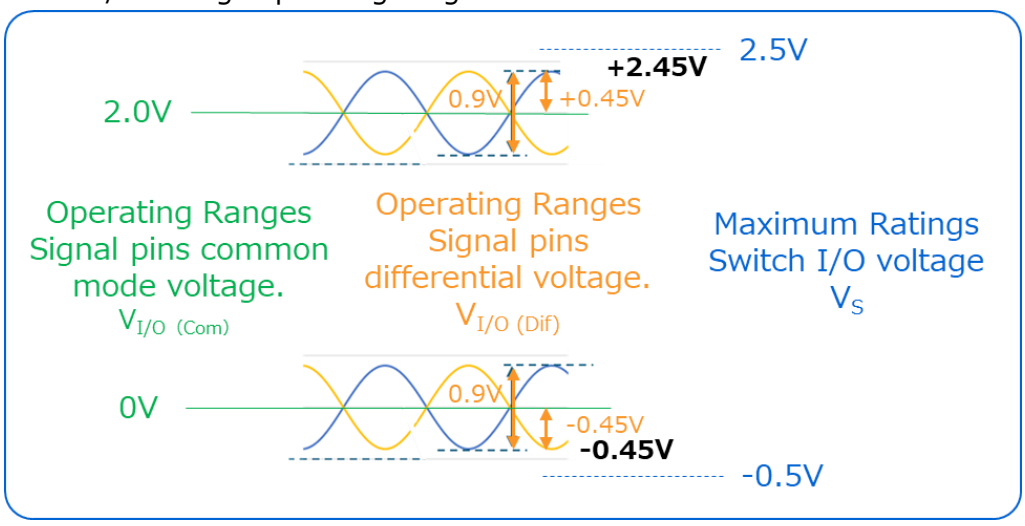


Fig. 23 Relationship Between Absolute Maximum Ratings and Operating Range for Sw I/O

When using these devices, ensure that the switch I/O voltage does not exceed the absolute maximum ratings and that the differential and common signal voltages remain within the operating range. Observing these conditions ensures stable operation.

4.2. Data Signal Connections

A bus switch is a passive switch that electrically connects I/O terminals through an internal switch. Therefore, the A, B, and C ports can be connected independently of the signal direction, allowing flexible use as a Mux/De-Mux as shown in Figure 24 and Figure 25.

Unlike active switches such as redrivers and retimers, no signal direction needs to be specified, providing flexibility in usage.

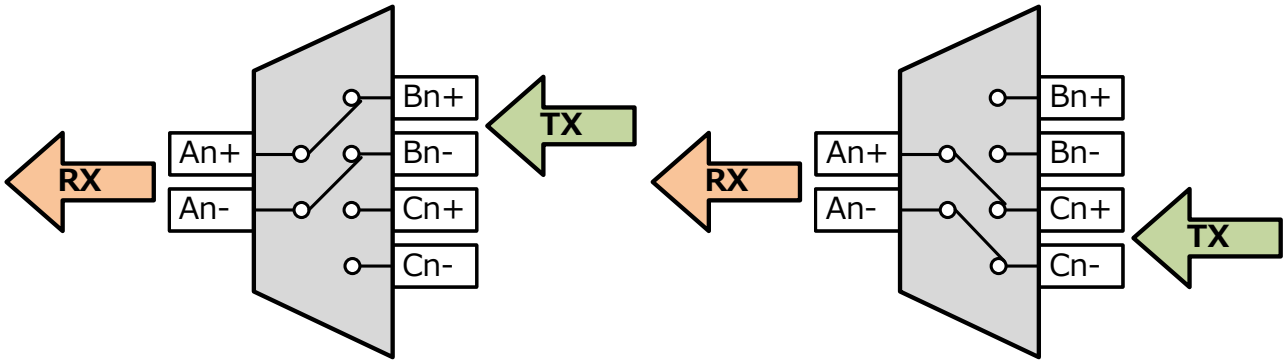


Fig. 24 Example of use as a Mux

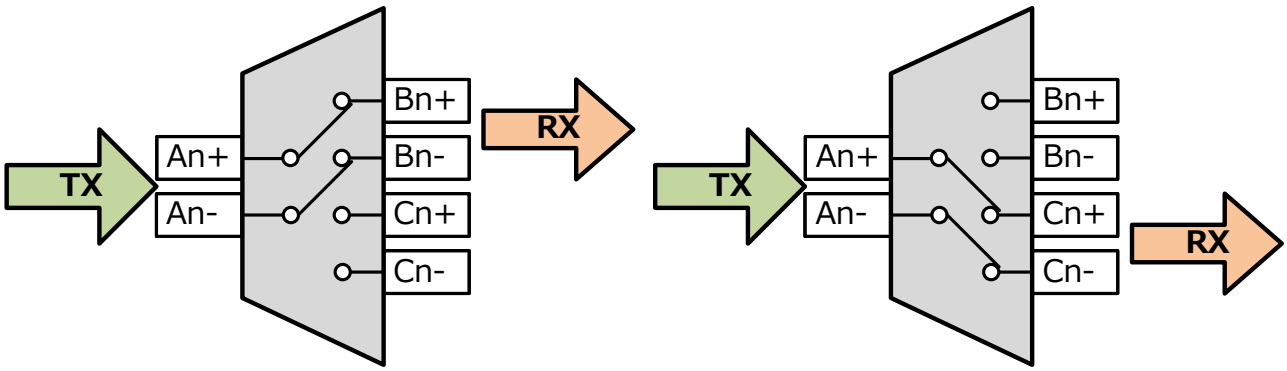


Fig. 25 Example of use as a De-Mux

Additionally, there are no restrictions on the polarity of signals passing through the switch. Differential signals can be transmitted even when the positive and negative polarities are reversed with respect to the terminal names.

For example, when $\overline{OE}$ = L and SEL = L, An+ ⇔ Bn+ and An− ⇔ Bn− are internally connected through the switch. Therefore, it is possible to pass a negative signal through the An+ ⇔ Bn+ path and a positive signal through the An− ⇔ Bn− path for communication.

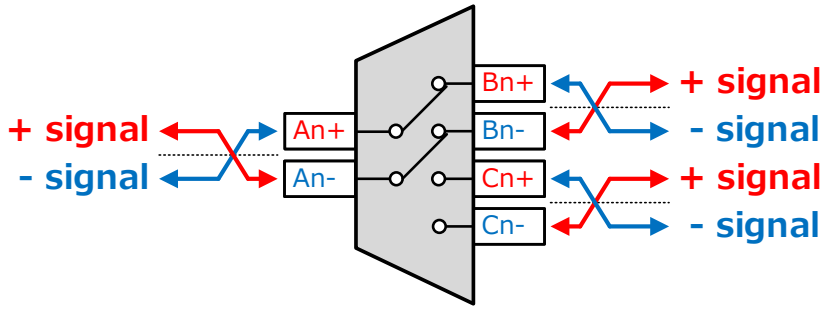


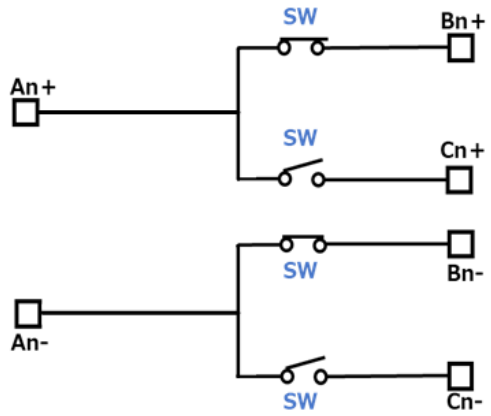
Fig. 26 Example of transmitting signals with reversed polarity relative to the terminal names

4.3. Internal Structure of Switch I/O Lines

The internal circuits of the data lines for the existing TDS4 series and the TDS5 series are shown in Figure 27 and Figure 28, respectively.

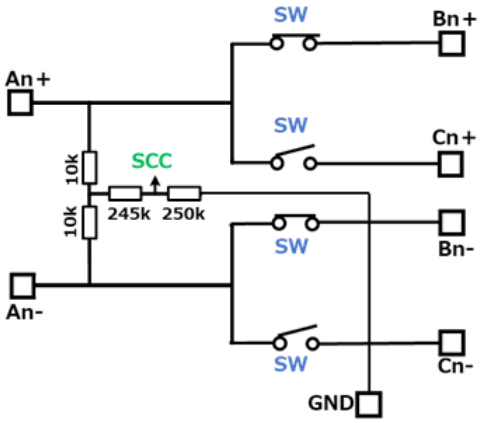
The TDS4 series is a passive switch with excellent high-frequency performance, designed to implement a PCIe 5-compatible Mux/De-Mux. As a result, both the common- and differential resistances of the data lines are infinite, as shown in Figure 27.

The TDS5 series, designed for the higher-speed PCIe 6, incorporates a circuit at the A port (An+/−) that monitors the common signal voltage ($V_{I/O(Com)}$) of the differential signal, as shown in Figure 28. A switch control circuit (SCC) then suppresses variations in the switch resistance (R_{ON}) caused by $V_{I/O(Com)}$ fluctuations.



TDS4A212MX, TDS4B212MX

Fig. 27 Internal circuit of the TDS4 series



TDS5B212MX, TDS5C212MX

Fig. 28 Internal circuit of the TDS5 series

Common resistance of the TDS5 series:

As shown in Figure 28, weak pull-down resistors are connected to An+ and An− (during differential signal operation, the equivalent common resistance from An+ and An− to GND is approximately 1 MΩ each). Although these resistors slightly bias the common-mode voltage ($V_{I/O\ (Com)}$) toward 0 V, their effect is negligible and does not influence the common-mode voltage of the external differential drivers/receivers connected to each port (An, Bn, Cn).

Differential resistance of the TDS5 series:

In addition, a weak 20 kΩ differential resistor (high impedance) is connected between An+ and An−. Since high-speed differential signals typically have a much lower differential impedance (e.g., 100 Ω), this resistor has no impact on the differential signals.

4.4. Land Pattern Dimensions (for reference only)

The land pattern dimensions for the XQFN16 package are shown below. Please refer to these data when designing the printed circuit board.

The metal area enclosed by the dashed line should be connected to the GND plane. Connecting the GND pin to the GND plane optimizes the high-frequency characteristics.

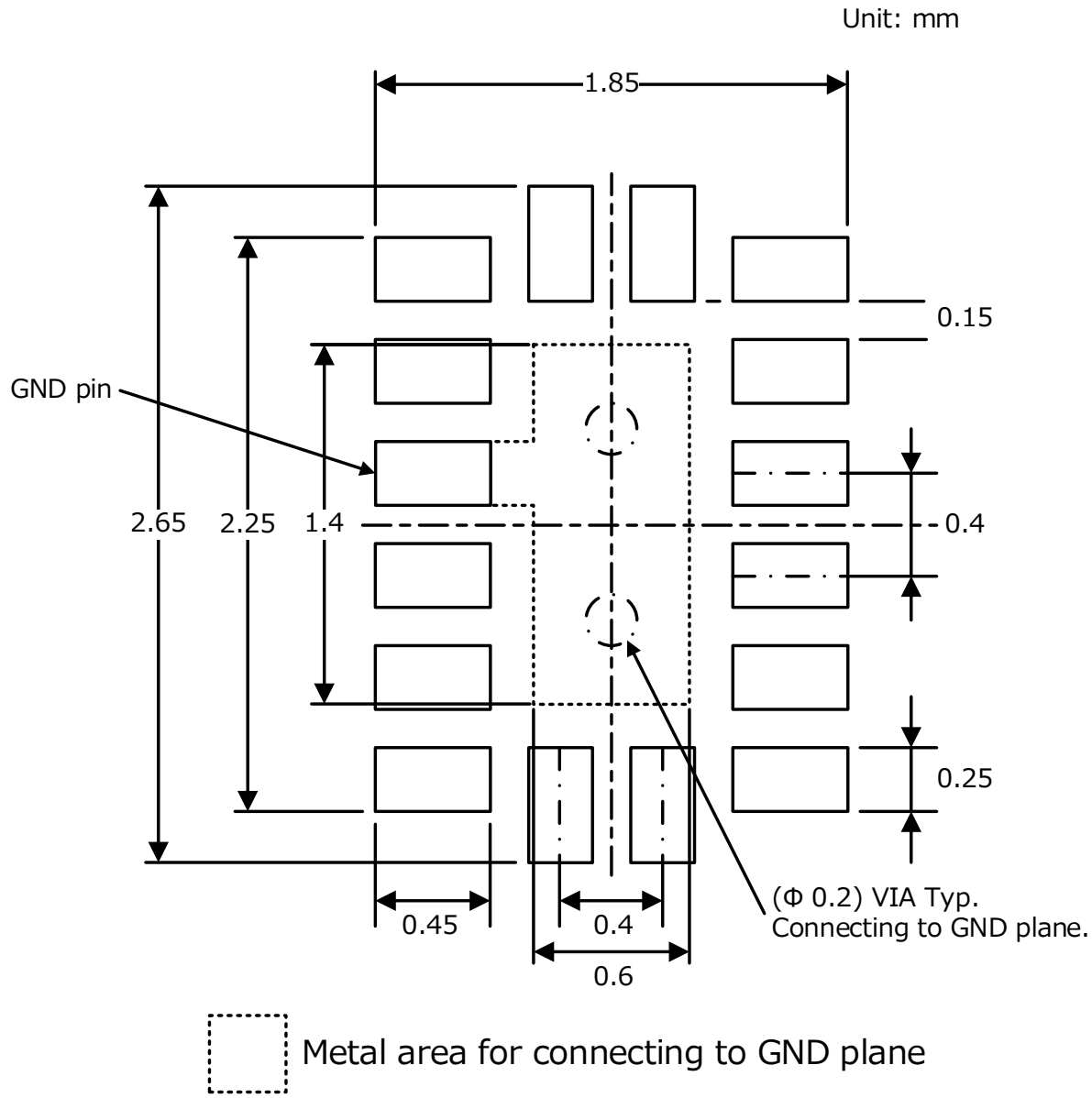


Fig. 29 Land pattern for the XQFN16 package (for reference only)

4.5. AC coupling

Many high-speed differential interfaces require a capacitor (AC coupling capacitor) to provide an AC coupling between the TX (transmitter) and the RX (receiver).

When a high-speed differential signal passes through an AC coupling capacitor, the DC components of the signal are removed, enabling signal transmission even when the common-mode voltage differs between the TX and the RX.

The figure below shows an example where the host board and the device board are connected by a connector. In many high-speed differential interfaces, if the TX and the RX are connected by connectors, it is recommended that AC coupling capacitors be placed between the TX and the connectors. Therefore, an AC coupling capacitor is placed in the position shown in Fig. 30.

If this happens, the high-speed differential signal passes through an AC coupling capacitor, which removes the DC components, so that the common-mode voltage is supplied from the TX prior to passing through an AC coupling capacitor, and the common-mode voltage is supplied from the RX after passing through an AC coupling capacitor.

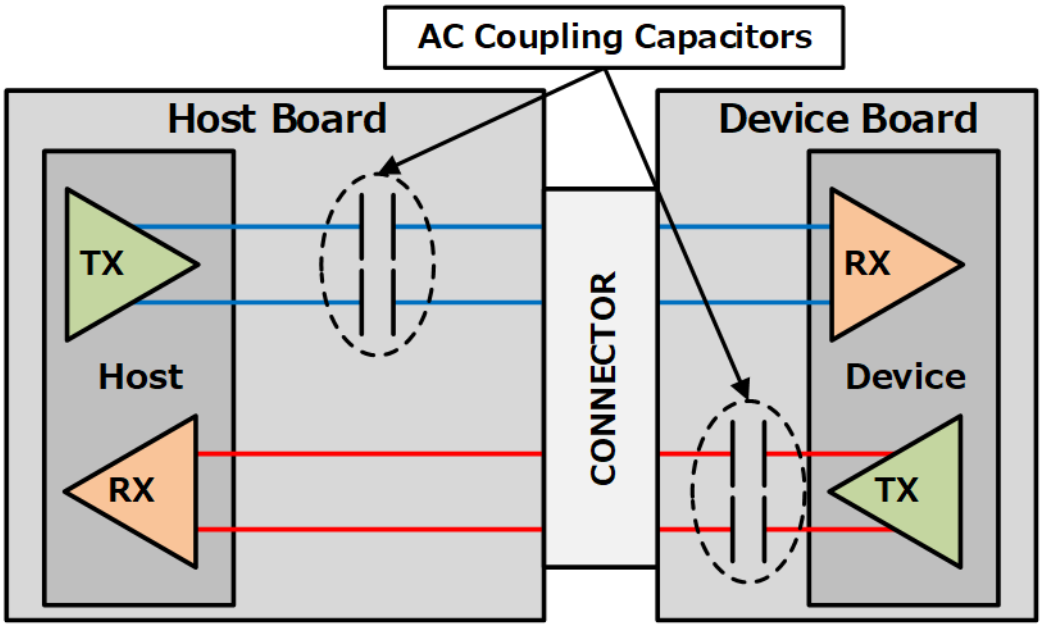


Fig. 30 AC Coupling Capacitor Layout

In addition, an AC coupling capacitor needs to select an appropriate capacitance according to the interface. For the same differential pair, place symmetrically with the same capacity and the same package size.

Package sizes of 0201 and 0402 are recommended.

The following example shows an exclusive connection between the host board and two device boards. The Mux/De-Mux is located on the host board. The switching is controlled by the host. Three typical arrangement patterns are shown below.

(a)Place a capacitor between Mux/De-Mux and the device*

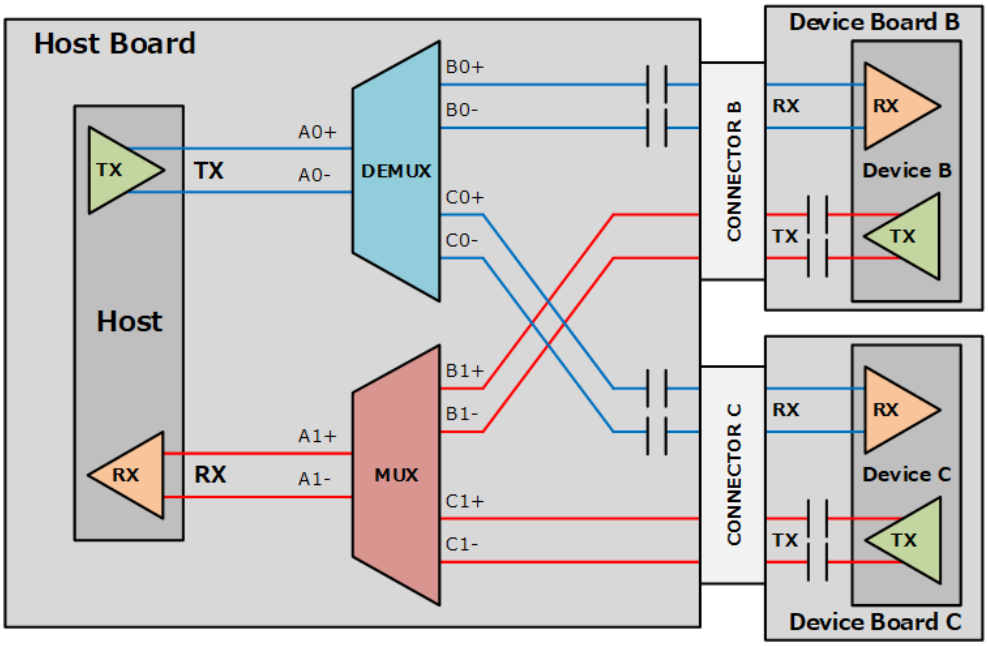


Fig. 31 An arrangement where a capacitor is placed between Mux/De-Mux and the device

*Check that the common-mode voltage of the host's TX and RX is within Mux/De-Mux's operating limits.

In the path passing through the De-Mux (blue line), an AC coupling capacitor is placed between the De-Mux and the connector.

Since the differential signal passes through the De-Mux prior to passing through the AC coupling capacitor, the De-Mux is supplied with the common-mode voltage from the host’s TX.

In the path passing through the Mux (red line), an AC coupling capacitor is placed between the TX of the device and the connector.

Since the differential signal passes through the Mux after passing through the AC coupling capacitor, the Mux is supplied with the common-mode voltage from the host’s RX.

Since it is recommended that the AC coupling capacitor be placed between the TX and the connector, the position to be placed is limited to this position.

(b)Place a capacitor between TX and Mux/De-Mux *

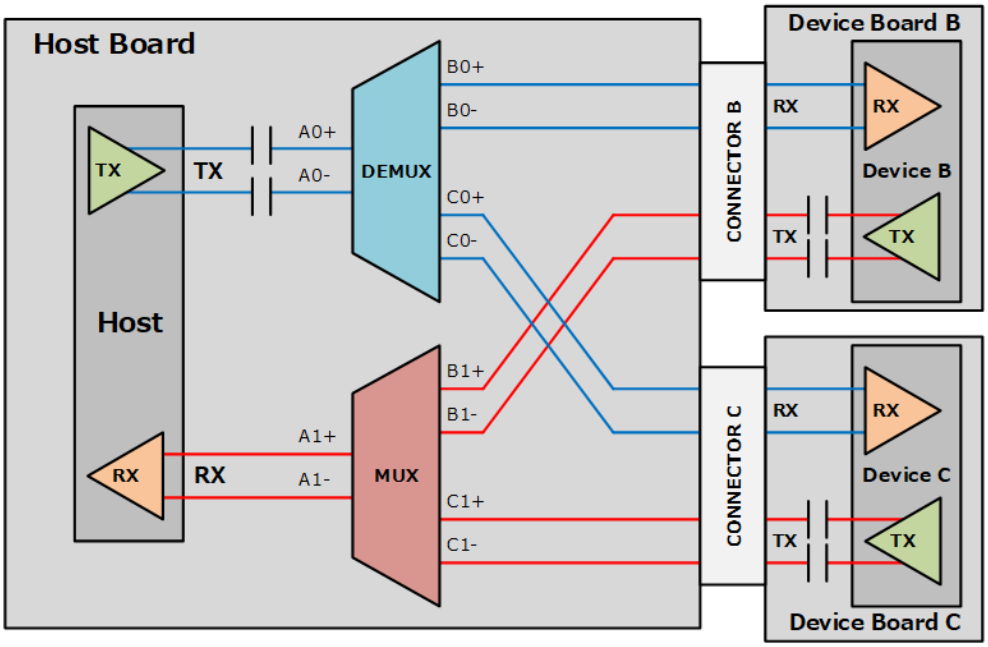


Fig. 32 An arrangement where a capacitor is placed between TX and Mux/De-Mux

*It can be used when the RX common mode voltage of the device is within the operating range of the De-Mux, and the RX common mode voltage of the device is within the operating range of the Mux.

In the path passing through the De-Mux (blue line), an AC coupling capacitor is placed between the TX and the De-Mux.

Since the differential signal passes through the AC coupling capacitor and then through the De-Mux, the RX of the device provides a common-mode voltage.

In the path passing through the Mux (red line), an AC coupling capacitor is placed between the TX of the device and the connector.

Since the differential signal passes through the Mux after passing through the AC coupling capacitor, the Mux is supplied with the common-mode voltage from the host's RX.

Since it is recommended that the AC coupling capacitor be placed between the TX and the connector, the position to be placed is limited to this position.

(c)Place capacitors on both sides of Mux/De-Mux *

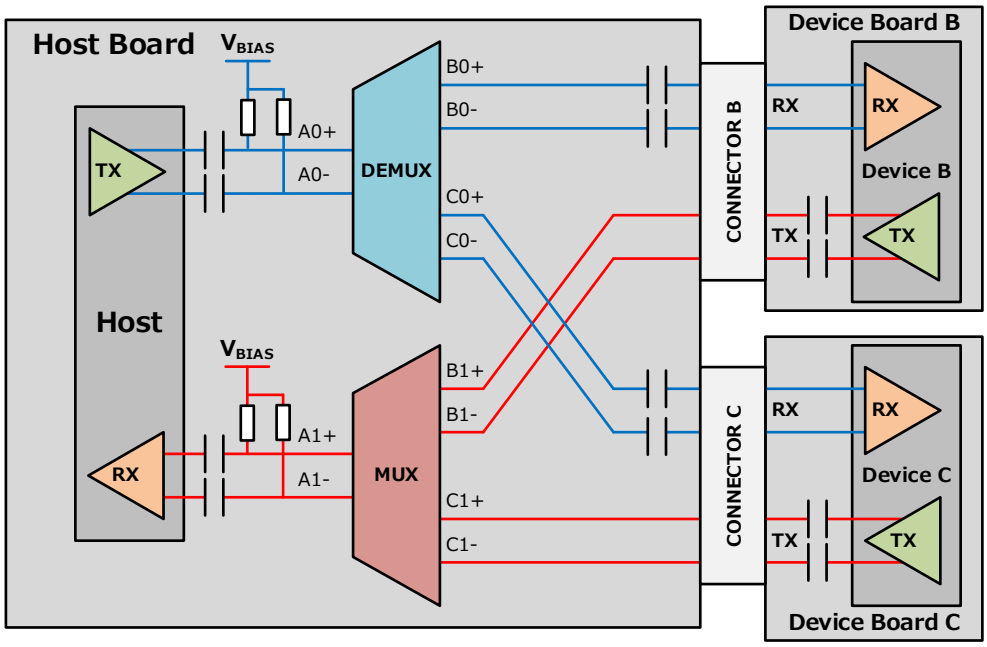


Fig. 33 An arrangement where capacitors are located on both sides of Mux/De-Mux

*This configuration is used when the common-mode voltage of the TX and RX of the host/device is outside of the operating limits of the Mux/De-Mux.

An AC coupling capacitor is placed on both sides of the Mux/De-Mux for both the path passing through the Mux and the path passing through the De-Mux.

In such an arrangement, the Mux/De-Mux will not receive common-mode power from both the host and the device.

Therefore, as shown in the diagram, apply a common-mode voltage between 0 and 2.0 V with a resistor of 10 kΩ or more.

5. Application

This chapter introduces specific application examples using the TDS5B212MX and TDS5C212MX. Through real-world cases such as PCIe, USB Type-C, docking stations, and semiconductor testers, this chapter illustrates the configurations and use cases in which these products can be effectively applied, providing a clear image of their adoption in actual systems.

5.1. Available interfaces

The TDS5B212MX and TDS5C212MX are high-speed differential 2:1 Mux (multiplexer) / 1:2 De-Mux (demultiplexer) devices that can be used to switch signals between two different paths.

By leveraging Toshiba's proprietary SOI process "TarfSOI™" together with a compact package, these devices achieve excellent high-frequency characteristics and support transfer rates of up to 64 GT/s.

In addition, they offer a wide common-mode voltage range (0 to 2.0 V) and differential signal voltage swing (0 to 1.8 Vpp), making them suitable for a wide variety of high-speed data protocols. Representative interfaces in which these devices can be used are listed below.

PCIe® family: PCIe 6.0 / 5.0 / 4.0 / 3.0
CXL™ family: CXL 3.0 / 2.0 / 1.0
USB family: USB4® Ver.2 / USB4 / USB3.2 Gen2×1 / Gen1×1
Thunderbolt™ family: Thunderbolt 5 / 4 / 3 / 2
DisplayPort™ family: DisplayPort 2.0 / 1.4 / 1.3 / 1.2

5.2. Use Case in PCIe Systems

The following shows how Mux/De-Mux switches the connectivity between the CPU and several PCIe slots.

Depending on the specifications of the PC and server, the PCIe lanes on the CPU may not be sufficient if there is a need to expand the PCIe slots. In such cases, a Mux/De-Mux can be used to connect the CPU to several PCIe slots. For instance, if you have 8 lanes of CPU with 16 lanes each of TX and RX directly connected to PCIe slot 1, and you want to use the remaining 8 lanes exclusively with PCIe slot 1 and PCIe slot 2, connect the 2:1 Mux/1:2 De-Mux as depicted in the figure below.

TDS5B212MX/TDS5C212MX can be switched between two lanes per device, thus it can be connected by placing eight devices between the CPU and PCIe slots.

Use AC coupling capacitors on the Mux/De-Mux to provide the appropriate common signal voltage as follows.

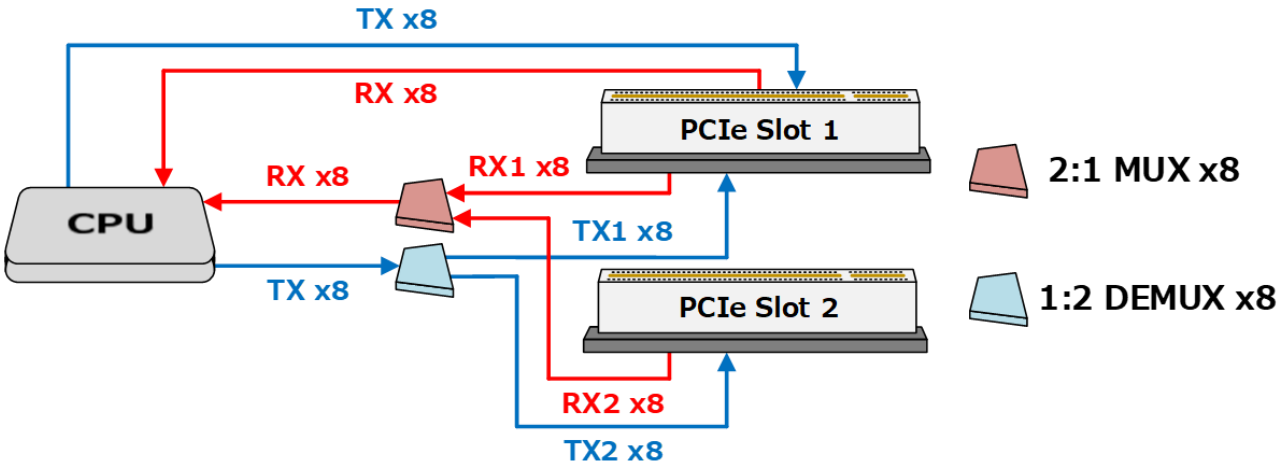


Fig. 34 Mux/De-Mux PCIe Use Case

5.3. Use Case in USB Type-C Systems

When USB Type-C requires plug flip, the following is a sample connection. Since USB Type-C has no front and back terminals, and signals must be transmitted and received in either direction, a Mux/De-Mux is used to switch between front and back. The orientation is determined by the CC terminal, and the USB control IC selects the Mux/De-Mux port connection. The following shows an example where the host board and device board are connected using Type-C cables on both sides.

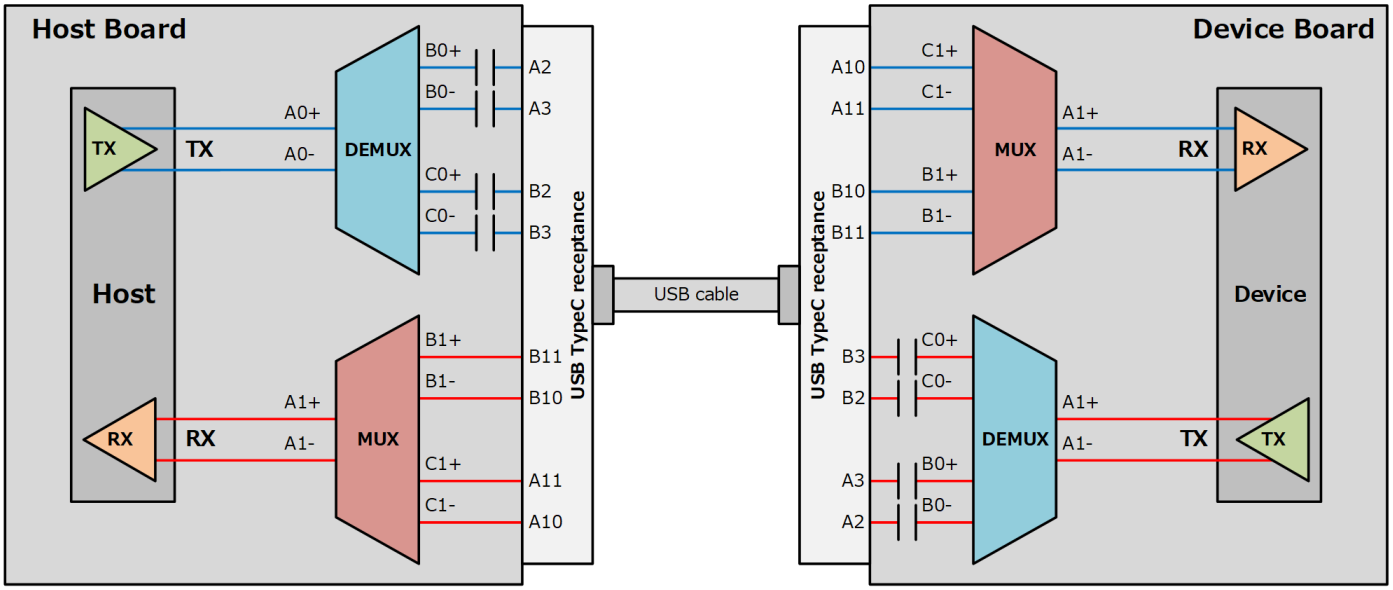


Fig. 35 USB Type-C Mux/De-Mux Use Case

5.4. Application Example in USB Hubs and Docking Stations

This section shows an example of switching the connection destination using the TDS5B212MX / TDS5C212MX in a USB hub or docking station.

In this configuration, the TDS5B212MX / TDS5C212MX is inserted as a 1:2 Mux/De-Mux between the upstream port of the USB hub or docking station and the hub IC. A control signal selectively connects either PC 1 or PC 2, allowing USB peripherals to be switched freely between the two PCs without unplugging the cable.

With its wideband and low-insertion-loss characteristics, the TDS5 series supports interfaces from USB4 to Thunderbolt™ 4/5, enabling stable signal transmission even for next-generation interfaces.

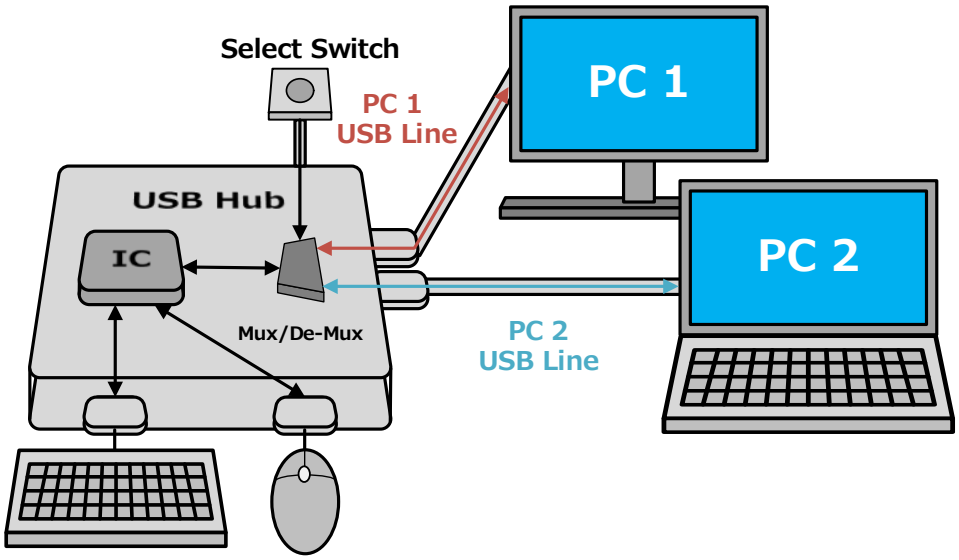


Fig. 36 Switching a USB hub/docking station between two PCs using a Mux/De-Mux

Inside USB hubs and docking stations, a USB hub IC handles core functions such as USB port distribution and video output. Recently, video output via USB Type-C has become mainstream in these hub ICs, and dedicated DisplayPort signal outputs are often limited to a single channel.

However, USB hubs and docking stations may need to support both DisplayPort and HDMI ports, which requires routing a single DisplayPort signal to either the DisplayPort or HDMI output. Using the TDS5 series for this switching stage enables selective output to either port with a simple circuit. Its wideband and low-insertion-loss characteristics also support high-speed video interfaces such as DisplayPort 2.1, ensuring high-quality signal transmission.

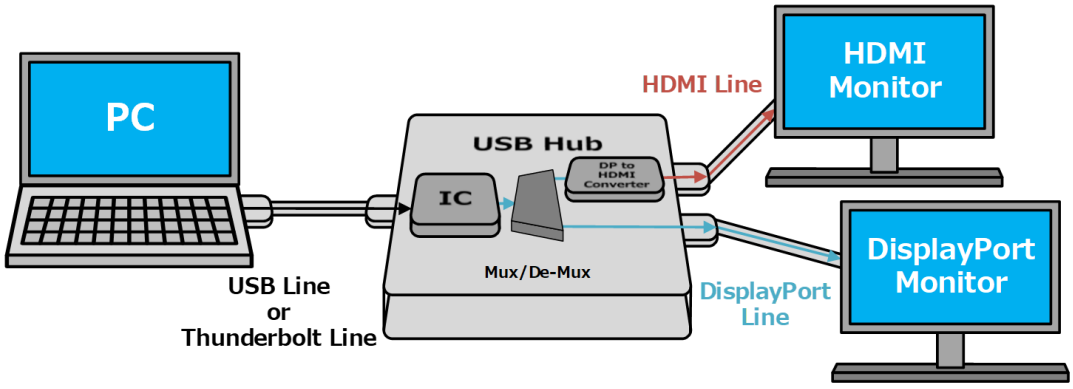


Fig. 37 Switching between HDMI and DisplayPort outputs using a Mux/De-Mux

5.5. Use as a 1:4 Mux/De-Mux via Cascade Connection

The TDS5B212MX and TDS5C212MX can also be used as a 1:4 Mux/De-Mux by connecting multiple devices in cascade (multi-stage connection).

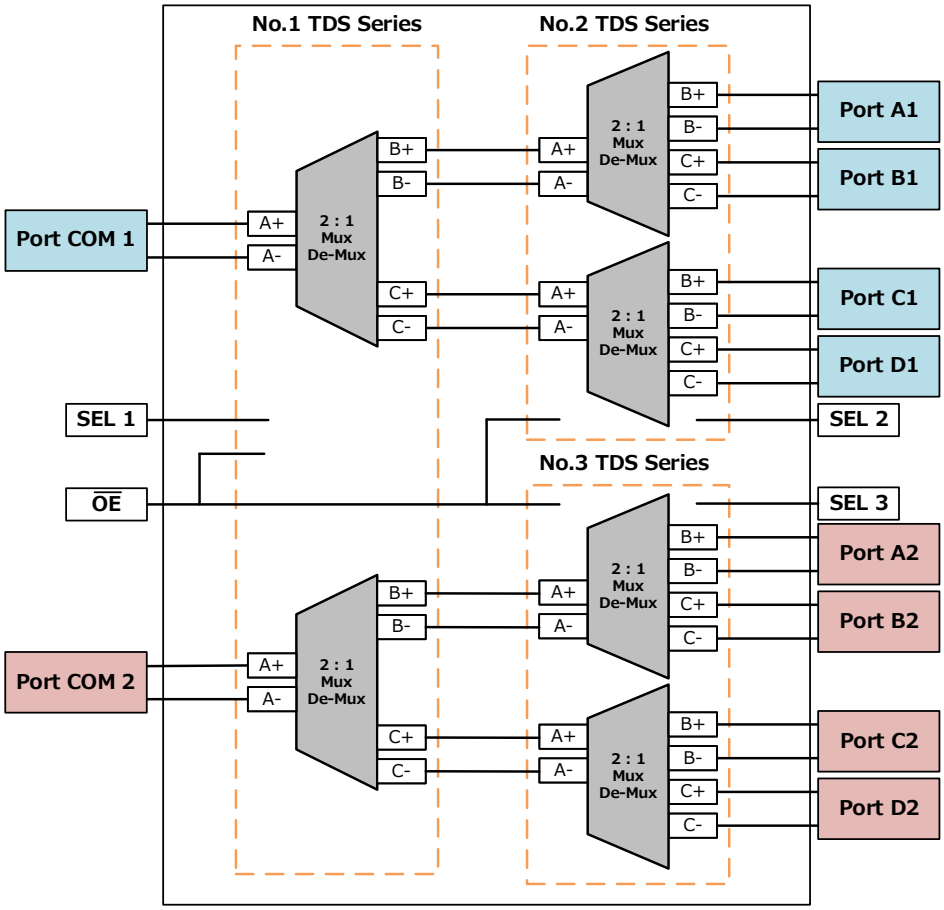


Fig. 38 2ch 1:4 Mux/De-Mux configured by cascade connection of three TDS5 series

Table 8 Truth table of the 2ch 1:4 Mux/De-Mux in cascade connection

Input $\overline{OE}$	Input SEL 1	Input SEL 2, 3	Function (n = 0, 1)
L	L	L	Port COMn ± =Port An ±
L	L	H	Port COMn ± =Port Bn ±
L	H	L	Port COMn ± =Port Cn ±
L	H	H	Port COMn ± =Port Dn ±
H	Don't care	Don't care	All Port Disconnect

In this configuration, the signal passes through two devices, so note that the on-resistance and insertion loss are also doubled accordingly.

The differential insertion loss shown below is the characteristic measured when the signal passes through two TDS5B212MX or TDS5C212MX devices.

The evaluation was performed using the evaluation board described earlier, which mounts two devices.

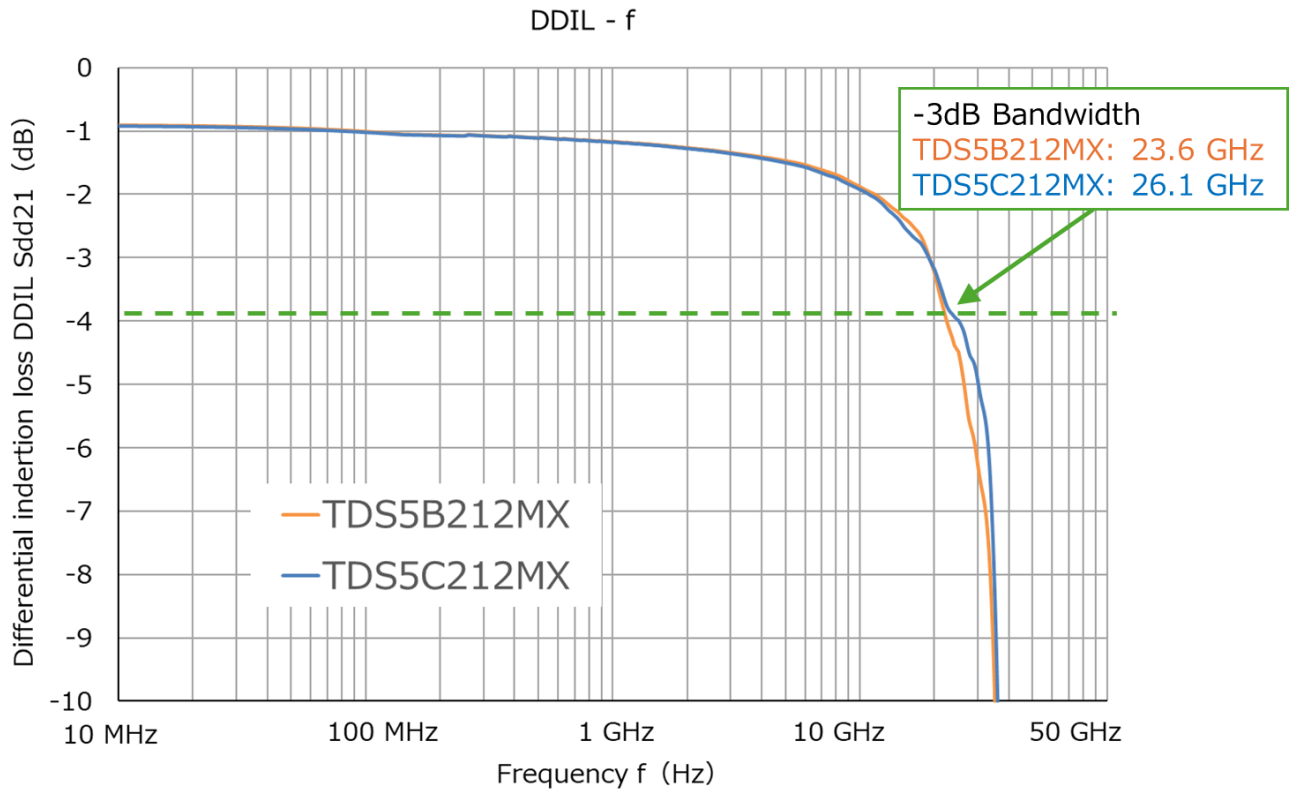


Fig. 39 Differential insertion loss vs. frequency for TDS5B/C212MX in cascade connection

Table 9 Differential insertion loss of TDS5B/C212MX in cascade connection

High frequency characteristics (Typ.)		TDS5B212MX	TDS5C212MX
-3dB Bandwidth		23.6 GHz	26.1 GHz
Differential insertion loss DDIL S_{dd21}	f = 2.5 GHz	-1.3 dB	-1.3 dB
	f = 4.0 GHz	-1.4 dB	-1.4 dB
	f = 5.0 GHz	-1.5 dB	-1.5 dB
	f = 8.0 GHz	-1.7 dB	-1.7 dB
	f = 10.0 GHz	-1.9 dB	-1.9 dB
	f = 12.8 GHz	-2.1 dB	-2.2 dB
	f = 16.0 GHz	-2.5 dB	-2.5 dB

5.6. Switching Between Loopback Circuit and ATE in Testers

In conventional ATE evaluation, high-speed loopback testing and functional testing required different signal paths, necessitating test board changes or relay-based path selection. This not only increased test time and system complexity but also caused high-speed signal degradation due to the bandwidth limitations and parasitic components of relays.

By using the TDS5B212MX and TDS5C212MX as shown in this figure, a wideband and low-loss signal path required for high-speed interface testing can be secured, while the following two evaluation paths can be switched on a single board:

High-speed loopback path: The DUT's TX signal is routed through the De-Mux to the loopback circuit, and the returned signal is fed back to the DUT's RX through the Mux.

Functional test path: The DUT's I/O pins are connected directly to the ATE tester, enabling functional testing via the ATE's TX/RX.

In high-speed serial standards such as PCI Express and USB, where channel loss and reflection directly affect communication quality, minimizing signal degradation through the switch is critical. With its low insertion loss and excellent high-frequency characteristics, the TDS5 series meets these requirements, enabling evaluation while maintaining communication quality.

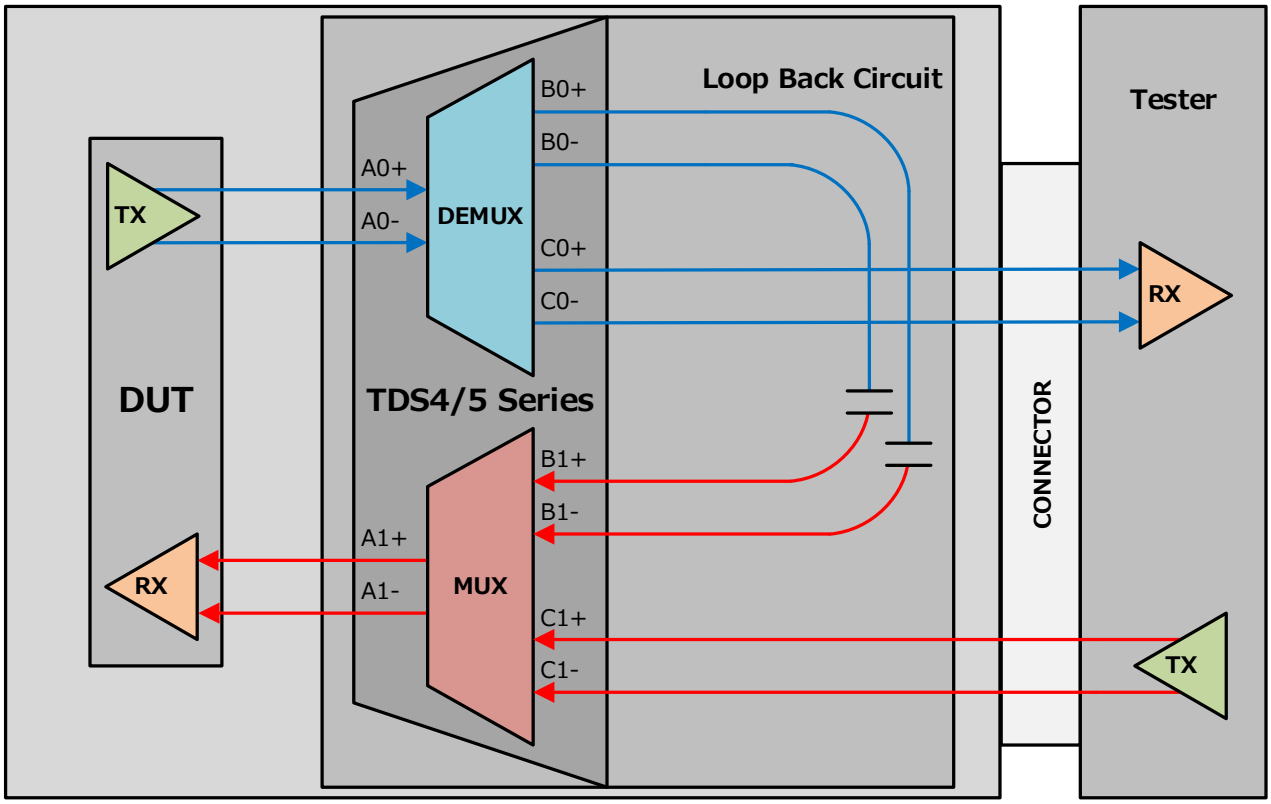


Fig. 40 Switching Between Loopback Circuit and ATE in Testers

6. Summary

This document describes our Mux/De-Mux bus-switch, the TDS5B212MX and the TDS5C212MX, for high-speed differential interfaces.

If you need a Mux, De-Mux for a PCIe, USB, Thunderbolt or other high-speed interfaces, we would like you to consider TDS5B212MX, TDS5C212MX. Please Refer to the data sheet for other detailed characteristics.

For TDS5B212MX product pages and data sheets, see → Click Here

For TDS5C212MX product pages and data sheets, see → Click Here

For a list of bus switches, see → Click Here

Here is an introduction to the Toshiba bus switch in the mini catalog → Click Here

Application notebook: Bus-switch basics here → Click Here

Application notebook: 32Gbps MUX/DEMUX Bus-Sw TDS4A212MX、TDS4B212MX → Click Here

This is FAQ for the bus switch → Click Here

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