Bi-CMOS Linear Integrated Circuit Silicon Monolithic

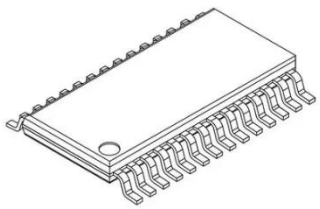
TB67B030FNG/FTG

Sensorless sine wave BLDC motor driver

1. Description

TB67B030FNG/FTG is a driver IC for 3-phase BLDC motor drives. It supports sensorless, 3-hall, and 1-hall position detection, and has sine wave, 150 °, and 120 ° (3-hall only) drive methods.

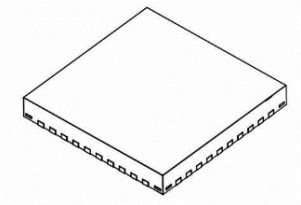
TB67B030FNG



P-HTSSOP28-0510-0.65-001

Weight: (0.107 g)

TB67B030FTG



P-VQFN40-0606-0.50-003

Weight: (0.091 g)

2. Applications

Cooling fan, ventilation fan, pump, BLDC motor.

3. Features

- Support sensorless sine wave
- Support Hall IC input
- Wide operation range: V_{VM} = 5.5 to 48 V
- Low R_{ON}: $R_{DS(H+L)}$ = 0.3 Ω (typ.)
- Built-in DCDC
- Serial I/F
- Standby mode: I_{VM_STBY} = 10 μA (typ.)
- Built-in NVM
- Shunt-less current detection
- Closed loop speed control
- Selectable rotating pulse signals
- Automatic lead angle control and fixed lead angle control
- Thermal shutdown detection (TSD)
- Power supply undervoltage lock out detection (UVLO)
- Overvoltage detection (OVP)
- Output current limit (OCL)
- Overcurrent shutdown detection (ISD)
- Motor lock detection

4. Block Diagram

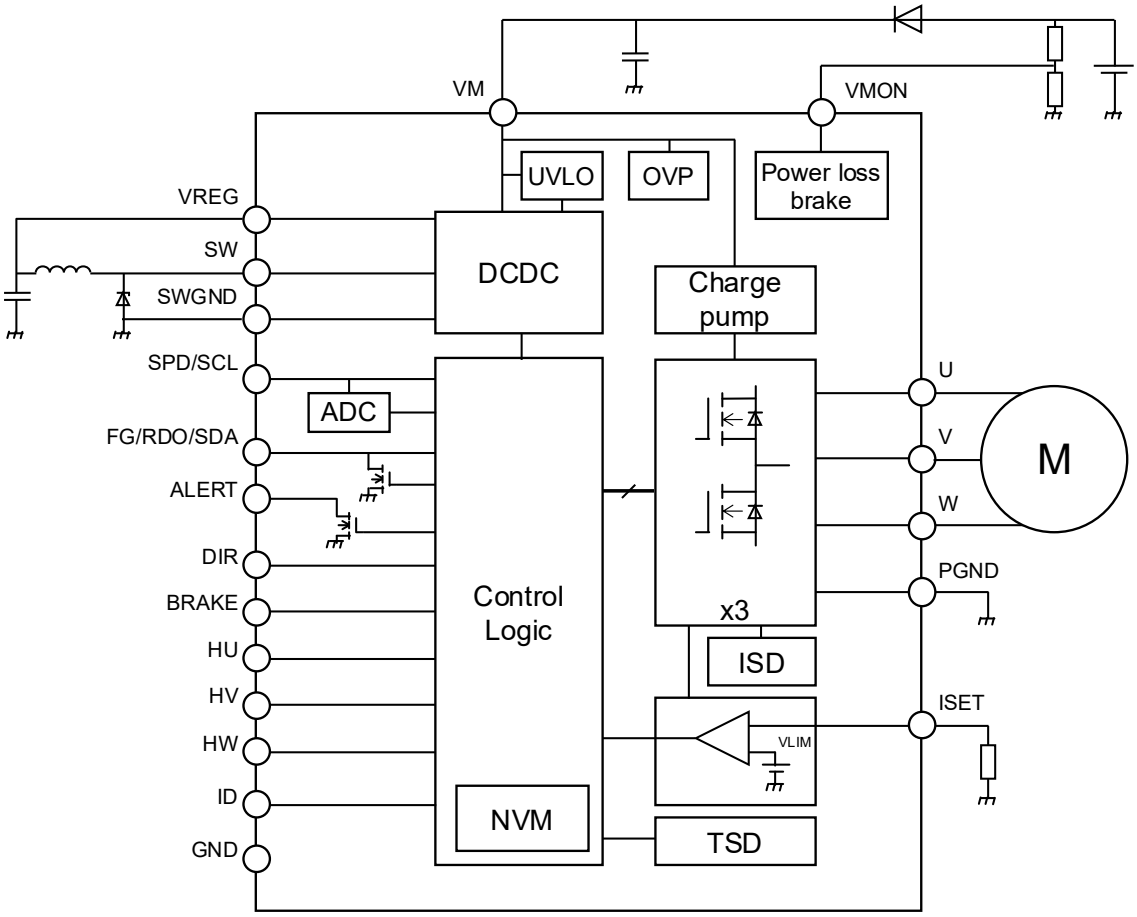


Figure 4.1 Block Diagram

Note: Some of the functional blocks, circuits or constants labels in the block diagram may have been omitted or simplified for explanation purposes.

5. Pin Assignments

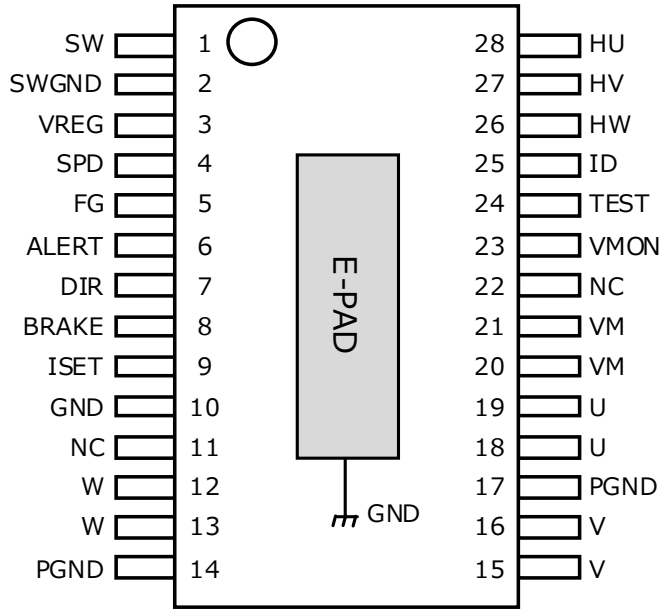


Figure 5.1 TB67B030FNG Pin Assignments

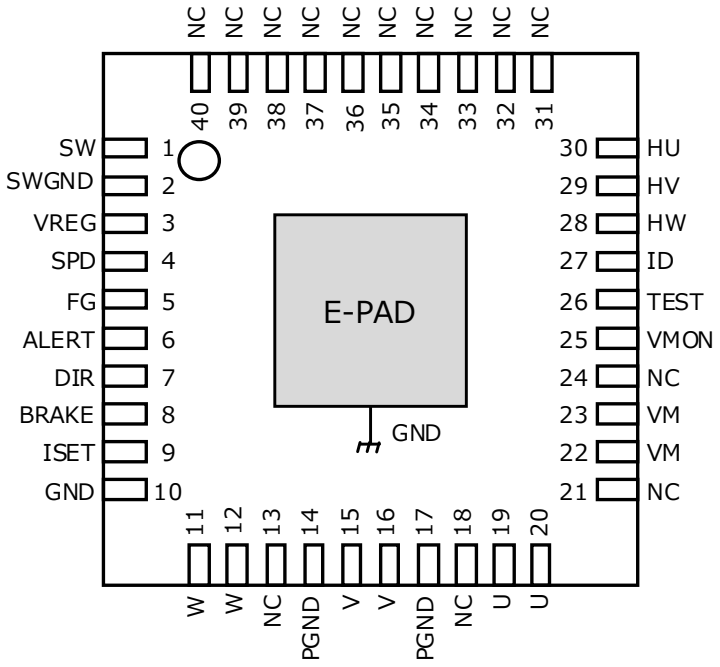


Figure 5.2 TB67B030FTG Pin Assignments

Note: The exposed metal pad on the bottom of the package (E-PAD) is used for heat dissipation. When using the device, always solder the E-PAD to the GND area of the board.

Note: There are two pins each for U, V, W, and VM, each of which should be used in Short. The GND pins consist of PGND and GND, which must also be used in Short.

6. Pin Description

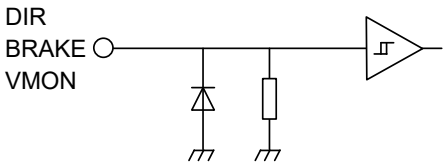
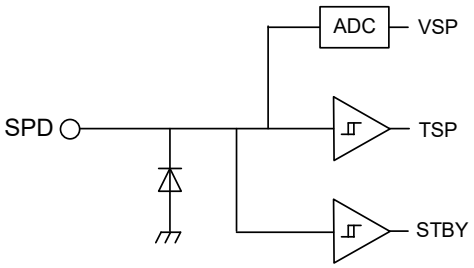
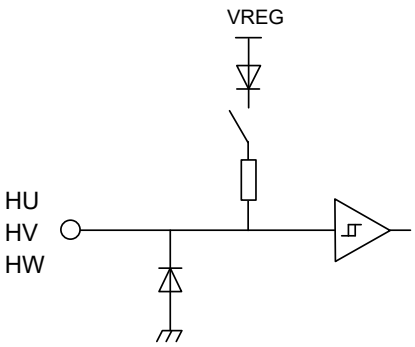
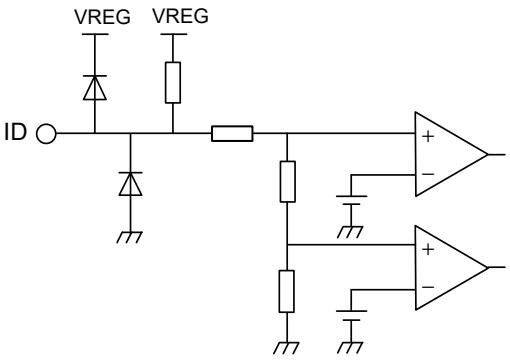
Table 6.1 Pin Description

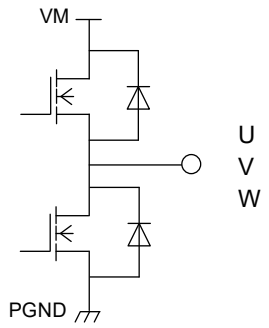
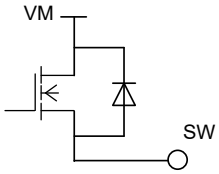
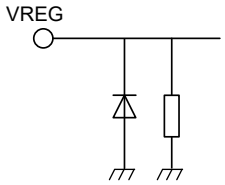
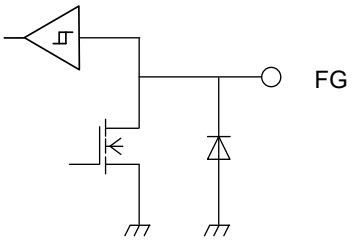
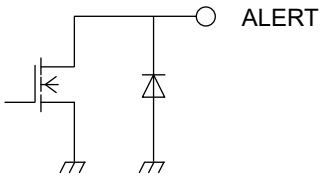
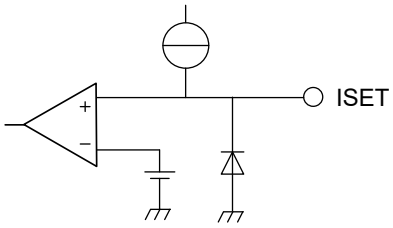
Name	Pin number FNG	Pin number FTG	I/O	Description
SW	1	1	Output	DCDC switching output
SWGND	2	2	Ground	DCDC GND
VREG	3	3	Power	DCDC voltage feedback Power supply for internal circuit
SPD	4	4	Input	Speed command input
SCL			Input	Serial I/F CLK input
FG	5	5	Output	Rotation signal output (Open drain)
RDO			Output	Rotation detection signal output (Open drain)
SDA			In/Out	Serial I/F DATA input/output
ALERT	6	6	Output	Alert signal output (Open drain)
DIR	7	7	Input	Rotation direction control input
BRAKE	8	8	Input	Brake control input
ISET	9	9	In/Out	Current limit setting
GND	10	10	Ground	GND
W	12, 13	11, 12	Output	W phase output
V	15, 16	15, 16	Output	V phase output
U	18, 19	19, 20	Output	U phase output
PGND	14, 17	14, 17	Ground	Large current GND
VM	20, 21	22, 23	Power	Power supply
VMON	23	25	Input	Power off monitor
TEST	24	26	Input	TEST pin (Note 1)
ID	25	27	Input	Serial I/F address setting
HW	26	28	Input	W phase hall signal input
HV	27	29	Input	V phase hall signal input
HU	28	30	Input	U phase hall signal input
NC	11, 22	13, 18, 21, 24 31 to 40	—	Not Connected (Note 2)

Note 1: Connect TEST pin to ground during normal use.
Note 2: The NC pins are not connected inside the IC. During layout, it is possible to connect them with the adjacent pins but be careful to avoid shorting to the power supply or ground.

7. Input and Output Equivalent Circuit

Table 7 Input and Output Equivalent Circuit

Pin name	Comment	Equivalent circuit
DIR, BRAKE, VMON	Logic input	
SPD	Speed command input Serial, Clock input	
HU, HV, HW	Hall IC signal input	
ID	ID setting pin	

Pin name	Comment	Equivalent circuit
U, V, W	Motor output	
SW	DCDC output	
VREG	IC internal power supply input DCDC voltage feedback input	
FG	Open drain output Serial communication, data input / output	
ALERT	Open drain output	
ISET	Current limit detection current output Current limit detection voltage input	

Note: The equivalent circuit diagrams may be simplified for explanatory purposes.

8. Absolute Maximum Rating

Table 8.1 Absolute Maximum Ratings

(T_a = -40 to 125 °C unless otherwise specified)

Characteristics	Symbol	Condition		Rating		Unit
Power supply voltage	V_{VM}			50		V
Input voltage	V_{IN}	VREG		-0.5 to 6	(Note 1)	V
		SPD		-0.5 to 6		V
		DIR, BRAKE, HU, HV, HW, ID		-0.5 to 6		V
		VMON		-0.5 to 6		V
		SCL, SDA		-0.5 to 6		V
		ISET		-0.5 to 6		V
		Differential between GND, PGND, SWGND		-0.5 to 0.5		V
Output voltage	V_{OUT}	U, V, W		-1 to V_{VM}+1	(Note 2)	V
		SW		-1 to V_{VM}+1	(Note 3)	V
		FG/RDO/SDA, ALERT		-0.5 to 6		V
Input current	I_{IN}	FG/RDO/SDA, ALERT		10		mA
Output current	I_{OUT}	U, V, W		5		A
		SW (DCDC mode)		100		mA
		SW (LDO mode)		20		mA
Power dissipation	P_D	TB67B030FNG	IC alone	0.42	(Note 4)	W
			JEDEC 2-layer board mounting	1.89	(Note 5)	W
			JEDEC 4-layer board mounting	3.47	(Note 6)	W
		TB67B030FTG	IC alone	0.61	(Note 7)	W
			JEDEC 2-layer board mounting	2.45	(Note 8)	W
			JEDEC 4-layer board mounting	4.45	(Note 9)	W
Junction temperature	$T_{j(max)}$	—		150		°C
Storage temperature	T_{stg}	—		-55 to 150		°C

Absolute Maximum Ratings

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant.
If any of these ratings would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage, and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions.
Before using, creating, and/or producing designs, refer to and comply with the precautions and conditions set forth in this document.

Note 1: VREG voltage should be the voltage generated by IC's DCDC.
Do not apply from an external power supply.
Note 2: The voltage of U/V/W is limited by the VM voltage.
(VM - U/V/W) and (U/V/W - PGND) should not exceed the range of -1 to 50 V.
Note 3: The voltage of SW is limited by the VM voltage.
(VM - SW) and (SW - SWGND) should not exceed the range of -1 to 50 V.
Note 4: When T_a exceeds 25 °C, derating at 3.4 mW/°C is required.
Note 5: When T_a exceeds 25 °C, derating at 15.1 mW/°C is required.
Note 6: When T_a exceeds 25 °C, derating at 27.8 mW/°C is required.
Note 7: When T_a exceeds 25 °C, derating at 4.9 mW/°C is required.
Note 8: When T_a exceeds 25 °C, derating at 19.6 mW/°C is required.
Note 9: When T_a exceeds 25 °C, derating at 35.6 mW/°C is required.

8.1. PD-Ta Graph (for Reference)

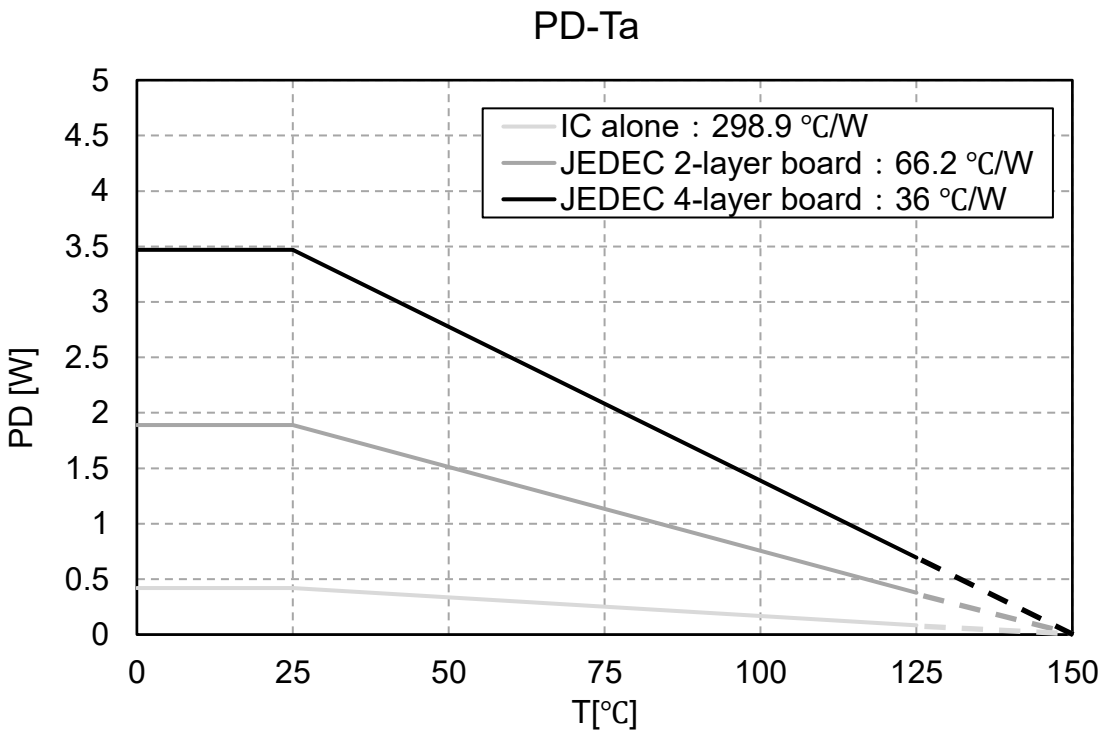


Figure 8.1 PD-Ta Graph for TB67B030FNG

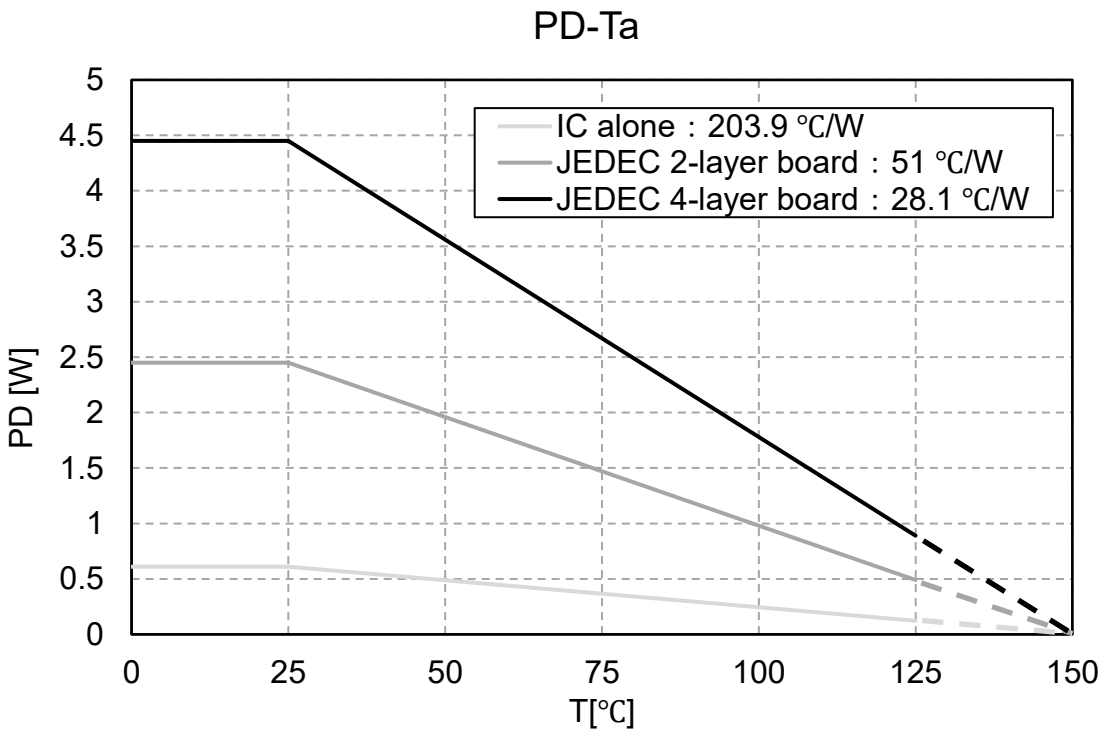


Figure 8.2 PD-Ta Graph for TB67B030FTG

9. Operation Ranges

Table 9.1 Operating Ranges

(T_a = -40 to 125 °C unless otherwise specified)

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Power supply voltage	V_{VM}	—	5.5	—	48	V
	V_{VM_NVM}	Program NVM	10.8	15	48	V
Output current	I_{OUT}	U, V, W	—	—	5	A
		SW (DCDC mode) (Note1)	—	—	80	mA
		SW (LDO mode) (Note1)	—	—	10	mA
Input voltage	V_{IN}	SPD, DIR, BRAKE, VMON, SCL, SDA	-0.3	—	5.5	V
		HU, HV, HW	-0.3	—	V_{VREG}	V
Pull-up voltage	V_{PU}	FG, RDO, ALERT, SDA	0	—	5.5	V
ISET voltage	V_{ISET}	—	0	—	4	V
Differential of GND pins	—	GND, PGND, SWGND	-0.1	—	0.1	V
SPD frequency	f_{SPD}	—	1	—	100	kHz
SCL frequency	f_{SCL}	—	—	—	400	kHz
Junction temperature	T_j	—	-40	—	125	°C

Note1: IC's current consumption included.

Table 9.2 NVM

Characteristics	Condition	Min	Typ.	Max	Unit
Program/Erase cycles	T_j = 25 °C	10	—	—	Cycle
Program/Erase time	V_{VM} = 15 V, T_j = 25 °C NVM_SAVE in progress	—	—	3.5	s

10. Electrical Characteristics

Table 10.1 Electrical Characteristics

(V_{VM} = 5.5 to 48 V, Tj = -40 to 125 °C unless otherwise specified)

Characteristics		Symbol	Condition	Min	Typ.	Max	Unit
Input current		I_{VM}	STBY release, V_{VM} = 24 V, DCDC mode SPD = 0 V, HU/HV/HW without Pull-up R	—	10	15	mA
			STBY release, V_{VM} = 24 V, LDO mode SPD = 0 V, HU/HV/HW without Pull-up R	—	19	24	mA
		I_{VM_STBY}	STBY mode, SPD = 0 V	—	10	20	μA
		I_{VREG}	STBY release, V_{VREG} = 5 V SPD = 0 V, HU/HV/HW without Pull-up	—	6	10	mA
Regulator voltage		V_{VREG}	DCDC mode, external load excluding IC: 0 to 80 mA, L_{SW} = 47 μH, C_{SW} = 10 μF	4.5	5	5.5	V
			LDO mode, external load excluding IC: 0 to 10 mA, R_{SW} = 39 Ω, C_{SW} = 10 μF	4.5	5	5.5	V
Internal OSC frequency		f_{OSC}	T_j = 25 °C	11.64	12	12.36	MHz
Output PWM frequency		f_{PWM}	f_{OSC} = 12 MHz, FPWM [2:0] = 000b	—	23.4	—	kHz
			f_{OSC} = 12 MHz, FPWM [2:0] = 001b	—	46.9	—	kHz
			f_{OSC} = 12 MHz, FPWM [2:0] = 010b	—	93.75	—	kHz
			f_{OSC} = 12 MHz, FPWM [2:0] = 011b	—	187.5	—	kHz
SPD							
STBY	Input voltage	V_{STBY_H}	Release threshold	—	1.2	1.4	V
		V_{STBY_L}	Transition threshold	0.8	1.0	—	V
		V_{STBY_HYS}	(Reference value)	—	200	—	mV
	Pulse width	t_{STBY_H}	STBY release pulse (Reference value)	150	—	—	ns
	Input current	I_{IN}	V_{IN} = 0 to 5 V	-1	—	1	μA
	Wake up time	t_{WAKE_UP} (Reference value)	From STBY release to Normal, L_{SW} = 47 μH, C_{SW} = 10 μF. I_{Load} = 0 to 80 mA	—	10	—	ms
			R_{SW} = 39 Ω, C_{SW} = 10 μF, I_{Load} = 0 mA	—	10	—	ms
PWM Duty	Input voltage	V_{IN_H}	High	2	—	5.5	V
		V_{IN_L}	Low	-0.3	—	0.8	V
		V_{IN_HYS}	(Reference value)	—	200	—	mV
	Input current	I_{IN}	V_{IN} = 0 to 5 V	-1	—	1	μA
Analog	Input voltage	V_{VSP_H}	ADC = 512 (100%)	3.9	4.0	4.1	V
		V_{VSP_L}	ADC = 0 (0%)	1.4	1.5	1.6	V
	Input current	I_{IN}	V_{IN} = 0 to 5 V	-1	—	1	μA
	Response time	t_{ADC}	—	—	—	10	ms
Logic Input							
DIR, BRAKE, VMON	Input voltage	V_{IN_H}	High	2	—	5.5	V
		V_{IN_L}	Low	-0.3	—	0.8	V
		V_{IN_HYS}	(Reference value)	—	200	—	mV
	Input current	I_{IN_H}	V_{IN} = 5 V	38	50	72	μA
		I_{IN_L}	V_{IN} = 0 V	-1	—	1	μA
	Pull-down resistor	R_{PD}	—	70	100	130	kΩ

Characteristics		Symbol	Condition	Min	Typ.	Max	Unit
Hall Signal Input							
HU, HV, HW	Input voltage	V_{IN_H}	High	2	—	5.5	V
		V_{IN_L}	Low	-0.3	—	0.8	V
		V_{IN_HYS}	(Reference value)	—	200	—	mV
	Input current	I_{IN}	Without Pull-up resistor, V_{IN} = 0 to 5 V	-1	—	1	μA
		I_{IN_L}	With Pull-up resistor, V_{IN} = 0 V	-1.1	-0.5	-0.3	mA
		I_{IN_H}	With Pull-up resistor, V_{IN} = V_{VREG}	-1	—	1	μA
	Pull-up resistor	R_{PU}	—	5	10	15	kΩ
Open Drain Output							
FG, ALERT	Output low voltage	V_{OUT_L}	I_{OUT} = 5 mA	—	0.15	0.3	V
	Output leakage current	I_{OUT_H}	V_{OUT} = 5 V	-1	—	1	μA
Address Setting Pin							
ID	Input voltage	V_{IN_H}	High	4	—	5.5	V
		V_{IN_M}	Middle	1.5	2.5	3.5	V
		V_{IN_L}	Low	-0.3	—	1.0	V
	Pull-up resistor	R_{PU}	—	30	50	70	kΩ
	Pull-down resistor	R_{PD}	—	30	50	70	kΩ
Motor Output Pin							
U, V, W	Output on resistor (H+L)	$R_{DS(H+L)}$	V_{VM} = 24 V, I_{OUT} = 0.2 A, T_j = 25 °C	—	0.3	0.43	Ω
			V_{VM} = 24 V, I_{OUT} = 0.2 A, T_j = 125 °C	—	0.4	—	Ω
	Switching characteristics (Reference value)	t_r	V_{VM} = 24 V, 10% to 90%, I_{OUT} = ±1 A OUT_SR [1:0] = 10b	—	350	—	V/μs
			V_{VM} = 24 V, 10% to 90%, I_{OUT} = ±1 A OUT_SR [1:0] = 01b	—	250	—	V/μs
			V_{VM} = 24 V, 10% to 90%, I_{OUT} = ±1 A OUT_SR [1:0] = 00b	—	150	—	V/μs
		t_f	V_{VM} = 24 V, 10% to 90%, I_{OUT} = ±1 A OUT_SR [1:0] = 10b	—	350	—	V/μs
			V_{VM} = 24 V, 10% to 90%, I_{OUT} = ±1 A OUT_SR [1:0] = 01b	—	250	—	V/μs
			V_{VM} = 24 V, 10% to 90%, I_{OUT} = ±1 A OUT_SR [1:0] = 00b	—	150	—	V/μs
DCDC							
VREG	Output voltage	V_{VREG}	DCDC mode, external load excluding IC: 0 to 80 mA, L_{SW} = 47 μH, C_{SW} = 10 μF	4.5	5	5.5	V
			LDO mode, external load excluding IC: 0 to 10 mA, R_{SW} = 39 Ω, C_{SW} = 10 μF	4.5	5	5.5	V
SW	Output on resistor	R_{DS}	V_{VM} = 24 V, U, V, W output stop	—	1	2	Ω
	PWM frequency	f_{DCDC}	f_{OSC} = 12 MHz	—	375	—	kHz

Characteristics		Symbol	Condition	Min	Typ.	Max	Unit
Serial I/F							
SCL, SDA	Input voltage	V_{IN_H}	High	2	—	5.5	V
		V_{IN_L}	Low	-0.3	—	0.8	V
		V_{IN_HYS}	(Reference value)	100	200	300	mV
	Input current (Note 1)	I_{IN}	V_{IN} = 0 to 5 V	-1	—	1	μA
	Output low voltage	V_{OUT_L}	I_{OUT} = 6 mA	—	—	0.4	V
	Output leakage current	I_{OUT_H}	SDA, V_{OUT} = 5 V	-1	—	1	μA
	Rise time	t_r	Input rise time	—	—	300	ns
	Fall time	t_f	Input fall time	—	—	300	ns
	Clock frequency	f_{SCL}	SCL clock frequency	0	—	400	kHz
	Clock Low time	t_{SCL_L}	SCL clock Low time	1.3	—	—	μs
	Clock High time	t_{SCL_H}	SCL clock High time	0.6	—	—	μs
	Data set-up time	t_{SU_DAT}	SDA data set-up time	100	—	—	ns
	Data hold time	t_{HD_DAT}	When IC is receiving (Note 2)	300	—	—	ns
		t_{DH}	When IC is transmitting	100	—	—	ns
	Data preparation time	t_{VD_DAT}	—	100	—	900	ns
	Noise filter	t_{mask}	(Reference value)	—	—	50	ns
	Capacity load	C_{LOAD}	Maximum permissible capacity (Reference value)	—	—	400	pF
Start Condition	Set-up time	t_{SU_S}	—	0.6	—	1000	μs
	Hold time	t_{HD_S}	—	0.6	—	—	μs
Stop Condition	Set-up time	t_{SU_P}	—	0.6	—	—	μs
	Bus free time	t_{BUF}	—	1.3	—	—	μs

Note 1: For current items, current flowing into the IC is indicated as positive, and current flowing out of the IC is indicated as negative.
Note 2: Considering the signal slew rate, please provide a hold time of 300 ns or more.

Characteristics		Symbol	Condition		Min	Typ.	Max	Unit
Circuit Protection Function								
Power supply voltage monitoring (VM)	VM undervoltage (UVLO) detection voltage	V_{VMUV_D}	When VM falls		4.5	4.8	5.1	V
	VM undervoltage (UVLO) release voltage	V_{VMUV_R}	When VM rises		4.8	5.1	5.4	V
	VM undervoltage (UVLO) detection hysteresis voltage	V_{VMUV_HYS}	—		—	300	—	mV
	Mask time	t_{MASK_VMUV}	f_{OSC} = 12 MHz		—	10	—	μs
	Overvoltage protection (OVP) detection voltage	V_{VMOV_D}	When VM rises	OVP_LVL [3:0] = 0000b	13.7	15.0	16.3	V
				OVP_LVL [3:0] = 1111b	41.7	45.0	48.3	V
	Overvoltage protection (OVP) release voltage	V_{VMOV_R}	When VM falls	OVP_LVL [3:0] = 0000b	12.3	13.5	14.7	V
				OVP_LVL [3:0] = 1111b	38.9	42.0	45.1	V
	OVP mask time	t_{MASK}	f_{OSC} = 12 MHz, Digital filter 6clk (Reference value)		—	500	—	ns
			f_{OSC} = 12 MHz, Digital filter 6clk (Reference value)		—	750	—	ns
VREG monitoring (DCDC)	Undervoltage (UVLO) detection voltage	V_{VREGUV_D}	When VREG falls		3.3	3.5	3.7	V
	Undervoltage (UVLO) release voltage	V_{VREGUV_R}	When VREG rises		3.5	3.7	3.9	V
	Undervoltage detection (UVLO) hysteresis voltage	V_{VREGUV_HYS}	—		—	200	—	mV
	Overvoltage (OVP) detection voltage	V_{VREGOV_D}	When VREG rises		5.55	5.75	6	V
	Overcurrent shutdown (ISD) detection current	I_{SW_ISD}	(Reference value)		—	1.25	—	A
Output current limit (OCL)	ISET current gain	G_{ISET}	—		—	50	—	μA/A
	ISET current accuracy	ΔI_{SET}	I_{Total} ≥ 1A, T_j = -40 to 125 °C		-10	—	10	%
			I_{Total} < 1A, T_j = -40 to 125 °C		-5	—	5	μA
	OCL detection voltage	V_{OCL}	OC_VTH = 0b00		1.65	1.75	1.85	V
			OC_VTH = 0b11		2.4	2.5	2.6	V
	OCL mask time	t_{MASK}	f_{OSC} = 12 MHz, Digital filter 6clk (Reference value)		—	500	—	ns
			f_{OSC} = 12 MHz, Digital filter 6clk (Reference value)		—	750	—	ns
Overcurrent shutdown (ISD)	ISD detection current	I_{ISD}	(Reference value)		—	6.4	—	A
	ISD mask time	t_{MASK}	f_{OSC} = 12 MHz, Digital filter 6clk (Reference value)		—	500	—	ns
			f_{OSC} = 12 MHz, Digital filter 6clk (Reference value)		—	750	—	ns
Thermal shutdown (TSD)	TSD detection temperature	T_{TSD_D}	When temperature rises (Reference value)		—	165	—	°C
	TSD release temperature	T_{TSD_R}	When temperature falls (Reference value)		—	135	—	°C
	TSD detection hysteresis temperature	T_{TSD_HYS}	(Reference value)		—	30	—	°C

Note: For current items, current flowing into the IC is indicated as positive, and current flowing out of the IC is indicated as negative.
Items marked (Reference value) are design guaranteed and are not tested at the time of product shipment.

11. Functional Description

11.1. Pin Description

11.1.1. VM

The VM pin is a power supply voltage input pin with an operating voltage range of 5.5 to 48 V.
External capacitors must be connected to the VM pin. A 0.1 µF ceramic capacitor and a 10 to 47 µF electrolytic capacitor are recommended.

11.1.2. U, V, W

U, V, and W are motor drive output pins.
The configuration consists of three half-bridges, and each half-bridge has an Nch+Nch structure.
The charge pump circuit and capacitor for high-side Nch MOSFET drive are built into the IC.
The output slew rate is selectable (150 / 250 / 350 V/µs) by register setting.
The default is 350 V/µs, and the dead time is automatically switched accordingly.

Table 11.1 Output Slew Rate Setting

Register: 12[7:6] OUT_SR	Slew rate target value (V/µs)	Dead Time (ns)
00b (Default)	150	566 (7clk)
01b	250	404 (5clk)
10b	350	323 (4clk)
11b	Don’t use	Don’t use

11.1.3. ISET

The ISET pin is used for current monitoring and output current limit (OCL) detection.
A small current proportional to the total current flowing from drain to source of the low-side MOSFETs is output from the ISET pin.
By connecting an external resistor to the ISET pin, a voltage is generated. When the voltage at the ISET pin exceeds the internal reference voltage, it is detected as a OCL condition.
An external resistor in the range of 10 kΩ to 20 kΩ is recommended.
To improve current detection accuracy, it is recommended to use a resistor with a tolerance of ±1% or less.

11.1.4. SPD

The SPD pin is used to control motor start/stop and rotation speed.
The type of signal input to the SPD pin can be selected between a PWM duty signal and an analog voltage signal using the register. The polarity of the signal can also be set with the register.
The SPD command can also be input directly from the serial I/F. In this case, the input voltage or Duty signal at the SPD pin is ignored.
Switching between STBY mode and normal mode is controlled by the SPD pin.
Applying a Low-level voltage to the SPD pin places the device into STBY mode, while applying a High-level voltage releases STBY mode.
The SPD pin is also shared as the serial interface clock input (SCL).

Table 11.2 Setting of SPD Input

Register: 1[7:6] SPD_SEL	SPD command type
00b (Default)	Analog voltage from SPD pin
01b	PWM Duty signal from SPD pin
10b, 11b	Setting via register Address39:38 SPD [9:0]

Note: When setting the SPD command via register, the 10-bit SPD data is stored as follows: the upper 8 bits at Address 38, and the lower 2 bits at Address 39. Since data written to each address is reflected immediately, the SPD value may temporarily differ from the target value during the update. As a result, the motor may momentarily stop or start unintentionally. Please take care when writing these values.

Table 11.3 Signal Polarity of SPD

Register: 1[5] SPD_INV	Analog voltage	PWM Duty
0b (Default)	SPD command = AD value V_{VSP_L} → SPD command = 0 (0%) V_{VSP_H} → SPD command = 512 (100%)	High active
1b	SPD command = 512 - AD value V_{VSP_L} → SPD command = 512 (100%) V_{VSP_H} → SPD command = 0 (0%)	Low active

Note: When a voltage in the range of 0.8 V (V_{STBY_L}) to 1.4 V (V_{STBY_H}) is applied to the SPD pin, leakage current may occur.
Therefore, please avoid allowing the voltage at the SPD pin to remain within this range during operation.

11.1.5. DIR

The DIR pin controls the forward (CW) and reverse (CCW) rotation of the motor. The High/Low and rotation direction relationship of the DIR pin can be set by the register.

Table 11.4 Motor Rotation Direction

Register: 1[4] DIR_INV	DIR pin	Motor rotation direction
0b (Default)	L	CW (U→V→W)
	H	CCW (W→V→U)
1b	L	CCW (W→V→U)
	H	CW (U→V→W)

11.1.6. BRAKE

The BRAKE pin controls the short brake operation. The relationship between the High/Low of the BRAKE pin and the operation can be set by the register.

Table 11.5 Brake Operation Control

Register: 1[3] BRK_INV	BRAKE pin	Output
0b (Default)	L	Normal operation
	H	Brake operation
1b	L	Brake operation
	H	Normal operation

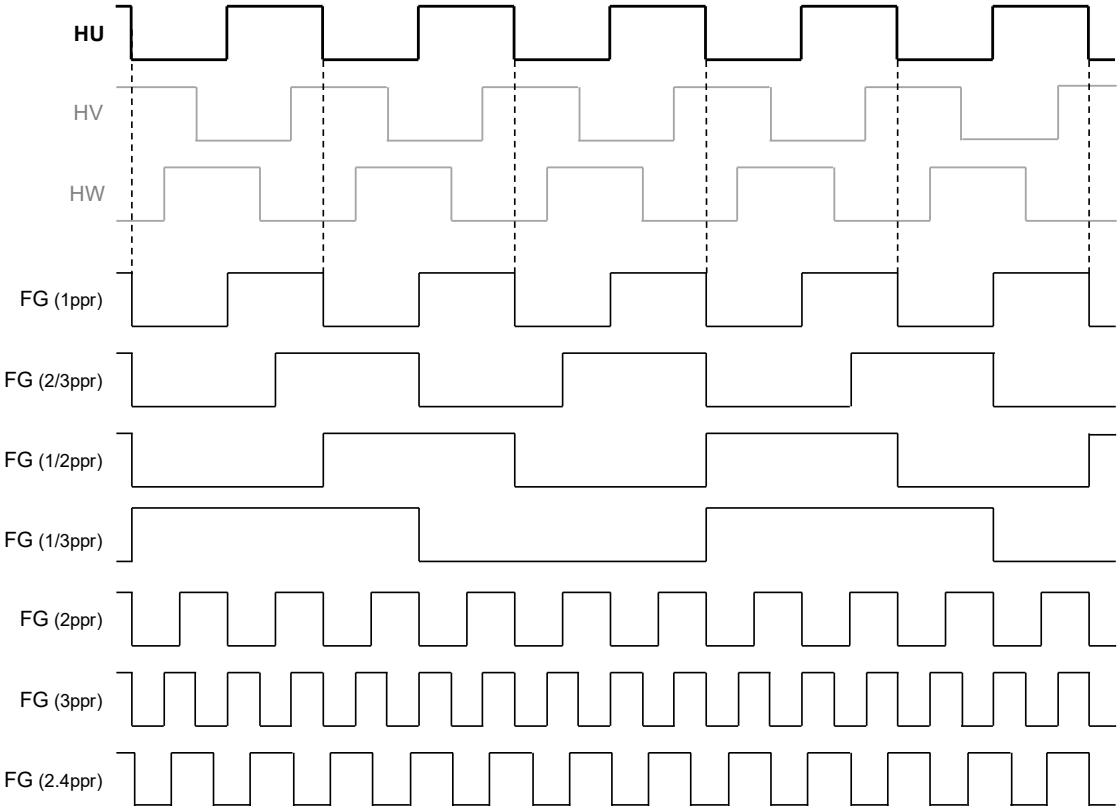
In brake(short-brake) operation, all low-side MOSFETs of the three-phase bridges are turned ON.
OCL is active during brake operation. When OCL is detected, the outputs are turned OFF and automatically restored by internal PWM control. If OVP is detected during OCL operation, all outputs are turned OFF, and short-brake operation resumes after OVP release.

11.1.7. FG

The FG pin is an open drain output. The motor speed signal can be output from the FG pin.
The FG signal can be selected from 1 ppr, 3 ppr, 2.4 ppr, 1/2 ppr, etc. The table below shows the number of FG pulses output in one rotation of the motor.
RDO signal can also be output from FG pin in case of start failure, lock detection (3-Hall, 1-Hall), or minimum speed error detection (sensorless) by setting the register. When an abnormality is detected, the output goes Low.

Table 11.6 FG Setting and The Pulses Output in One Motor Rotation

Register 2[7:5] FG_SEL	FG signal	Motor's pole					
		2 poles	4 poles	6 poles	8 poles	10 poles	12 poles
000b (Default)	1 ppr	1	2	3	4	5	6
001b	2/3 ppr	2/3	4/3	2	8/3	10/3	4
010b	1/2 ppr	1/2	1	3/2	2	5/2	3
011b	2 ppr	2	4	6	8	10	12
100b	3 ppr	3	6	9	12	15	18
101b	2.4 ppr	2.4	4.8	7.2	9.6	12	14.4
110b	1/3 ppr	1/3	2/3	1	4/3	5/3	2
111b	RDO signal						



Note: The timing chart is simplified for the purpose of explaining functions and operations.

Figure 11.1 FG Signal Timing Chart during Closed/Open Loop Operation

Table 11.7 FG Output Except During Closed/Open Loop

FG Signal Setting	Sensorless			3-Hall			1-Hall		
	Forward free-run	Reverse free-run	Startup	Forward free-run	Reverse free-run	Startup	Forward free-run	Reverse free-run	Startup
1 ppr	1 ppr	1/5 ppr	1 ppr	1 ppr	1 ppr	1 ppr	1 ppr	1 ppr	1 ppr
2/3 ppr	- (Note 1)			2/3 ppr	2/15 ppr	2/3 ppr	2/3 ppr	2/3 ppr	2/3 ppr
1/2 ppr	1/2 ppr	1/10 ppr	1/2 ppr	1/2 ppr	1/10 ppr	1/2 ppr	1/2 ppr	1/2 ppr	1/2 ppr
2 ppr	- (Note 1)			2 ppr	2/5 ppr	2 ppr	2 ppr	2 ppr	2 ppr
3 ppr	3 ppr	3/5 ppr	3 ppr (Note 2)	3 ppr	3 ppr	3 ppr	3 ppr	3 ppr	3 ppr
2.4 ppr	- (Note 1)			2.4 ppr	0.48 ppr	2.4 ppr	2.4 ppr	2.4 ppr	2.4 ppr
1/3 ppr	- (Note 1)			1/3 ppr	1/15 ppr	1/3 ppr	1/3 ppr	1/3 ppr	1/3 ppr

Forward free-run: The state in which the motor rotates in the forward direction (same as the DIR setting) while the output is stopped.

Reverse free-run: The state in which the motor rotates in the reverse direction (opposite to the DIR setting) while the output is stopped.

Note 1: When the FG signal is set to [2/3 ppr, 2 ppr, 2.4 ppr, 1/3 ppr], unintended pulses may occur in the FG output during periods other than normal rotation (Closed/Open loop), which may prevent accurate speed detection. Therefore, when using [2/3 ppr, 2 ppr, 2.4 ppr, 1/3 ppr] settings, it is recommended to output the FG signal only during normal rotation (FG_ON = 000b).

Note 2: In sensorless mode, when starting from a stopped state or from forward free-run, the FG signal is output at 3 ppr.
When starting from the reverse free-run state, the motor is first decelerated by DC excitation, then restarted with soft start after stopping. Until normal rotation (Closed/Open loop) is reached, the FG signal is output according to the soft start/brake settings in FG_ON. However, when set to 3 ppr, the output is 1 ppr.

The FG pin also functions as the serial interface data input/output pin (SDA). For serial communication, the FG pin is set to a Hi-Z state when the motor's rotation speed is lower than the forced commutation frequency (f_{FORCE}).

Table 11.8 Forced Commutation Frequency

Register: 10[7:6] FST	Forced commutation frequency f_{FORCE} (Hz)
00b (Default)	1.6
01b	3.2
10b	6.4
11b	12.8

By register settings, the FG pin can be fixed to a Hi-Z state according to the IC status.

Table 11.9 FG Output

Register 2[4:2] FG_ON	Closed loop /Open loop	Brake(Note 2) Soft start(Note 3)	Idle mode Wait sequence(Note 4) (No SPD command)	OFF mode 1/2/3
000b (Default)	Output enabled(Note 1)	Hi-Z	Hi-Z	Hi-Z
001b	Output enabled(Note 1)	Hi-Z	Hi-Z	Output enabled(Note 1)
010b	Output enabled(Note 1)	Output enabled(Note 1)	Hi-Z	Hi-Z
011b	Output enabled(Note 1)	Output enabled(Note 1)	Hi-Z	Output enabled(Note 1)
100b	Output enabled(Note 1)	Output enabled(Note 1)	Output enabled(Note 1)	Hi-Z
101b	Output enabled(Note 1)	Output enabled(Note 1)	Output enabled(Note 1)	Output enabled(Note 1)
110b	Hi-Z	Hi-Z	Hi-Z	Hi-Z
111b	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Note 1: Even in the output-enabled state, the FG pin becomes Hi-Z when the motor rotation speed is at or below the forced commutation frequency.
Note 2: During sensorless control, the FG pin is fixed to Hi-Z during the following periods:
- During short brake operation
- During power-off brake operation
- During transition from the stopped state to the startup sequence, and during the DC excitation period

Note 3: The soft start period includes the DC excitation and forced commutation sequences. However, during DC excitation, the motor is determined to be in the stopped state, so the FG pin is set to Hi-Z.
Note 4: FG output during Wait Sequence:
- Sensor control: FG output enabled
- Sensorless control: FG output enabled only when FG_OFF is set

Regardless of the FG_ON bit setting, the IC stops outputting the FG signal from the FG pin during the period from the detection of the Start Condition to the detection of the Stop Condition in serial communication.
During this period, the FG pin functions as a dedicated SDA signal pin.

When the FG pin is set to the RDO output, the FG pin may be held Low depending on the IC status, and communication may not be possible. Please refer to the FG_PORT setting when using this function.

Table 11.10 FG Pin Output Setting

Register: 2[1] FG_PORT	FG Pin	ALERT Pin
0b (Default)	FG signal / RDO signal (According to FG_SEL and FG_ON settings)	ALERT signal (According to ALERT related settings)
1b	Hi-Z fixed	FG signal / RDO signal (According to FG_SEL and FG_ON settings)

11.1.8. ALERT

The ALERT pin is an open drain output. When various abnormal conditions are detected, a signal is output from the ALERT pin.
The ALERT output is released after the device is shifted to Open loop/Closed loop.
In automatic recovery mode, the error flag is cleared automatically upon recovery from an error.
In latch mode, the error flag is cleared automatically after the latch is released and the device recovers from the error.

Table 11.11 Error Flag

Addr	D7	D6	D5	D4	D3	D2	D1	D0
0	VM_UVLO	VM_OVP	ISD	TSD	LOCK	ST_FAIL	UD_SPD	OV_SPD
	0b: Normal (Default), 1b: Fault							

The types of abnormal conditions output from the ALERT pin can be configured with register settings.

Table 11.12 Abnormal Conditions Output

Addr	D7	D6	D5	D4	D3	D2	D1
3	ALT_UVLO	ALT_OVP	ALT_ISD	ALT_TSD	ALT_LOCK	ALT_OVS	REP_HSPD
	0b: Do not output. However, reflected in error flag (Default), 1b: Output. Reflected in error flag						

Please refer to the table below for the detail relationship between error flag and abnormal conditions output.

Table 11.13 Relationship between Error Flag and Abnormal Conditions Output

Abnormal condition	Error flag	ALERT output
VM undervoltage lock out	VM_UVLO	ALT_UVLO
VM overvoltage protection	OVP	ALT_OVP
Overcurrent shutdown	ISD	ALT_ISD
Thermal shutdown	TSD	ALT_TSD
Motor lock detection	LOCK	ALT_LOCK
Startup failure	ST_FAIL	
Under speed detection	UD_SPD	
Over speed detection	OV_SPD	ALT_OVS
High speed limit	—	REP_HSPD

Register settings allow the polarity of the ALERT signal to be set.

Table 11.14 Signal Polarity of ALERT Output

Register: 3[0] ALERT_INV	ALERT output after detection
0b (Default)	Low
1b	Hi-Z

11.1.9. HU/ HV/ HW

HU/HV/HW are Hall signal input pins. Please input Hall IC signals.
The built-in pull-up resistor can be enabled/disabled by setting the register.

Table 11.15 Built-in Pull-up Resistor

Register: 1[0] HALL_PU	HALL_PU	Built-in pull-up resistor
0b (Default)	0	Disable
1b	1	Enable

The polarity of the Hall IC signals can be inverted by register settings.

Table 11.16 Signal Polarity of Hall IC

Register: 1[1] HALL_INV	Hal IC signal polarity inversion
0b (Default)	Positive logic
1b	Negative logic

11.1.10. VMON

This pin is used for power off monitor. Please generate the input voltage by dividing the external power supply using resistors.
For details, refer to “Power Off Brake.”
If the power off brake function is not used, short the VMON pin to GND.

11.1.11. Serial I/F

The clock input pin (SCL) of the serial I/F is also used as the SPD pin. The data input/output pin (SDA) of the serial I/F serves also as the FG pin.
The ID pin can be used to set the address of the serial I/F.

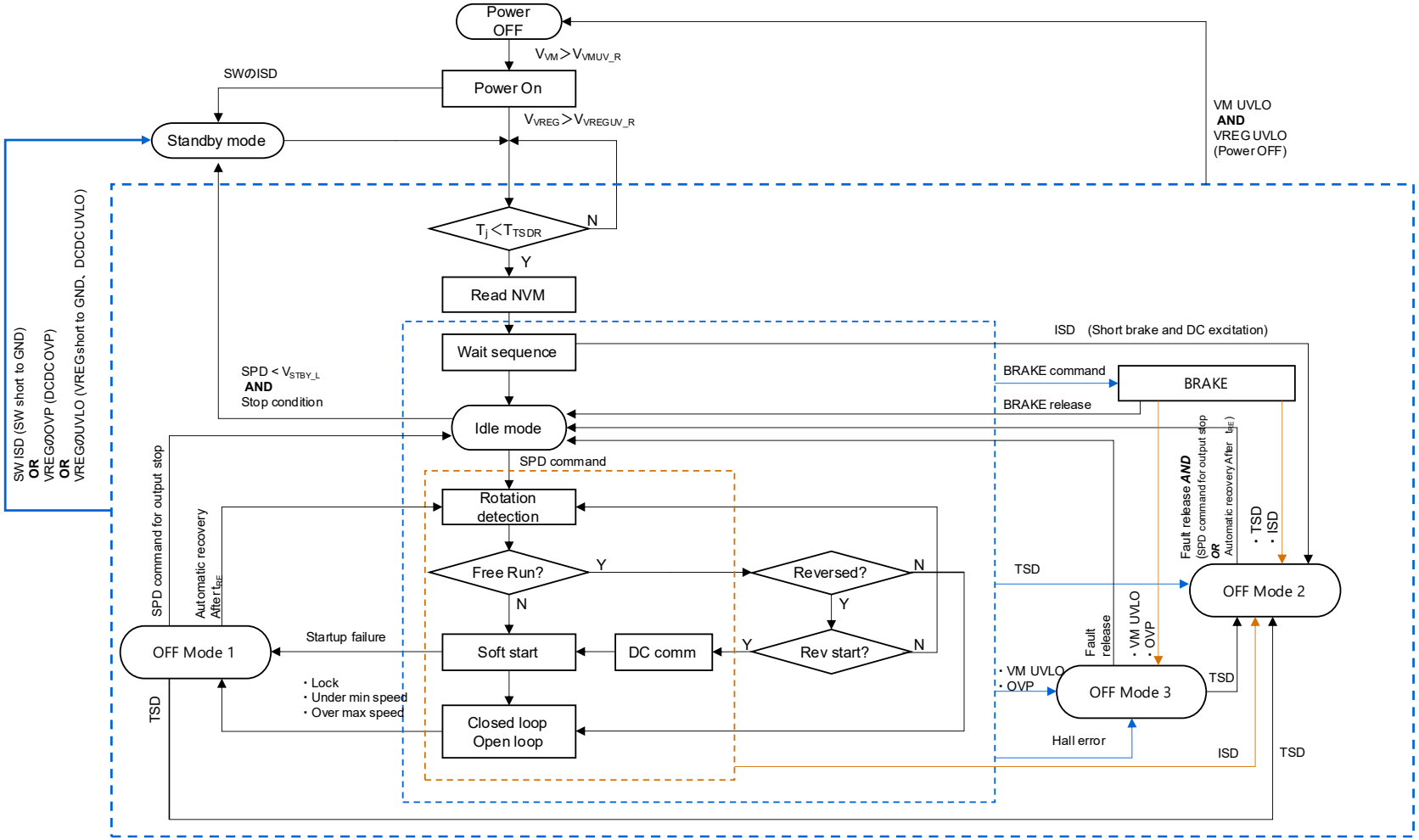
Table 11.17 Setting of the IC Address

ID	IC Address
Low (Short with GND)	IC_ADDR17 [6:0] 0101001b (Initial)
Open	0110010b
High (Short with VREG)	0101001b

Note: Do not apply a voltage to the ID pin from any power supply other than VREG.
Set the state of the ID pin before starting serial communication, and do not change the ID pin state during communication.

11.2. Basic Operation

11.2.1. Flow Chart and Status Transitions



Note: The flow chart is simplified for explanatory purposes of functions and operations.

Figure 11.2 Basic Operation Flow

11.2.2. IC Condition for Each State

Table 11.18 Block/Function for Each IC condition

Condition	Description	Each block / Function							
		Internal 5V	DCDC	FG	RDO	ALERT	Serial I/F	Register	U/V/W
Standby	Standby	Stop	Stop	Hi-Z	-	Hi-Z	Not allowed	Undefined R/W not allowed	Hi-Z
UVLO	Internal power supply startup	Startup	Startup	Hi-Z	-	Hi-Z	Not allowed	RESET R/W not allowed	Hi-Z
TSD wait	At startup, T_j is at or above TSD detection temperature	5V	Operate	Low fixed	-	Hi-Z	Not allowed	RESET R/W not allowed	Hi-Z
NVM read	NVM reading	5V	Operate	Low fixed	-	Hi-Z	Not allowed	Updating R/W not allowed	Hi-Z
Idle mode	Output stopped Waiting for SPD command	5V	Operate	Hall output[Note2,3]	Hi-Z[Note2]	State maintained	Allowed[Note1]	R/W OK	Hi-Z
Normal	Motor driving	5V	Operate	Hall output[Note2]	Hi-Z[Note2]	Fault output available	Allowed[Note1]	R/W allowed	Output allowed
PWM OFF	After fault detection[Note4] OCL	5V	Operate	Hall output	Hi-Z[Note2]	State maintained	Allowed[Note1]	R/W allowed	Hi-Z
OFF mode 1	After fault detection Lock, OV_SPD, UD_SPD, ST_FAIL	5V	Operate	Hi-Z fixed[Note3]	Hi-Z (OV_SPD) Low fixed (Others)	Fault output	Allowed[Note1]	R/W allowed	Hi-Z
OFF mode 2	After fault detection TSD, ISD	5V	Operate	Hi-Z fixed[Note3]	Hi-Z[Note2]	Fault output	Allowed[Note1]	R/W allowed	Hi-Z
OFF mode 3	After fault detection VM_UVLO, OVP Hall signal fault	5V	Operate	Hi-Z fixed[Note3]	Hi-Z[Note2]	Fault output	Allowed[Note1]	R/W allowed	Hi-Z

Note 1: Operation depends on the states of SPD and FG.
Note 2: After OFF mode 1, when rotation detection is completed in Open/Closed loop, the Hi-Z fixed state of FG and the Low fixed state of RDO are released, and output operation resumes.
Note 3: The state of FG can be configured by the FG_ON register.
Note 4: This operation applies when ALL OFF is selected after OCL detection.

11.2.3. Standby Mode

Standby mode is disabled by default. To enable it, register configuration is required.

Table 11.19 Standby Mode

Register: 2[0] STBY	Standby mode
0b (Default)	Disabled
1b	Enabled

When Standby mode is enabled, the device transitions to Standby mode when both of the following conditions are satisfied:

1. The voltage at the SPD pin is equal to or lower than V_{STBY_L}
2. The motor has remained in the stopped state for longer than T_{ON}

The motor stopped state for Standby mode transition is defined as follows:

- 1-Hall / 3-Hall: The frequency of the Hall signals is 1 Hz or lower.
- Sensorless: The motor speed is equal to or lower than the forced commutation frequency (f_{FORCE}) (UD_SPD / Under speed detection).

During serial communication, T_{ON} counting is stopped and the counter is cleared. After the motor enters the stopped state, T_{ON} counting restarts.

Table 11.20 Forced Communication Frequency

Register: 10[7:6] FST	Forced communication frequency f_{FORCE} (Hz)
00b (Default)	1.6
01b	3.2
10b	6.4
11b	12.8

11.2.4. Wait Sequence

The operation during the wait sequence and the wait time can be configured by register settings.
In addition, the state to which the device transitions after completion of the wait sequence can also be configured by register settings.

Table 11.21 Time Setting of Wait Sequence

Register: 7[7:5] WAIT_TIME	Wait sequence time (s)
000b (Default)	0 (No wait sequence)
001b	1
010b	2
011b	3
100b	4
101b	5
110b	6
111b	7

Table 11.22 Operation during Wait Sequence

Register: 7[3] WAIT_MODE	Drive mode	Output state
0b (Default)	Don't care	OFF (Hi-Z)
1b	Don't care	Short brake

Table 11.23 State after Wait Sequence

Register: 7[2] WAIT_CON	State
0b (Default)	After the wait sequence time has elapsed, the WAIT_MODE state is released, and the output stage enters Hi-Z. However, if an SPD command is present, the device starts from the last state.
1b	The WAIT_MODE state is maintained even after the Wait sequence time has elapsed. After an SPD command, the device starts from the last state. When WAIT_TIME = 0, this setting is disabled.

11.2.5. Idle Mode

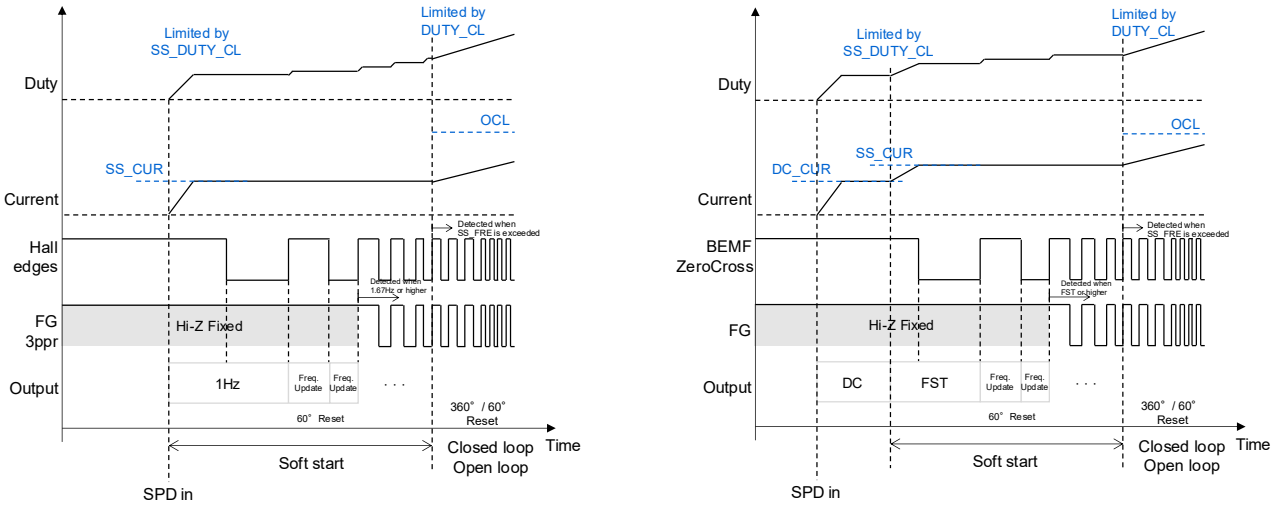
When a speed control command for output stop is issued during normal rotation or during OFF mode 1/2, the device transitions to Idle mode.
In Idle mode, all U/V/W output stages are turned OFF.
When a speed control command to resume output is detected during Idle mode, the device transitions to the startup sequence.

11.2.6. Startup Sequence

The motor stopped state is defined as follows:

- 1-Hall / 3-Hall: The frequency of the Hall signals is 1 Hz or lower
- Sensorless: The BEMF frequency is equal to or lower than the free-run detection frequency (f_{ROTDET})

When the motor starts from the stopped state, the device performs a soft start operation.
The output duty is increased gradually from 0% (SS_DUTY_CL).
During Soft start, the output duty is limited so that the output current does not exceed the start-up current (SS_CUR, or DC_CUR when DC excitation is used).
Once the start-up current level is reached, the output duty is held, and duty increase resumes at the timing of waveform reset or energized phase switching.
When the rotation frequency reaches SS_FREQ, the soft start operation is completed, and the device transitions to normal rotation control.



Note: The timing charts are simplified for explanatory purposes of functions and operations.

Figure 11.3 Startup Sequence Image of 3-Hall (left) and Sensorless (right)

Table 11.24 Startup Current

Register: 9[4:2] SS_CUR	Startup current
000b (Default)	OCL_VTH x 12.5%
001b	OCL_VTH x 25.0%
010b	OCL_VTH x 37.5%
011b	OCL_VTH x 50.0%
100b	OCL_VTH x 62.5%
101b	OCL_VTH x 75%
110b	OCL_VTH x 87.5%
111b	OCL_VTH x 100%

Table 11.25 Time of DC Excitation

Register: 10[2:0] TIP	Time (s)
000b (Default)	0.1
001b	0.2
010b	0.4
011b	0.6
100b	0.8
101b	1
110b	1.5
111b	2

Table 11.26 Acceleration / Deceleration Rate During Soft Start

Register: 11[7:5] SS_DUTY_CL	Duty change per 2.7 ms	Time (s) (0 to 512)
000b (Default)	2/8	5.53
001b	3/8	3.69
010b	5/8	2.21
011b	8/8	1.38
100b	15/8	0.74
101b	25/8	0.44
110b	40/8	0.28
111b	64/8	0.17

Table 11.27 Soft Start Switching Frequency

Register: 9[7:5] SS_FREQ	Frequency (Hz)
000b (Default)	2
001b	4
010b	6
011b	8
100b	10
101b	12
110b	14
111b	16

Table 11.28 DC Excitation Current

Register: 10[4:3] DC_CUR	DC excitation current
00b (Default)	SS_CUR x 25%
01b	SS_CUR x 50%
10b	SS_CUR x 75%
11b	SS_CUR x 100%

Table 11.29 Forced Commutation / Free-run Detection Frequency

Register: 10[7:6] FST	Forced commutation f_{FORCE} (Hz)	Free-run detection f_{ROTDET} (Hz)
00b (Default)	1.6	5
01b	3.2	10
10b	6.4	20
11b	12.8	40

For sensorless operation, if the soft start switching frequency is lower than the forced commutation frequency, the frequency is automatically increased.

Table 11.30 Automatic Soft Start Switching Frequency Correction (Sensorless)

Register: 10[7:6] FST	Forced commutation f_{FORCE} (Hz)	Register: 9[7:5] SS_FREQ	Soft start switching frequency (Hz)
00b (Default)	1.6	Don't care	Not change
01b	3.2	000b	2 → 4
10b	6.4	000b	2 → 8
		001b	4 → 8
		010b	6 → 8
11b	12.8	000b	2 → 14
		001b	4 → 14
		010b	6 → 14
		011b	8 → 14
		100b	10 → 14
		101b	12 → 14

Table 11.31 Hysteresis Voltage of the Position Detection Comparator During Free-run Detection

Register: 11[1:0] COMP_HYS	Hysteresis voltage (mV)
00b (Default)	None
01b	± 100
10b	± 200
11b	± 300

11.2.7. Drive Mode

TB67B030FNG/FTG can support the following drive modes.
Please configure SEN_TYPE according to WAVE_TYPE.

Table 11.32 Settings of Sensor Type

Register: 17[7] SEN_TYPE	Sensor setting
0b (Default)	With sensor
1b	Sensorless

Table 11.33 Available Drive Modes

Register: 8[7:4] WAVE_TYPE	Position Detection	Drive type	Motor wiring type	Soft switching (Note)	Reset	Lead angle control
0000b (Default)	3-Hall	120°	—	None	60°	No
0001b	sensorless	Sine wave	—	—	360°	Yes
0010b	sensorless	Sine wave	—	—	60°	Yes
0011b	sensorless	150°	—	15° each front and back	60°	Yes
0100b	1-Hall	Sine wave	Y	—	360°	Yes
0101b	1-Hall	Sine wave	Δ	—	360°	Yes
0110b	1-Hall	Sine wave	Y	—	180°	Yes
0111b	1-Hall	Sine wave	Δ	—	180°	Yes
1000b	3-Hall	Sine wave	Y	—	60°	Yes
1001b	3-Hall	Sine wave	Δ	—	60°	Yes
1010b	3-Hall	Sine wave	Y	—	360°	Yes
1011b	3-Hall	Sine wave	Δ	—	360°	Yes
1100b	1-Hall	150°	Y	15° each front and back	360°	Yes
1101b	1-Hall	150°	Δ	15° each front and back	360°	Yes
1110b	3-Hall	150°	Y	15° each front and back	60°	Yes
1111b	3-Hall	150°	Δ	15° each front and back	60°	Yes

Note: The soft switching function refers to an operation in which the output PWM duty changes stepwise during output energization switching, enabling a smooth transition between conduction states.
Depending on the motor characteristics, the efficiency and noise performance may vary by adjusting the drive type and the advance angle settings.

Table 11.34 Phase Relationship Between Hall Signals and Back-EMF

Motor wiring type	Phase relationship	
Y	CW	150° lead
	CCW	30° lead
Δ	CW	180° lead
	CCW	0° lead

11.2.8. Setting for Motor Pole Pairs and Rotation Speed

For functions controlled in terms of rotational speed [rpm], such as speed control, the electrical angular frequency is converted to rotational speed [rpm] based on the motor pole pair setting (POLE_PAIR).

Rotation speed [rpm] = Electrical angular frequency [Hz] × (60 [s] / Number of motor pole pairs)

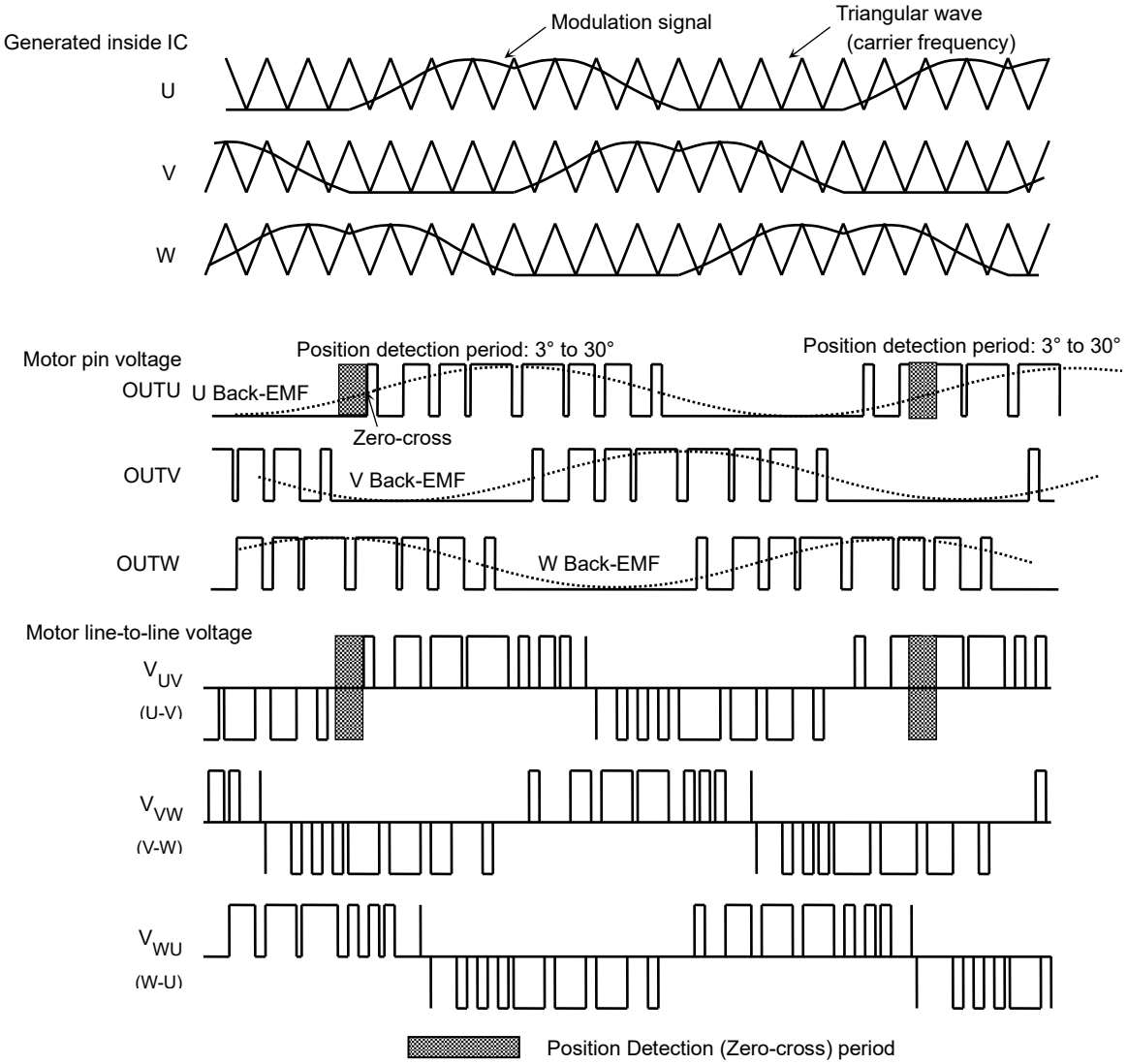
Table 11.35 Setting for Motor Pole Pairs

Register: 18[7:5] POLE_PAIR	Motor pole pairs
000b (Default)	1
001b	2
010b	3
011b	4
100b	5
101b	6
110b	7
111b	8

11.2.9. Timing Chart by Drive Mode

11.2.9.1. Sensorless Sine Wave Drive

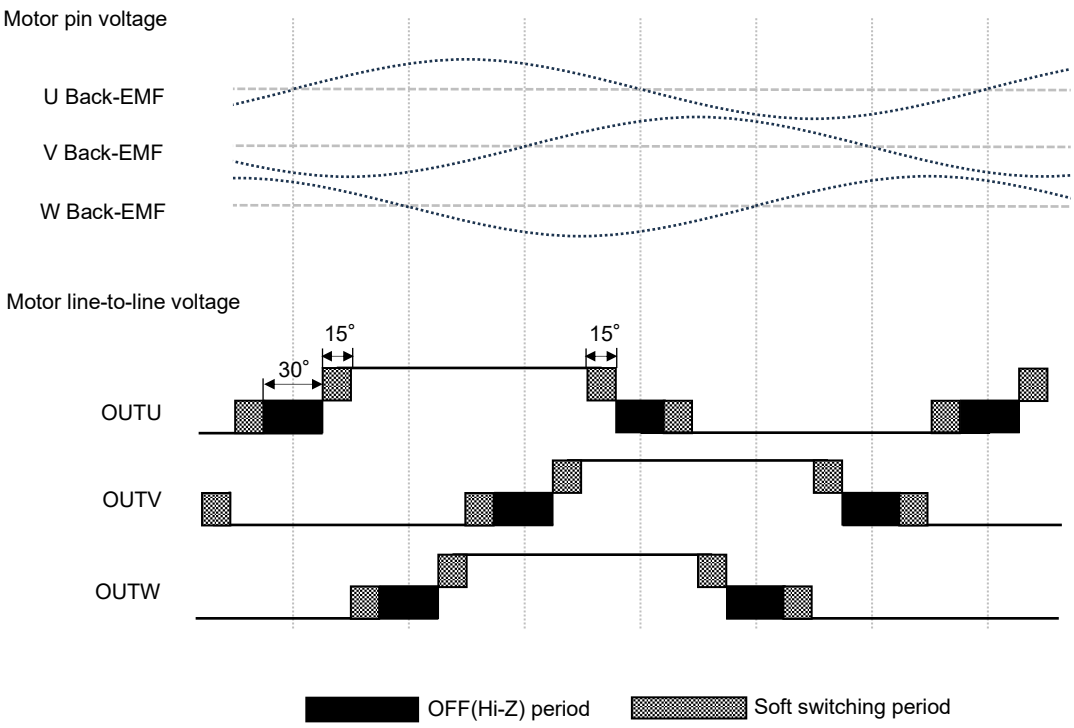
During the sine wave drive, the rising zero-cross of the U-phase back-EMF is used for position detection. The drive is turned OFF during that period.



Note: The timing charts are simplified for explanatory purposes of functions and operations.

Figure 11.4 Timing Chart of Sensorless Sine Wave Drive

11.2.9.2. Sensorless 150° Drive



Note: The timing charts are simplified for explanatory purposes of functions and operations.

Figure 11.5 Timing Chart of Sensorless 150° Drive

11.2.9.3. 1-Hall, 3-Hall Drive

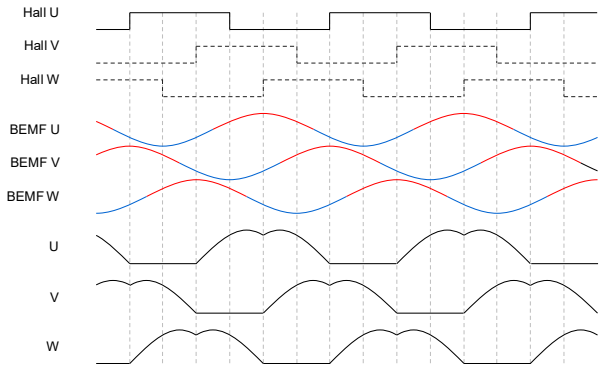


Figure 11.6 Wye Connection Sine Wave CW

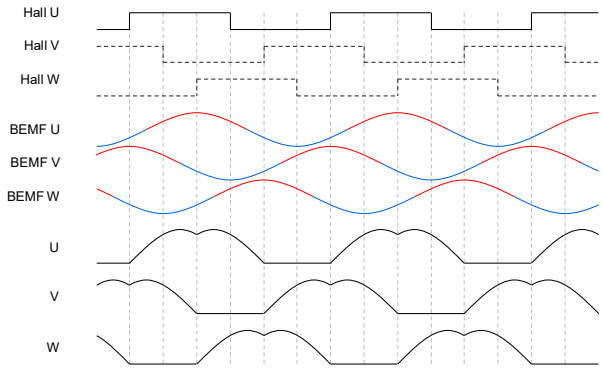


Figure 11.7 Wye Connection Sine Wave CCW

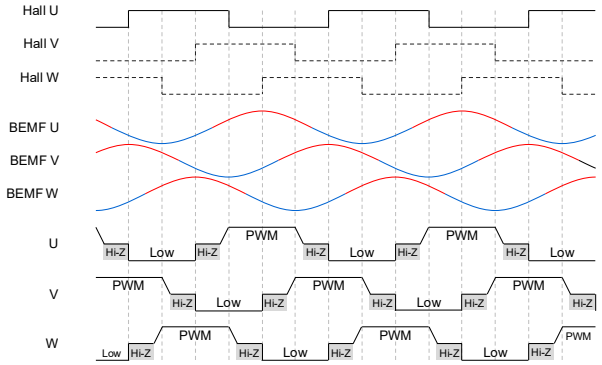


Figure 11.8 Wye Connection 150° CW

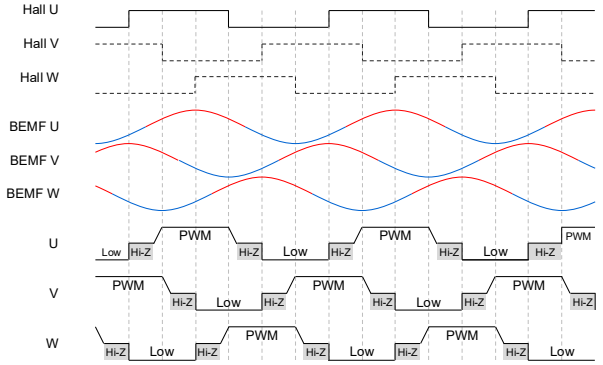


Figure 11.9 Wye Connection 150° CCW

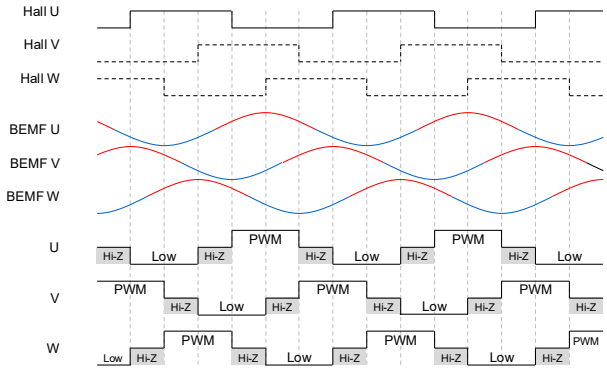


Figure 11.10 Wye Connection 120° CW

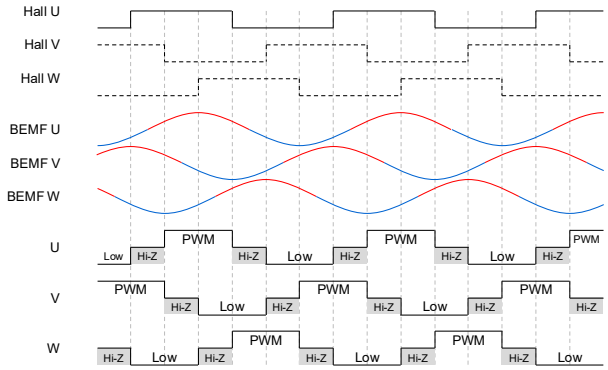


Figure 11.11 Wye Connection 120° CCW

Note: The timing charts are simplified for explanatory purposes of functions and operations.

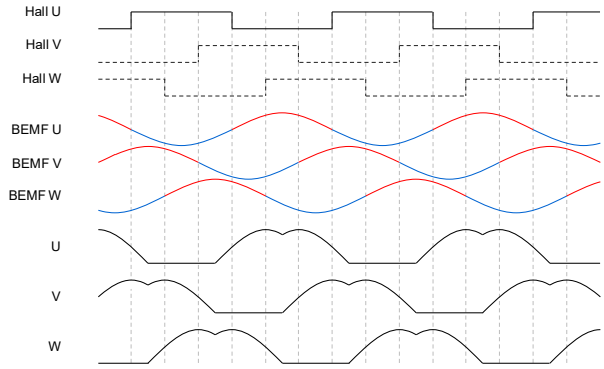


Figure 11.12 Delta Connection Sine Wave CW

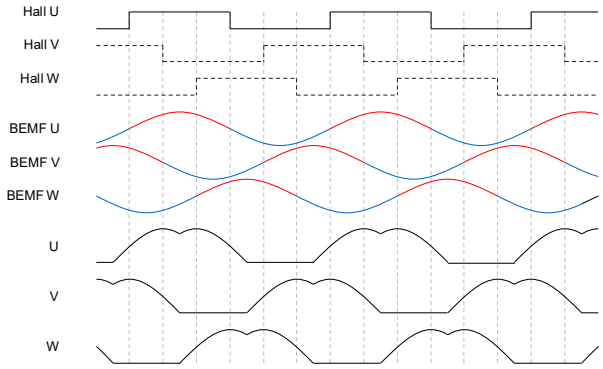


Figure 11.13 Delta Connection Sine Wave CCW

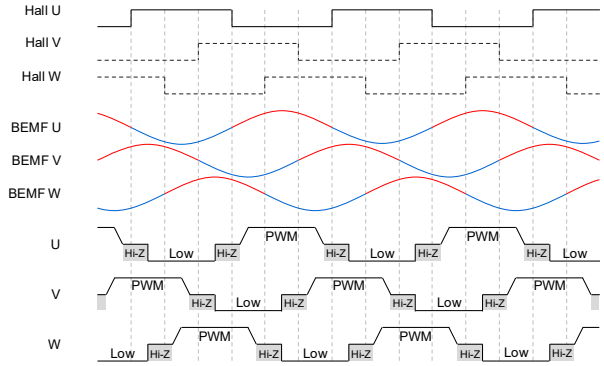


Figure 11.14 Delta Connection 150° CW

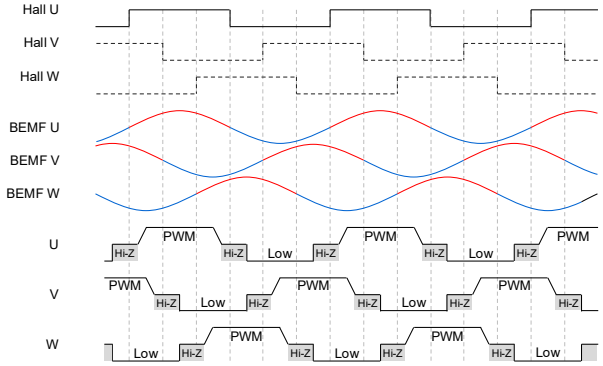


Figure 11.15 Delta Connection 150° CCW

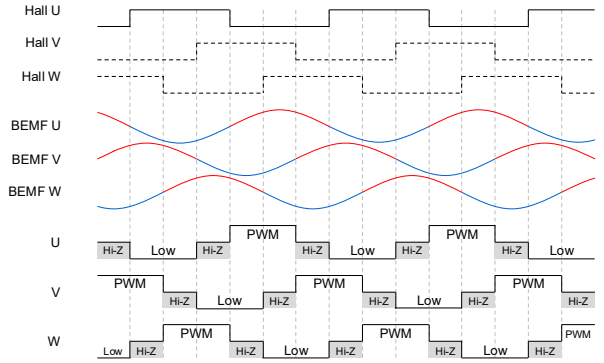


Figure 11.16 Delta Connection 120° CW

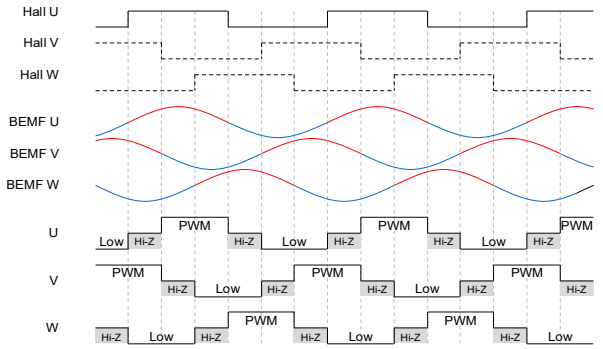


Figure 11.17 Delta Connection 120° CCW

Note: The timing charts are simplified for explanatory purposes of functions and operations.

11.2.9.4. Output PWM Frequency

The output PWM frequency can be selected as shown in the table below.

Table 11.36 Setting of Output PWM Frequency

Register 8[2:0] FPWM		Output PWM frequency F_{PWM} (kHz)					
	Acceleration	0 < f ≤ 0.2	0.2 < f ≤ 0.4	0.4 < f ≤ 0.6	0.6 < f ≤ 0.8	0.8 < f ≤ 1	1 < f
	Deceleration	0 < f ≤ 0.1	0.1 < f ≤ 0.3	0.3 < f ≤ 0.5	0.5 < f ≤ 0.7	0.7 < f ≤ 0.9	0.9 < f (Note1)
000b (Default)		23.4					
001b		46.9					
010b		93.7					
011b		187.5					
100b		46.9	46.9	93.7	93.7	93.7	187.5
101b		23.4	46.9	93.7	93.7	93.7	93.7
110b		23.4	23.4	46.9	46.9	93.7	93.7
111b		23.4	46.9	93.7	93.7	187.5	187.5

Note1: f represents the rotational speed (kHz).

11.2.10. Lead Angle Control

Since the rotation speed changes due to motor impedance and others, a phase difference is generated between the motor voltage and current. Then, the motor driving efficiency is lowered. To improve its efficiency, the lead angle control is necessary to reduce this phase difference.
Besides fixed lead angle, automatic lead angle linked with speed commands is supported. Additionally, when using Hall sensors, automatic lead angle control (Intelligent Phase Control) that aligns the phase of the Hall signal with the phase of the motor drive current is also supported.

Table 11.37 Setting of Lead Angle Function

Register: 12[2:0] LA_TYPE	Setting of Lead Angle function
000b (Default)	Linear Curve Lead Angle: LA offset Valid
001b	Linear Curve Lead Angle: SPD offset Valid
010b	Quadratic Curve Lead Angle: LA offset Valid
011b	Quadratic Curve Lead Angle: SPD offset Valid
100b	Lead Angle of Quadratic Curve with Inflection Point
101b	Fixed Lead Angle
110b	Automatic Lead Angle (Intelligent Phase Control) (Note1)
111b	Lead Angle 0°

Note1: Automatic lead angle (Intelligent Phase Control) is effective only during sine wave drive.
- 1-Hall and 3-Hall drive: The phase advance is automatically adjusted by comparing the U-phase current phase with the U-phase Hall signal.
- Sensorless drive: IPC is disabled, and the phase advance is fixed at 0 °.

Table 11.38 Register for Lead Angle Function

Address	Register	Bit	Contents of setting	Input range	Setting value
12 [2:0]	LA_TYPE [2:0]	3	Lead angle function selection	0 to 7	Lead Angle function
13 [7]	LA_REF	1	Lead angle table reference	0 or 1	0b: Output Duty reference (Default) 1b: SPD command reference
13 [6:0]	LA [6:0]	7	①Maximum lead angle value / Fixed lead angle value	0 to 127	0 to 59.5 °
13 [6:0]	LA [6:0]	7	Maximum lead angle value of Automatic Lead Angle	0 to 127	0 to 59.5 °
14 [7:0]	LA_MAXSPD [7:0]	8	②SPD value for maximum lead angle	0 to 255	256 to 511
15 [7:0]	LA_CHGSPD [7:0]	8	③SPD value for quadratic curve inflection point	0 to 255	0 to 510
15 [7:0]	LA_CHGSPD [7:0]	8	Start point of Automatic Lead Angle	0 to 255	0 to 255
16 [5:0]	LA_OFFSET [5:0]	6	④LA offset	0 to 63	0 to 29.5 °
16 [5:0]	LA_OFFSET [5:0]	6	Minimum lead angle value of Automatic Lead Angle	0 to 63	0 to 29.5 °
16 [7:0]	LA_OFFSET [7:0]	8	⑤SPD offset	0 to 255	0 to 255

Note: Phase advance control is supported for sine wave drive and 150 ° drive.
However, 3-Hall 120 ° drive does not support phase advance control.
The maximum phase advance is 15 degrees for sensorless 150 ° drive, and 30 ° for sensorless sine wave drive.

11.2.10.1. Linear Curve Lead Angle: LA Offset Valid

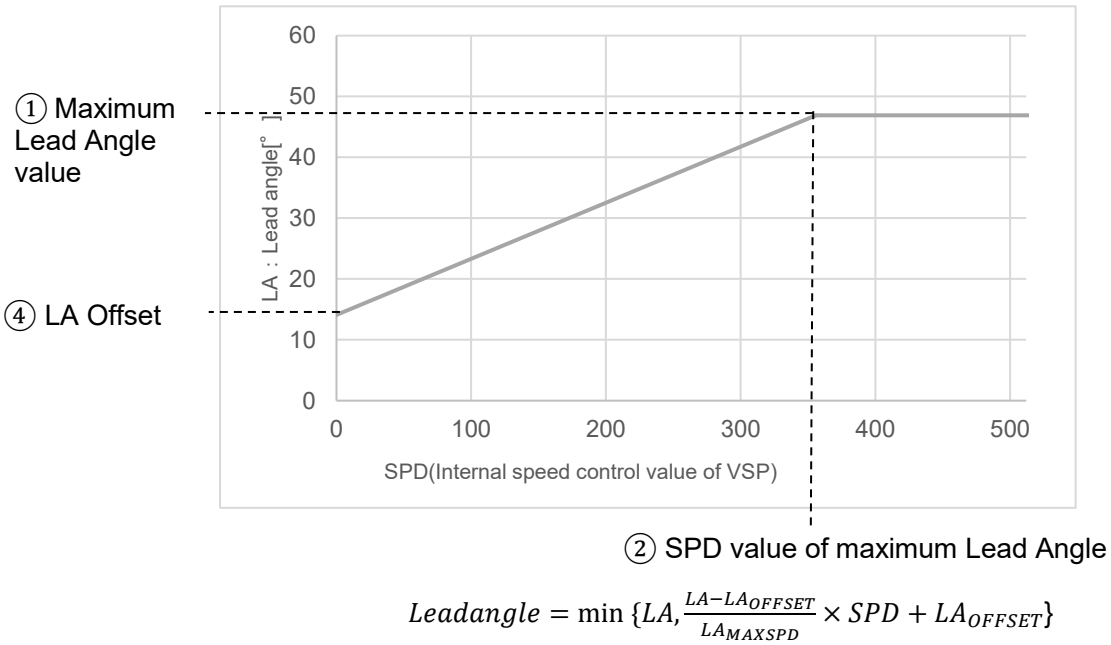
When " Linear Curve Lead Angle: LA Offset Valid" is selected, the Lead Angle indicates the behavior of a linear curve with respect to the Speed Command SPD (Internal Speed Command Figure) and can be set as shown below.

①The Maximum Lead Angle value is determined with the setting of LA x Resolution (60/128).
Example: when the setting of LA = 100,
the Maximum Lead Angle is 100 x 60 / 128 = 46.9 °

②SPD value for Maximum Lead Angle = LA_MAXSPD setting + 256.
Example: When LA_MAXSPD/LA_CHGSPD setting = 100,
SPD value for Maximum Lead Angle = 100 + 256 = 356.

④LA offset = LA_OFFSET setting × resolution (60/128).
Example: When LA_OFFSET setting = 30,
LA offset = 30 × 60/128 = 14.1°.

Example: The lead angle when SPD = 200 with the above settings is as follows.
Lead angle [°] = [{(LA-LA_OFFSET) / (LA_MAXSPD/LA_CHGSPD+256) × SPD} + LA_OFFSET]
× (60/128)
Lead angle [°] = [(100-30) / (100+256) × 200} + 30] × (60/128)
Lead angle [°] = 32.5
When LA < LA_OFFSET, LA-LA_OFFSET = 0.



$$Leadangle = \min\{LA, \frac{LA - LA_{OFFSET}}{LA_{MAXSPD}} \times SPD + LA_{OFFSET}\}$$

Figure 11.18 Linear Curve Lead Angle: Settings of LA Offset Valid

11.2.10.2. Linear Curve Lead Angle: SPD Offset Valid

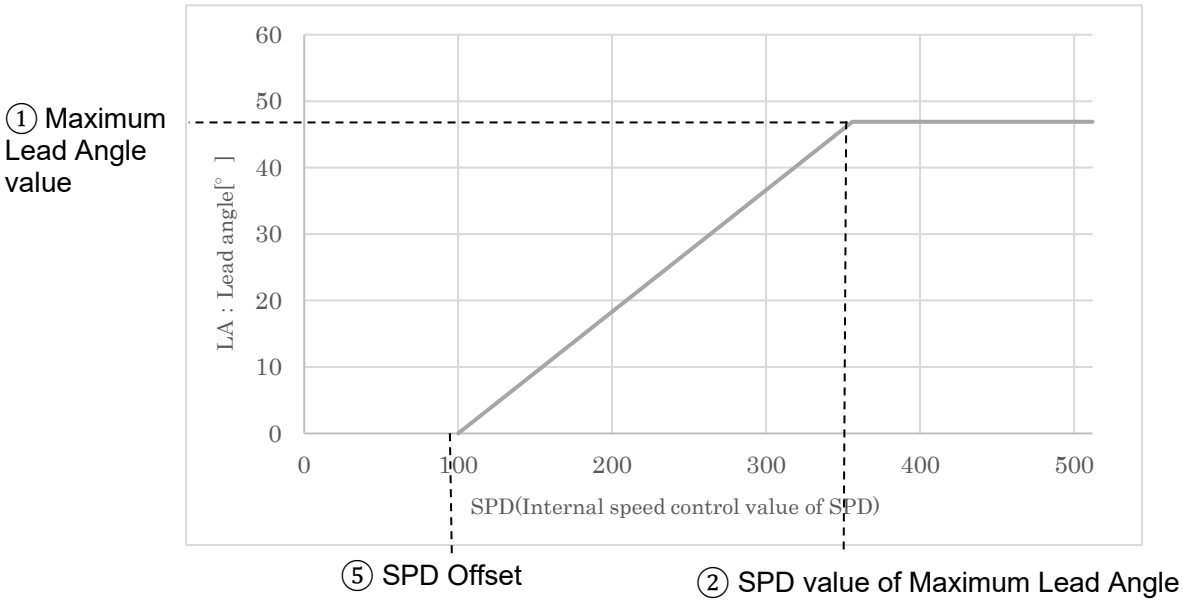
When the " Linear curve Lead angle: SPD offset valid" is selected, the lead angle indicates the behavior of a linear curve with respect to the Speed Command SPD (Internal Speed Command Figure) and can be set as shown below.

①The Maximum Lead Angle value is determined with the setting of LA x Resolution (60 / 128).
Example: when the setting of LA = 100,
the Maximum Lead Angle is 100 x 60 / 128 = 46.9 °

②SPD value for Maximum Lead Angle = LA_MAXSPD setting + 256.
Example: When LA_MAXSPD/LA_CHGSPD setting = 100,
SPD value for Maximum Lead Angle = 100 + 256 = 356.

⑤SPD offset = determined by LA_OFFSET setting.
Example: When LA_OFFSET setting = 100,
SPD offset = 100.

Example: The lead angle when SPD = 200 with the above settings is as follows.
Lead angle [°] = LA × (SPD-LA_OFFSET) / (LA_MAXSPD/LA_CHGSPD+256-LA_OFFSET) × (60/128)
Lead angle [°] = 100 × (200-100) / (100+256-100) × (60/128)
Lead angle [°] = 18.3
When SPD＜LA_OFFSET, Lead Angle [°] is 0.



$$Leadangle = \min\left\{LA, \frac{LA}{LA_{MAXSPD} - SPD_{OFFSET}} \times min\{0, SPD - SPD_{OFFSET}\}\right\}$$

Figure 11.19 Linear Curve Lead Angle: Settings of SPD Offset Valid

11.2.10.3. Quadratic Curve Lead Angle: LA Offset Valid

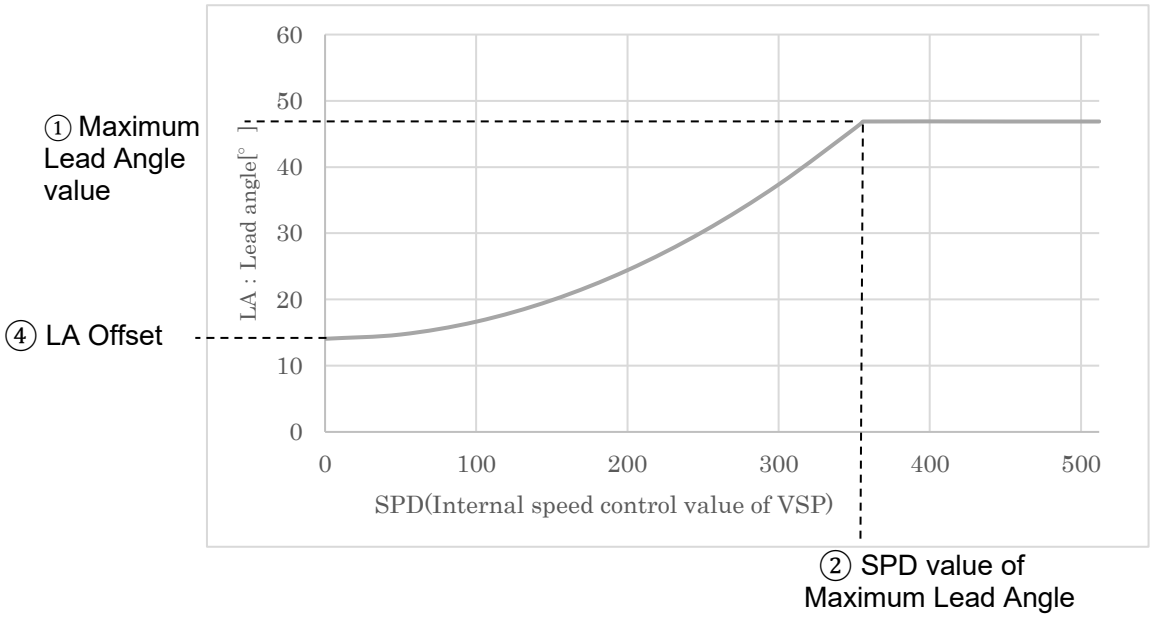
When the "Quadratic curve Lead Angle: LA offset valid" is selected, the lead angle indicates the behavior of a quadratic curve with respect to the Speed Command SPD (Internal Speed Command Figure) and can be set as follows.

①The Maximum Lead Angle value is determined with the setting of LA x Resolution (60/128).
Example: when the setting of LA = 100,
the Maximum Lead Angle is 100 x 60 / 128 = 46.9 °

②SPD value for Maximum Lead Angle = LA_MAXSPD setting + 256.
Example: When LA_MAXSPD/LA_CHGSPD setting = 100,
SPD value for Maximum Lead Angle = 100 + 256 = 356.

④LA offset = LA_OFFSET setting × resolution (60/128).
Example: When LA_OFFSET setting = 30,
LA offset = 30 × 60/128 = 14.1°.

Example: The lead angle when SPD = 200 with the above settings is as follows.
Lead angle [°] = [(LA-LA_OFFSET) / (LA_MAXSPD/LA_CHGSPD+256) ^2 × SPD^2} + LA_OFFSET]
× (60/128)
Lead angle [°] = [100-30) / (100+256) ^2 × 200^2} + 30] × (60/128)
Lead angle [°] = 22.9
When LA < LA_OFFSET, LA-LA_OFFSET = 0.



$$Leadangle = \min\left\{LA, \frac{LA - LA_{OFFSET}}{LA_{MAXSPD}{}^{2}} \times SPD^{2} + LA_{OFFSET}\right\}$$

Figure 11.20 Quadratic Curve Lead Angle: Settings of LA Offset Valid

11.2.10.4. Quadratic Curve Lead Angle: SPD Offset Valid

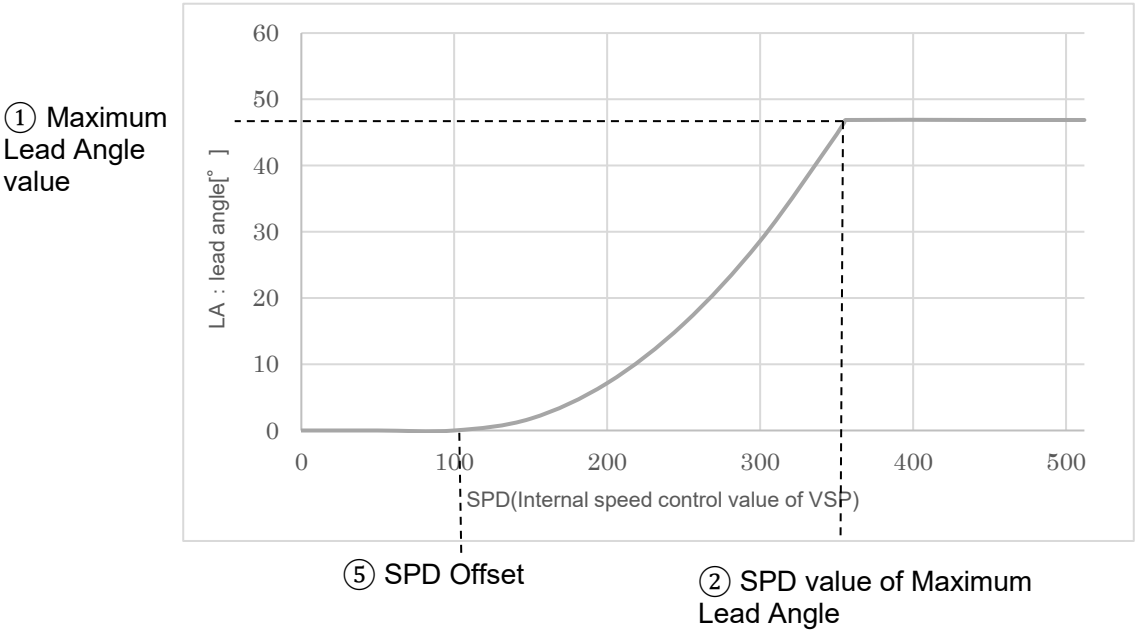
When the "Quadratic curve Lead Angle: SPD offset valid" is selected, the lead angle indicates the behavior of a quadratic curve with respect to the Speed Command SPD (Internal Speed Command value) and can be set as shown below.

①The Maximum Lead Angle value is determined with the setting of LA x Resolution (60 / 128).
Example: when the setting of LA = 100,
the Maximum Lead Angle is 100 x 60 / 128 = 46.9 °

②SPD value for Maximum Lead Angle = LA_MAXSPD setting + 256.
Example: When LA_MAXSPD/LA_CHGSPD setting = 100,
SPD value for Maximum Lead Angle = 100 + 256 = 356.

⑤SPD offset = LA_OFFSET setting.
Example: When LA_OFFSET setting = 100,
SPD offset = 100.

Example: The lead angle when SPD = 200 with the above settings is as follows.
Lead angle [°] = LA × (SPD - LA_OFFSET) ^2 / (LA_MAXSPD/LA_CHGSPD + 256 - LA_OFFSET) ^2 × (60/128)
Lead angle [°] = 100 × (200 - 100) ^2 / (100 + 256 - 100) ^2 × (60/128)
Lead angle [°] = 7.2
When SPD＜LA_OFFSET, Lead Angle [°] is 0.



$$Leadangle = \min\left\{LA,\ \frac{LA}{(LA_{MAXSPD} - SPD_{OFFSET})^2} \times \min\{0, SPD - SPD_{OFFSET}\}^2\right\}$$

Figure 11.21 Settings of Quadratic Curve Lead Angle: SPD Offset Valid

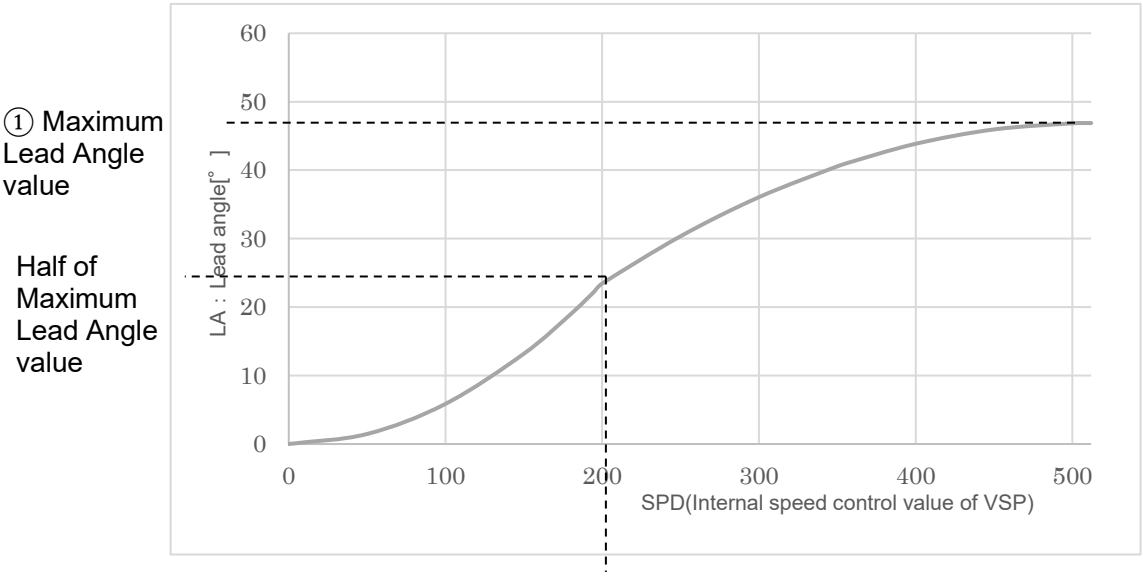
11.2.10.5. Lead Angle of Quadratic Curve with Inflection Point

When the "Lead Angle of Quadratic Curve with Inflection Point" is selected, the Lead Angle indicates the behavior of a quadratic curve with respect to the Speed Command SPD (Internal Speed Command value) and can be set as shown below.

①The Maximum Lead Angle value is determined with the setting of LA x Resolution (60 / 128).
Example: when the setting of LA = 100,
the Maximum Lead Angle is 100 x 60 / 128 = 46.9 °

③SPD value with quadratic curve inflection point = LA_CHGSPD setting × 2.
Example: When LA_MAXSPD/LA_CHGSPD setting = 100,
SPD value with quadratic curve inflection point = 100 × 2 = 200.

Example: The lead angle when SPD = 100 with the above settings is as follows.
When inflection point > SPD,
Lead angle [°] = LA × SPD^2 / 2 × (2 × LA_MAXSPD/LA_CHGSPD) ^2} × (60/128)
Lead angle [°] = 100 × 100^2 / 2 × (2 × 100) ^2} × (60/128)
Lead angle [°] = 5.9
Example: The lead angle when SPD = 300 with the above settings is as follows.
When inflection point ≤ SPD,
Lead angle [°] = (LA - [LA × (512 - SPD) ^2) / 2 × (512 - 2 × LA_MAXSPD/LA_CHGSPD) ^2]) × (60/128)
Lead angle [°] = (100 - [{100 × (512 - 300) ^2)} / {2 × (512 - 2 × 100) ^2}]) × (60/128)
Lead angle [°] = 36.1



SPD < LA_CHGSPD:

$$Leadangle = \frac{LA_{MAXSPD}}{2} \times \frac{SPD^2}{LA_{CHGSPD}{}^2}$$

LA_CHGSPD ≤ SPD ≤ LA_MAXSPD:

$$Leadangle = LA_{MAXSPD} - \frac{LA_{MAXSPD}}{2} \times \frac{(512 - SPD)^2}{(512 - LA_{CHGSPD})^2}$$

LA_MAXSPD ≤ SPD:

$$Leadangle = LA_{MAXSPD} - \frac{LA_{MAXSPD}}{2} \times \frac{(512 - LA_{MAXSPD})^2}{(512 - LA_{CHGSPD})^2}$$

Figure 11.22 Settings of Lead Angle of Quadratic Curve with Inflection Point

11.2.10.6. Fixed Lead Angle

When the "Fixed Lead Angle" is selected, the Lead Angle is constant with respect to the Speed Command SPD (Internal Speed Command value) and can be set as follows.

①Fixed Lead Angle is determined with the setting of LA x resolution (60 / 128).
Example: When LA setting = 100,
the Maximum Lead Angle is 100 x 60 / 128 = 46.9°.

① Fixed Lead Angle

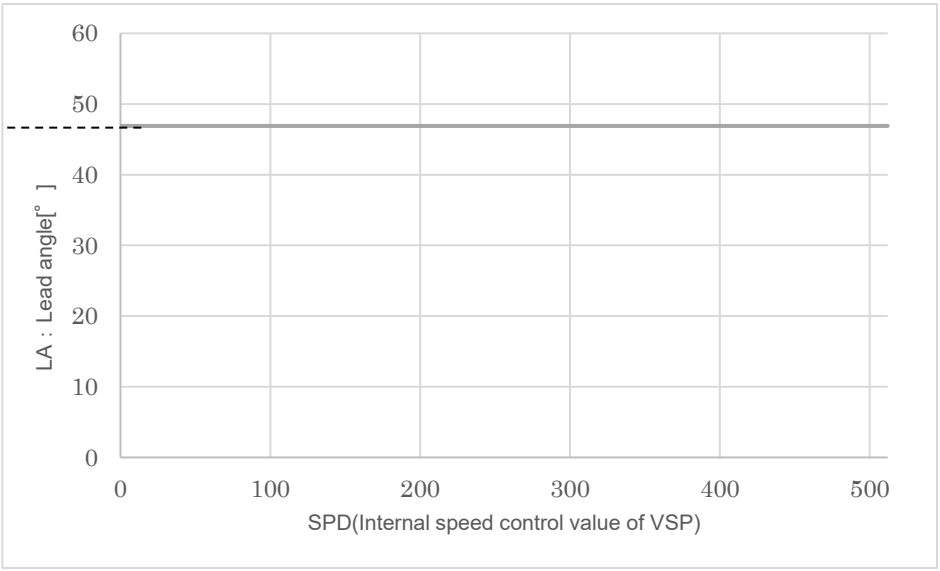


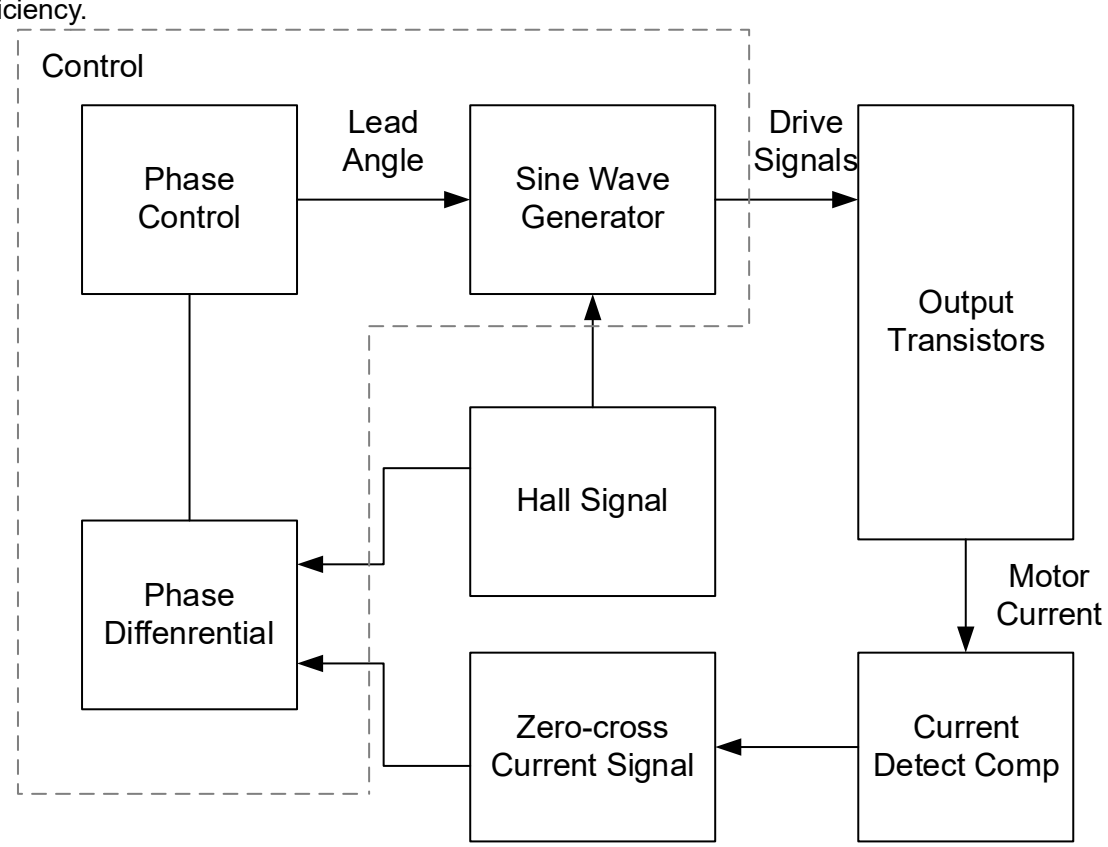
Figure 11.23 Settings of Fixed Lead Angle

11.2.10.7. Lead Angle 0 °

When the “Lead Angle 0°” is selected, the Lead Angle remains 0° for any Speed Command SPD (Internal Speed Command Value).

11.2.10.8. Automatic Lead Angle Control by Intelligent Phase Control

The Intelligent Phase Control function compares the phase of the motor current (current information) with the phase of the motor voltage (Hall signal), and feeds back to the motor current control signal (control signal) to automatically adjust the phase between motor voltage and motor current, achieving high efficiency.



Note: Some of the functional blocks and circuits in the block diagram may have been omitted or simplified for explanation purposes.

Figure 11.24 Image of IPC System Block Diagram

When the comparator detects zero-cross motor current, it generates the zero-cross current signal.
The lead angle is adjusted automatically to match the zero cross of hall signal with the zero-cross current signal.

11.2.11. Speed Control

Motor speed control can be selected between closed loop control and open loop control.

Table 11.39 Speed Control Setting

Register: 27[7] OPENLOOP	Speed control
0b ((Default))	Closed loop
1b	Open loop

11.2.11.1. Closed loop

In the case of closed loop control, an example of the speed curve is shown below.
The details of the speed curve can be adjusted by the register.

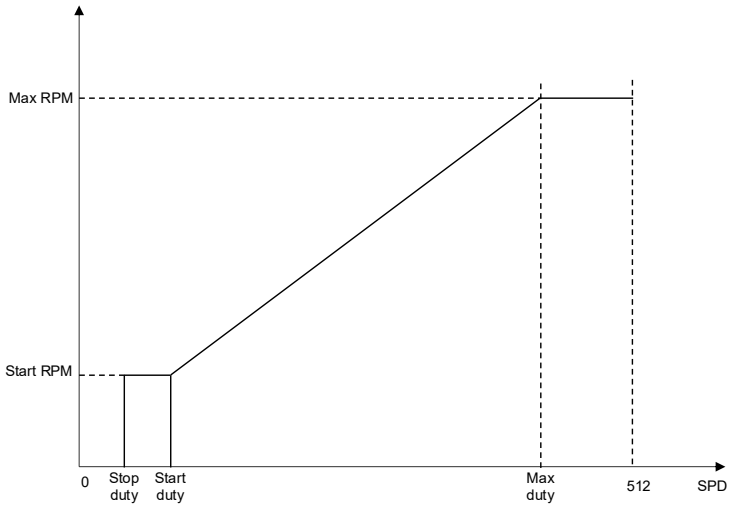


Figure 11.25 Speed Curve of Closed Loop

Table 11.40 Settings of Speed Curve

Item	Register	Setting range	Relationship
Max RPM	19, 20 [15:0] MAX_RPM	0 to 65535	Max RPM = MAX_RPM
Max duty	24[7:0] MAX_DUTY	0 to 255	Max duty = MAX_DUTY +257
Start duty	21[7:0] ST_DUTY	0 to 255	Start duty = ST_DUTY
Start RPM	22[7:0] ST_RPM	0 to 255	Start RPM = MAX_RPM × ST_RPM / 256
Stop duty	23[7:0] STOP_DUTY	0 to 255	Stop duty = STOP_DUTY

Note: Do not set Stop duty to a value equal to or greater than Start duty.

When Current Duty ≤ Start duty → Current Duty > Start duty:

Target RPM = $\left(\frac{256-ST\_RPM}{MAX\_DUTY+257-ST\_DUTY} \times (Current\ Duty - ST\_DUTY) + ST\_RPM\right) \times MAX\_RPM / 256$

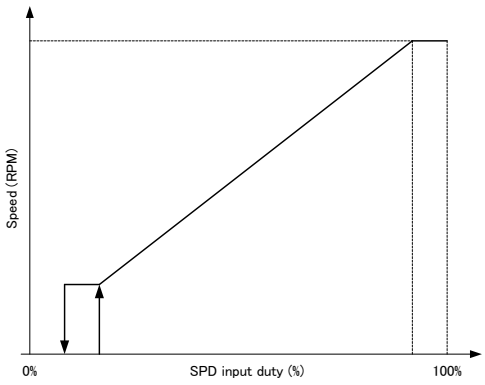
When Current Duty > Start duty → Current Duty > Start duty:

Target RPM = $\left(\frac{256-ST\_RPM}{MAX\_DUTY+257-ST\_DUTY} \times (Current\ Duty - ST\_DUTY) + ST\_RPM\right) \times MAX\_RPM / 256$

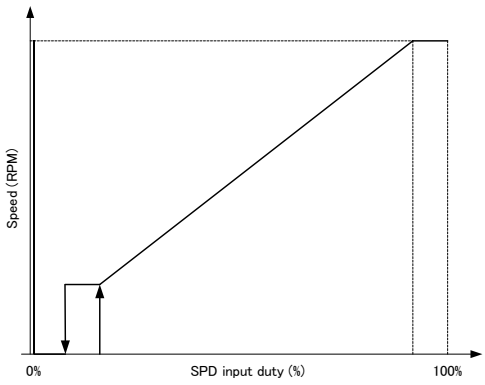
When Current Duty > Start duty → Current Duty ≥ Stop duty:

Target RPM = MAX_RPM × ST_RPM / 256

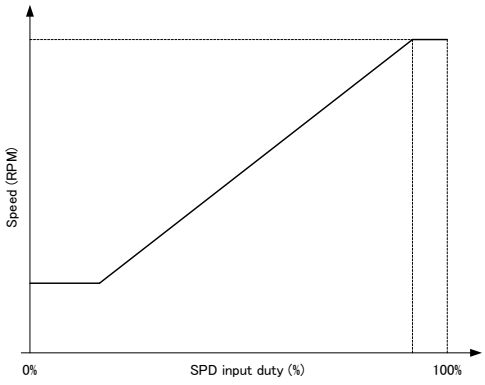
MAXOPEN = 0



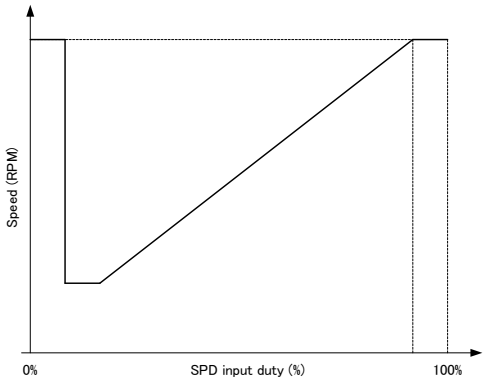
NOSTOP=0, MAXOFF=0



NOSTOP=0, MAXOFF=1

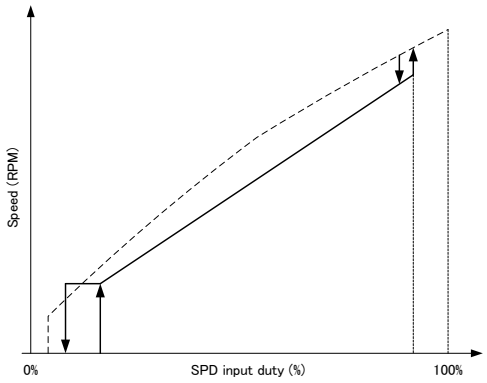


NOSTOP=1, MAXOFF=0

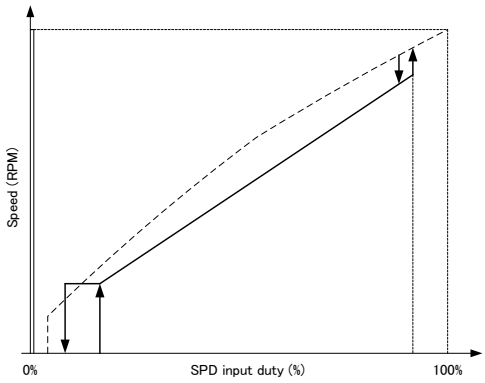


NOSTOP=1, MAXOFF=1

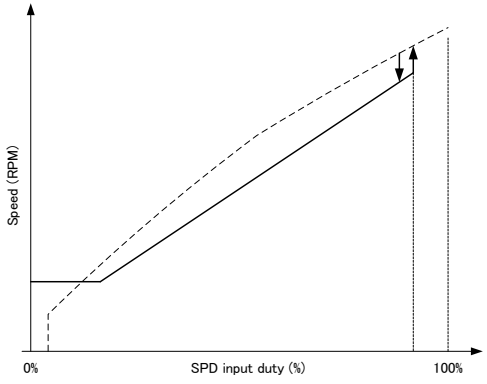
MAXOPEN = 1



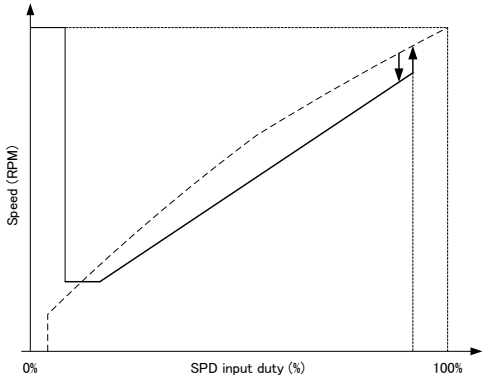
NOSTOP=0, MAXOFF=0



NOSTOP=0, MAXOFF=1



NOSTOP=1, MAXOFF=0



NOSTOP=1, MAXOFF=1

Figure 11.26 Examples of Closed Loop Speed Curve

Up to five inflection points can be added to the speed curve.

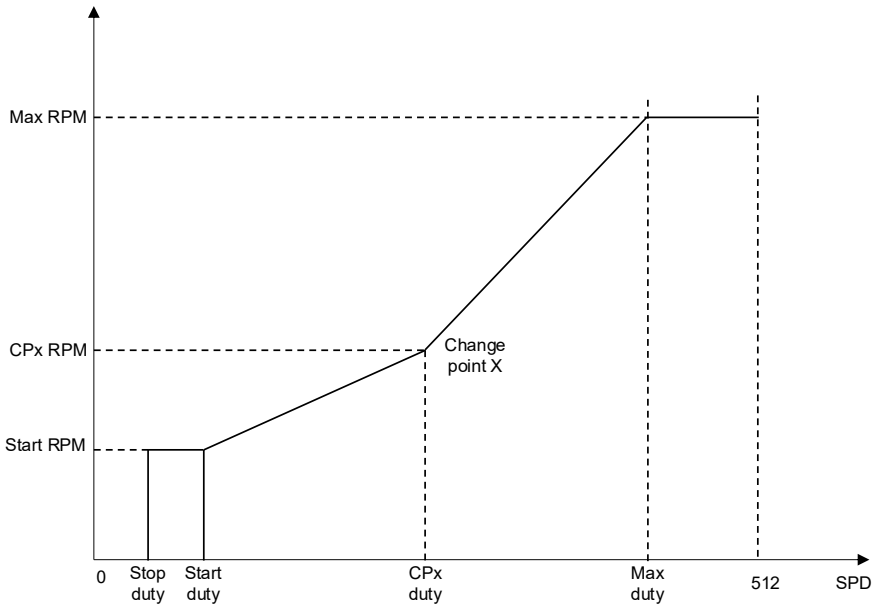


Figure 11.27 Speed Curve of Closed Loop with Inflection Point

Table 11.41 Settings of Speed Curve of Closed Loop with Inflection Point

Item	Register	Setting range	Relationship
Max RPM	19, 20 [15:0] MAX_RPM	0 to 65535	Max RPM = MAX_RPM
Max duty	24[7:0] MAX_DUTY	0 to 255	Max duty = MAX_DUTY + 257
Start duty	21[7:0] ST_DUTY	0 to 255	Start duty = ST_DUTY
Start RPM	22[7:0] ST_RPM	0 to 255	Start RPM = MAX_RPM × ST_RPM / 256
Stop duty	23[7:0] STOP_DUTY	0 to 255	Stop duty = STOP_DUTY
CPx duty	28,30,32,34,36[6:0] Px_DUTY	0 to 127	CPx duty = 512 × Px_DUTY / 128
CPx RPM	29,31,33,35,37[7:0] Px_RPM	0 to 255	CPx RPM = MAX_RPM × Px_RPM / 256

Enable inflection points consecutively starting from P1. If there is a non-enabled inflection point in between, the speed curve becomes invalid and the output becomes a straight line at 0.
Additionally, inflection points must satisfy the following conditions. If not satisfied, the speed curve becomes invalid.

・Duty must be in ascending order (Pn+1_DUTY > Pn_DUTY)

・RPM must be the same or in ascending order (Pn+1_RPM ≥ Pn_RPM)

Calculation example:

・Start Duty < Current Duty ≤ CP1 duty

$$\text{Target RPM} = \left(\frac{P1\_RPM - ST\_RPM}{P1\_DUTY \times 4 - ST\_DUTY} \times (Current\ Duty - ST\_DUTY) + ST\_RPM\right) \times \frac{MAX\_RPM}{256}$$

・CPn Duty < Current Duty ≤ CPn+1 duty

$$\text{Target RPM} = \left(\frac{Pn{+}1\_RPM - Pn\_RPM}{(Pn{+}1\_DUTY - Pn\_DUTY) \times 4} \times (Current\ Duty - (Pn\_DUTY \times 4)) + Pn\_RPM\right) \times \frac{MAX\_RPM}{256}$$

・CPn Duty < Current Duty ≤ Max duty

$$\text{Target RPM} = \left(\frac{256 - Pn\_RPM}{\text{MAX\_DUTY} + 257 - Pn\_DUTY \times 4} \times (Current\ Duty - (Pn\_DUTY \times 4)) + Pn\_RPM\right) \times \frac{MAX\_RPM}{256}$$

11.2.11.2. Open loop

In the case of open loop control, an example of the output curve is shown below.
The details of the output curve can be adjusted by the register.

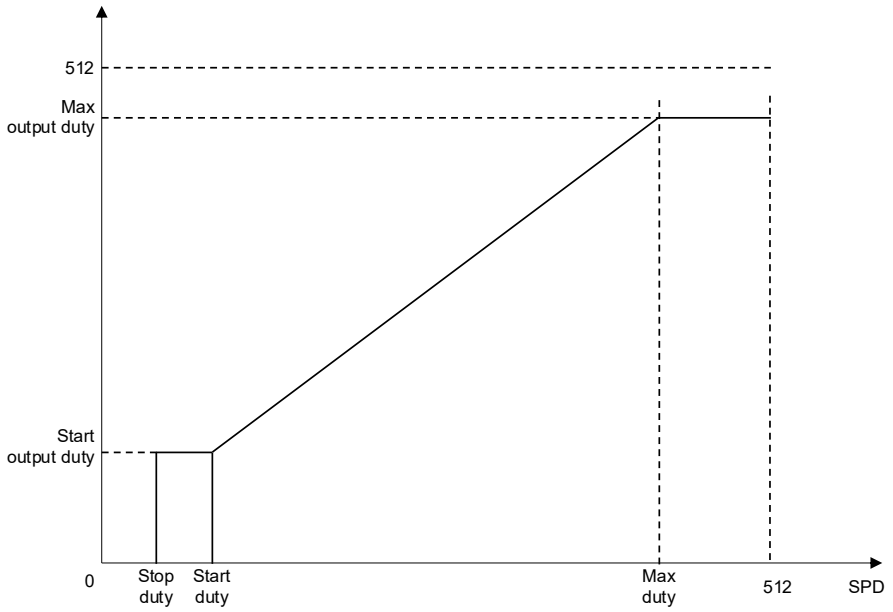


Figure 11.28 Output Curve of Open Loop

Table 11.42 Settings of Output Curve

Item	Register	Setting range	Relationship
Max output duty	19, 20 [15:0] MAX_RPM	0 to 255	Max output duty = MAX_RPM 19[7:0] + 257
Max duty	24[7:0] MAX_DUTY	0 to 255	Max duty = MAX_DUTY + 257
Start duty	21[7:0] ST_DUTY	0 to 255	Start duty = ST_DUTY
Start output duty	22[7:0] ST_RPM	0 to 255	Start output duty = (MAX_RPM [7:0] + 257) × ST_RPM /256
Stop duty	23[7:0] STOP_DUTY	0 to 255	Stop duty = STOP_DUTY

Note: Do not set Stop duty to a value equal to or greater than Start duty.

When Current Duty ≤ Start duty → Current Duty > Start duty:

$$\text{Target Duty} = \left(\frac{256-ST\_RPM}{MAX\_DUTY+257-ST\_DUTY} \times (Current\ Duty - ST\_DUTY) + ST\_RPM\right) \times \frac{(MAX\_RPM[7:0]+257)}{256}$$

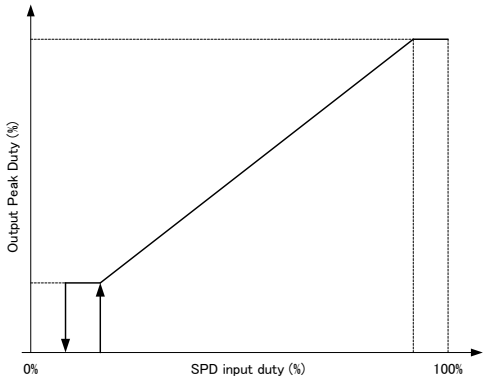
When Current Duty > Start duty → Current Duty > Start duty:

$$\text{Target Duty} = \left(\frac{256-ST\_RPM}{MAX\_DUTY+257-ST\_DUTY} \times (Current\ Duty - ST\_DUTY) + ST\_RPM\right) \times \frac{(MAX\_RPM[7:0]+257)}{256}$$

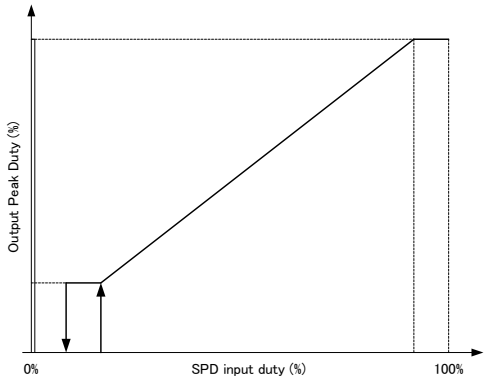
When Current Duty > Start duty → Current Duty ≥ Stop duty:

Target Duty = (MAX_RPM [7:0] +257)×ST_RPM / 256

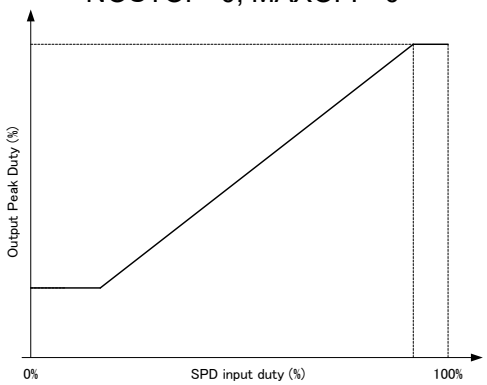
MAXOPEN = 0



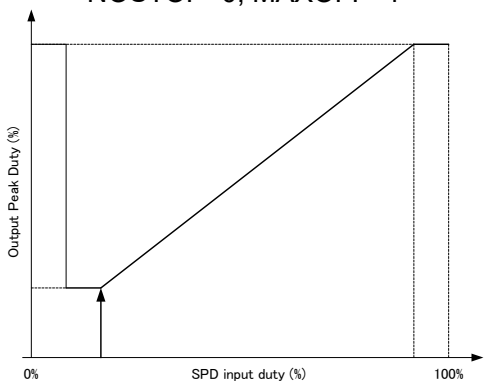
NOSTOP=0, MAXOFF=0



NOSTOP=0, MAXOFF=1

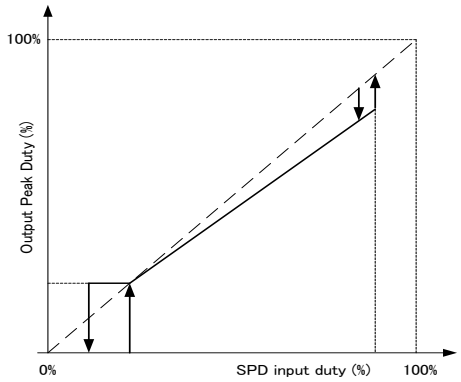


NOSTOP=1, MAXOFF=0

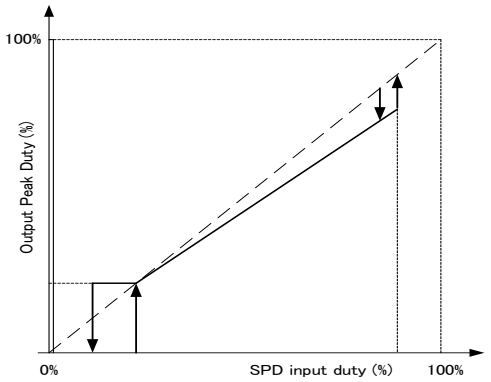


NOSTOP=1, MAXOFF=1

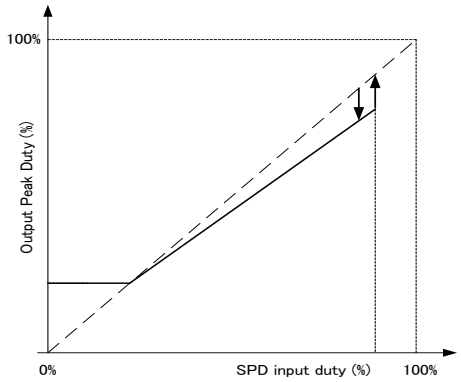
MAXOPEN = 1



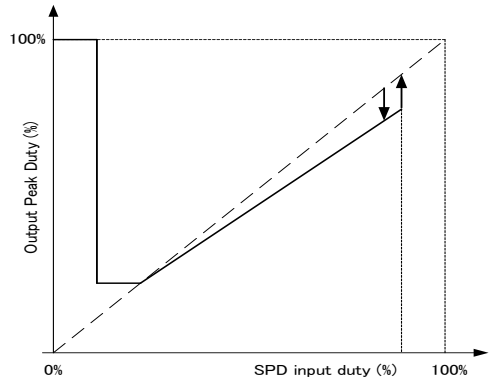
NOSTOP=0, MAXOFF=0



NOSTOP=0, MAXOFF=1



NOSTOP=1, MAXOFF=0



NOSTOP=1, MAXOFF=1

Figure 11.29 Examples of Open Loop Speed Curve

Up to five inflection points can be added to the output curve.

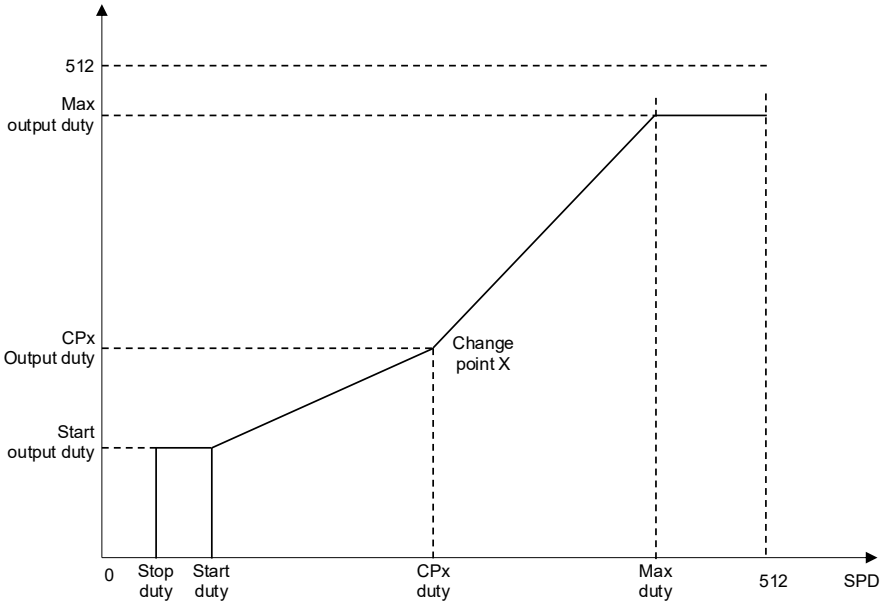


Figure 11.30 Ouput Curve of Open Loop with Inflection Point

Table 11.43 Settings of Output Curve of Open Loop with Inflection Point

Item	Register	Setting range	Relationship
Max output duty	19, 20 [15:0] MAX_RPM	0 to 255	Max output duty = MAX_RPM 19[7:0] + 257
Max duty	24[7:0] MAX_DUTY	0 to 255	Max duty = MAX_DUTY +257
Start duty	21[7:0] ST_DUTY	0 to 255	Start duty = ST_DUTY
Start output duty	22[7:0] ST_RPM	0 to 255	Start output duty = (MAX_RPM [7:0] + 257) × ST_RPM / 256
Stop duty	23[7:0] STOP_DUTY	0 to 255	Stop duty = STOP_DUTY
CPx duty	28,30,32,34,36[6:0] Px_DUTY	0 to 127	CPx duty = 512 × Px_DUTY / 128
CPx output duty	29,31,33,35,37[7:0] Px_RPM	0 to 255	CPx output duty = (MAX_RPM [7:0] + 257) × Px_RPM / 256

Enable the inflection points consecutively starting from P1. If there is an inflection point that has not been enabled in between, the speed curve becomes invalid and the output becomes a straight line at 0. Additionally, the inflection points must satisfy the following conditions. If not satisfied, the speed curve becomes invalid.

・Duty must be in ascending order (Pn+1_DUTY > Pn_DUTY)

・RPM must be the same or in ascending order (Pn+1_RPM ≥ Pn_RPM)

Calculation example:

・Start Duty < Current Duty ≤ CP1 duty

Target RPM = $\left(\frac{P1\_RPM-ST\_RPM}{P1\_DUTY\times4-ST\_DUTY}\times(Current\ Duty-ST\_DUTY)+ST\_RPM\right)\times\frac{(MAX\_RPM[7:0]+257)}{256}$

・CPn Duty < Current Duty ≤ CPn+1 duty

Target RPM = $\left[\frac{Pn+1\_RPM-Pn\_RPM}{(Pn+1\_DUTY-Pn\_DUTY)\times4}\times\left(Current\ Duty-(Pn\_DUTY\times4)\right)+Pn\_RPM\right]\times\frac{(MAX\_RPM[7:0]+257)}{256}$

・CPn Duty < Current Duty ≤ Max duty

Target RPM = $\left[\frac{256-Pn\_RPM}{\mathrm{MAX\_DUTY}+257-Pn\_DUTY\times4}\times(Current\ Duty-(Pn\_DUTY\times4))+Pn\_RPM\right]\times\frac{MAX\_RPM[7:0]+257}{256}$

11.2.11.3. Acceleration and Deceleration Control

- **For Open loop**

The DUTY_CL setting limits the amount of change in the output duty per unit time.
This limitation is applied to both acceleration and deceleration.

Table 11.44 Duty Change Unit Time

Register: 10[5] CHG_INTV	Unit time (ms)
0b (Default)	2.7
1b	10.8

Table 11.45 Duty Change Limitation Settings for Open Loop Acceleration/Deceleration

Register: 11[4:2] DUTY_CL	Duty change per unit time	Acceleration/Deceleration time (s) (0 to 512)@2.7 ms
000b (Default)	2/8	5.53
001b	3/8	3.69
010b	5/8	2.21
011b	8/8	1.38
100b	15/8	0.74
101b	25/8	0.44
110b	40/8	0.28
111b	Disabled	—

Note: When DUTY_CL=111, this limitation is disabled.

- **For Closed Loop**

When the SPD change amount is 64 or greater during acceleration, the motor is first accelerated in Open Loop.
During Open Loop acceleration, the change in the output duty is limited by DUTY_CL.
When DUTY_CL = 111, the duty change per unit time is 64/8.
The unit time is determined by the CHG_INTV setting.

Table 11.46 Duty Change Limitation Settings for Closed Loop Acceleration/Deceleration

Register: 11[4:2] DUTY_CL	Duty change per unit time	Acceleration/Deceleration time (s) (0 to 512)@2.7 ms
000b (Default)	2/8	5.53
001b	3/8	3.69
010b	5/8	2.21
011b	8/8	1.38
100b	15/8	0.74
101b	25/8	0.44
110b	40/8	0.28
111b	64/8	0.17

When the output duty reaches the range of (target duty to target duty + 64), or when the rotational speed reaches ±32 rpm of the target speed, the control switches to Closed loop control and converges to the target speed.
In Closed loop control, PI control is executed at a fixed cycle of 2.7 ms.
Although the output duty is updated by the PI control, the maximum duty change per 2.7 ms is limited by DUTY_CL.
When SPD control is performed using the VSP setting, even if the difference before and after the VSP change is 64 or greater, the IC internally divides the change into multiple steps. As a result, the Open loop acceleration mode may not be entered.
Acceleration with an SPD change amount less than 64, deceleration by an SPD command, and acceleration/deceleration caused by external factors are controlled by Closed loop control, converging to the target speed.
In Closed loop control, when the deceleration amount is large, DN_LIM limits the deceleration to prevent the output duty from becoming 0 due to the inability to update the rotational speed.

Table 11.47 Target Rotation Speed Change During Deceleration

Register: 18[4:3] DN_LIM	Target rotation speed change during deceleration
00b (Default)	No limit
01b	500
10b	2000
11b	5000

11.2.12. Power-off Brake

As shown in the figure below, disconnection of the external power supply to the area indicated by the red hatched region can be detected by the VMON pin.

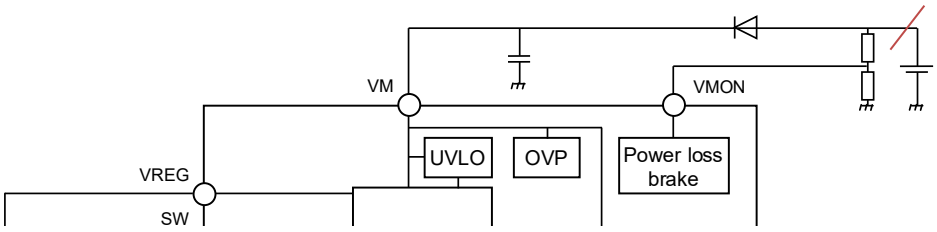


Figure 11.31 Application Circuit Example for Power-off Detection

Table 11.48 Settings of Power-off Brake

Register: 7[0] PLB_ENB	Power-off Brake
0b (Default)	Disabled
1b	Enabled

When PLB_ENB = 1, if a power-off condition is detected, the output transitions to short-brake operation.
If a current limit is detected during short-brake operation, the output is temporarily stopped.
Short-brake operation and output stop are repeated. When the power supply voltage exceeds V_{TH} = 13.5 V (typ.), the output remains stopped until the voltage falls below VTH.
When the IC supply voltage falls to V_{VMUV_D} = 4.8 V (typ.) or lower, the output is stopped. When the supply voltage rises above V_{VMUV_D}, short-brake operation resumes.
If VMON recovers during power-off brake operation, the short brake is released, and the IC restarts from Idle mode.
A 2.5 µs digital filter is built into the VMON pin.

11.3. DCDC

A DC/DC circuit capable of 5 V output is built in. The operating frequency of DCDC is f_{DCDC} = 375 kHz. The DCDC circuit supports two operating modes: DCDC mode and LDO mode. Use DCDC mode when supplying power to external loads.

11.3.1. DCDC Mode

An example application circuit for use in DCDC mode is shown below.

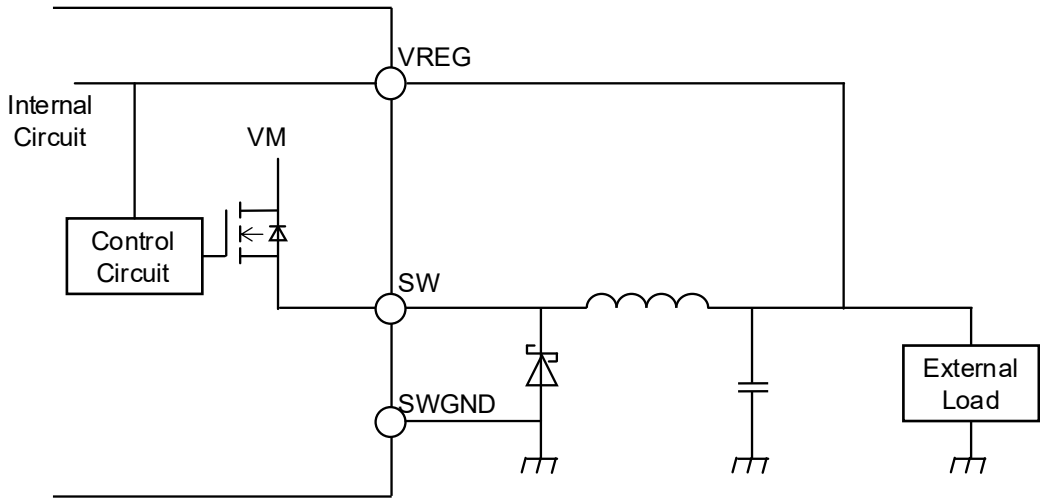


Figure 11.32 Example of DCDC Mode Application Circuit

Table 11.49 BOM list (for Reference)

Designator	Value	Characteristic
L_{SW}	47 μH	Within ±20%, current rating > 1 A, low ESR
C_{SW}	10 μF	Within ±20%, over 10 Vdc, X5R/X7R
D_{SW}	SBD	Reverse voltage rating 60 V, forward current > 1 A, low V_F

11.3.2. LDO Mode

An example application circuit for use in LDO mode is shown below.

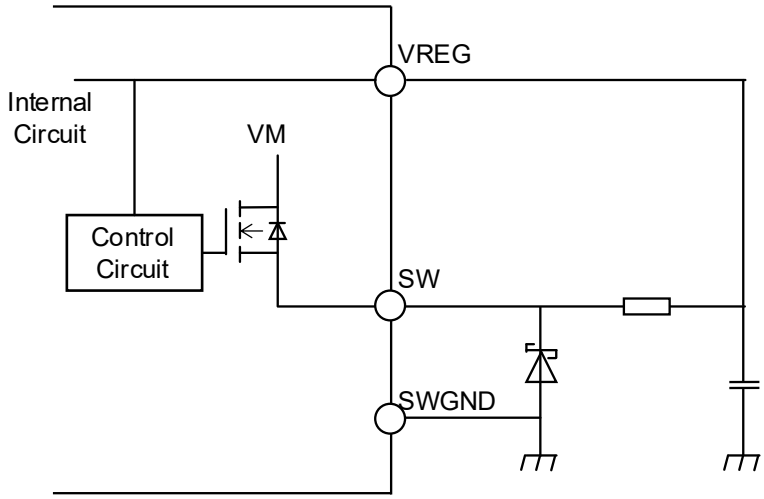


Figure 11.33 LDO mode application circuit example

Table 11.50 BOM list (for Reference)

Designator	Value	Characteristic
R_{SW}	39 Ω	Within ±5%
C_{SW}	10 μF	Within ±20%, over 10 Vdc, X5R/X7R
D_{SW}	SBD	Reverse voltage rating 60 V, forward current > 1 A, low V_F

The power consumption of resistor RSW can be approximately estimated as follows:

$P_{RSW} = I_{ON}^2 \times R_{SW} \times (I_{VREG} / I_{ON})$

Example:

- When V_M = 24 V, I_{ON} = (24 V – 5 V) / (1.5 Ω + 39 Ω) = 0.47 A
  P_{DCDC} = 0.006 W + 0.003 W + 0.003 W = 0.012 W
  P_{RSW} = 0.146 W
- When V_M = 48 V, I_{ON} = (48 V – 5 V) / (1.5 Ω + 39 Ω) = 1.06 A
  P_{DCDC} = 0.013 W + 0.016 W + 0.016 W = 0.044 W
  P_{RSW} = 0.331 W

The power consumption of R_{SW} depends on the power supply voltage. When selecting the resistor, please ensure that the absolute maximum ratings are not exceeded.

11.4. Protection Function

11.4.1. Output Current Limit (OCL) & Current Monitor (CMON)

A small current proportional to the sum of the currents flowing from drain to source of the low-side MOSFETs flows out from the ISET pin.
By connecting an external resistor to the ISET pin to generate a voltage, the condition where the ISET voltage exceeds the internal reference voltage is detected as a current limit.
If the value of the external resistor is too small, the current-limit set current may exceed the absolute maximum ratings. Be sure to set the resistor value with sufficient margin.

Table 11.51 OCL Detection Internal Reference Voltage

Register: 6[1:0] OCL_VTH	V_{OCL} (V)
00b (Default)	1.75
01b	2.0
10b	2.25
11b	2.5

Table 11.52 OCL Detection Mask Time

Register: 7[1] ERR_MASK	Mask time (ns)
0b (Default)	500
1b	750

During sine-wave drive, when a current limit is detected, it is possible to select whether to turn off the H-side or to turn off all three phases.
Current-limit control is performed for each PWM cycle.

Table 11.53 OCL Operation

Register: 6[2] OCL_ACT	OCL operation
0b (Default)	H-side OFF
1b	ALL OFF

During 150 ° drive and 120 ° drive, when a current limit is detected, the H-side is turned off.
In this case as well, current-limit control is performed for each PWM cycle.
The voltage obtained by smoothing the ISET pin voltage with an RC filter correlates with the motor drive current.
This voltage can be used as a current monitor.

11.4.2. High Speed Limit

When the rotation speed rises abnormally due to power supply fluctuation or load fluctuation, in Open loop control, when the rotation speed exceeds a predetermined threshold, it forcibly switches to Closed loop control and keeps the rotation speed within a certain range.
The target rotation speed for Closed loop RPM_limit = MAX_RPM[15:8] × 256 can be set in the range of 0 to 65280 RPM.
During Closed loop control, when the output Duty matches the Duty during Open loop, Closed loop control is released and returns to Open loop control.

When high speed limit is detected, if REP_HSPD = 1 is set, a notification is output from the ALERT terminal. When returning from Closed loop to Open loop, the ALERT output is also released.
Note that there is no dedicated error flag register for high speed limit.

When MAX_RPM[15:8] = 0, the rotation speed limit function is disabled.

11.4.3. Various Abnormality Detection

11.4.3.1. Abnormal Detection and Priority

Table 11.54 Types of Abnormal Detection and Priority

A \ B	DCDC	TSD	ISD	Lock	ST_FAIL	UD_SPD	OV_SPD	VM UVLO	OVP	Hall	OCL
DCDC	-	>>	>>	>>	>>	>>	>>	>>	>>	>>	>>
TSD	<<	-	=	>>	>>	>>	>>	>>	>>	>>	>>
ISD	<<	=	-	>	>	>	>	>	>	>	>>
Lock	<<	<<	<	-	X/=	X/=	X/=	>	>	>	>>
ST_FAIL	<<	<<	<	X/=	-	X/=	=	>	>	>	>>
UD_SPD	<<	<<	<	X/=	X/=	-	X/=	>	>	X	>>
OV_SPD	<<	<<	<	X/=	=	X/=	-	>	>	X	>>
VM UVLO	<<	<<	<	<	<	<	<	-	X	=	>>
OVP	<<	<<	<<	<	<	<	<	X	-	=	>>
Hall	<<	<<	<	<	<	X	X	=	=	-	>>
OCL	<<	<<	<<	<<	<<	<<	<<	<<	<<	<<	-

>>: When A and B are detected simultaneously, A has priority.
If A is detected while B protection is active, A protection is executed.
<<: When A and B are detected simultaneously, B has priority.
If B is detected while A protection is active, B protection is executed.
>: When A and B are detected simultaneously, A has priority.
If A is detected while B protection is active, A is not detected.
<: When A and B are detected simultaneously, B has priority.
If B is detected while A protection is active, B is not detected.
=: A and B have equal priority.
X: A and B are not detected simultaneously.

11.4.3.2. Recovery after Abnormality Detection

For VM UVLO, OVP, current limit (OCL), and Hall signal abnormalities, the IC automatically recovers when the recovery conditions are satisfied.

For DCDC ISD, VREG UVLO, and VREG overvoltage detection abnormalities, the IC recovers under the standby mode release conditions.

For other abnormality detections (TSD, ISD, Lock, Startup failure, Minimum rotation speed abnormality, Maximum rotation speed abnormality), auto-recovery or latch can be selected. The recovery time t_{RE} can be set via register.
In the latch mode, the latch can be released either by transitioning to Idle mode or by re-applying the power supply.

Table 11.55 Recovery Mode

Register: 4[0] LATCH	Recovery mode
0b (Default)	Automatic recovery
1b	Latch mode

Table 11.56 Automatic Recovery Time

Register: 5[6:4] TRE	Automatic recovery time (s)
000b (Default)	0.0109
001b	0.5
010b	1
011b	1.5
100b	2
101b	3
110b	6
111b	10

The enable/disable of each abnormality detection can be configured using register settings.
When DIS_xxx is set, the corresponding abnormal condition is not detected by the logic and is not reflected in the error flags or the ALERT signal.

Table 11.57 Setting for Abnormality Detection

Addr	D7	D6	D5	D4	D3	D2	D1
4	DIS_VM_UVLO	DIS_OVP	DIS_ISD	DIS_TSD	DIS_LOCK	DIS_OVSPD	DIS_OCL
	0b: Abnormality detection enabled(Default), 1b: Abnormality detection disabled						

Register	Abnormal detection type
DIS_VM_UVLO	VM undervoltage lock out mask
DIS_OVP	VM overvoltage protection mask
DIS_ISD	Overcurrent shutdown mask
DIS_TSD	Thermal shutdown mask
DIS_LOCK	Motor lock detection mask Startup failure mask Under speed detection mask
DIS_OVSPD	Over speed detection mask
DIS_OCL	Output current limit mask

11.4.3.3. DCDC Abnormality Detection

The DCDC circuit incorporates abnormality detection functions for undervoltage (UVLO), overvoltage (OVP), and overcurrent detection (ISD).

Table 11.58 DCDC Abnormality Detection

Function	Explanation
DCDC Undervoltage (VREG UVLO)	When the VREG pin voltage falls to 3.5 V (typ.) or lower, an undervoltage condition is detected, the DCDC output is stopped, and the IC transitions to Standby mode.
DCDC Overvoltage (VREG OVP)	When the VREG pin voltage rises to 5.75 V (typ.) or higher, an overvoltage condition is detected, the DCDC output is stopped, and the IC transitions to Standby mode.
DCDC Overcurrent (SW ISD)	When a current of 1.25 A (typ.) or higher is detected in the internal output stage, the DCDC output is stopped, and the IC transitions to Standby mode.

11.4.3.4. VM Undervoltage Lock Out (VM_UVLO)

The IC incorporates a VM supply voltage monitoring function.
When the voltage falls below the threshold, an undervoltage lock out (UVLO) condition is detected and the output is turned OFF.
UVLO detection is followed by automatic recovery. When the voltage rises into the operating range of the IC, the UVLO condition is released.

11.4.3.5. Hall Signal Abnormality

In the case of 3-Hall, when the position detection signals HU/HV/HW become All-High or All-Low, it is detected as a Hall signal abnormality.
After detection, the output is turned OFF, and the IC restarts from free-run detection with any other signal combination.

Hall signal abnormality detection is not output from the ALERT pin.

11.4.3.6. Motor Lock Detection (LOCK)

For 3-Hall and 1-Hall drive, during Closed loop or Open loop control, if the Hall signal reset timing is not detected for a certain period (t_{ON} or longer), the condition is recognized as a Motor Lock state.
After a lock is detected, the IC turns OFF the output for a fixed period (t_{RE}) and then automatically recovers.
The lock detection time (t_{ON}) and the output-OFF time (t_{RE}) can be configured using register settings.

Table 11.59 Lock Detection Time

Register: 5[7] TON	Lock detection time (s)
0b (Default)	0.3
1b	0.6

By issuing a speed command that causes the output to stop, the IC can be transitioned to Idle mode.
While in Idle mode, if a speed control command to restart the output is detected, the IC can restart without waiting for the t_{RE} period.

When latch mode is selected, the IC transitions to Idle mode, and when a speed control command to restart the output is detected during Idle mode, the latch is released and the IC restarts.

The ALERT signal is cleared after transitioning to Open loop or Closed loop control.

11.4.3.7. Startup Failure (ST_FAIL)

If the transition from soft start to normal rotation cannot be completed within a specified time, a startup failure is detected.
However, the DC excitation period is excluded from the startup failure detection count.

- 3-Hall: Time from 1 Hz forced commutation to SS_FREQ or higher
  (time from SPD input to SS_FREQ or higher)
- 1-Hall: Time from 1 Hz forced commutation to SS_FREQ or higher
  (time from SPD input to SS_FREQ or higher)
- Sensorless: Time from the start of forced commutation (f_{FORCE}) to SS_FREQ or higher

Table 11.60 Startup Failure Detection Time

Register: 5[3:2] TST	Startup failure detection time (s)
00b (Default)	0.6
01b	1.5
10b	3.0
11b	6.0

For sensorless drive, the detection also depends on the setting of the forced commutation frequency (f_{FORCE}).

When a start-up failure is detected, the IC stops the output for a fixed period (t_{RE}) and then automatically recovers.
By applying a speed command that causes the output to stop, the IC can be transitioned to Idle mode.
While in Idle mode, if a speed control command to restart the output is detected, the IC can restart without waiting for the t_{RE} period.

When latch mode is selected, the IC transitions to Idle mode, and when a speed control command to restart the output is detected during Idle mode, the latch is released and the IC restarts.

The ALERT signal is cleared after transitioning to Open loop or Closed loop control.

11.4.3.8. Under Speed Detection (UD_SPD)

For sensorless drive, when the motor speed decreases and falls to the forced commutation frequency (f_{FORCE}) or lower, an under-speed abnormality is detected.
When an under-speed abnormality is detected, the IC stops the output for a fixed period (t_{RE}) and then automatically recovers.

Table 11.61 Setting of Forced Commutation Frequency

Register: 10[7:6] FST	Forced commutation frequency f_{FORCE} (Hz)
00b (Default)	1.6
01b	3.2
10b	6.4
11b	12.8

By applying a speed command that causes the output to stop, the IC can be transitioned to Idle mode.
While in Idle mode, if a speed control command to restart the output is detected, the IC can restart without waiting for the t_{RE} period.

When latch mode is selected, the IC transitions to Idle mode, and when a speed control command to restart the output is detected during Idle mode, the latch is released and the IC restarts.

The ALERT signal is cleared after transitioning to Open loop or Closed loop control.

11.4.3.9. Over Speed Detection (OV_SPD)

For sensorless drive, when the motor speed exceeds the maximum rotation frequency setting, an over-speed abnormality is detected.
When an over-speed abnormality is detected, the IC stops the output for a fixed period (t_{RE}) and then automatically recovers.

Table 11.62 Setting of Over Speed Detection

Register: 5[1:0] FMAX	Over speed detection frequency (kHz)
00b (Default)	0.75
01b	1.5
10b	3.0
11b	4.5

By applying a speed command that causes the output to stop, the IC can be transitioned to Idle mode.
While in Idle mode, if a speed control command to restart the output is detected, the IC can restart without waiting for the t_{RE} period.

When latch mode is selected, the IC transitions to Idle mode, and when a speed control command to restart the output is detected during Idle mode, the latch is released and the IC restarts.

The ALERT signal is cleared after transitioning to Open loop or Closed loop control.

11.4.3.10. VM Overvoltage Protection (OVP)

The IC incorporates a power supply overvoltage detection function.
This function prevents abnormal voltage from being applied to the motor. When a power supply voltage increase (overvoltage) is detected, the output can be turned OFF. When the voltage falls below the recovery voltage, the output can be restarted. When restarting the output, refer to the start-up sequence.

Table 11.63 Setting of Overvoltage Protection

Register 6:[7:4] OVP_LVL	Detection voltage			Release voltage		
	Min	Typ.	Max	Min	Typ.	Max
0000b (Default)	13.7	15.0	16.3	12.3	13.5	14.7
0001b	15.1	16.5	17.9	13.7	15.0	16.3
0010b	16.5	18.0	19.5	15.1	16.5	17.9
0011b	17.9	19.5	21.1	16.5	18.0	19.5
0100b	19.3	21.0	22.7	17.9	19.5	21.1
0101b	20.7	22.5	24.3	19.3	21.0	22.7
0110b	22.0	24.0	26.0	20.7	22.5	24.3
0111b	23.5	25.5	27.5	22.0	24.0	26.0
1000b	24.8	27.0	29.2	23.5	25.5	27.5
1001b	26.3	28.5	30.7	24.8	27.0	29.2
1010b	27.7	30.0	32.3	26.3	28.5	30.7
1011b	30.5	33.0	35.5	27.7	30.0	32.3
1100b	33.3	36.0	38.7	30.5	33.0	35.5
1101b	36.1	39.0	41.9	33.3	36.0	38.7
1110b	38.9	42.0	45.1	36.1	39.0	41.9
1111b	41.7	45.0	48.3	38.9	42.0	45.1

The mask time for overvoltage detection can be configured using the same register as OCL.

Table 11.64 Mask Time of OVP Detection

Register: 7[1] ERR_MASK	Mask time (ns)
0b (Default)	500
1b	750

11.4.3.11. Overcurrent Shutdown Detection (ISD)

To detect and limit excessive current flow through the IC, the currents flowing through the output-stage MOSFETs are individually monitored.
When the current exceeds the threshold, the entire output stage is turned OFF.
By register settings, automatic recovery or latch mode can be selected.
In automatic recovery mode, the output automatically recovers after the output-OFF period (t_{RE}).
In latch mode, after an output overcurrent is detected, the entire output stage remains OFF.
The latch can be released by transitioning to Idle mode or by reapplying the power supply.
After the output restarts and transitions to Open loop or Closed loop control, the error flags and the ALERT signal are cleared.
The mask period for ISD detection can be configured using the same register as OCL.

Table 11.65 Mask Time of ISD Detection

Register: 7[1] ERR_MASK	Mask time (ns)
0b (Default)	500
1b	750

11.4.3.12. Thermal Shutdown Detection (TSD)

The IC incorporates a thermal shutdown (TSD) circuit.
When the junction temperature (T_j) reaches 165 °C (typ.) or higher, the TSD circuit operates and turns OFF the entire output stage.
In automatic recovery mode, after the t_{RE} period has elapsed and the temperature falls to 135 °C (typ.) or lower, the IC recovers automatically.
In latch mode, after a thermal shutdown is detected, the entire output stage remains OFF.
The latch can be released by transitioning to Idle mode or by reapplying the power supply, and recovery occurs when the temperature falls to 135 °C (typ.) or lower.
After recovery and transition to Open loop or Closed loop control, the error flags and the ALERT signal are cleared.

11.5. Serial I/F and NVM

Various parameters can be set by accessing the registers inside the IC via the serial I/F. The set parameters can also be saved in NVM.

11.5.1. Communication Format

The internal registers can be accessed via the serial I/F. The start condition, stop condition, and data changeable period during communication are shown below.

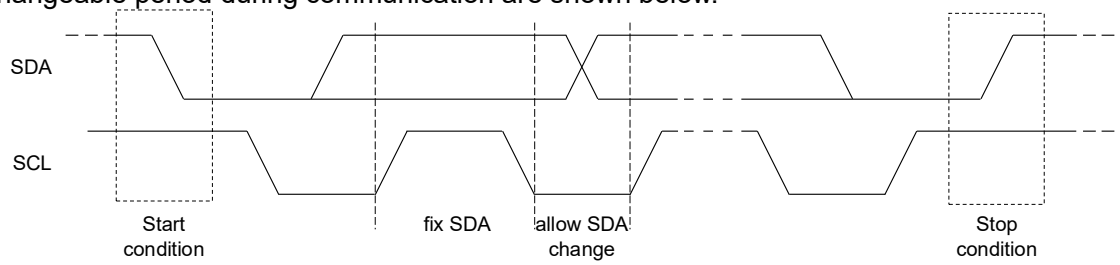
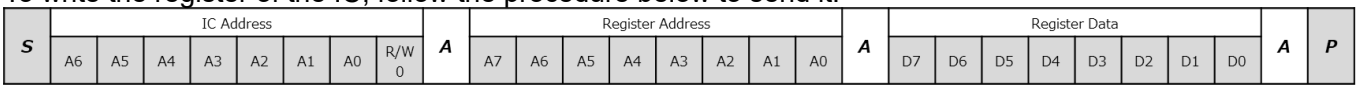


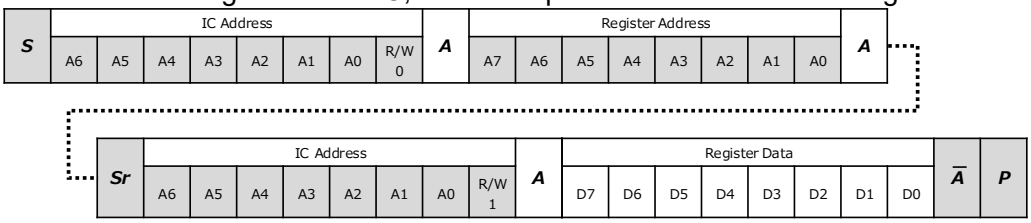
Figure 11.34 Timing Chart

To write the register of the IC, follow the procedure below to send it.



S: Start condition
A: Acknowledge
P: Stop condition
Upper microcontroller to IC
IC to upper microcontroller

To read out the register of the IC, follow the procedure below for sending and receiving.



S: Start condition
A: Acknowledge
Ā: Not Acknowledge
Sr: Start condition (repeat start condition)
P: Stop condition
Upper microcontroller to IC
IC to upper microcontroller

11.5.2. Register Details

Table 11.66 Register Details

Address	Bit	Name	Description	R/W	Initial value	NVM
0	7	VM_UVLO	VM undervoltage lock out flag (0: Normal, 1: Fault)	R	0	—
	6	VM_OVP	VM overvoltage protection flag (0: Normal, 1: Fault)	R	0	—
	5	ISD	Overcurrent shutdown flag (0: Normal, 1: Fault)	R	0	—
	4	TSD	Thermal shutdown flag (0: Normal, 1: Fault)	R	0	—
	3	LOCK	Motor lock flag (0: Normal, 1: Locked)	R	0	—
	2	ST_FAIL	Startup failure flag (0: Normal, 1: Startup failure)	R	0	—
	1	UD_SPD	Under speed detection flag (0: Normal, 1: Fault)	R	0	—
	0	OV_SPD	Over speed detection flag (0: Normal, 1: Fault)	R	0	—
1	7:6	SPD_SEL [1:0]	SPD command type	R/W	00	Yes
	5	SPD_INV	SPD input polarity (0: Normal logic, 1: Inverted logic)	R/W	0	Yes
	4	DIR_INV	DIR input polarity (0: Normal logic, 1: Inverted logic)	R/W	0	Yes
	3	BRK_INV	BRAKE input polarity (0: Normal logic, 1: Inverted logic)	R/W	0	Yes
	2		Reserved (Please do not change)	R/W	1	Yes
	1	HALL_INV	Hall signal polarity (0: Normal logic, 1: Inverted logic)	R/W	0	Yes
	0	HALL_PU	HU/HV/HW pin pull-up resistor (0: Disabled, 1: Enabled)	R/W	0	Yes
2	7:5	FG_SEL [2:0]	FG pulse select setting	R/W	000	Yes
	4:2	FG_ON [2:0]	FG output condition setting	R/W	000	Yes
	1	FG_PORT	FG/ALERT output signal setting	R/W	0	Yes
	0	STBY	Standby mode setting (0: Disabled, 1: Enabled)	R/W	0	Yes
3	7	ALT_UVLO	VM UVLO fault output (0: Do not output, 1: Output)	R/W	0	Yes
	6	ALT_OVP	VM OVP fault output (0: Do not output, 1: Output)	R/W	0	Yes
	5	ALT_ISD	ISD fault output (0: Do not output, 1: Output)	R/W	0	Yes
	4	ALT_TSD	TSD fault output (0: Do not output, 1: Output)	R/W	0	Yes
	3	ALT_LOCK	LOCK, ST_FAIL, UD_SPD fault output (0: Do not output, 1: Output)	R/W	0	Yes
	2	ALT_OVS	OV_SPD fault output (0: Do not output, 1: Output)	R/W	0	Yes
	1	REP_HSPD	Speed limit detection output (0: Do not output, 1: Output)	R/W	0	Yes
	0	ALERT_INV	ALERT signal polarity setting (0: L=Fault, 1: Hi-Z=Fault)	R/W	0	Yes
4	7	DIS_VM_UVLO	VM UVLO fault mask (0: Fault detection enabled, 1: Fault detection disabled)	R/W	0	Yes
	6	DIS_OVP	VM OVP fault mask (0: Fault detection enabled, 1: Fault detection disabled)	R/W	0	Yes
	5	DIS_ISD	ISD fault mask (0: Fault detection enabled, 1: Fault detection disabled)	R/W	0	Yes
	4	DIS_TSD	TSD fault mask (0: Fault detection enabled, 1: Fault detection disabled)	R/W	0	Yes
	3	DIS_LOCK	LOCK, ST_FAIL, UD_SPD fault mask (0: Fault detection enabled, 1: Fault detection disabled)	R/W	0	Yes
	2	DIS_OVSPD	OV_SPD mask (0: Fault detection enabled, 1: Fault detection disabled)	R/W	0	Yes
	1	DIS_OCL	Output current limit mask (0: OCL enabled, 1: OCL disabled)	R/W	0	Yes
	0	LATCH	Recovery mode (0: Automatic recovery, 1: Latch mode)	R/W	0	Yes

Address	Bit	Name	Description	R/W	Initial value	NVM
5	7	TON	Lock detection time (0: 0.3 s, 1: 0.6 s)	R/W	0	Yes
	6:4	TRE [2:0]	Automatic recovery time	R/W	000	Yes
	3:2	TST [1:0]	Startup failure detection time	R/W	00	Yes
	1:0	FMAX [1:0]	Over speed detection frequency	R/W	00	Yes
6	7:4	OVP_LVL [3:0]	OVP detection voltage/recovery voltage setting	R/W	0000	Yes
	3	CYC_CHG	Deceleration judgment (0: Deceleration judgment enabled, 1: Deceleration judgment disabled)	R/W	0	Yes
	2	OCL_ACT	Operation after OCL detection (sine wave drive only)	R/W	0	Yes
	1:0	OCL_VTH [1:0]	OCL detection internal reference voltage	R/W	00	Yes
7	7:5	WAIT_TIME [2:0]	Wait sequence time	R/W	000	Yes
	4		Reserved (Please do not change)	R/W	0	Yes
	3	WAIT_MODE	Wait sequence operation (0: Hi-Z, 1: Short brake)	R/W	0	Yes
	2	WAIT_CON	State after wait sequence	R/W	0	Yes
	1	ERR_MASK	Detection mask time	R/W	0	Yes
	0	PLB_ENB	Power-off shutdown brake (0: Disabled, 1: Enabled)	R/W	0	Yes
8	7:4	WAVE_TYPE [3:0]	Drive type setting	R/W	0000	Yes
	3	120DELTA	0: No change, 1: Advance 60° during CCW	R/W	0	Yes
	2:0	FPWM [2:0]	Output PWM frequency setting	R/W	000	Yes
9	7:5	SS_FREQ [2:0]	Soft start switching frequency	R/W	000	Yes
	4:2	SS_CUR [2:0]	Startup current	R/W	000	Yes
	1	SS_DC	(Please do not change)	R/W	0	Yes
	0	REV_ST	Startup from reverse rotation (0: Disabled, 1: Enabled)	R/W	0	Yes
10	7:6	FST [1:0]	Forced commutation frequency setting	R/W	00	Yes
	5	CHG_INTV	Duty change unit time (0: 2.7 ms, 1: 10.8 ms)	R/W	0	Yes
	4:3	DC_CUR [1:0]	DC excitation current	R/W	00	Yes
	2:0	TIP [2:0]	DC excitation time	R/W	000	Yes
11	7:5	SS_DUTY_CL [2:0]	Acceleration/deceleration speed setting during soft start	R/W	000	Yes
	4:2	DUTY_CL [2:0]	Open loop / Closed loop acceleration/deceleration speed setting	R/W	000	Yes
	1:0	COMP_HYS [1:0]	Hysteresis voltage of position detection comparator during free running	R/W	00	Yes
12	7:6	OUT_SR [1:0]	Output slew rate adjustment	R/W	00	Yes
	5:3		Reserved (Please do not change)	R/W	0	Yes
	2:0	LA_TYPE [2:0]	Lead angle type setting	R/W	000	Yes
13	7	LA_REF	Lead angle control reference (0: Output duty reference, 1: SPD command reference)	R/W	0	Yes
	6:0	LA [6:0]	Lead angle setting	R/W	ALL0	Yes
14	7:0	LA_MAXSPD [7:0]	SPD value for maximum lead angle	R/W	ALL0	Yes
15	7:0	LA_CHGSPD [7:0]	SPD value of quadratic curve inflection point / IPC operation start point	R/W	ALL0	Yes
16	7:0	LA_OFFSET [7:0]	LA offset and SPD offset setting	R/W	ALL0	Yes
17	7	SEN_TYPE	Sensor setting (0: With sensor, 1: Sensorless)	R/W	0	Yes
	6:0	IC_ADDR [6:0]	IC address for serial communication	R/W	0101001	Yes

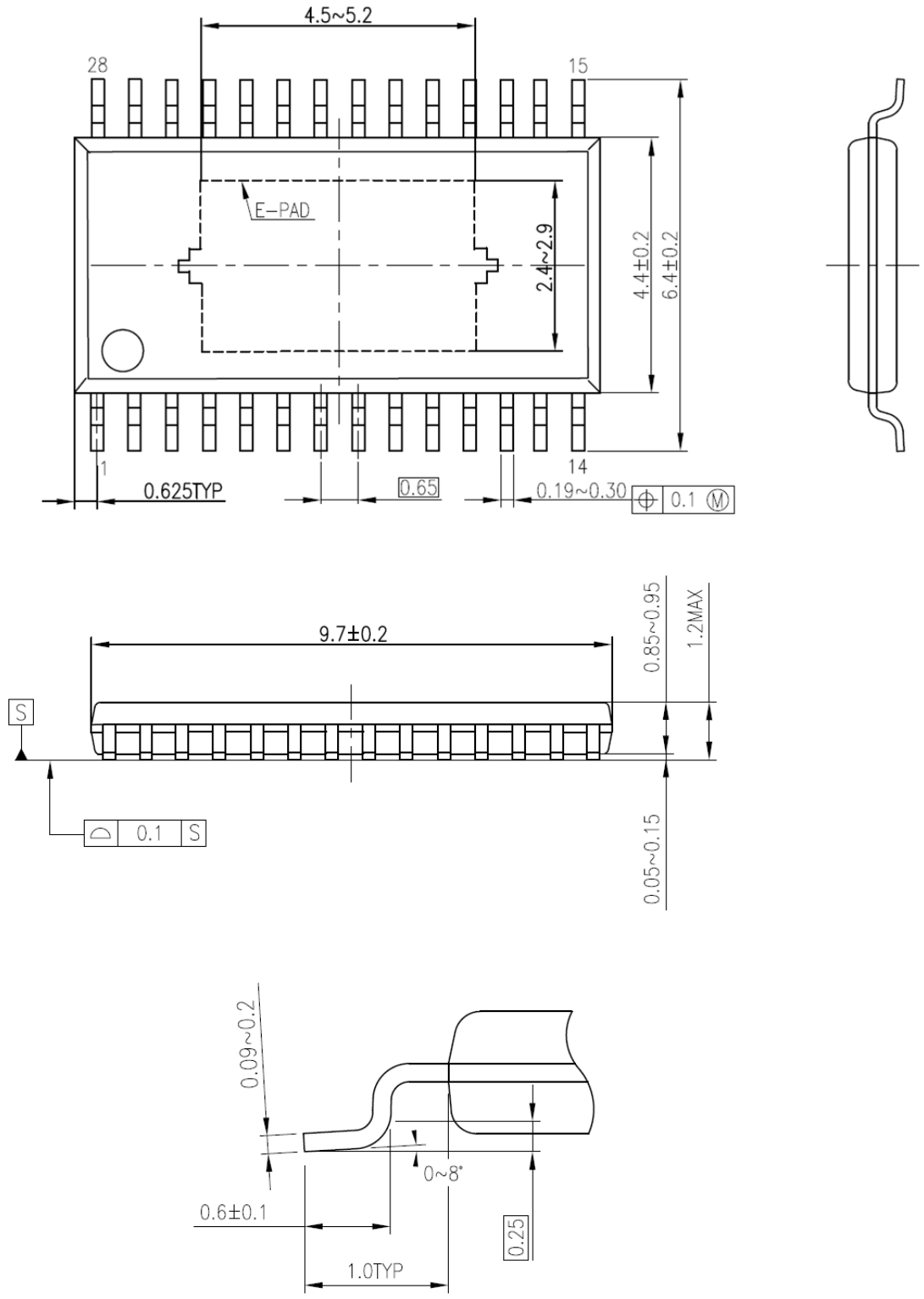
Address	Bit	Name	Description	R/W	Initial value	NVM
18	7:5	POLE_PAIR [2:0]	Motor pole pair setting	R/W	000	Yes
	4:3	DN_LIM [1:0]	Target rotation speed variation during deceleration	R/W	00	Yes
	2:0	RPM_RANGE [2:0]	Rotation speed range setting	R/W	000	Yes
19	7:0	MAX_RPM [7:0]	Maximum rotation speed setting	R/W	ALL0	Yes
20	7:0	MAX_RPM [15:8]	Maximum rotation speed setting	R/W	ALL0	Yes
21	7:0	ST_DUTY [7:0]	Start duty = ST_DUTY	R/W	ALL0	Yes
22	7:0	ST_RPM [7:0]	Start RPM = MAX_RPM×ST_RPM / 256	R/W	ALL0	Yes
23	7:0	STOP_DUTY [7:0]	Stop duty = STOP_DUTY	R/W	ALL0	Yes
24	7:0	MAX_DUTY [7:0]	Max duty = MAX_DUTY +257	R/W	ALL0	Yes
25	7:6	KPX [1:0]	Kp gain multiplier (00: x2, 01: x8, 10: x32, 11: x64)	R/W	00	Yes
	5:0	KP [5:0]	Kp gain	R/W	ALL0	Yes
26	7:6	KIX [1:0]	Ki gain multiplier (00: x2, 01: x8, 10: x32, 11: x64)	R/W	00	Yes
	5:0	KI [5:0]	Ki gain	R/W	ALL0	Yes
27	7	OPENLOOP	0: Closed loop, 1: Open loop	R/W	0	Yes
	6	NOSTOP	Non-stop mode (0: Disabled, 1: Enabled)	R/W	0	Yes
	5	MAXOFF	Full speed when SPD command OFF (0: Disabled, 1: Enabled)	R/W	0	Yes
	4	MAXOPEN	Open loop above maximum duty (0: Disabled, 1: Enabled)	R/W	0	Yes
	3:0	MAXDUTY_HYS [3:0]	Hysteresis for open loop ⇔ closed loop	R/W	0000	Yes
28	7	P1_ENB	Inflection point 1 (0: Disabled, 1: Enabled)	R/W	0	Yes
	6:0	P1_DUTY [6:0]	Duty setting for inflection point 1	R/W	0	Yes
29	7:0	P1_RPM [7:0]	Rotation speed setting for inflection point 1	R/W	0	Yes
30	7	P2_ENB	Inflection point 2 (0: Disabled, 1: Enabled)	R/W	0	Yes
	6:0	P2_DUTY [6:0]	Duty setting for inflection point 2	R/W	0	Yes
31	7:0	P2_RPM [7:0]	Rotation speed setting for inflection point 2	R/W	0	Yes
32	7	P3_ENB	Inflection point 3 (0: Disabled, 1: Enabled)	R/W	0	Yes
	6:0	P3_DUTY [6:0]	Duty setting for inflection point 3	R/W	0	Yes
33	7:0	P3_RPM [7:0]	Rotation speed setting for inflection point 3	R/W	0	Yes
34	7	P4_ENB	Inflection point 4 (0: Disabled, 1: Enabled)	R/W	0	Yes
	6:0	P4_DUTY [6:0]	Duty setting for inflection point 4	R/W	0	Yes
35	7:0	P4_RPM [7:0]	Rotation speed setting for inflection point 4	R/W	0	Yes
36	7	P5_ENB	Inflection point 5 (0: Disabled, 1: Enabled)	R/W	0	Yes
	6:0	P5_DUTY [6:0]	Duty setting for inflection point 5	R/W	0	Yes
37	7:0	P5_RPM [7:0]	Rotation speed setting for inflection point 5	R/W	0	Yes
38	7:0	SPD [7:0]	Speed command	R/W	0	—
39	7:6	SPD [9:8]	Speed command	R/W	0	—
40	7:0	HZ_CNT [7:0]	Rotation frequency	R	0	—
41	7:0	HZ_CNT [15:8]	Rotation frequency	R	0	—
86	0	NVM_WR	NVM READ/WRITE (0: READ enabled, 1: WRITE enabled)	R/W	0	—
87	0	NVM_ST	NVM processing (0: Processing completed, 1: Processing started)	R/W	0	—

12. Package Information

12.1. Package Dimensions of TB67B030FNG

P-HTSSOP28-0510-0.65-001

Unit: mm



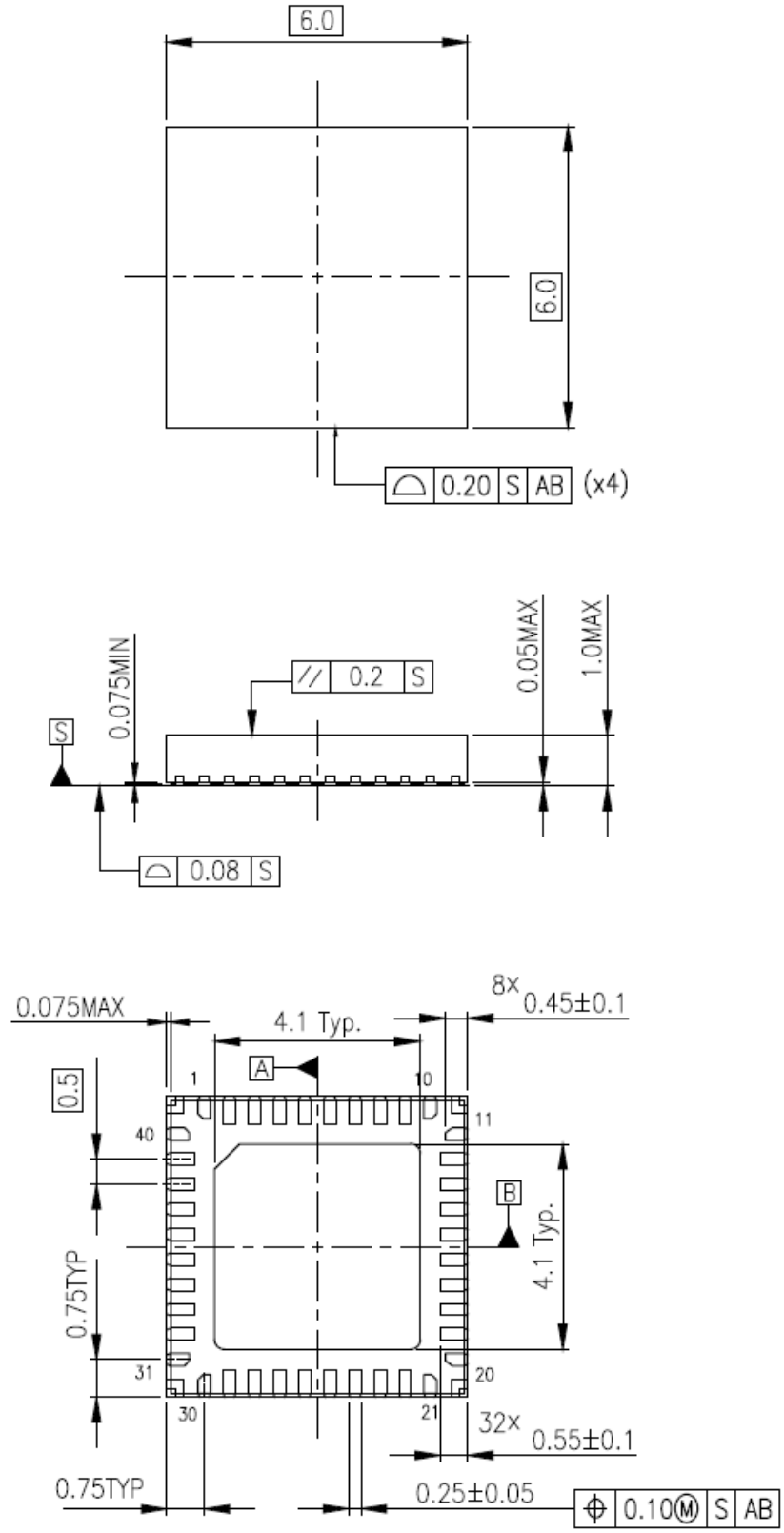
Weight: (0.107 g)

Figure 12.1 Package Dimensions of TB67B030FNG

12.2. Package Dimensions of TB67B030FTG

P-VQFN40-0606-0.50-003

Unit: mm



Weight: (0.091 g)

Figure 12.2 Package Dimensions of TB67B030FTG

13. Notes on Contents

Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Input / Output Equivalent Circuit

The equivalent circuit diagrams may be simplified for explanatory purposes.

Timing Charts

Timing charts may be simplified for explanatory purposes.

Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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14. IC Usage Considerations

14.1. Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator. If there is a large amount of leakage current such as from input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure may cause smoke or ignition. (The overcurrent may cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection-type IC that inputs output DC voltage to a speaker directly.

14.2. Points to Remember on Handling of ICs

(1) Overcurrent Protection Circuit
Overcurrent protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Overcurrent protection circuits operate against the over current, clear the over current status immediately.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature clears the heat generation status immediately.

(3) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF
When a motor reverses the rotation direction, stops or slows down abruptly, a current flow back to the motor’s power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device’s motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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