1.6kW 48V Output Telecommunication Equipment Power Supply (Upgraded)

Design Guide

RD250-DGUIDE-01

Toshiba Electronic Devices & Storage Corporation

Table of Contents

1. Introduction

This design guide describes the design overview of each circuit block of the 1.6kW 48V Output Telecommunication Equipment Power Supply (Upgraded) (hereinafter referred to as "this design").

This design is a power supply for telecommunications equipment that converts an AC input voltage of 90V to 264V into a 48V DC output with a maximum power rating of 1.6kW. It employs a semi-bridgeless Power Factor Correction (PFC) topology and an isolated Phase Shifted Full Bridge (PSFB) converter to achieve highly efficient power conversion.

In addition, the output stage incorporates an ORing circuit, enabling highly reliable operation in an N+1 redundant power system configuration. By utilizing compact components, the design can be adapted to a variety of form factors and applications, including standard 1U power supplies. High-speed switching Toshiba power MOSFETs are used as the switching devices, enabling both high efficiency and high power density.

The semi-bridgeless PFC stage employs the TK125N60Z1 power MOSFET as the switching device and the TRS8A65F SiC Schottky Barrier Diode (SBD) in the boost section. The PSFB converter uses the TK095N65Z5 power MOSFETs on the primary side and the TPM7R10CQ5 power MOSFETs for secondary-side synchronous rectification. Signal transmission between the primary and secondary sides of the PSFB converter is achieved using the DCL540C01 digital isolator. The output ORing circuit employs the TPM1R908QM power MOSFET.

By incorporating these latest Toshiba devices, this design achieves higher efficiency than the previous 1.6 kW 48V Power Supply for Telecommunications Equipment, which employed the same circuit topology and was released in March 2021, resulting in an even more efficient power supply solution.

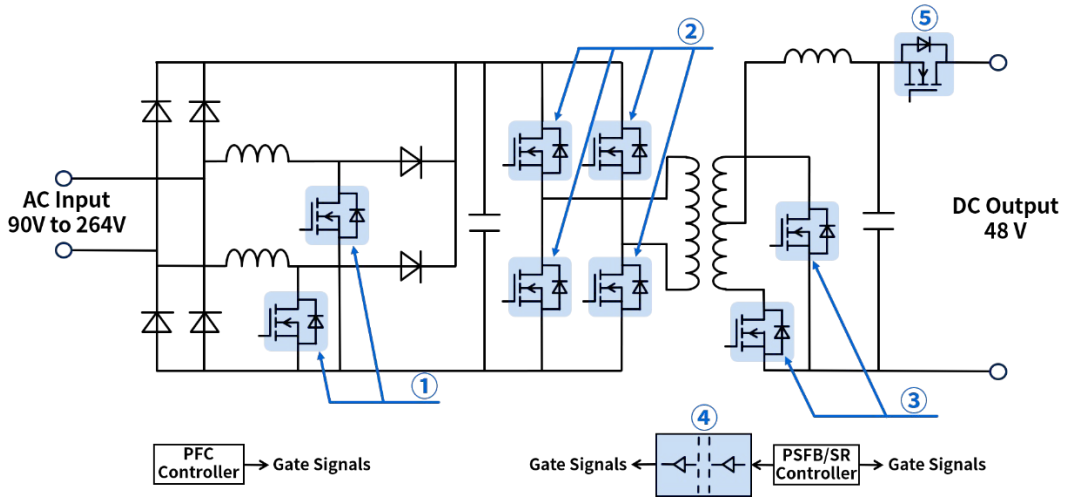

Figure 1.1 Block Diagram

Table 1.1 Updated Toshiba Devices

No.	Existing design	This upgraded design	Updates
①	TK25N60X	TK125N60Z1	DTMOS IV→VI
②	TK25N60X5	TK095N65Z5	DTMOS IV→VI
③	TPH2900ENH	TPM7R10CQ5	UTMOS VIII→X
④	TLP2767	DCL540C01	Photocoupler → Digital Isolator
⑤	TPH2R408QM	TPM1R908QM	Lower $R_{DS(on)}$ device (same generation)

Table 1.1 lists the major Toshiba devices that were updated in this upgraded design.

By optimizing the primary-side and secondary-side switching devices and their associated components, the conversion efficiency under the conditions of V_{in} = 230V and 100% load improved from 94.46% to 95.52%, achieving approximately a 1% increase in efficiency. In addition, power loss was reduced by approximately 20%, resulting in a more efficient 48V output power supply.

2. Main Components

This chapter describes the main components used in this design.

2.1. Power MOSFET TK125N60Z1

This design uses the Power MOSFET (TK125N60Z1) as the switching device in the semi-bridgeless PFC circuit. The main features of the TK125N60Z1 are as follows.

- Low ON-state resistance due to the Super Junction DTMOS structure: $R_{DS(on)}$ = 0.105Ω (typ.)
- Fast switching capability resulting from low device capacitance.
- Enhancement-mode device for simplified handling and drive circuitry: V_{th} = 3 to 4V (V_{DS} = 10V, I_D = 0.73mA)

Appearance and Terminal Layout

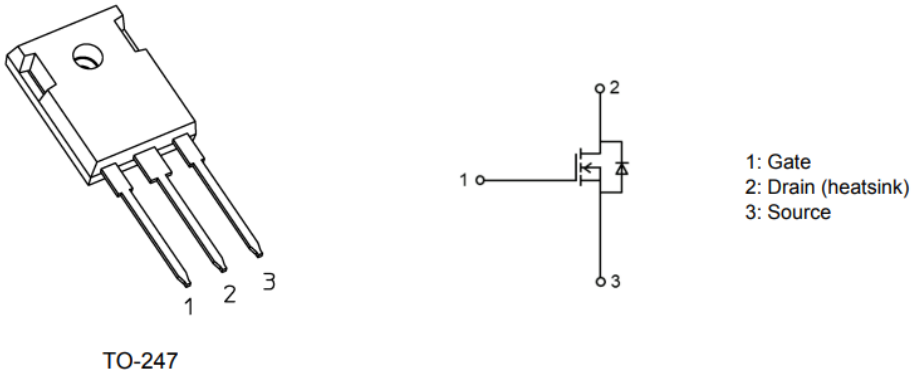

Figure 2.1 Appearance and Terminal Layout of TK125N60Z1

2.2. Power MOSFET TK095N65Z5

This design uses the Power MOSFET (TK095N65Z5) as the primary-side switching device in the PSFB converter. The main features of the TK095N65Z5 are as follows.

- Low ON-state resistance enabled by the Super Junction DTMOS structure: $R_{DS(on)}$ = 0.105Ω (typ.)
- Fast switching performance achieved through low capacitance characteristics.
- Enhancement-mode device for simplified gate-drive implementation: V_{th} = 3 to 4V (V_{DS} = 10V, I_D = 0.73mA)

Appearance and Terminal Layout

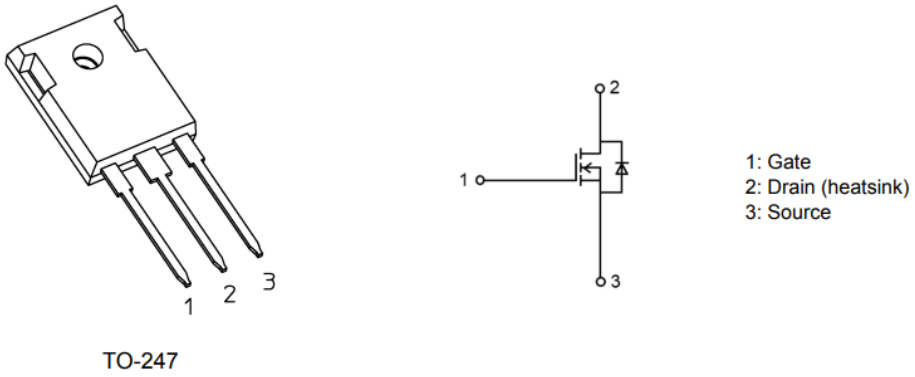

Figure 2.2 Appearance and Terminal Layout of TK095N65Z5

2.3. Power MOSFET TPM7R10CQ5

This design uses the Power MOSFET (TPM7R10CQ5) for secondary-side synchronous rectification in the PSFB converter. The main features of the TPM7R10CQ5 are as follows.

- Fast reverse recovery characteristics: t_{rr} = 45ns (typ.)
- Low reverse recovery charge: Q_{rr} = 43nC (typ.)
- Low gate switching charge: Q_{SW} = 18nC (typ.)
- Low ON-state resistance: $R_{DS(on)}$ = 5.7mΩ (typ.) at V_{GS} = 10V
- Low leakage current: I_{DSS} = 10μA (max) at V_{DS} = 150V
- Enhancement-mode device for simplified gate-drive implementation: V_{th} = 3.1 to 4.5V (V_{DS} = 10V, I_D = 1.2mA)

Appearance and Terminal Layout

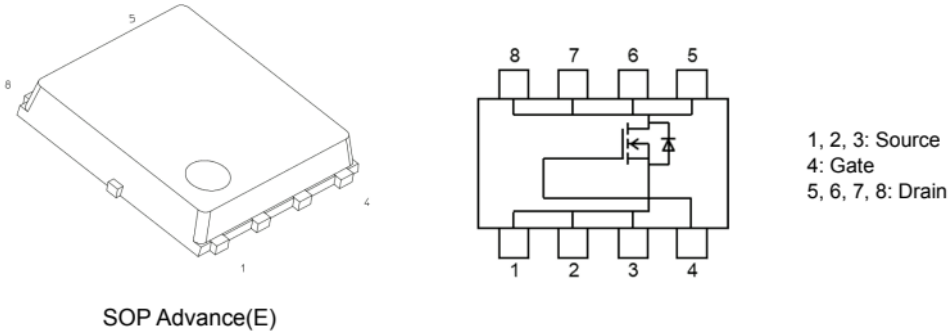

Figure 2.3 Appearance and Terminal Layout of TPM7R10CQ5

2.4. Power MOSFET TPM1R908QM

This design uses the Power MOSFET (TPM1R908QM) in the output ORing circuit. The main features of the TPM1R908QM are as follows.

- Fast switching performance.
- Low gate switching charge: Q_{SW} = 35nC (typ.)
- Low output charge: Q_{oss} = 111nC (typ.)
- Low ON-state resistance: $R_{DS(on)}$ = 1.5mΩ (typ.) at V_{GS} =10V
- Low leakage current: I_{DSS} = 10μA (max) at V_{DS} = 80V
- Enhancement-mode device for simplified gate-drive implementation: V_{th} = 2.5 to 3.5V (V_{DS} = 10V, I_D = 1.2mA)

Appearance and Terminal Layout

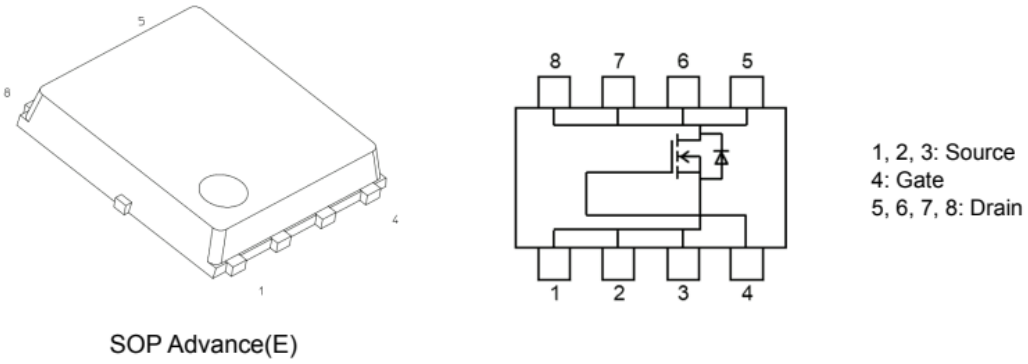

Figure 2.4 Appearance and Terminal Layout of TPM1R908QM

2.5. SiC Schottky Barrier Diode TRS8A65F

This design uses the SiC Schottky Barrier Diode (SBD) (TRS8A65F) as the boost diode in the semi-bridgeless PFC circuit. The main features of the TRS8A65F are as follows.

- Incorporates a second-generation chip design
- High surge current capability: I_{FSM} = 65A (max)
- Low junction capacitance: C_j = 28pF (typ.)
- Low leakage current: I_R = 0.4μA (typ.)
- Isolated package: TO-220F-2L

Appearance and Terminal Layout

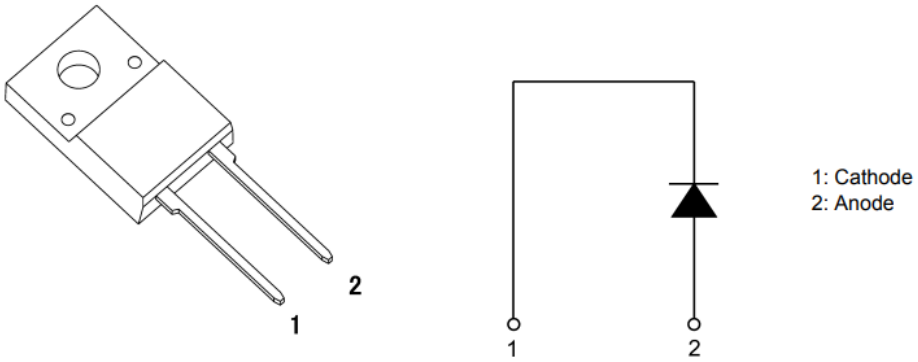

Figure 2.5 Appearance and Terminal Layout of TRS8A65F

2.6. Digital Isolator DCL540C01

This design uses the 4-channel digital isolator (DCL540C01) for signal transmission between the primary and secondary sides of the PSFB converter. The main features of the DCL540C01 are as follows.

- High data transmission rate: 150Mbps (max)
- Wide supply voltage range: 2.25V to 5.5V
- Wide operating temperature range: −40°C to 110°C
- Low propagation delay: 10.9ns (typ.) at V_{DD} = 5.0V
- Default output options: High or Low
- High common-mode transient immunity (CMTI): ±100kV/μs
- High isolation withstand voltage: 5kV_{rms}
- Safety Certifications:
  UL : UL1577, File No. E519997
  cUL : CSA Component Acceptance Service Notice No. 5A, File No. E519997
  VDE : DIN VDE V 0884-11(VDE V 0884-11) Certificate No. 40055132
  CQC : GB 4943.1-2022 Certificate No. CQC22001345018

Appearance and Terminal Layout

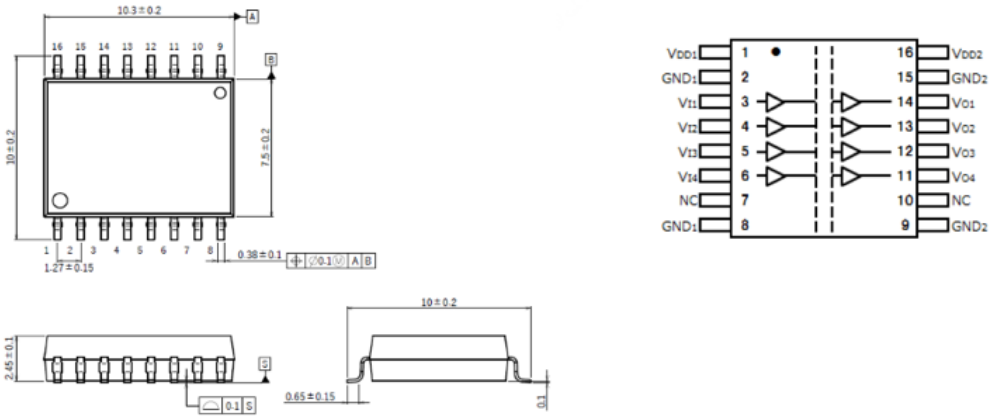

Figure 2.6 Appearance and Terminal Layout of DCL540C01

3. Circuit Design

This chapter describes the key circuit design considerations.

3.1. AC Line Circuit Design

This section describes the design of the AC input line circuit used in this design. The AC line circuit is shown in Figure 3.1.

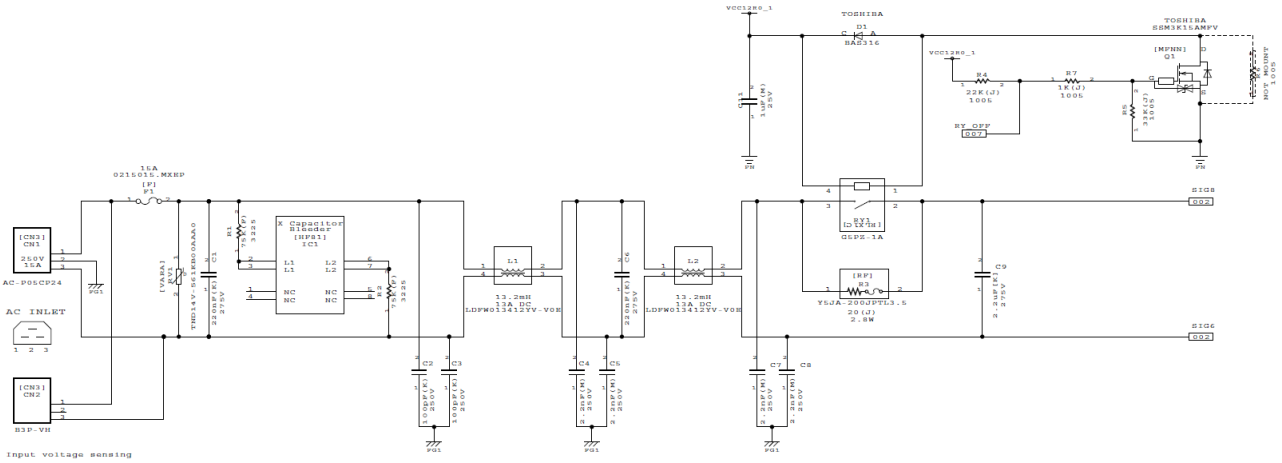

Figure 3.1 AC Line Circuit Design

Fuse

Fuse F1 is provided in the AC input line to protect the circuit by disconnecting the AC line when an abnormal current flows. The fuse rating is selected based on the maximum AC input current. The RMS value of the maximum AC input current is calculated as follows.

$$\textbf{Maximum AC Input Current (RMS)} = \frac{\textbf{Maximum Output Power}}{\textbf{Power Supply Efficiency} \times \textbf{Power Factor} \times \textbf{Minimum RMS Input Voltage}}$$

This design is rated as 1.6kW output when operated from a 200V AC input system and 800W output when operated from a 100V AC input system. If the efficiency of the PFC stage remained constant regardless of the input voltage, the maximum AC line input current would be the same at all input voltages. In practice, however, PFC efficiency generally decreases as the input voltage decreases. Therefore, the maximum AC line current is calculated using the minimum input voltage of the 100V AC input range, namely 90V.

Assuming a minimum input voltage (RMS) of 90V, a maximum output power of 800W, a power conversion efficiency of 93%, and a power factor of 0.99, the maximum AC line current of this design is approximately 10A.

In this design, a 15A fuse is selected to provide sufficient design margin. When selecting a fuse, it is also necessary to consider factors such as the inrush current generated during AC power-on and whether the fuse complies with the applicable safety standards required for the end product.

Varistor

A ceramic varistor (RV1) is implemented in the AC input line to protect the system from surge voltages caused by events such as lightning-induced surges. The varistor is selected based on the voltage rating of the AC input line.

In this design, the maximum AC line voltage is 264V RMS, corresponding to a peak voltage of 373V. Taking sufficient design margin into account, a varistor with a maximum allowable circuit voltage of 350V AC and a varistor voltage of 560V is used.

When selecting a varistor, it is necessary to consider not only the voltage ratings described above, but also factors such as surge current capability and energy absorption capability.

In addition, because the most common failure mode of a varistor is short-circuit failure, it is recommended to install a fuse on the upstream side (AC input side) when incorporating a varistor into the design.

X Capacitor Discharge Circuit

To prevent the risk of electric shock when the AC input is disconnected, the charge stored in the X capacitors (C1, C6, and C9) must be discharged promptly.

In this design, the HF81 is used as the X-capacitor discharge IC. Since this IC disconnects the discharge path while AC power is present, it contributes to improved system power efficiency.

When AC power is removed, the IC and its external resistors (R1 and R2) form a discharge circuit that discharges the charge stored in the X capacitors, reducing the capacitor voltage to 37% or less of its initial value within 1 second.

Because this design incorporates approximately 2.6μF of X capacitance, external resistors of 75kΩ × 2 are used to provide the required discharge characteristics.

If the X-capacitor value is changed, for example to improve EMI performance, it may be necessary to adjust the values of the external resistors connected to the IC to maintain the required discharge time.

Alternatively, the discharge IC may be replaced with conventional discharge resistors to reduce system cost. However, in that case, continuous power loss occurs through the discharge resistors whenever AC power is applied. Therefore, it is necessary to verify that the resulting standby power consumption satisfies the system's power-efficiency requirements.

EMI Suppression Components

To suppress common-mode noise, Y capacitors (C2, C3, C4, C5, C7, and C8) and common-mode chokes (L1 and L2) are implemented. To suppress differential-mode noise, X capacitors (C1, C6, and C9) are used.

EMI performance is affected by factors such as PCB layout and enclosure design. Depending on the system requirements, the above components may need to be modified, removed, or added.

Increasing the capacitance of the Y capacitors can improve common-mode noise suppression; however, it also increases leakage current. Therefore, it is necessary to verify that the resulting leakage current complies with the applicable safety standards required for the system.

Inrush Current Limiting Components

To suppress the inrush current generated when AC power is applied, a fusible resistor (R3) and a relay (RY1) are implemented.

When the design is started according to the recommended procedure, the relay circuit remains off when AC power is initially applied. As a result, the input current flows through the 20Ω fusible resistor, limiting the inrush current.

The relay circuit is designed to turn on after AC power is applied and the primary-side 12V auxiliary power supply, which is generated for system operation and control, becomes available. Once the relay is turned on, the input current bypasses the fusible resistor and flows through the relay contacts, which have significantly lower resistance, thereby reducing power loss during normal operation.

It is important to verify that the relay turn-on and turn-off conditions, as well as their timing, satisfy the requirements of the target system.

Primary-Side and Secondary-Side 12V Power Supplies

In this design, a primary-side 12V power supply and a secondary-side 12V power supply are generated by a flyback converter for system operation and control.

Depending on the system requirements, additional loads such as cooling fans may need to be powered from these auxiliary supplies. In such cases, a flyback converter should be designed to provide sufficient current capacity to support the required loads.

3.2. PFC Circuit Design

This design employs a semi-bridgeless PFC topology based on the Texas Instruments UCC28070A (PFC controller) to achieve high efficiency. The following sections describe the basic design considerations of the semi-bridgeless PFC circuit. For detailed information on the controller and its peripheral circuitry, refer to the UCC28070A datasheet and related documentation from Texas Instruments. Figure 3.2 shows the PFC controller peripheral circuitry.

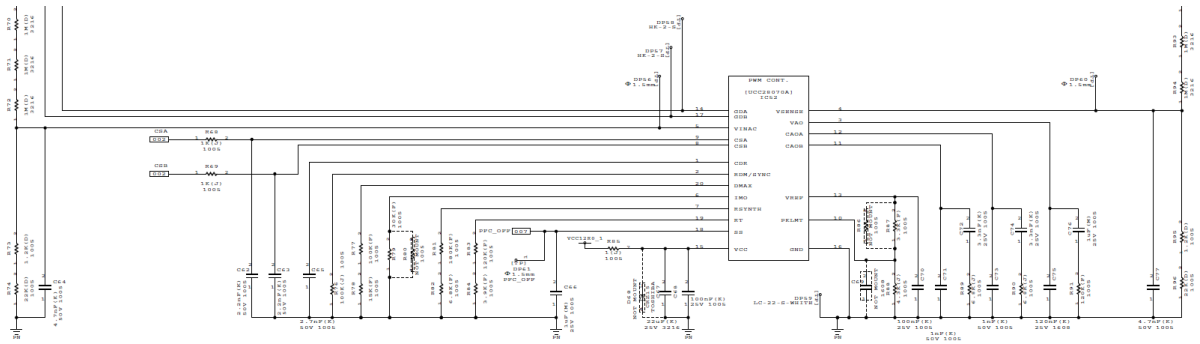

Figure 3.2 PFC Circuit 1 (PFC Controller Peripheral Circuitry)

Output Voltage

The PFC output voltage, PFC_OUT, can be adjusted using the external resistors R92, R93, R94, R95, and R96.

The output voltage is regulated by comparing the output-voltage sensing signal (VSENSE), generated by the resistor divider network, with the internal reference voltage (3.0V) of the PFC controller.

The output voltage setting can be calculated using the following equation.

$$PFC\ OUT(V) = \frac{3 \times (R92 + R93 + R94 + R95 + R96)}{(R95 + R96)}$$

When changing the PFC output voltage, the AC line voltage sensing resistors R70, R71, R72, R73, and R74 must also be changed proportionally.

The default output-voltage setting is established using resistor values of 22kΩ for R96 and R74, 1.2kΩ for R95 and R73, and 1MΩ for R70, R71, R72, R92, R93, and R94.

With these values, the PFC output voltage is approximately 391V.

Adjust the resistor values as required to obtain the desired output voltage.

Switching Frequency

The PFC switching frequency, f_{PWM}, can be configured using the external resistors R83 and R84.

According to the controller configuration, the switching frequency can be calculated using the following equation.

$$f_{PWM}(kHz) = \frac{7500}{R83+R84\,(k\Omega)}$$

The default the combined resistance of R83 and R84 is approximately 124kΩ.
which results in a switching frequency of approximately 60kHz.
Adjust the resistor values as necessary to obtain the desired switching frequency.

Soft Start

The soft-start time of the PFC circuit can be configured using the external capacitor C66. The soft-start time is calculated using the following equation.

$$T_{SS}(s) = C66 \times \frac{2.25(V)}{10(\mu A)}$$

The default setting is C66 = 1µF, which provides a soft-start time of approximately 225ms.
Adjust the capacitance value of C66 as required to obtain the desired soft-start time.
When selecting the soft-start time, it is necessary to verify that:

- The current limiter does not operate during the soft-start period.
- The output voltage recovers to its normal operating range during restart following a hold-up period.

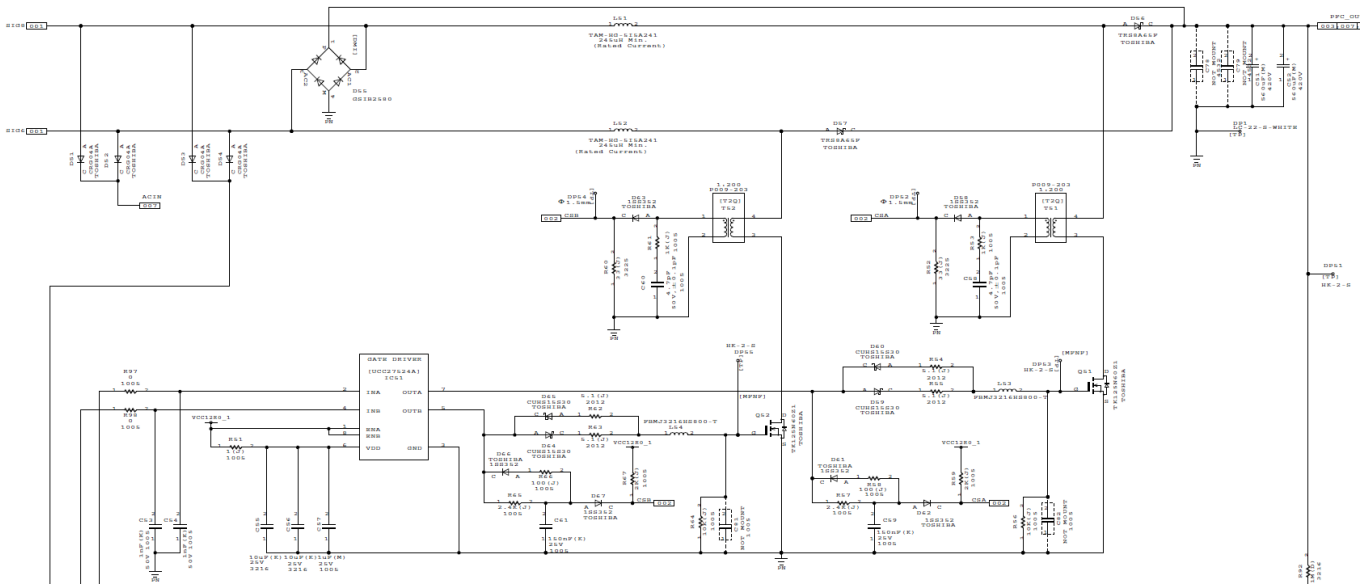

Figure 3.3 PFC Circuit 2 (Power MOSFETs, Bridge Diodes, and Inductors)

Figure 3.3 shows the circuitry surrounding the power MOSFETs and inductors.

Inductors

The inductors (L51 and L52) are selected by setting the inductor ripple current, ΔI, to 50% of the peak AC line input current, AC_{in_peak}. When the AC input voltage is denoted by V_{inAC}, the PFC output voltage by V_{out_PFC}, the switching frequency by F, the power conversion efficiency of the PFC stage by η_1, and the power conversion efficiency of the downstream PSFB stage by η_2, the required inductance can be calculated as follows.

$$AC_{in\_peak} = \frac{P_{in} \times \sqrt{2}}{V_{inAC}} = \frac{(P_{out}/\eta 2) \times \sqrt{2}}{V_{inAC} \times \eta 1}$$

$$\Delta I = AC_{in\_peak} \times 50\%$$

When V_{inAC} = 90V, P_{out} = 800W, η_1 = 93%, and η_2 = 96%, ΔI is calculated to be 7.05A.
The inductance is determined by the maximum voltage applied to the inductor while the PFC switching device (MOSFET) is on, the MOSFET on-time, which is expressed as the switching period T multiplied by the duty cycle, and the change in current ΔI.

$$L = V \times \frac{dt}{di} = \sqrt{2} \times V_{inAC} \times \frac{T \times D}{\Delta I}$$

Expressing T in terms of the MOSFET switching frequency F gives the following equation.

$$T = \frac{1}{F}$$

The duty cycle of the PFC circuit is expressed by the following equation.

$$D = \frac{V_{PFC\_OUT} - \sqrt{2} \times V_{inAC}}{V_{PFC\_OUT}}$$

Substituting the equations for T and D into the inductance equation gives the following equation.

$$L = \sqrt{2} \times V_{inAC} \times \frac{(V_{out_{PFC}} - V_{inAC})}{V_{out\_PFC} \times \Delta I \times F}$$

In this design, when V_{out_PFC} = 390V and F =60kHz, the required inductance is calculated to be 231µH. Therefore, a 250µH inductor is used.

Current Limiter

The current limit function of the PFC circuit can be configured using the current transformers (T51 and T52), current-sense resistors (R52 and R60), and threshold-setting resistors (R87 and R88).

When the detected current reaches the configured threshold, the PFC controller disables the gate-drive signals (GDA and GDB). The current limit level, I_{limit}, can be calculated using the current-limit threshold voltage V_s, the reference voltage V_{ref} = 6.0V, the current transformer turns ratio N_{ct} = 200, and the current-sense resistance R_s, where R52 = R60 = 33Ω. Substituting these values gives:

$$V_s = \frac{R88}{R87 + R88} \times V_{ref}$$

$$I_{limit} = \frac{V_s \times N_{ct}}{R_s}$$

The default current-limit setting is 20.5A.

On the other hand, the maximum current flowing through the PFC switching devices can be calculated using the following equation.

$$I_{peak} = (\frac{(P_{out}/\eta 2) \times \sqrt{2}}{\eta 1 \times VinAC} + \frac{\Delta I}{2}) \times Margin$$

For V_{inAC} = 90V, P_{out} = 800W, PFC efficiency η_1 = 93%, ΔI = 7.05A, and a design margin of 1.1, the peak current through the switching device is calculated to be 19.4A.

Adjust the component values as necessary to obtain the desired current-limit level.

Gate Drive Circuit

The design of the gate drive circuit affects both power conversion efficiency and EMI performance. In general, power efficiency and EMI performance have a trade-off relationship, and the gate drive circuit must be designed to achieve an appropriate balance between them.

If EMI noise reduction is required, it is recommended to increase the values of the gate resistors (R54, R55, R62, and R63) and evaluate their effect on noise performance.

The gate drive circuit in this design allows the turn-on speed and turn-off speed of the MOSFETs to be adjusted independently.

If prior analysis has identified whether the noise source is generated primarily during the MOSFET turn-on interval or turn-off interval, it is not necessary to modify all gate resistors.

- If turn-on noise is the primary concern, increasing R55 and R63 may help reduce EMI noise.
- If turn-off noise is the primary concern, increasing R54 and R62 may help reduce EMI noise.

It should be noted that increasing the gate resistance slows the switching speed of the MOSFETs, which may result in reduced power conversion efficiency.

Therefore, whenever the gate resistance values are modified, it is necessary to verify that the system still satisfies the required efficiency and thermal performance specifications.

In addition, if EMI requirements can be met by adjusting only the turn-on characteristics or only the turn-off characteristics, the negative impact on system efficiency may be minimized compared with a solution that slows both turn-on and turn-off transitions.

Bridge Diode

A bridge diode (D55) is used as the rectifier diode in this design.

Because this design employs a semi-bridgeless PFC topology, the diodes between pins 2 and 1 and between pins 3 and 1 of the bridge diode contribute only to the rectification operation during startup and do not participate in normal operation thereafter.

The bridge diode (D55) may also be replaced with a half-bridge diode configuration or surface-mount diodes. When using surface-mount diodes, devices with sufficient inrush current capability must be selected to withstand the startup current.

Output Capacitors

The capacitance of the output capacitors (C51 and C52) is determined based on the hold-up time requirement.

The hold-up time, T_{hold}, can be calculated using the following equation, where C_{out} is the output capacitance, V_{out_PFC} is the PFC output voltage, V_{min} is the minimum output voltage, and P_{out} is the maximum output power.

$$T_{hold} = C_{out} \times \frac{({V_{out\_PFC}}^2 - {V_{min}}^2)}{2 \times P_{out}/\eta 2}$$

Using the default design parameters of Cout = 660µF, V_{out_PFC} = 390V, V_{min} = 328.42V, P_{out} = 1600W, and η2 = 96% for the PSFB conversion efficiency, the hold-up time is calculated to be approximately 8.76ms.

Adjust the output capacitance as necessary to satisfy the hold-up time requirement of the target system.

If an output ripple voltage specification is imposed, the required capacitance to satisfy the ripple specification should also be calculated. The larger value between the capacitance required for hold-up time and that required for ripple voltage should be selected.

In addition, capacitor tolerances and long-term capacitance degradation should be taken into consideration when selecting the output capacitors.

3.3. Phase-Shifted Full-Bridge (PSFB) Converter Design

This design generates the 48V output using a PSFB converter stage following the semi-bridgeless PFC circuit. To improve power conversion efficiency, the design employs the Texas Instruments UCC28950 (PSFB controller), which enables Zero-Voltage Switching (ZVS) operation over a wide load range.

The following sections describe the basic design considerations for the PSFB converter used in this design. For detailed information on the PSFB controller and its peripheral circuitry, refer to the UCC28950 datasheet and related documentation provided by Texas Instruments.

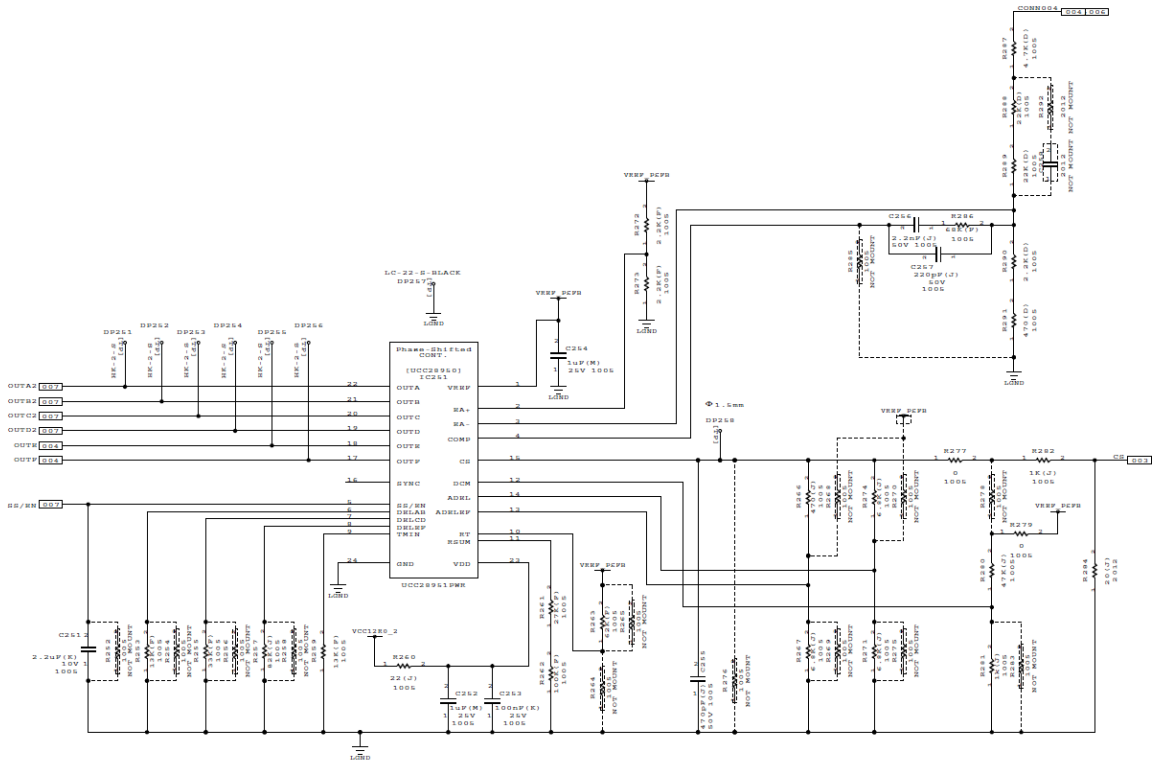

Figure 3.4 PSFB Circuit 1 (PSFB Controller Peripheral Circuitry)

Output Voltage

The PSFB converter output voltage, V_{out}, can be adjusted using the external resistors R42, R43, R44, R45, and R75. The output voltage setting is determined by these resistors and the PSFB controller's internal voltage reference used for output-voltage regulation (V_{REF} = 5.0V) and can be calculated using the following equation.

$$V_{out}(V) = \frac{V_{REF}(V) \times R273 \times (R287 + R288 + R289 + R290 + R291)}{(R272 + R273) \times (R290 + R291)}$$

The default output voltage is set by configuring R272, R273, and R290 to 2.2kΩ, R287 to 4.7kΩ, R288 and R289 to 22kΩ, and R291 to 0.47kΩ. With these resistor values, the output voltage is approximately 48.10V. To obtain a different output voltage, adjust the resistor values as required.

Switching Frequency

The PSFB converter switching frequency, f_{PWM}, can be configured using the external resistor R263. Based on the controller configuration, the switching frequency can be calculated using the following equation.

$$f_{PWM}(kHz) = \frac{2.5 \times 10^3}{\frac{R263(k\Omega)}{V_{REF}(V) - 2.5} + 1}$$

The default setting is R263 = 62kΩ, which results in a switching frequency of approximately 96.90kHz. Adjust the resistor value as necessary to obtain the desired switching frequency.

Soft Start

The soft-start time of the PSFB converter can be configured using the external capacitor C251. The soft-start time can be calculated using the following equation.

$$T_{SS}(s) = \frac{C251(\mu F) \times (\frac{V_{REF}(V) \times R273}{R272 + R273} + 0.55)}{25}$$

The default setting is C251 = 2.2µF, which provides a soft-start time of approximately 268.4ms. Adjust the capacitance value of C251 as required to obtain the desired soft-start time.

When configuring the soft-start time, it is important to verify that the current limiter does not activate during the soft-start period.

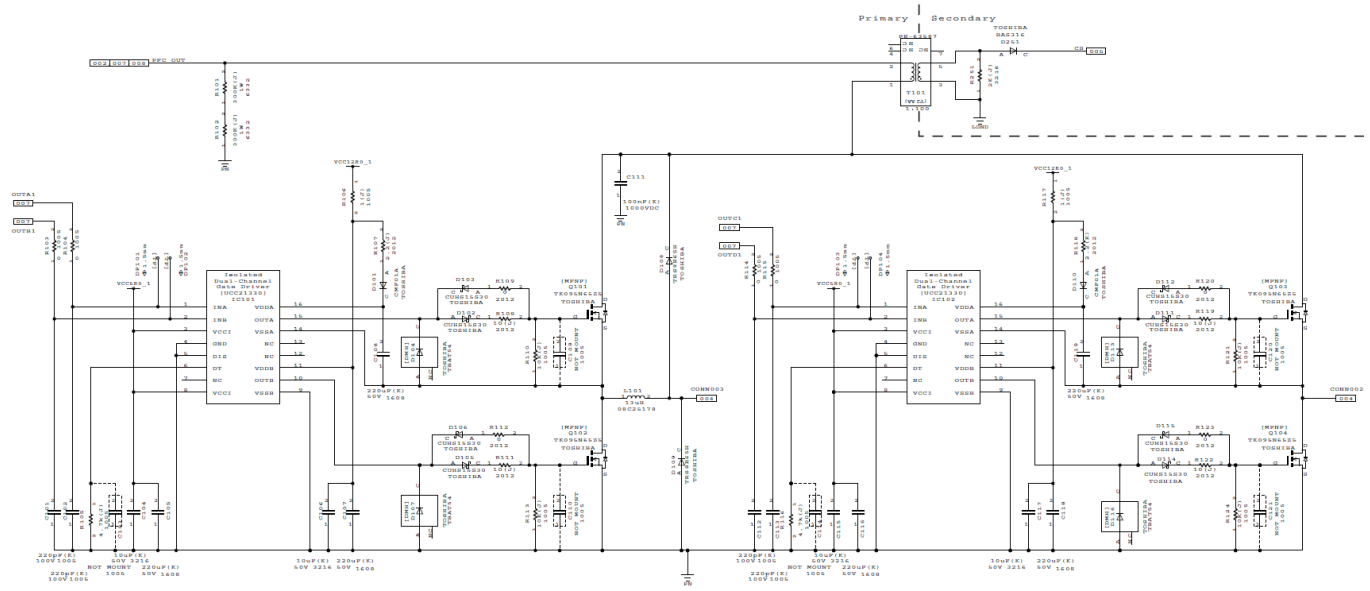

Figure 3.5 PSFB Circuit 2 (Primary-Side MOSFET Circuitry)

Figure 3.5 shows the circuitry surrounding the primary-side MOSFETs.

Current Limiter

The current limit function of the PSFB converter can be configured using the current transformer (T101), current-sense resistor (R284), and the controller's current-limit threshold voltage (2V).

When the current flowing through the current-sense resistor reaches the threshold level, the PSFB controller limits the drive of the primary-side MOSFETs to prevent excessive current from flowing on the secondary side.

In this design, the current transformer has a turns ratio of 100:1, meaning that the current flowing through the current-sense resistor is one-hundredth of the actual current. Therefore, the current-limit level, I_{limit}, can be calculated using the following equation.

$$I_{limit} = \frac{2.0}{R284} \times 100$$

With the default setting of R284 = 20Ω, the current-limit level is 10A.
Adjust the component value as required to obtain the desired current-limit level.

Gate Drive Circuit

The design of the gate drive circuit affects both power conversion efficiency and EMI performance. In general, power efficiency and EMI performance have a trade-off relationship, and the gate drive circuit must be designed to achieve an appropriate balance between them.

The PSFB converter operates with Zero-Voltage Switching (ZVS). However, if hard-switching operation occurs under certain conditions and is identified as a source of EMI noise, it is recommended to increase the values of the gate resistors (R109-R112 and R119-R122) of the corresponding MOSFETs (Q101-Q104) and evaluate the resulting noise performance.

As with the PFC gate drive circuit, this design allows the turn-on and turn-off characteristics to be adjusted independently. If EMI performance can be improved by adjusting only the turn-on or only the turn-off transition, the impact on overall system efficiency may be reduced compared with delaying both transitions.

When modifying the gate resistor values, verify that the system continues to meet the required power-efficiency and thermal-performance specifications.

Transformer

In the PSFB converter, the synchronous rectifier conduction duty is designed to be approximately 85% under steady-state conditions. Since the output voltage is 48V, a square-wave voltage of approximately 56V is required on the transformer secondary side.

Because the PFC output voltage of this design is 390V, a transformer turns ratio of 27:4:4 (center-tapped configuration) is selected for transformers T151 and T201. With this turns ratio, a square-wave voltage of approximately 57.8V is generated at the secondary-side rectifier input.

In addition to the turns ratio, transformer design must consider factors such as:

- Primary-to-secondary isolation withstand voltage
- Winding temperature rise
- Magnetic flux saturation
- Core loss

For detailed specifications of the transformer used in this design, refer to the BOM.

The secondary-side synchronous rectifier MOSFETs are subjected to approximately 115.6V, which is twice the secondary winding voltage, during their off state. Therefore, considering derating requirements, 150V-rated MOSFETs are selected for the secondary-side synchronous rectification stage.

Furthermore, this design utilizes the transformer's leakage inductance to achieve Zero-Voltage Switching (ZVS). If the resonance provided by the leakage inductance is insufficient, ZVS may not be achieved, potentially resulting in reduced power conversion efficiency and increased EMI noise.

When modifying the transformer design, it is important to verify that ZVS operation is maintained over the required load range. If transformer changes result in insufficient resonant inductance and ZVS cannot be achieved, an additional resonant inductor (L101) should be used to ensure ZVS operation across a wide load range.

In the default design, a 13µH resonant inductor is connected in addition to the transformer leakage inductance to achieve ZVS operation.

Output Capacitors

The output capacitors must be selected to ensure that the output voltage ripple remains within the limits required by the target system.

The output voltage ripple, V_{ripple}, is composed of the voltage components generated by the ripple current ΔI flowing through the output capacitor's ESR, capacitance (Cap), and ESL. When the switching voltage is denoted by V_{sw}, the output voltage by V_{out}, and the switching frequency by F, the ripple-voltage components generated by the ESR, capacitance, and ESL can be calculated using the following equations.

$$V_{ripple\_ESR} = \Delta I \times ESR$$

$$V_{ripple\_Cap} = \frac{\Delta I}{8 \times Cout \times F \times 2}$$

$$V_{ripple\_ESL} = \frac{V_{SW} \times ESL}{L}$$

Where:

$$\Delta I = \frac{(V_{SW} - V_{out}) \times V_{out}}{V_{SW} \times F \times 2 \times L} \times 2(phases)$$

Assuming V_{sw} = 60V, V_{out} = 48V, a switching frequency of F = 97.05kHz, and an output inductor value of L = 27µH, the ripple current can be calculated. Because the secondary-side output frequency of the PSFB converter is twice the primary-side switching frequency, a conservative approach is used in which the ripple-current value is doubled and the switching frequency is multiplied by two. Under these conditions, the calculated ripple current is ΔI = 3.66A.

Using the default design values of C_{out} = 330µF × 6, ESR = 40mΩ, ESL = 5nH, and L = 27µH, the ripple-voltage components are calculated as V_{ripple_ESR} = 146mV, V_{ripple_Cap} = 1.2mV, and V_{ripple_ESL} = 11.1mV.

Strictly speaking, the voltage generated by the capacitance component is phase-shifted relative to the ESR- and ESL-generated voltages and therefore cannot be directly summed with them. However, because the capacitive component is relatively small, a simple summation provides a practical approximation of the total ripple voltage. The output capacitance should be adjusted as necessary to meet the ripple-voltage requirements of the target system.

In addition, it is important to verify that the output undershoot and overshoot during load-transient conditions remain within the specified voltage limits and that the selected capacitors have sufficient ripple-current handling capability for the intended operating conditions.

3.4. Communication Between the Primary and Secondary Sides of the PSFB Converter

As shown in Figure 3.6, a 4-channel digital isolator, DCL540C01, is used for signal transmission between the primary and secondary sides of the PSFB converter. The MOSFET gate-drive signals for the primary-side full-bridge circuit, generated by the PSFB controller located on the secondary side, are transmitted through DCL540C01.

While an optocoupler transmits signals by turning an LED on and off within a package containing both a light-emitting device (LED) and a photodetector, electrically isolated by a light-transmitting resin, a digital isolator consists of a modulation chip and a demodulation chip integrated within the same package and separated by an insulating barrier. Depending on the device architecture, signal transmission is achieved through magnetic or capacitive coupling. The DCL540C01 employs Toshiba's proprietary magnetic-coupling isolation technology.

The DCL540C01 employs Toshiba's proprietary magnetic-coupling isolation technology, achieving a high Common-Mode Transient Immunity (CMTI) of 100kV/µs (min). This high CMTI improves immunity to noise-induced malfunctions and contributes to stable system operation.

In addition, the device offers a low pulse-width distortion of 3.0ns (max) and a high data transmission rate of 150Mbps (max), making it well suited for high-speed communication applications.

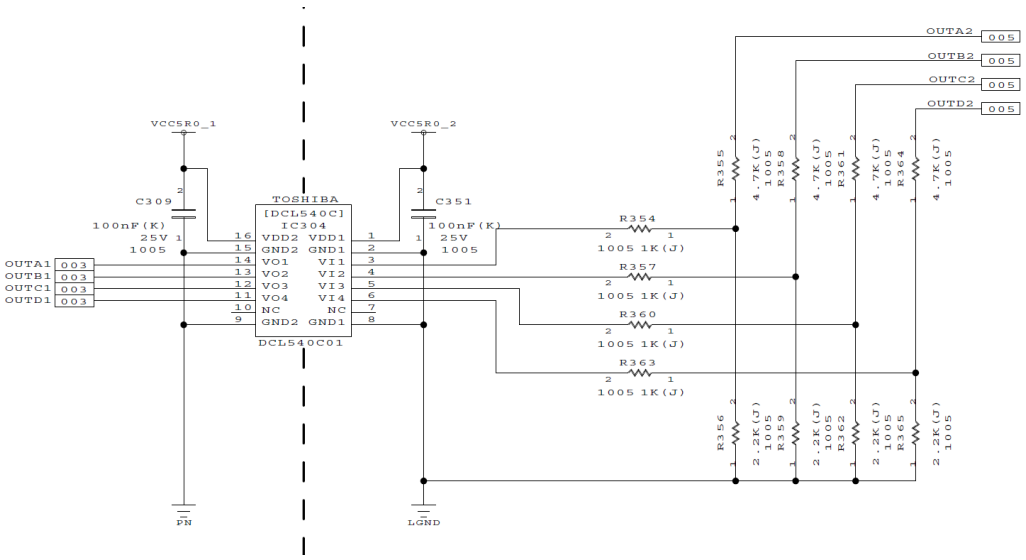

Figure 3.6 Digital Isolator (DCL540C01)

3.5. ORing Circuit Design

This design incorporates an ORing circuit at the output stage to support N+1 redundant operation. The ORing circuit consists of the LM74700 ORing controller from Texas Instruments and the on/off control MOSFETs (Q501-Q503).

When this design is connected in parallel with other power supplies and the output voltage of this design is higher than that of the other power supplies, the ORing controller turns on the MOSFETs and supplies current to the load. Conversely, when the output voltage of this design is lower than that of the other power supplies, the ORing controller turns off the MOSFETs, preventing reverse current from flowing from the other power supplies back into this design.

The following sections describe the basic design considerations for the ORing circuit used in this design. For detailed information regarding the ORing controller and its peripheral circuitry, refer to the LM74700 datasheet and related documentation provided by Texas Instruments.

The type and number of MOSFETs used for the on/off switching function must be selected such that the voltage drop and power dissipation caused by the MOSFET ON-resistance remain within the allowable limits of the system at the maximum load current (33A).

In this design, three TPM1R908QM MOSFETs are connected in parallel.

It should be noted that the ON-resistance of a MOSFET increases with temperature. Therefore, MOSFET selection must take into account both the maximum ambient temperature supported by the system and the junction temperature rise of the MOSFETs under maximum-load conditions.

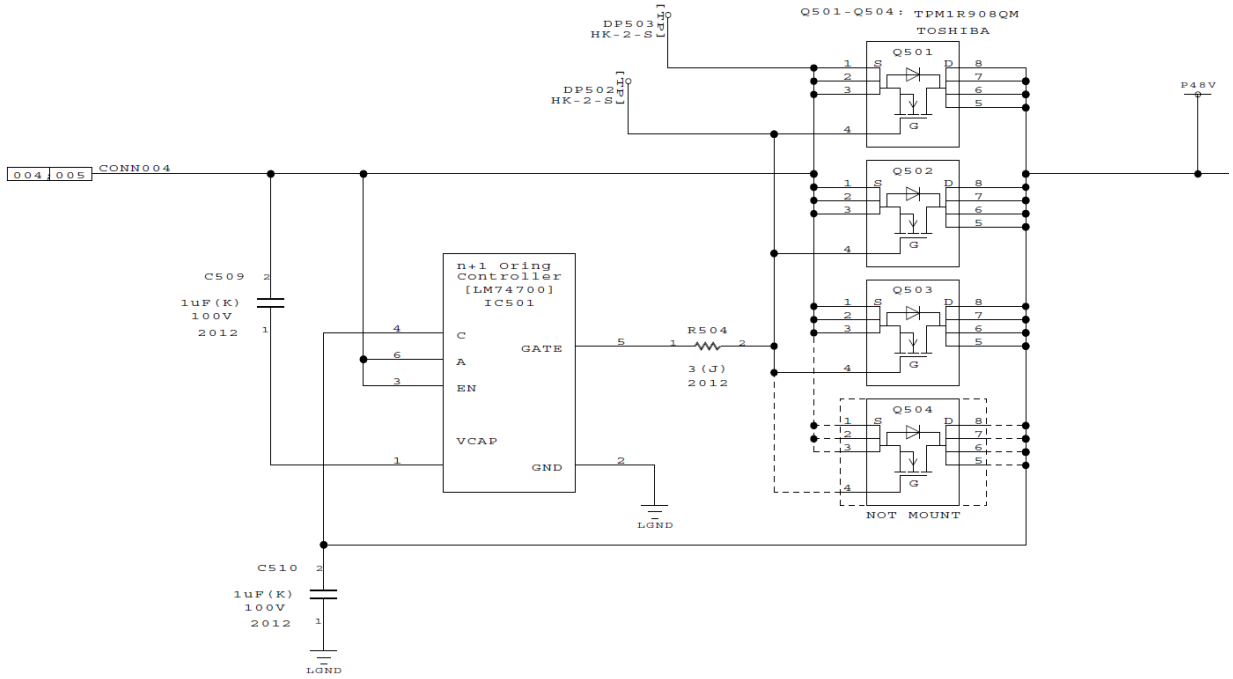

Figure 3.7 ORing Circuit

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