

iXPLV® SiC MOSFET Module Gate Driver

Reference Guide

RD258-RGUIDE-01

Toshiba Electronic Devices & Storage Corporation

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1. Introduction

This reference guide describes the specifications, usage, and characteristics of the iXPLV® SiC MOSFET Module Gate Driver (hereinafter referred to as “this design”).

Switching devices used in power conversion equipment for industrial applications, such as motor drives, railway vehicle inverters and converters, and energy storage systems (ESS), must support high voltages and large currents. IGBT modules using Si (silicon) have traditionally been widely used for these applications. In recent years, SiC MOSFET modules using SiC (silicon carbide), which offer faster switching characteristics than IGBTs and excellent operation in high-temperature environments, have become increasingly common. The use of SiC MOSFET modules enables smaller and more efficient equipment.

This design is a gate driver that provides isolated drive for a SiC MOSFET module containing two devices in an iXPLV® package. Isolation between the primary-side circuit in the signal input section and the secondary-side circuit in the output section is implemented using the TLP2861L high-speed communication photocoupler (under development), which provides longer creepage and clearance distances than conventional products. A creepage distance of 15mm and a clearance distance of 14.2mm are secured between the primary and secondary sides.

The N-channel MOSFET [SSM6K804R](#) used as a buffer enables high-current gate drive. The design also incorporates protection circuits, including DESAT (desaturation) detection and an active Miller clamp. Each section can be adjusted to match the SiC MOSFET module being driven and the actual specifications. When making adjustments, refer to the Design Guide, the datasheets for the SiC MOSFET module and other mounted components, and the related documents.

A two-tier structure connects the two circuit boards vertically. This achieves a size equivalent to the iXPLV® package while maintaining the creepage and clearance distances described above. Because the board can be mounted directly above the SiC MOSFET module, it is easy to handle and reduces parasitic inductance in the wiring.

When using this design in an actual application, consider creepage and clearance distances, design for an appropriate operating voltage according to the applicable safety standards and operating environment, and perform sufficient verification and evaluation on the actual equipment.

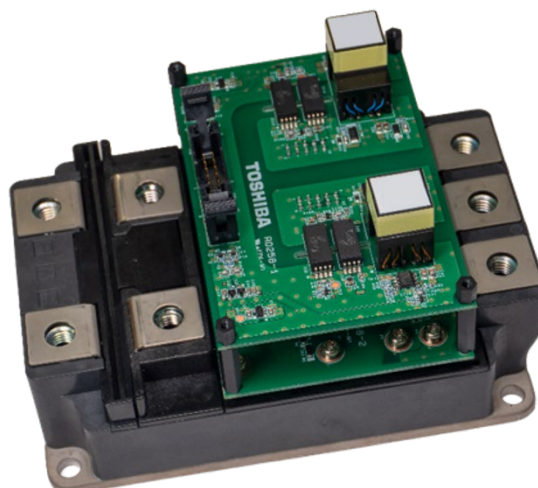


Figure 1.1 This Design Mounted Directly on a Toshiba iXPLV SiC MOSFET Module1

2. Specifications

2.1. Specifications

Table 2.1 lists the specifications of this design.

Table 2.1 Specifications of This Design

Item	Specifications		
Control power supply voltage	DC 24V		
Number of Drive Channels	2ch : Low-side, High-side		
Gate Control Signal Input	INPUT	H Level	4.0V to 5.0V
		L Level	0V to 1.8V
Gate Drive Frequency	20kHz (Max.)		
Enable Signal Input	INPUT	H Level	4.0V to 5.0V
		L Level	0V to 1.8V
Gate Drive Output	+20V (Typ.) / -6.7V (Typ.)		
Fault Detection Output	Collector Output (2ch)		
Protection Functions	Gate drive voltage UVLO Overcurrent protection by DESAT detection Soft turn-off upon DESAT detection Active Miller Clamp (AMC)		
Board Size	68 x 100mm		
Board Structure	FR-4 1.6mm thick, 4 layer Copper thickness: outer layers 18μm, inner layers 35μm Silkscreen and component mounting on both sides		

2.2. Block Diagram

Figure 2.1 shows a block diagram of the functional operation of this design.

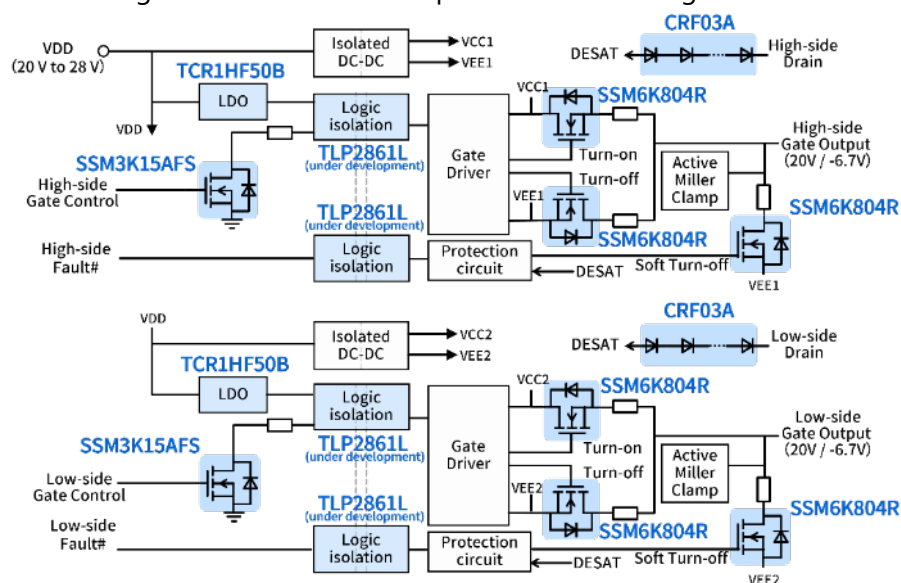


Figure 2.1 Block Diagram1

2.3. Appearance

Figure 2.2 shows the appearance of this design.

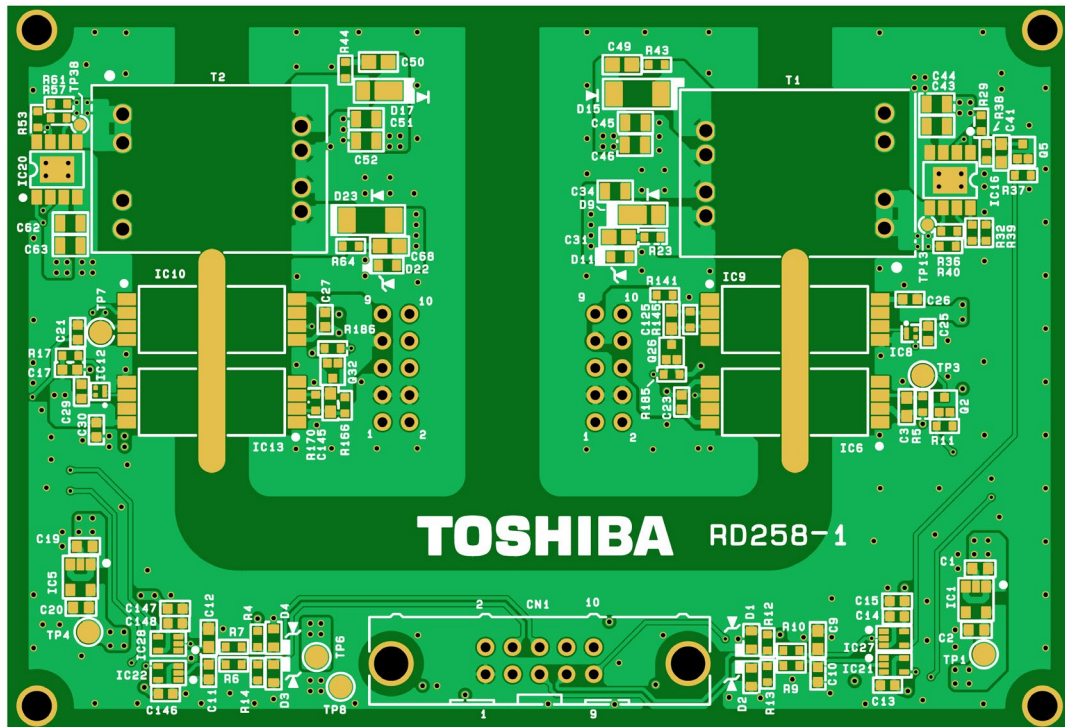


Figure 2.2 Appearance of This Design2

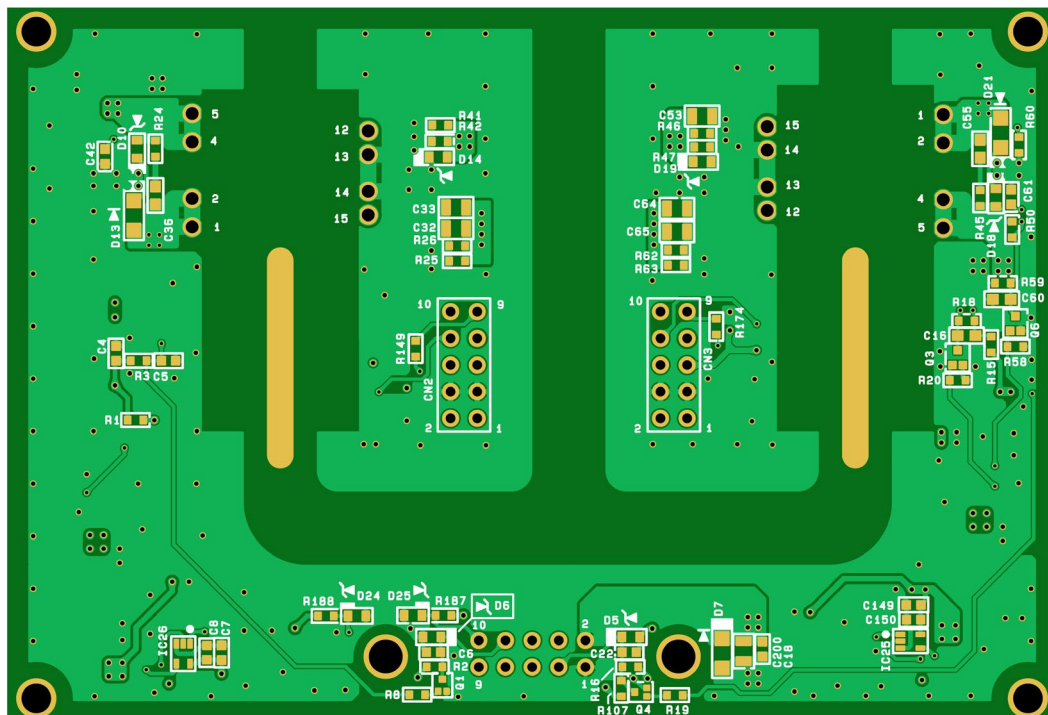
Dimensions 68mm x 100mm

2.4. PCB Component Layout

Figure 2.3 and Figure 2.4 show the component layouts of the input board and output board that constitute this design.

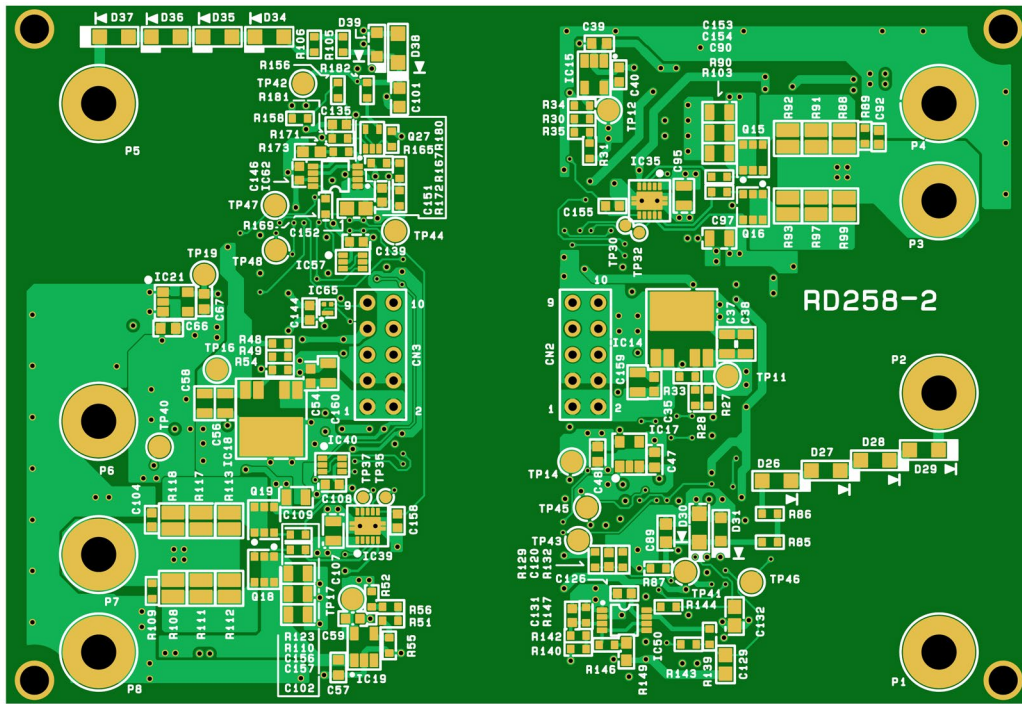


<Front Side>

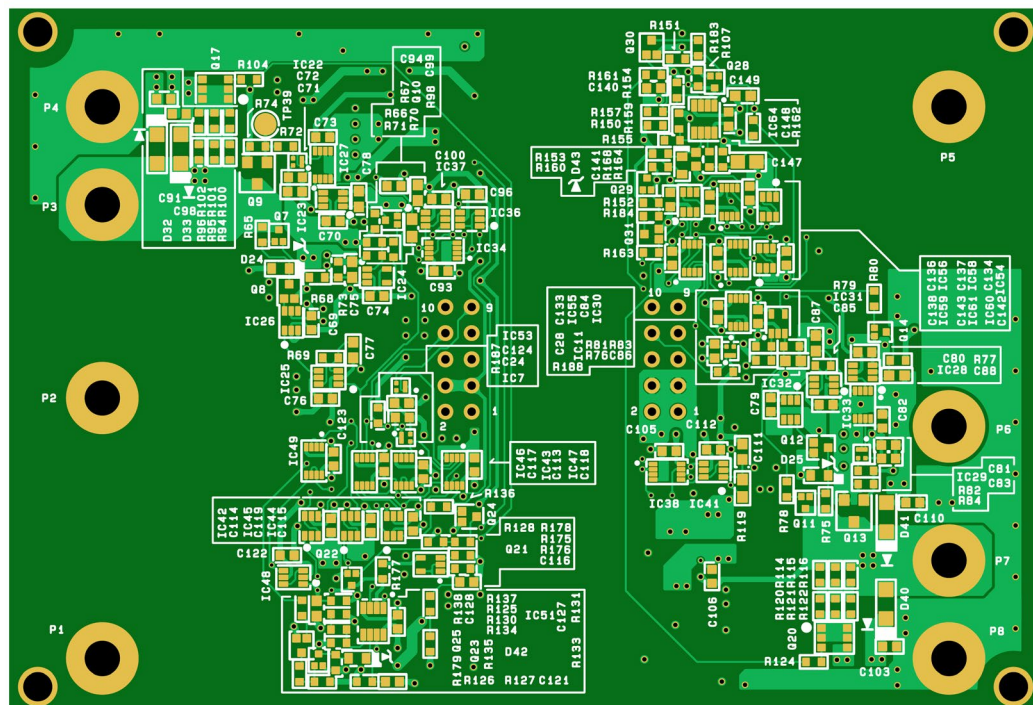


<Back Side>

Figure 2.3 Input Board Component Layout3



<Front Side>



<Back Side>

Figure 2.4 Output Board Component Layout

3. Schematic, BOM, and PCB Layers

3.1. Schematic

Refer to the following files:

RD258-SCHEMATIC1-xx.pdf (Input board)

RD258-SCHEMATIC2-xx.pdf (Output board)

(xx is the revision number)

3.2. BOM (Bill of Materials)

Refer to the following files:

RD258-BOM1-xx.pdf (Input board)

RD258-BOM2-xx.pdf (Output board)

(xx is the revision number)

3.3. PCB Layers

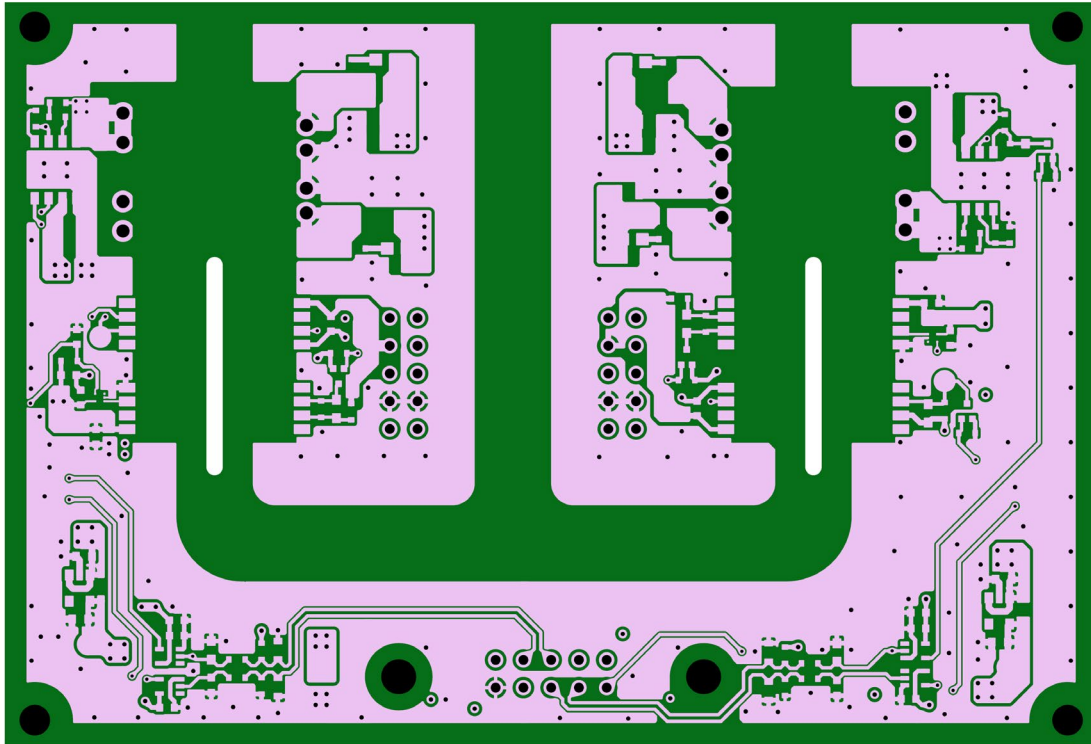
Figure 3.1 and Figure 3.2 show the PCB layers of the input board and the output board respectively.

Also refer to the following files:

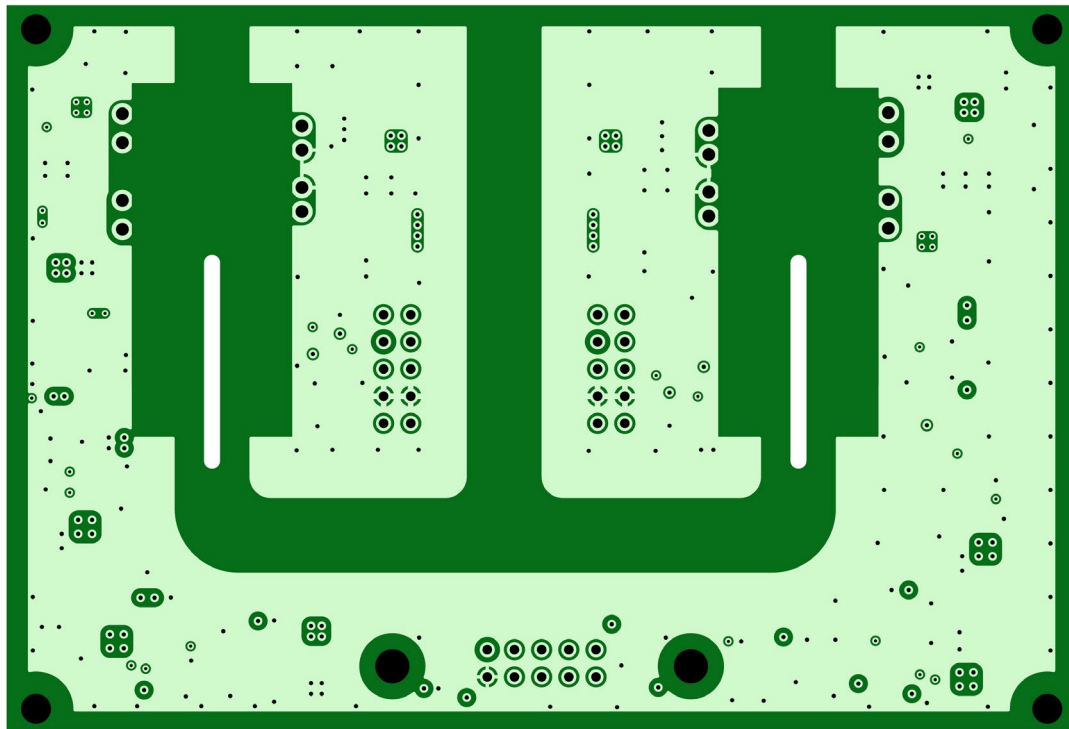
RD258-LAYER1-xx.pdf (Input board)

RD258-LAYER2-xx.pdf (Output board)

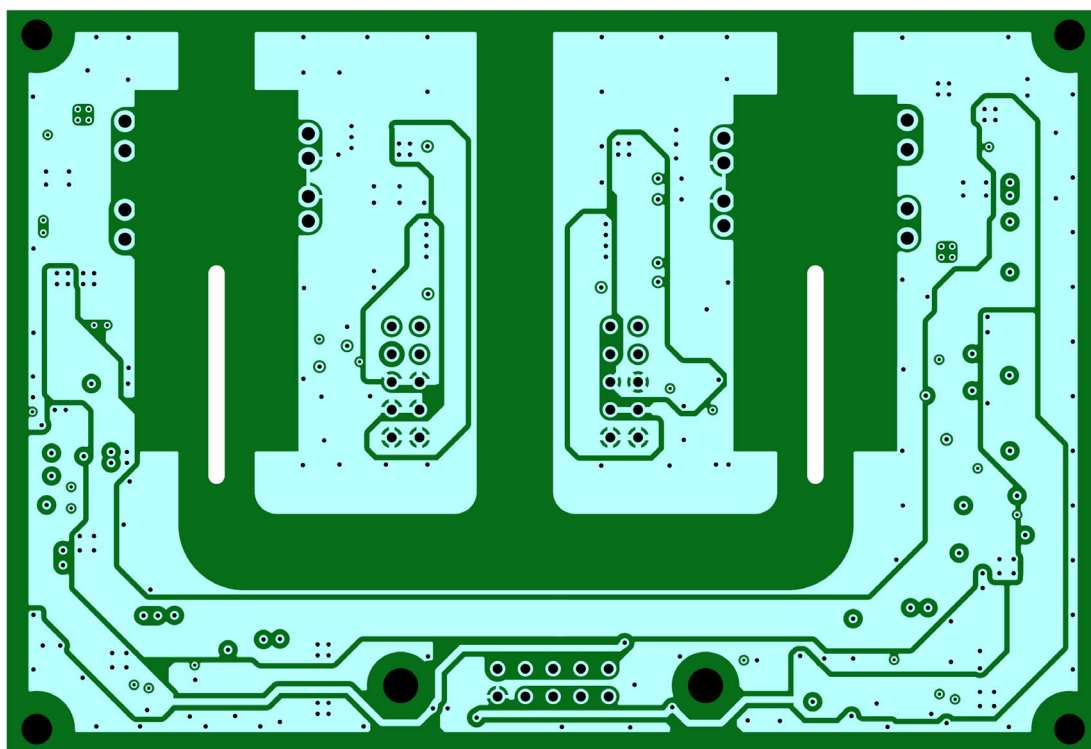
(xx is the revision number)



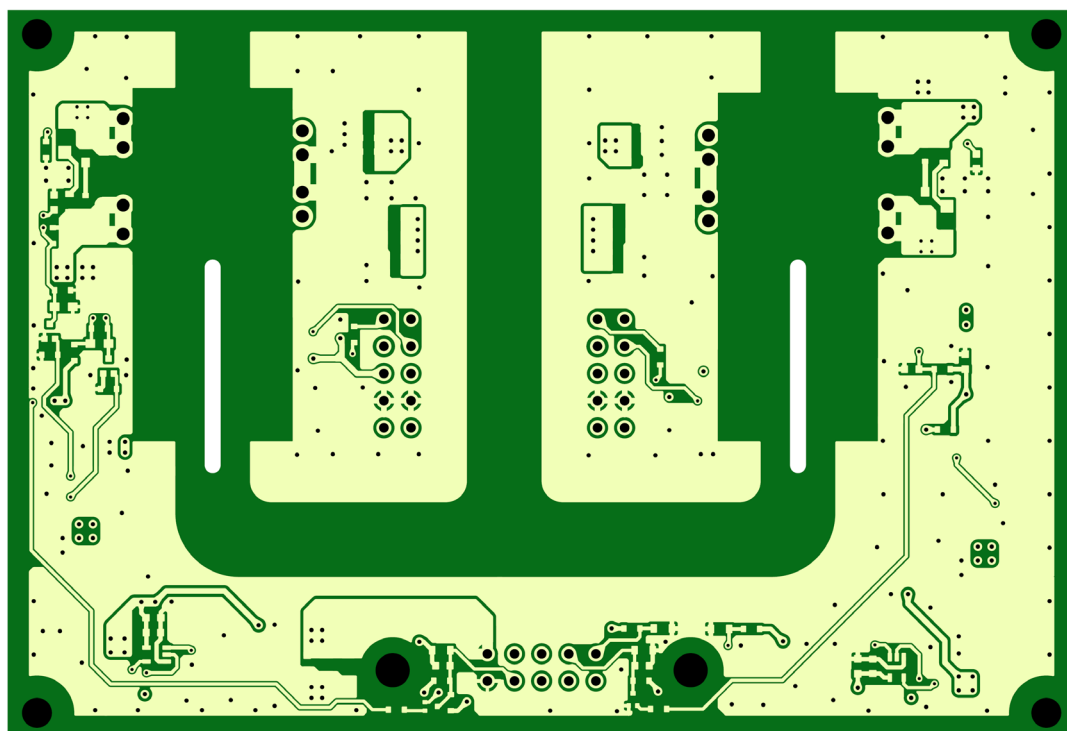
<L1 (Top Layer)>



<L2>

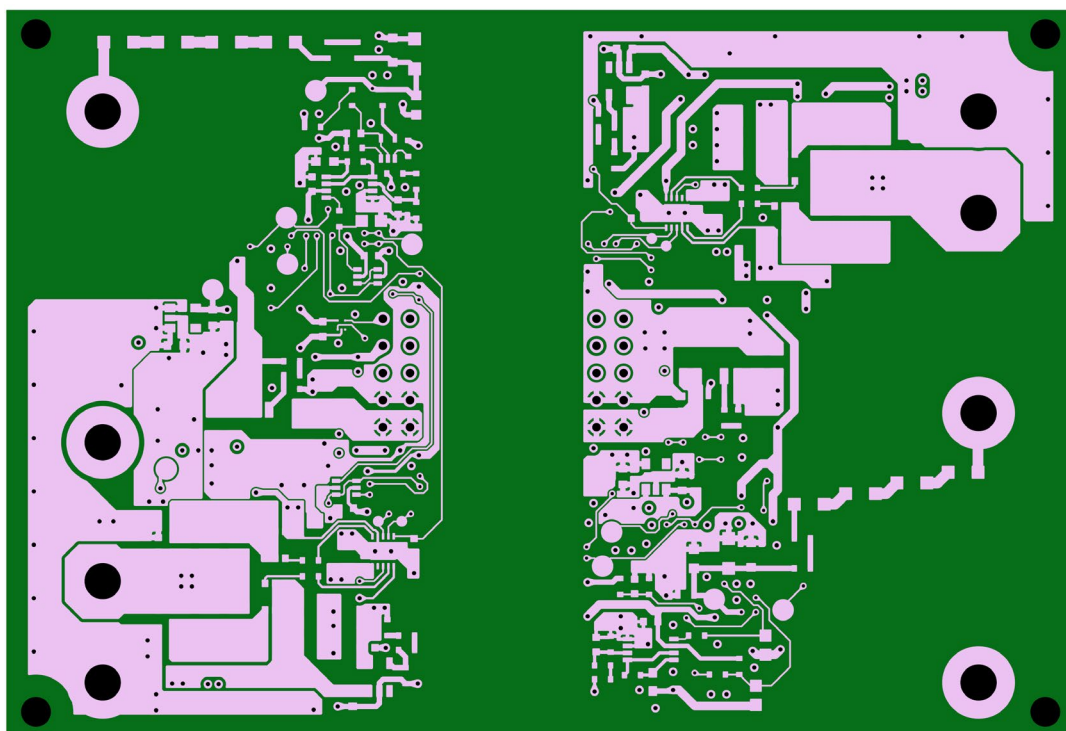


<L3>

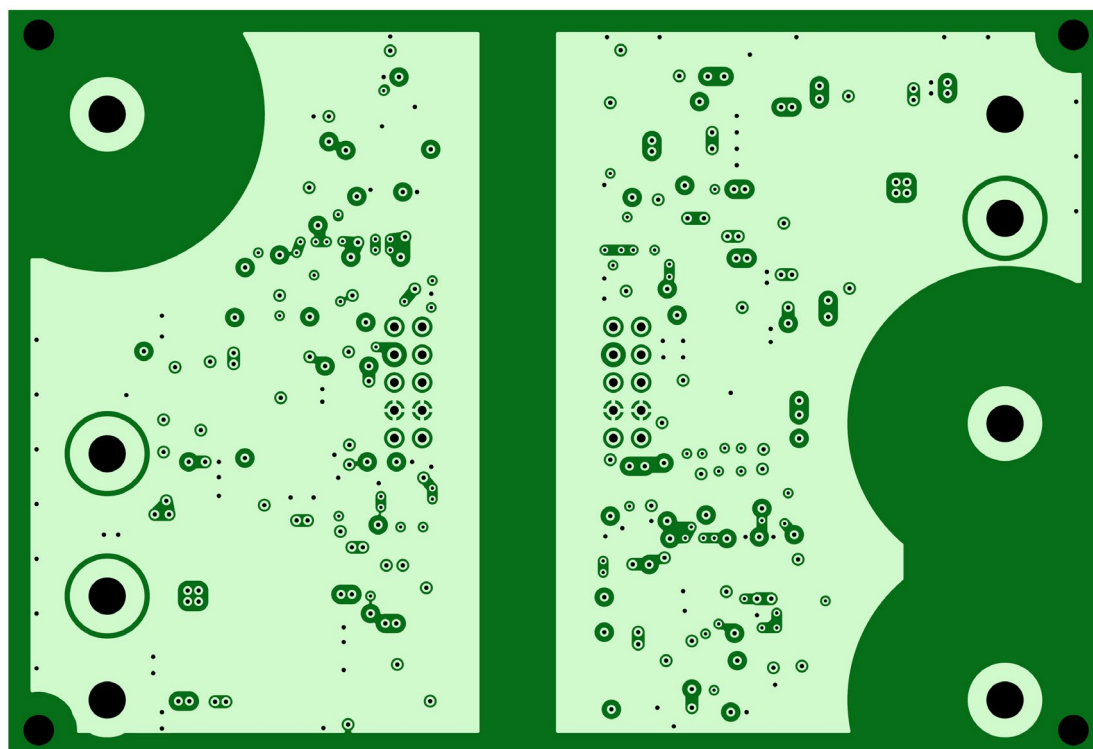


<L4 (Bottom Layer)>

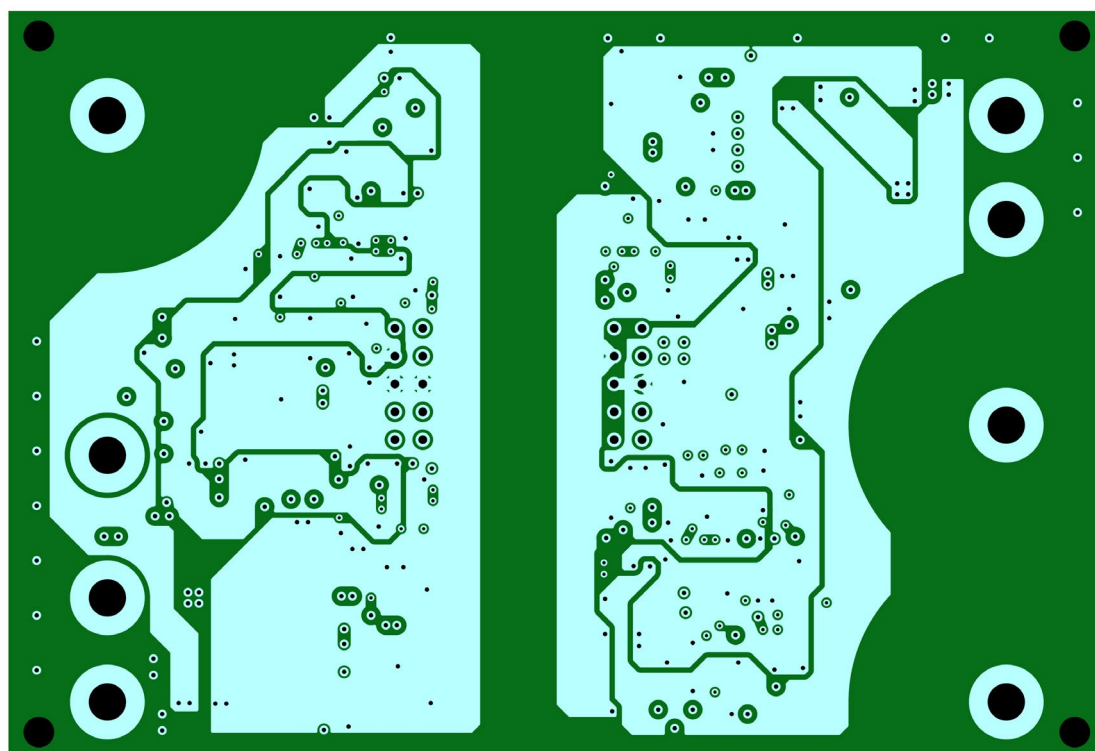
Figure 3.1 Input Board PCB Pattern Diagram (Top View)1



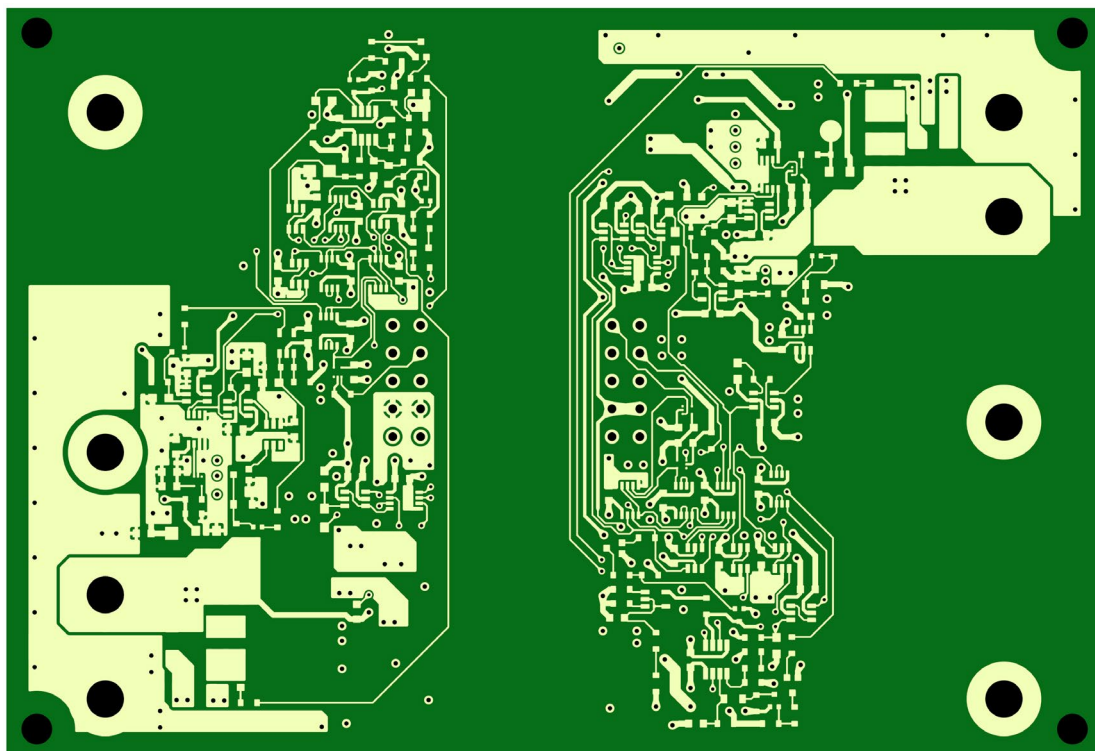
<L1 (Top Layer)>



<L2>



<L3>



<L4 (Bottom Layer)>

Figure 3.2 Output Board PCB Pattern Diagram (Top View)

4. Operation Procedure

This section describes the operation procedure for this design.

4.1. Names and Functions of Each Part

4.1.1. Power and Signal Connector (CN1)

Figure 4.1 shows the external connection terminals of this design. The area outlined in red is the power and signal connector (CN1).

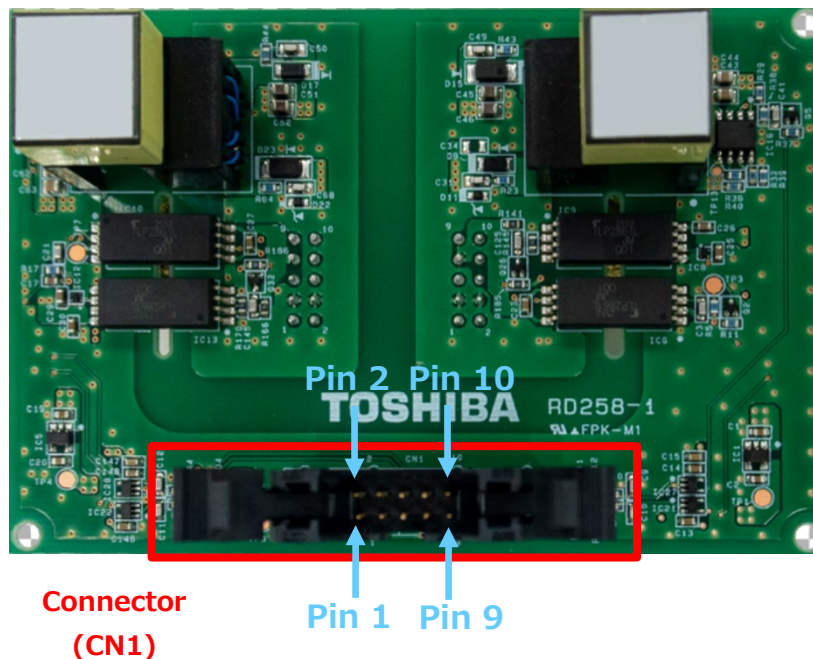


Figure 4.1 External Connection Terminals

The power and signal connector (CN1) is an XG4A-1431 manufactured by OMRON.

Table 4.1 Connector (CN1)

Pin#	Signal Name	I/O	Description	Pin#	Signal Name	I/O	Description
1	GND	-	GND	2	V _{DD}	-	Control power supply voltage
3	B_FLT	O	Low-side fault detection output (Collector output with resistor)	4	B_INA	I	Low-side gate control signal input
5	A_INA	I	High-side gate control signal input	6	B_ENA	I	Low-side enable signal input
7	A_ENA	I	High-side enable signal input	8	A_FLT	O	High-side fault detection output
9	VP_5_A	O	High-side 5V power output	10	VP_5_B	O	Low-side 5V power output

4.1.2. Through-Holes for Connecting the SiC MOSFET Module (P1 to P8)

These through-holes are used to connect to the terminals of the SiC MOSFET module.

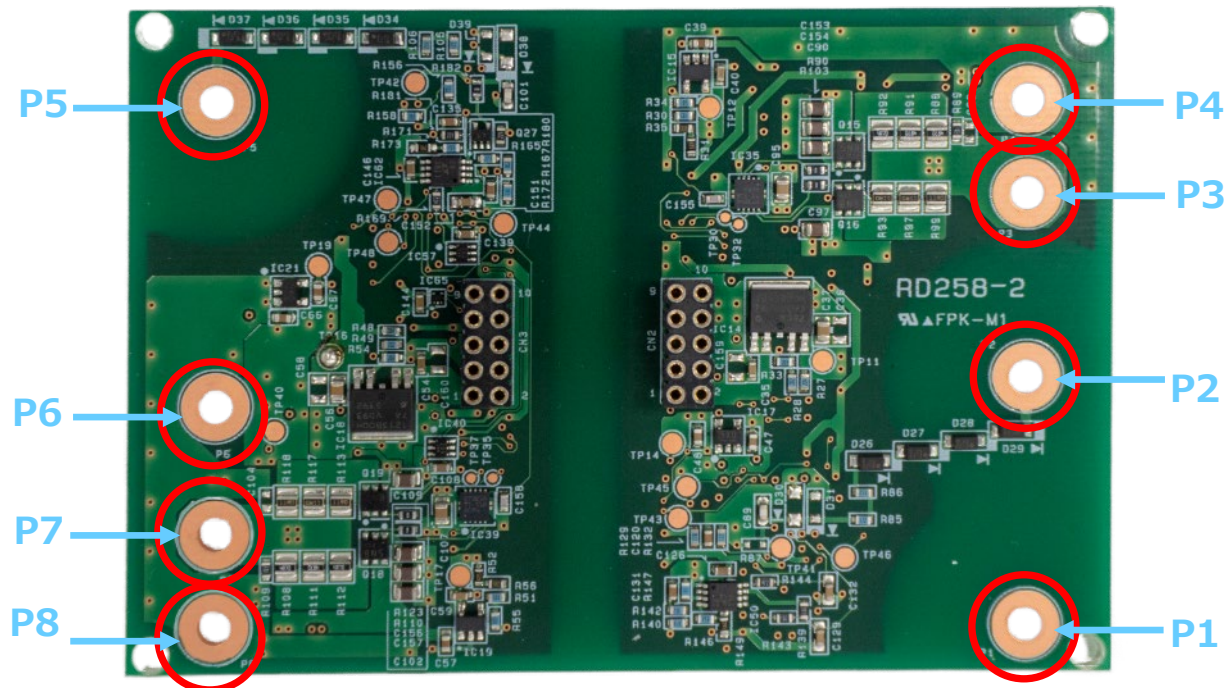


Figure 4.2 Through-Hole Layout on PCB

Table 4.2 Through-Hole Specifications

Through-Hole Name	Description (SiC MOSFET Module Terminal)
P1	N (sense) / Current sense
P2	P (sense)
P3	High-side gate
P4	High-side source sense
P5	AC (sense)
P6	Thermistor
P7	Low-side gate
P8	Low-side source sense

4.2. Preparation

- Connect the input board and output board. When connecting the boards, ensure that the orientation of the silkscreen text on their surfaces is aligned. If the orientation is incorrect, the vertical positions of the input and output boards will be offset.
- Place this design on the SiC MOSFET module and confirm that the eight signal terminals aligns with the terminals of this design (see the red circles in Figure 4.2).
- Secure the eight signal terminals (red circles) to the terminals of this design with screws to establish electrical connections.

For the securing method, refer to the following application note.

[SiC MOSFET Module iXPLV Handling Instruction Application Note](#)

4.3. Operation Check (with SiC MOSFET Module Mated)

Perform the operation check with this design electrically connected to the SiC MOSFET module.

Check DC operation using the following procedure.

- (1) Insert a socket with a flat cable into CN1.
- (2) To avoid triggering the overcurrent protection function, short P2-P4 using hook clips or equivalent when measuring the High-side gate drive output voltage, and short P5-P8 using hook clips or equivalent when measuring the Low-side gate drive output voltage.
- (3) Without applying voltage to the main terminals (P and N terminals) of the SiC MOSFET module, apply the 24V control power supply voltage to CN1.
- (4) Apply voltages to the gate control signal input and enable signal input terminals in accordance with Table 4.3, and check the gate drive output and fault detection output.

Table 4.3 High-side and Low-side Operation Check

Gate Control Signal Input Voltage (CN1: pins 4 and 5)	Enable Signal Input Voltage (CN1: pins 6 and 7)	Gate Drive Output Voltage Measurement points: P3(+)-P4(-), P7(+)-P8(-)	Fault Detection Output Voltage Measurement points: CN1 (pins 3 and 8)
No input or 0V	No input or 5V	-6.7V±5%	5V
5V		20V±5%	
No input or 0V	0V	-6.7V±5%	
5V			

Common Precautions for Evaluation

Please read and follow the precautions below to ensure safe evaluation work.

- **Precautions for Electric Shock Prevention**

- Before applying power, **confirm that the polarity of connectors, terminals, and wiring is correct.**
- Some parts of the board may be exposed to high voltage. **Do not touch the board or components while power is applied.**
- Even after the power is turned off, capacitors may retain residual charge. **Ensure that all capacitors are fully discharged before touching the board.**
- When measuring voltage or current waveforms, **take sufficient precautions to avoid electric shock and maintain a safe distance.**

- **Precautions for Burn Prevention (High-Temperature Components)**

- MOSFETs, diodes, inductors, coils, and semiconductor devices may become **very hot during operation.** Handle them carefully to avoid burns.
- Under high load conditions, heat generation increases. **Use appropriate cooling (such as fans).**
- Component temperatures may remain high immediately after power-off. **Allow sufficient cooling time before touching.**

- **Precautions for the Evaluation Environment**

- During operation checks, implement safety measures such as **covering the board with a non-conductive enclosure** if necessary (e.g., acrylic case).
- When using motors or other moving parts, **take measures to prevent contact during operation.**
- For designs with shunt or jumper settings, **verify that the settings are correct before operation.**

- **Other Precautions**

- Loads connected to output terminals may generate heat. **Pay attention to load temperature rise.**
- Keep flammable and conductive materials away during evaluation to **avoid short circuits and accidents.**

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