

# **iXPLV<sup>®</sup> SiC MOSFET Module Gate Driver**

## **Design Guide**

**RD258-DGUIDE-01**

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**Toshiba Electronic Devices & Storage Corporation**

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## 1. Introduction

This design guide describes the circuit configuration and design overview of the iXPLV<sup>®</sup> SiC MOSFET Module Gate Driver (hereinafter referred to as “this design”).

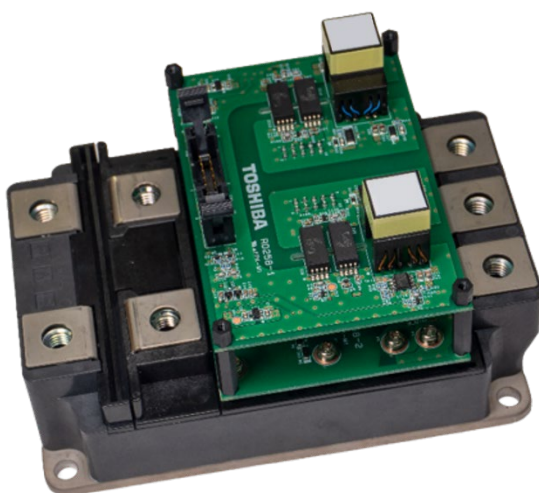
Switching devices used in power conversion equipment for industrial applications, such as motor drives, railway vehicle inverters and converters, and energy storage systems (ESS), must support high voltages and large currents. IGBT modules using Si (silicon) have traditionally been widely used for these applications. In recent years, SiC MOSFET modules using SiC (silicon carbide), which offer faster switching characteristics than IGBTs and excellent operation in high-temperature environments, have become increasingly common. The use of SiC MOSFET modules enables smaller and more efficient equipment.

This design is a gate driver that provides isolated drive for a SiC MOSFET module containing two devices in an iXPLV<sup>®</sup> package. Isolation between the primary-side circuit in the signal input section and the secondary-side circuit in the output section is implemented using the TLP2861L high-speed communication photocoupler (under development), which provides longer creepage and clearance distances than conventional products. A creepage distance of 15mm and a clearance distance of 14.2mm are secured between the primary and secondary sides.

The N-channel MOSFET [SSM6K804R](#) used as a buffer enables high-current gate drive. The design also incorporates protection circuits, including DESAT (desaturation) detection and an active Miller clamp. Each section can be adjusted to match the SiC MOSFET module being driven and the actual specifications. When making adjustments, refer to this Design Guide, the datasheets for the SiC MOSFET module and other mounted components, and the related documents.

A two-tier structure connects the two circuit boards vertically. This achieves a size equivalent to the iXPLV<sup>®</sup> package while maintaining the creepage and clearance distances described above. Because the board can be mounted directly above the SiC MOSFET module, it is easy to handle and reduces parasitic inductance in the wiring.

When using this design in an actual application, consider creepage and clearance distances, design for an appropriate operating voltage according to the applicable safety standards and operating environment, and perform sufficient verification and evaluation on the actual equipment.



**Figure 1.1 This Design Mounted Directly on a Toshiba iXPLV SiC MOSFET Module1**

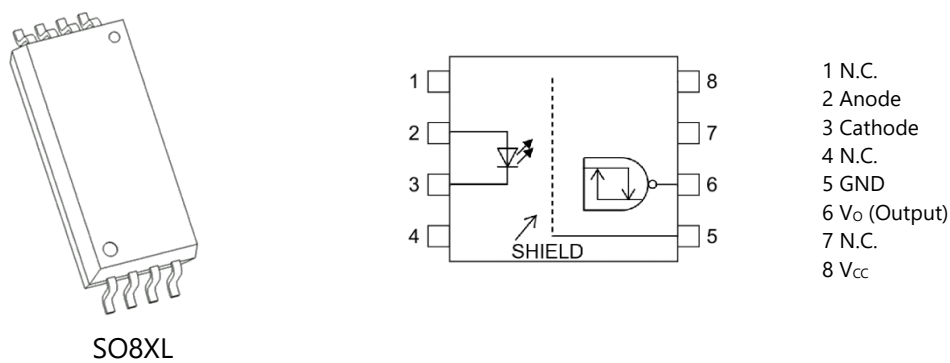
## 2. Main Components Used

This section describes the main components used in this design.

### 2.1. Photocoupler TLP2861L (Under Development)

TLP2861L photocoupler is used to transmit the gate control and fault signals with isolation between the control side and the gate-drive side. The main features of the TLP2861L are as follows:

- Inverting logic output type (totem-pole output)
- Data transmission rate: 15MBd (Typ.) (NRZ)
- Common-mode transient immunity:  $\pm 20\text{kV}/\mu\text{s}$  (Min)
- Isolation voltage:  $7500\text{V}_{\text{rms}}$  (Min)
- Creepage distance: 15mm



**Figure 2.1 TLP2861L Appearance and Internal Circuit Configuration**

### 2.2. LDO Regulator TCR1HF50B

A 150mA output [TCR1HF50B](#) LDO regulator is used to generate the 5V supply for the signal interface circuit, isolated signal transmission circuit, and the control and protection circuits of the gate-drive section. The main features of the TCR1HF50B are as follows:

- Wide input voltage range: absolute maximum rating 40V; operating range 4V to 36V
- Low bias current:  $I_{BON} = 1\mu A$  (Typ.) at  $I_{OUT} = 0mA$
- Fast load transient response:  $-60mV / +50mV$  at 3.3V output,  $I_{OUT} = 0mA$  to 10mA
- Wide output voltage lineup ( $V_{OUT} = 1.8V$  to  $5.0V$ )
- High output voltage accuracy:  $\pm 1\%$  ( $T_a = 25^\circ C$ )

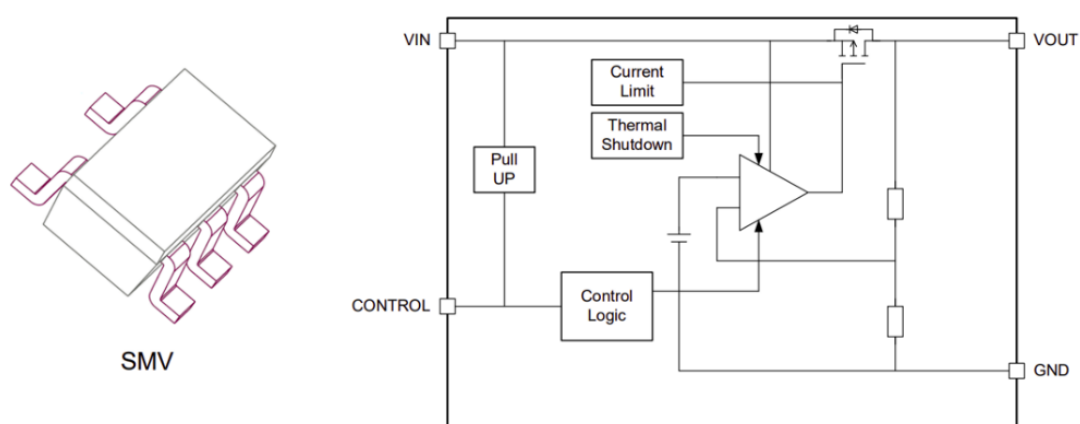


Figure 2.2 TCR1HF50B Appearance and Internal Circuit Configuration

### 2.3. MOSFET SSM3K15AFS

[SSM3K15AFS](#) N-channel MOSFET is used for signal control in the isolation circuit, isolated power-supply shutdown control circuit, and gate protection circuit. The main features of the SSM3K15AFS are as follows:

- 2.5V drive
- Low on-resistance:  $R_{DS(ON)} = 3.6\Omega$  (Max) at  $V_{GS} = 4V$ ;  $R_{DS(ON)} = 6.0\Omega$  (Max) at  $V_{GS} = 2.5V$

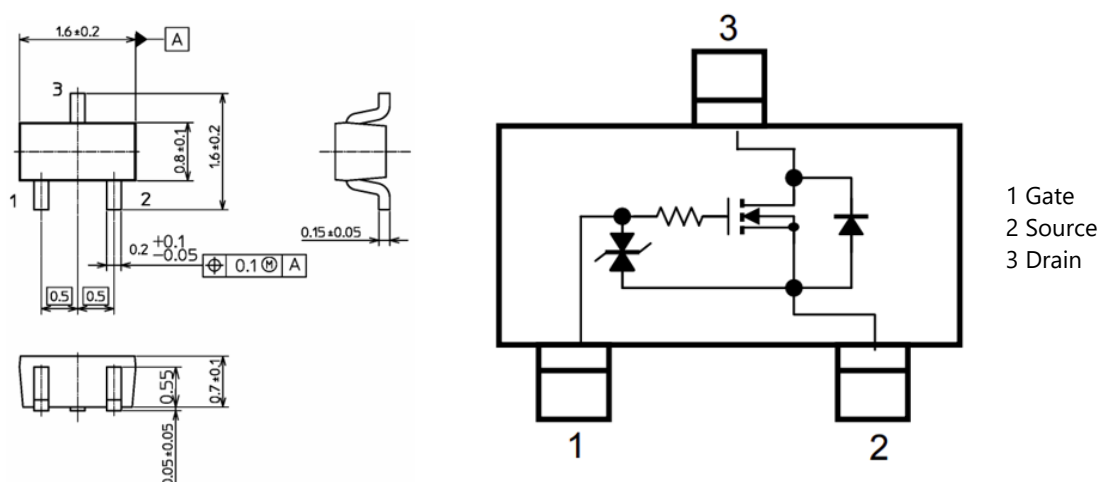
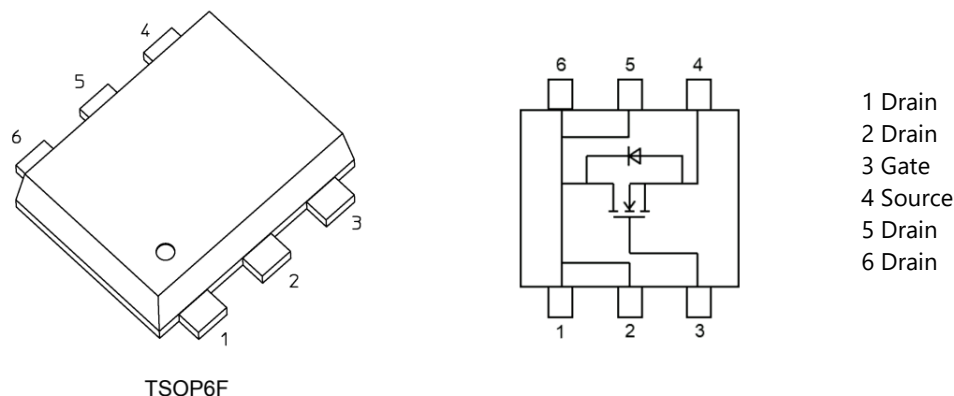


Figure 2.3 SSM3K15AFS Appearance and Internal Circuit Configuration

### 2.4. MOSFET SSM6K804R

[SSM6K804R](#) N-channel MOSFET is used in the output stage that drives the gate of the SiC MOSFET module. The main features of the SSM6K804R are as follows:

- 175°C MOSFET
- 4.5V drive
- Low on-resistance:  $R_{DS(ON)} = 12m\Omega$  (Typ.) at  $V_{GS} = 4.5V$ ;  $R_{DS(ON)} = 9m\Omega$  (Typ.) at  $V_{GS} = 10V$

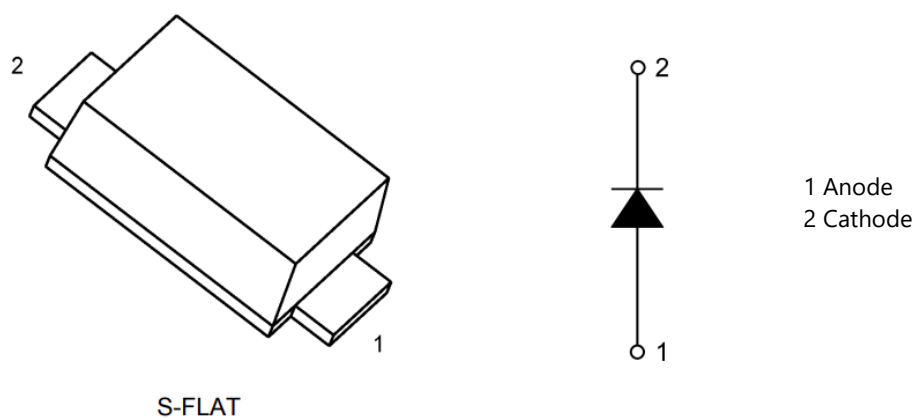


**Figure 2.4 SSM6K804R Appearance and Internal Circuit Configuration**

### 2.5. Fast-Recovery Diode CRF03A

[CRF03A](#) fast-recovery diode is used in the protection circuits of the SiC MOSFET module. The main features of the CRF03A are as follows:

- Repetitive peak reverse voltage:  $V_{RRM} = 600V$
- Average forward current:  $I_{F(AV)} = 0.7A$
- Peak forward voltage:  $V_{FM} = 2.0V$  (Max) at  $I_{FM} = 0.7A$  (pulse measurement)
- Reverse recovery time:  $t_{rr} = 100ns$  (Max) at  $I_F = 1.0A$ ,  $di/dt = -30A/\mu s$
- Compact, thin surface-mount package



**Figure 2.5 CRF03A Appearance and Internal Circuit Configuration**

### 2.6. PNP Transistor HN4A56JU

[HN4A56JU](#) PNP transistor is used in the High-side and Low-side protection circuits on the output board. The main features of HN4A56JU are as follows:

- Two devices in an ultra-super-mini 5-pin package
- High withstand voltage:  $V_{CEO} = -50V$
- High collector current:  $I_C = -150mA$  (Max)
- High current gain:  $h_{FE} = 120$  to  $400$

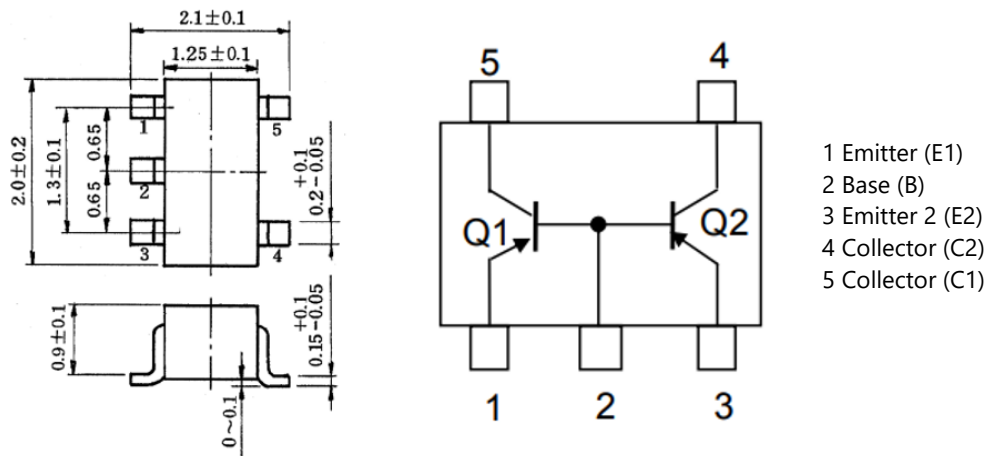


Figure 2.6 HN4A56JU Appearance and Internal Circuit Configuration

### 3. Overview of the Gate Driver for SiC MOSFET Modules

This design is a gate driver capable of driving Toshiba dual SiC MOSFET modules. It includes gate-drive circuits and various protection circuits.

#### 3.1. Features

- High-current gate drive using external buffer MOSFETs
- Single power-supply input (DC24V)
- Overcurrent protection (DESAT detection)
- Soft turn-off upon DESAT detection
- Gate-drive voltage protection (UVLO)
- Active Miller clamp (AMC)
- Output enable/disable control (EN control)
- Fault detection output (FLT signal output)

This design provides a creepage distance of 15mm at the board-mounting areas of the photocouplers and transformers and a photocoupler clearance distance of 14.2mm. Consider additional insulation treatment according to the operating environment and operating voltage.

#### 3.2. Pin Description

This design is equipped with a connector for power and signal (CN1) and uses XG4A-1431 (manufactured by OMRON).

**Table 3.1 Connector (CN1)**

| Pin# | Signal name | I/O | Description                                                      | Pin# | Signal name     | I/O | Description                        |
|------|-------------|-----|------------------------------------------------------------------|------|-----------------|-----|------------------------------------|
| 1    | GND         | -   | GND                                                              | 2    | V <sub>DD</sub> | -   | Control supply voltage             |
| 3    | B_FLT       | O   | Low-side fault detection output (collector output with resistor) | 4    | B_INA           | I   | Low-side gate control signal input |
| 5    | A_INA       | I   | High-side gate control signal input                              | 6    | B_ENA           | I   | Low-side enable signal input       |
| 7    | A_ENA       | I   | High-side enable signal input                                    | 8    | A_FLT           | O   | High-side fault detection output   |
| 9    | VP_5_A      | O   | High-side 5V power output                                        | 10   | VP_5_B          | O   | Low-side 5V power output           |

### 3.3. Specifications

Table 3.2 shows the recommended operating range of this design, and Table 3.3 shows the gate drive output voltage and the electrical characteristics of the protection function.

**Table 3.2 Recommended Operating Range**

| Item                                                                        |          | Min.    | Typ. | Max. | Unit |
|-----------------------------------------------------------------------------|----------|---------|------|------|------|
| Control Supply Voltage                                                      | $V_{DD}$ | 20.0    | 24   | 28.0 | V    |
| Input Signal<br>(gate control signal, enable signal)                        | INPUT    | H level | 4.0  | -    | V    |
|                                                                             |          | L Level | 0    | -    |      |
| Switching frequency <sup>(Note 3.1)</sup><br>(SiC MOSFET module gate drive) | $f_{sw}$ | -       | -    | 20   | kHz  |

(Note 3.1) Set the operating conditions so that each component remains within its rated temperature under actual use conditions.

**Table 3. 3 Electrical Characteristics**

| item                                                                  | Symbol                  | Conditions                    | Min  | Typ. | Max  | Unit |
|-----------------------------------------------------------------------|-------------------------|-------------------------------|------|------|------|------|
| Gate-driven output<br>H-level voltage                                 | $V_{P\_20\_A}$          |                               | 19   | 20   | 21   | V    |
| Gate-driven output<br>L-level voltage                                 | $V_{N\_6\_VEE\_A}$      |                               | -7.0 | -6.7 | -6.4 | V    |
| UVLO_High-side<br>threshold<br>( $V_{P\_24\_A}-V_{0\_VE\_A}$ )        | $V_{UVLOP\_A}$          | Protection activation voltage | -    | 15   | -    | V    |
|                                                                       | $V_{UVLOP\_+A}$         | Protection release voltage    | -    | 16   | -    |      |
| UVLO_Low-Side<br>threshold<br>( $V_{P\_24\_B}-V_{0\_VE\_B}$ )         | $V_{UVLOP\_B}$          | Protection activation voltage | -    | 15   | -    | V    |
|                                                                       | $V_{UVLOP\_+B}$         | Protection release voltage    | -    | 16   | -    |      |
| When DESAT is<br>detected<br>Drain-to-source<br>voltage<br>(Note 3.2) | $V_{DS}$<br>(High-side) | $T_a = 25^{\circ}\text{C}$    | 2.7  | -    | -    | V    |

(Note 3. 2) The drain-source voltage at DESAT detection is equal to the DESAT threshold voltage minus the voltage drops across diodes D26, D27, D28, and D29 and resistors R85 and R86. Refer to "DESAT (Desaturation) Detection Circuit Operation" in section 4 and Figure 4.8.

### 4.1. Overall Block Diagram

The figure consists of two circuit diagrams, one for a high-side MOSFET driver and one for a low-side MOSFET driver. Both diagrams share a common power supply section on the left, which includes a VDD input (20V to 28V), a TCR1HF50B, an LDO, and an SSM3K15AFS MOSFET. The high-side driver (top) features an isolated DC-DC converter providing VCC1 and VEE1 to a gate driver. The gate driver controls an SSM6K804R MOSFET, which is connected to a high-side drain. A protection circuit is also shown, featuring a DESAT signal and a soft turn-off mechanism. The low-side driver (bottom) features an isolated DC-DC converter providing VCC2 and VEE2 to a gate driver. The gate driver controls an SSM6K804R MOSFET, which is connected to a low-side drain. A protection circuit is also shown, featuring a DESAT signal and a soft turn-off mechanism. Both diagrams include logic isolation and TLP2861L (under development) components for signal isolation.

### Figure 4. 1 Gate Driver Block Diagram for SiC MOSFET Modules

## 4.2. Gate Control Circuit (Primary-Side)

Figure 4.2 shows the primary-side (input side) circuit of this design.

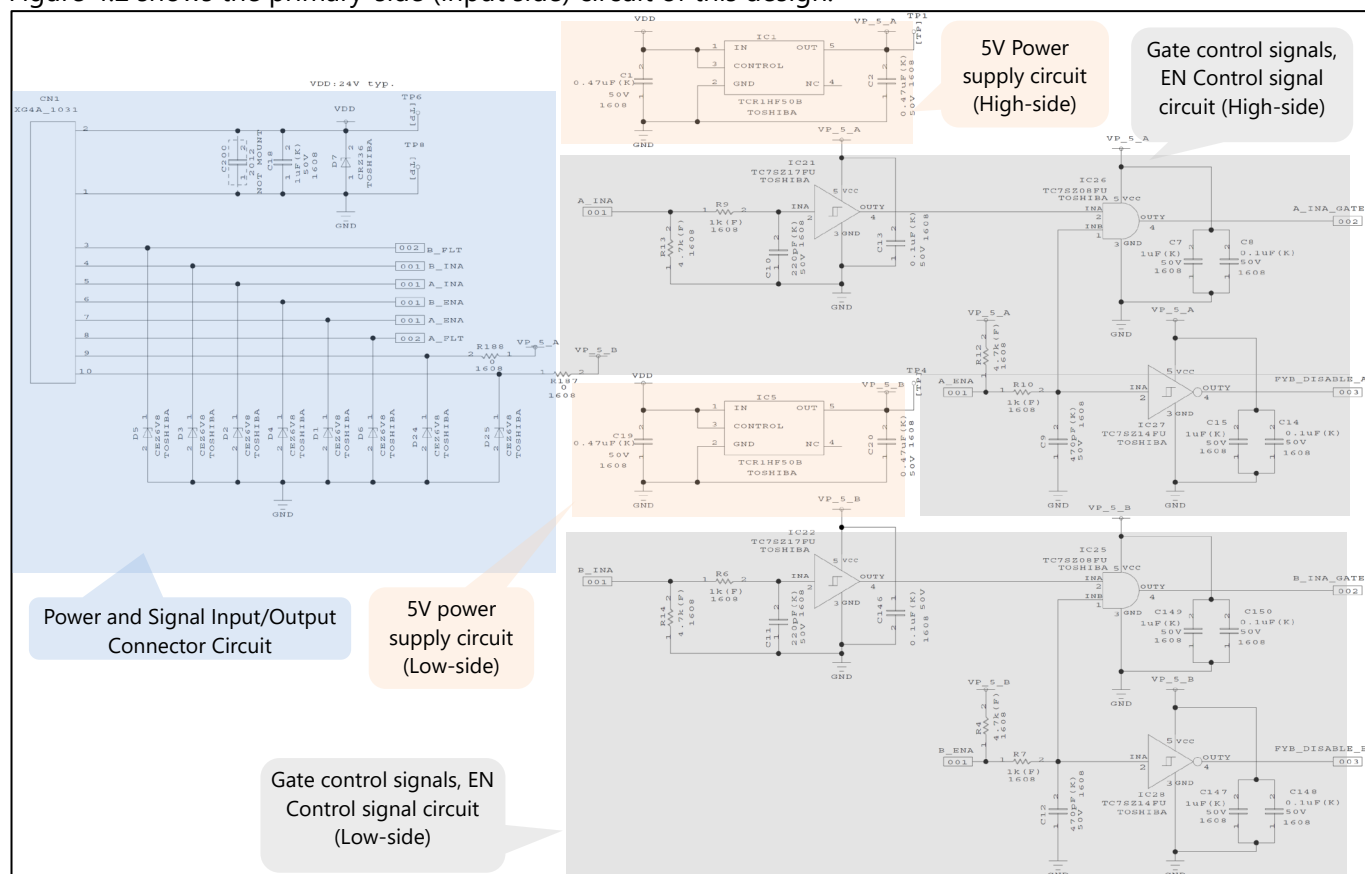


Figure 4. 2 Primary-Side Circuit Diagram

### Internal 5V Power Supply Circuit

TCR1HF50B LDO regulators (IC1 and IC5) generate a 5V supply from the V<sub>DD</sub> supply voltage.

The 5V output of the TCR1HF50B is supplied to the primary-side logic ICs (IC2, IC3, and IC4) and to the input signal circuits of the TLP2861L (IC6, IC9, IC10, and IC13).

### Gate Control Signal Input

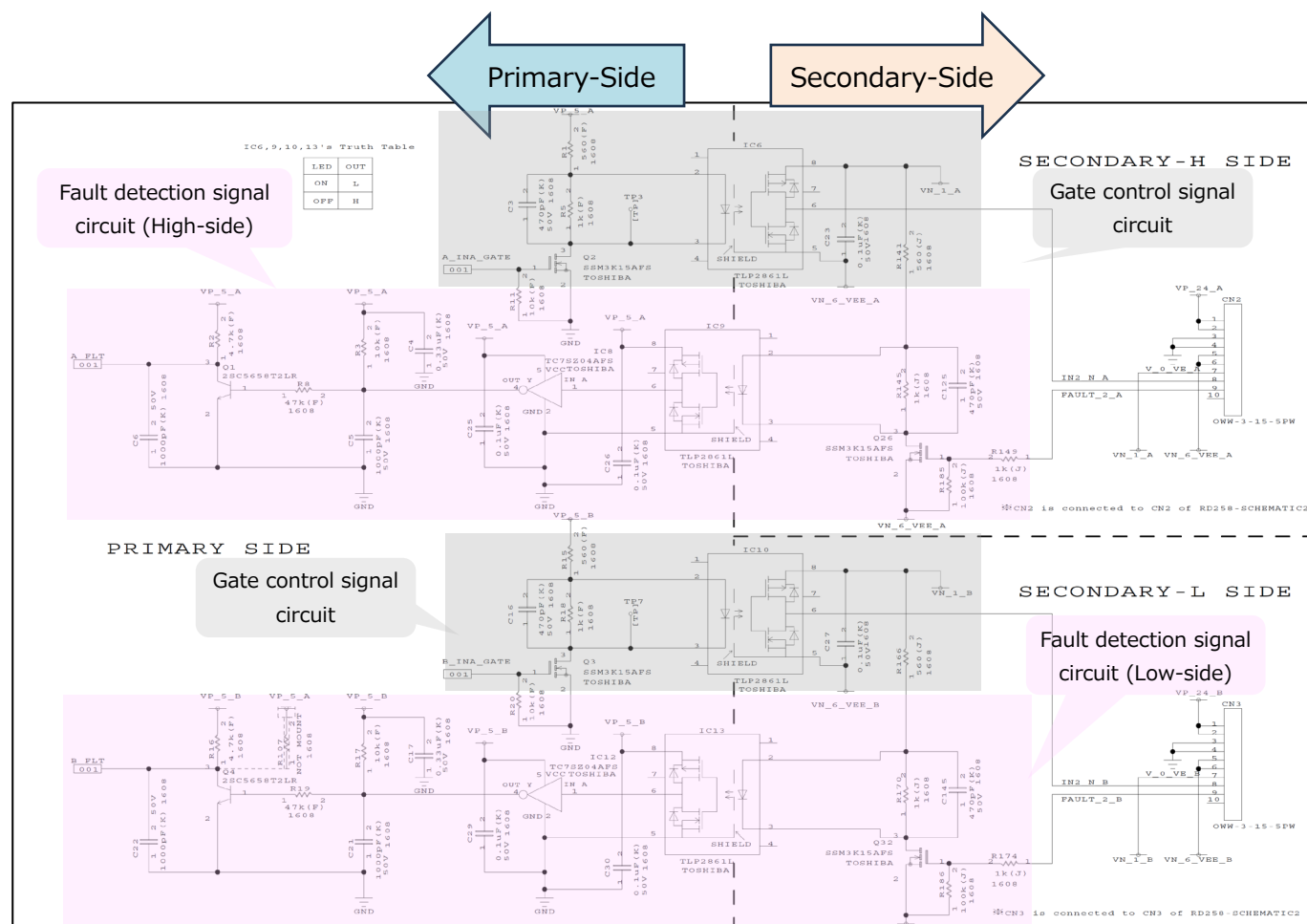
For High-side, gate control signal inputs include A\_INA (input signal) and A\_ENA (enable). A\_ENA can control whether the gate drive output is enabled or disabled. When enabled, the A\_ENA signal is at the H level, and when disabled, it is at the L level. When A\_ENA is open, it is enabled because it is pulled up by the internal circuit.

Table 4. 1 Truth Value Table

| A_INA<br>(CN1:Pin5) | A_ENA<br>(CN1:Pin7) | SiC MOSFET<br>Module_A |
|---------------------|---------------------|------------------------|
| L                   | L                   | OFF                    |
| H                   | L                   | OFF                    |
| H                   | H                   | ON                     |
| L                   | H                   | OFF                    |

Because a pull-up resistor is connected to the A\_ENA pin in this design, the circuit is active when no A\_ENA signal is input. A Low-level input is required to disable the circuit using A\_ENA.

The Low-side gate control inputs B\_INA (input signal) and B\_ENA (enable) operate in the same manner as the High-side inputs. Table 4.1 shows the truth table.



**Figure 4.3 Isolated Signal Circuit Between the Primary and Secondary Sides Using Photocouplers**

### Fault Detection Output Circuit

Figure 4.3 shows the High-side and Low-side fault detection output circuits.

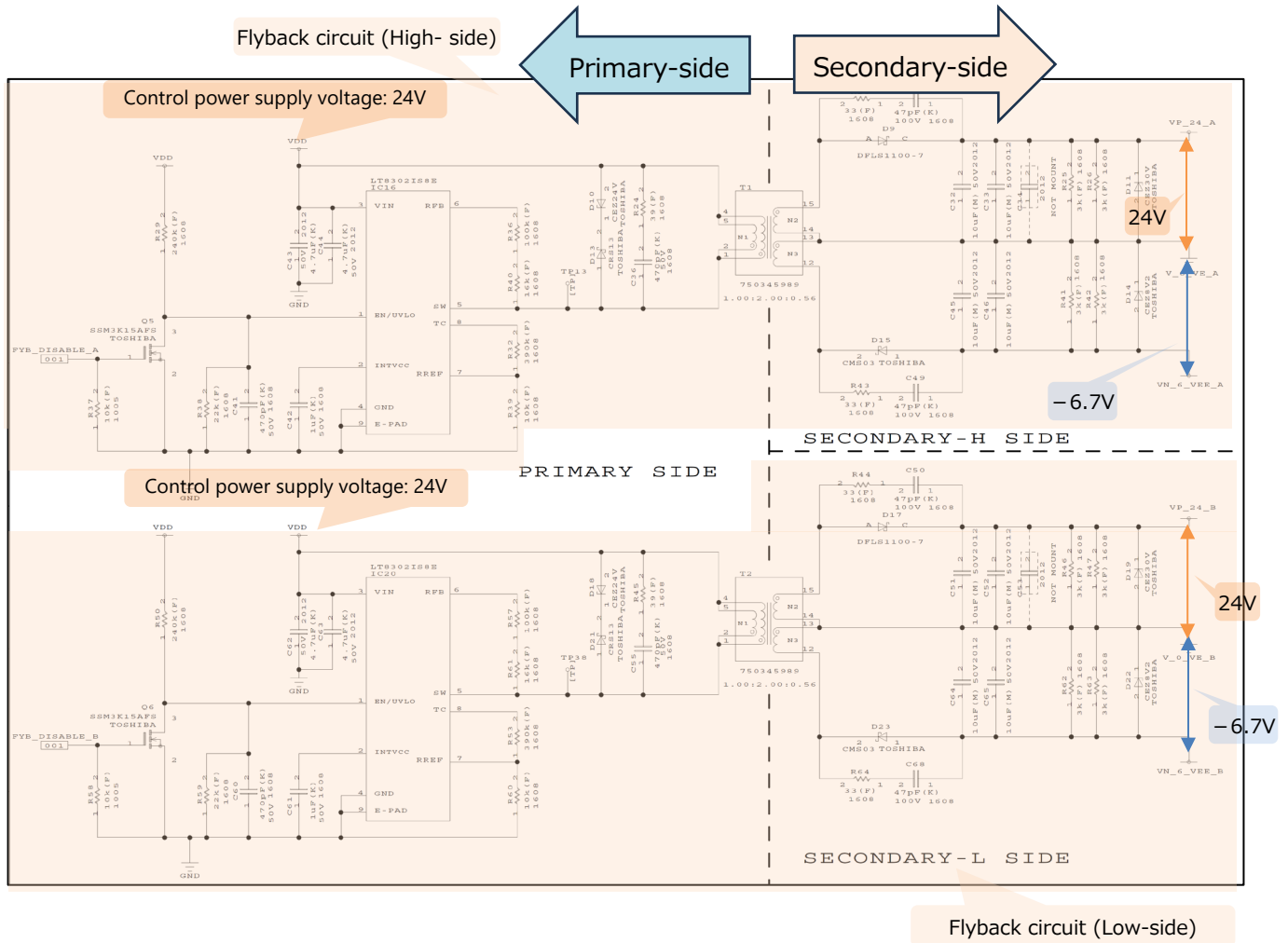
When a High-side fault is detected in the SiC MOSFET module (undervoltage protection or DESAT operation), the fault signal is transmitted from the secondary-side to the primary-side through photocoupler TLP2861L (IC9).

When a fault is detected, FAULT\_A goes High, transistor Q1 turns on, and A\_FLT goes Low. A\_FLT and B\_FLT are resistor pull-up collector outputs (Q1), allowing wired-OR connection. When normal operation resumes, the A\_FLT pin output changes from Low to High.

**Table 4. 2 Truth Value Table**

| UVLO   | DESAT detection | FLT output (CN1: pins 8 and pin 3) |
|--------|-----------------|------------------------------------|
| lift   | None            | H Level                            |
| action | None            | L Level                            |
| lift   | Available       | L Level                            |
| action | Available       | L Level                            |

B\_FLT on the Low-side operates in the same manner as the high-side. Table 4.2 shows the truth table.



**Figure 4.4. Isolated Flyback DC-DC Converter Circuit**

### Isolated Flyback DC-DC Converter Circuit

Figure 4.4 shows the isolated flyback DC-DC converter circuit. It converts the VDD control supply voltage into a positive 24V supply ( $V_{P\_24\_A} - V_{E\_0\_VE\_A}$ ) and a negative voltage of -6.7V ( $V_{E\_0\_VE\_A} - V_{N\_6\_VEE\_A}$ ).

These output voltages are set considering the rated gate voltage, gate switching characteristics, and low voltage detection (UVLO) of the SiC MOSFET module used.

The Low-side gate-drive power-supply circuit has the same configuration.

The LT8302 is used as the flyback converter control IC. The output voltages can be set by the external resistors (R36, R39, and R40) and transformer T1 turns ratios ( $N_{PS2}$  and  $N_{PS3}$ ), as shown in the following equations.

$$V_{P\_24\_A} - V_{E\_0\_VE\_A} = V_{REF(LT8302)} \times \left( \frac{R36 + R40}{R39} \right) \times \left( \frac{1}{N_{PS2}} \right) - V_F$$

$$V_{E\_0\_VE\_A} - V_{N\_6\_VEE\_A} = V_{REF(LT8302)} \times \left( \frac{R36 + R40}{R39} \right) \times \left( \frac{1}{N_{PS3}} \right) - V_F$$

$V_{REF(LT8302)} = 1.0V$  (LT8302 internal reference voltage)

The turn ratios of the T1 in this design are shown in Table 4.3.

Table 4. 3 Transformer Turn Ratio

|                  | Voltage | Turn ratio              |
|------------------|---------|-------------------------|
| Positive voltage | 24V     | $N_{PS2} = 0.5 (N1:N2)$ |
| Negative voltage | -6.7V   | $N_{PS3} = 1.8 (N1:N3)$ |

### 4.3. Secondary-Side Control Circuit

#### Secondary-Side Power-Supply Circuit

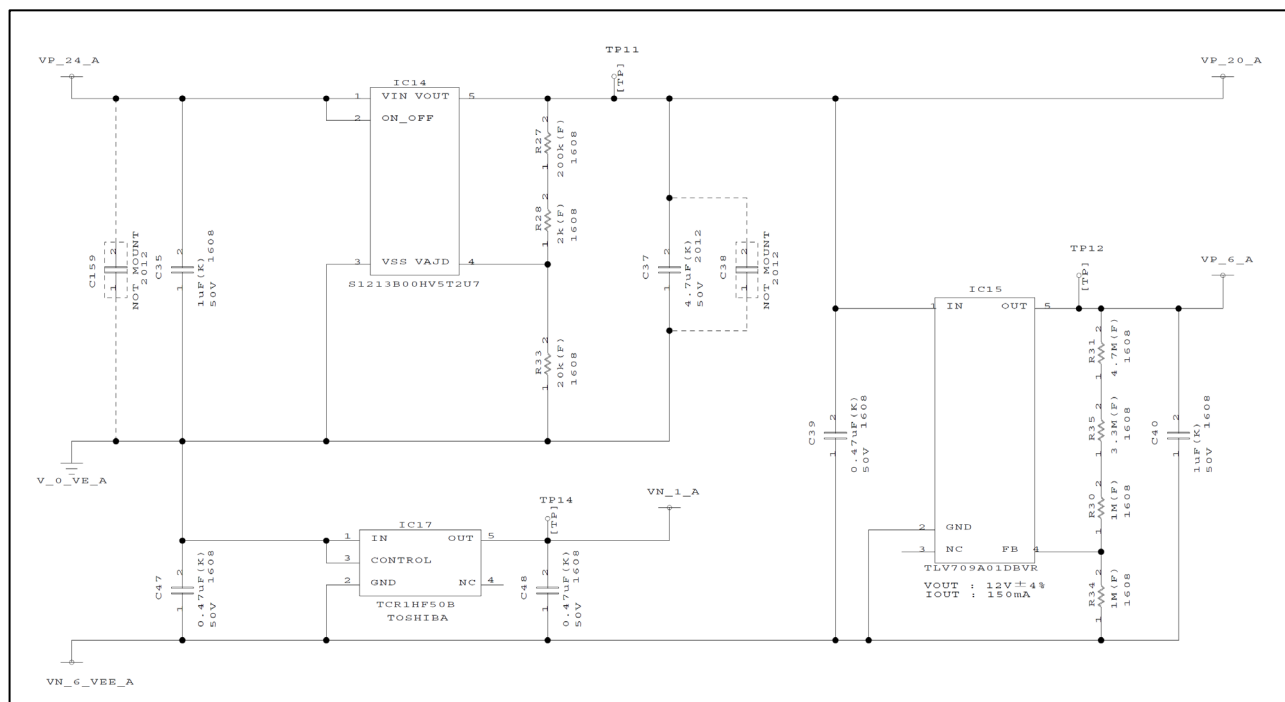


Figure 4. 5 Secondary-Side Power Supply Circuit

Figure 4.5 shows the secondary-side power-supply circuit. The voltages supplied to the secondary-side,  $V_{P\_24\_A}$  (24V) and  $V_{N\_6\_VEE\_A}$  (-6.7V), are used to generate the voltages required on the secondary-side. LDO IC14 outputs a regulated 20V supply. LDO IC17 outputs a regulated 5V supply between  $V_{N\_1\_A}$  and  $V_{N\_6\_VEE\_A}$ , which is the main supply for the secondary-side control logic. LDO IC15 generates  $V_{P\_6\_A}$ . The voltage between  $V_{P\_6\_A}$  and  $V_{N\_6\_VEE\_A}$  is 12V and supplies IC35, which controls gate-voltage turn-on and turn-off.

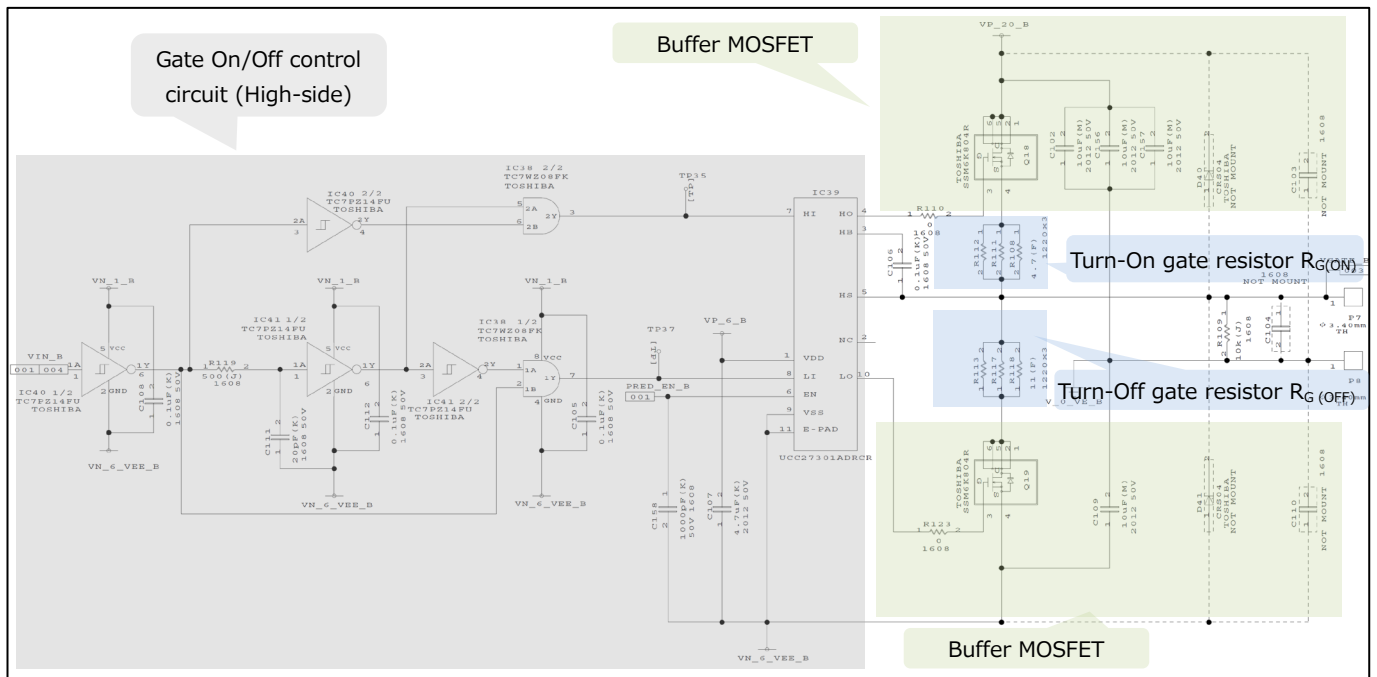


Figure 4. 6 Gate Drive Circuit (High-Side)

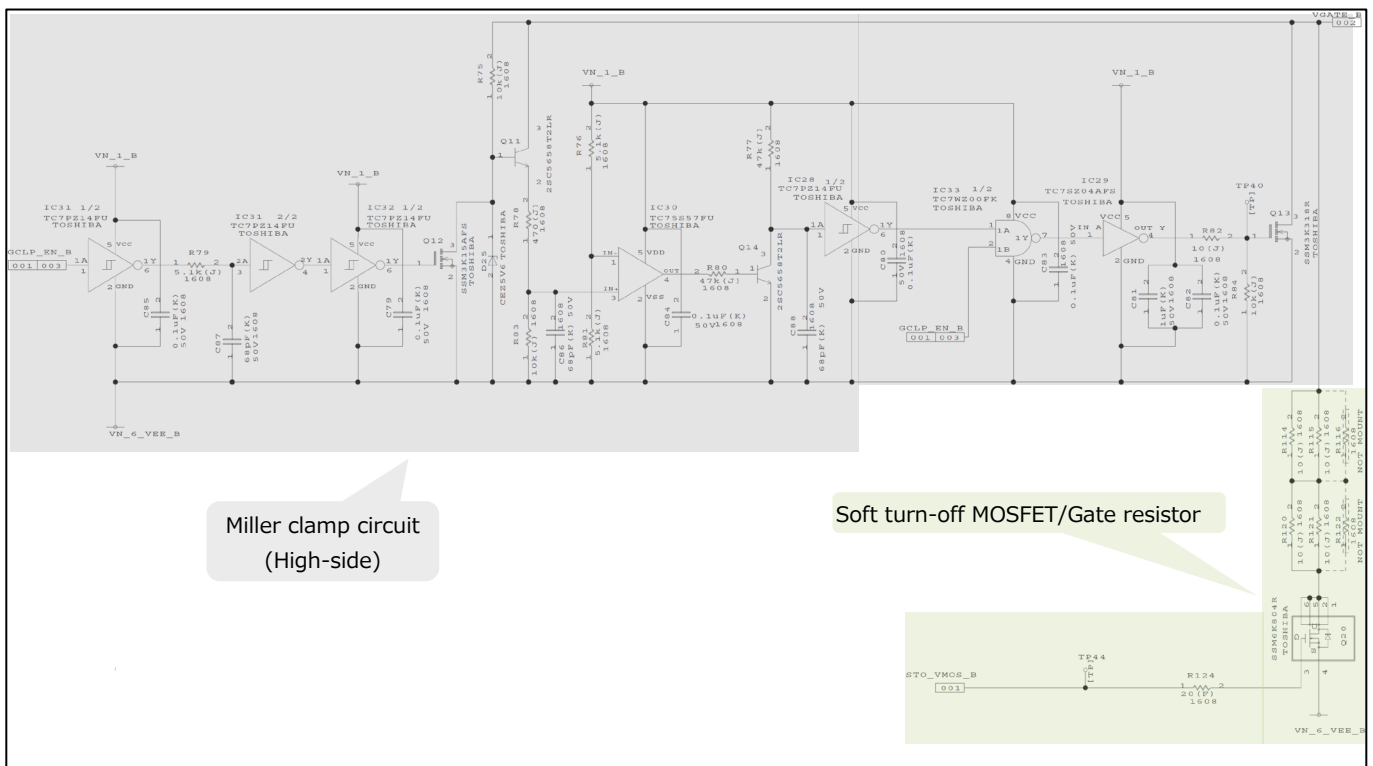


Figure 4. 7 Active Miller Clamp Circuit (High-Side)

### **Gate Drive Circuit**

Figure 4.6 shows the gate drive circuit for the high-side. The Low-side has the same configuration as the High-side.

The gate drive circuit consists of buffer MOSFETs for high-current gate drive (Q15, Q16), gate resistors for turn-on and turn-off adjustment, DESAT detection circuits, MOSFETs for soft turn-off, and resistors for overcurrent protection.

When the gate control signal input to A\_INA (CN1 pin 5) goes High, the HO output of gate-driver IC35 goes High and turns on buffer N-channel MOSFET Q15. This charges the gate of the SiC MOSFET module and turns on the SiC MOSFET.

When the gate control signal input to A\_INA (CN1 pin 5) goes Low, the LO output of gate-driver IC35 goes High and turns on buffer N-channel MOSFET Q16. This removes charge from the gate of the SiC MOSFET module and turns off the SiC MOSFET module.

### **Active Miller Clamp**

In a bridge configuration in which devices are connected in series on the upper and lower sides, the high drain-source  $dv/dt$  generated when one device turns on can cause displacement current to flow through the drain-gate capacitance of the other device that is off, resulting in unintended gate operation. This failure mode is called self-turn-on. The active Miller clamp prevents this malfunction.

Figure 4.7 shows the Miller clamp circuit.

### 4.4. Protection Circuits and Additional Features

This section describes the High-side protection circuits. The Low-side circuits have the same configuration.

#### DESAT (Desaturation) Detection Circuit Operation

The DESAT detection function monitors the drain-source voltage ( $V_{DS}$ ) of the on-state SiC MOSFET module at the DESAT\_A pin to protect the module from damage due to excessive current.

If an abnormally large drain current ( $I_D$ ) flows through the SiC MOSFET module,  $V_{DS}$  increases with  $I_D$  according to the static  $I_D$ - $V_{DS}$  characteristic curve. The DESAT\_A pin monitors  $V_{DS}$ . If it exceeds the DESAT threshold voltage,  $V_{DESAT} = 11.9V$  (Typ.), which is the reference voltage of comparator IC51, operation of the SiC MOSFET module is stopped and the A\_FLT output at CN1 changes from High to Low.

The DESAT detection method cannot directly monitor drain current ( $I_D$ ), so high accuracy is not possible. However, its relatively simple configuration makes it suitable for emergency shutdown when a large current occurs.

Figure 4.8 shows the DESAT detection circuit.

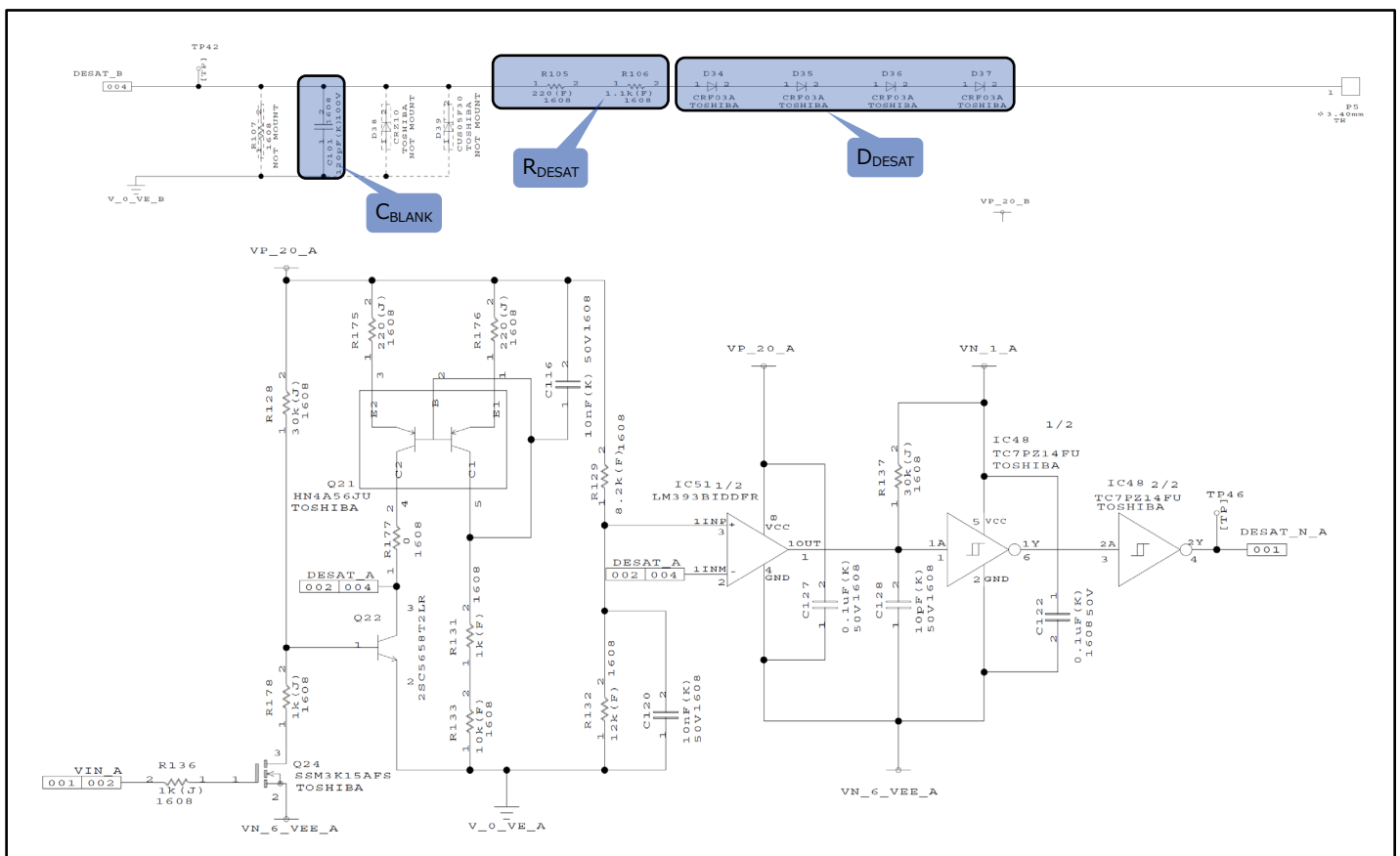


Figure 4.8 DESAT Detection Circuit

When the SiC MOSFET is on, the DESAT\_A pin acts as a constant-current source and supplies an approximately 1.8mA blanking-capacitor charging current  $I_{CHG}$  to charge blanking capacitor  $C_{BLANK}$  (C89), connected between the DESAT\_A and  $V_{0\_VE\_A}$  pins. The voltage across  $C_{BLANK}$  equals the voltage drop produced when  $I_{CHG}$  flows through  $R_{DESAT}$  (R85 and R86), high-voltage diodes  $D_{DESAT}$  (D26, D27, D28, and D29), and the drain-source path  $V_{DS}$  of the SiC MOSFET module. The voltage between DESAT\_A and  $V_{0\_VE\_A}$ , i.e.  $V_{DESAT\_A(ON)}$  is expressed by the following equation.

$$V_{DESAT\_A(ON)} = V_{DS} + V_F(D_{DESAT}) + I_{CHG} \times R_{DESAT}$$

$$V_{DESAT\_A(ON)} = V_{DS} + V_F(D26 + D27 + D28 + D29) + I_{CHG} \times (R85 + R86)$$

Because the SiC MOSFET module is on,  $I_{CHG}$  is superimposed on the drain current  $I_D$  of several tens of amperes or more flowing between the drain and source. Therefore,  $V_{DS}$  in the equation above is the voltage generated according to the static  $I_D$ - $V_{DS}$  characteristic curve of the SiC MOSFET module, and the voltage drop caused by the small  $I_{CHG}$  current is included in the voltage drop caused by  $I_D$  and is not separately visible.

During normal on-state operation,  $V_{DS}$  of the SiC MOSFET module is determined by  $I_D$ . When overcurrent occurs,  $V_{DS}$  also rises. If  $V_{DESAT\_A(ON)}$  exceeds  $V_{DESAT}$ , the circuit determines that a fault has occurred and turns on soft-turn-off MOSFET Q17. Resistor  $R_s$  connected to the drain of Q17 gradually removes the gate charge. This suppresses the spike voltage generated between the drain and source and softly shuts down the SiC MOSFET module to prevent damage (Figure 4.7). Because the DESAT detection condition is  $V_{DESAT\_A(ON)} = V_{DESAT}$ , it is expressed by the following equation.

$$V_{DESAT} = V_{DESAT\_A(ON)} = V_{DS} + V_F(D26 + D27 + D28 + D29) + I_{CHG} \times (R85 + R86) \quad (4-1)$$

By modifying Equation (4-1),  $R85$  and  $R86$  can be represented by Equation (4-2).

$$R85 + R86 = \frac{(V_{DESAT} - V_F(D26 + D27 + D28 + D29) - V_{DS})}{I_{CHG}} \quad (4-2)$$

$V_{DS}$  at DESAT detection is obtained by selecting the overcurrent value and referring to the drain-source voltage ( $V_{DS}$ ) versus drain current ( $I_D$ ) characteristics of the SiC MOSFET module used (Figure 4.9). In this design, based on the specifications of the MG800FXF2YMS3, the DESAT overcurrent  $I_{DESAT}$  is set to  $I_D \leq 1600A$  at  $T_{CH} = 25^\circ C$ . When  $I_{DESAT} = 1600A$ , the  $V_{DS}$  of the MG800FXF2YMS3 can be read as 2.7V from Figure 4.9.

In this design,  $(R85 + R86)$  is calculated under the following conditions.

DESAT overcurrent  $I_{DESAT}$ : 1600A

MG800FXF2YMS3 drain-source voltage  $V_{DS}$ : 2.7V

DESAT threshold voltage  $V_{DESAT}$ : 11.9V

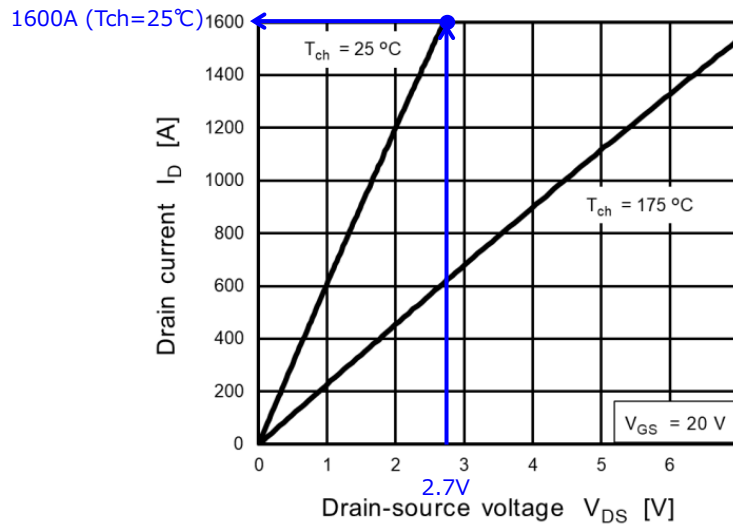
Blanking-capacitor charging current  $I_{CHG}$ : 1.8mA

Forward voltage  $V_F$  of high-voltage diodes  $D_{DESAT}$  (D26 to D29): 5.2V

From equation (4-2),  $R85$  and  $R86$  are:

$$R85 + R86 = \frac{(11.9V - 5.2V - 2.7V)}{1.8mA} \cong 2222\Omega \quad (4-3)$$

Here, R85 is set to 2kΩ and R86 to 240Ω. Design appropriate values according to the actual specifications and thoroughly verify operation on the actual equipment.



**Figure 4.9  $I_D$ - $V_{DS}$  Characteristics (MG800FXF2YMS3)**

The DESAT\_A pin is connected to the drain of the SiC MOSFET module through high-voltage diodes  $D_{DESAT}$ . When the SiC MOSFET module is on, external noise may cause the module drain voltage to fluctuate, which can in turn cause the DESAT\_A voltage to fluctuate through the junction capacitance of  $D_{DESAT}$ . If this fluctuation exceeds  $V_{DESAT}$ , the protection operation starts and softly shuts down the SiC MOSFET module. Because noise generated in high-voltage inverter circuits is large, blanking capacitor  $C_{BLANK\_A}$  (C89) is added to form a low-pass filter.

As a trade-off of adding  $C_{BLANK\_A}$  (C89), a blanking time  $t_{BLANK}$  occurs after overcurrent begins until  $V_{DESAT\_A(ON)}$  reaches  $V_{DESAT}$ .

The blanking time  $t_{BLANK}$  is given by the following equation.  $t_{r(ON)}$  is the turn-on time of transistor Q21 used in the current-mirror circuit that generates the blanking-capacitor charging current  $I_{CHG}$ .

$$t_{BLANK} = (C89 \times V_{DESAT}) / I_{CHG} + t_{r(ON)} \quad (4-4)$$

In this design,  $t_{BLANK}$  is calculated using the following conditions.

Blanking capacitor  $C_{BLANK\_A}$  (C89): 120pF

DESAT threshold voltage  $V_{DESAT}$ : 11.9V

Blanking-capacitor charging current  $I_{CHG}$ : 1.8mA

Q21 turn-on time  $t_{r(ON)}$ : 240ns

From Equation (4-4), the blanking time  $t_{BLANK}$  is approximately 1.03μs. Desaturation is not detected during the blanking time.

The time from the occurrence of overcurrent until the gate voltage turns off,  $t_{DESAT\_TOTAL}$ , is the sum of  $t_{BLANK}$  and  $t_{DESAT(delay)}$ , which includes the delay of comparator IC51 used for DESAT detection and the delays of logic ICs IC48, IC49, IC47, and IC53.

$$t_{DESAT\_TOTAL} = t_{BLANK} + t_{DESAT(delay)} \quad (4-5)$$

In this design,  $t_{\text{DESAT\_TOTAL}}$  is calculated using Equation (4-5) under the following conditions.

Blanking capacitance  $C_{\text{BLANK}}$ : 120pF

DESAT threshold voltage  $V_{\text{DESAT}}$ : 11.9V

Blanking-capacitor charging current  $I_{\text{CHG}}$ : 1.8mA

DESAT delay time  $t_{\text{DESAT(delay)}}$ : 0.3μs

$t_{\text{DESAT\_TOTAL}}$  is 1.33μs, as shown by the following equation.

$$t_{\text{DESAT\_TOTAL}} = 1.03\mu\text{s} + 0.3\mu\text{s} \cong 1.33\mu\text{s}$$

If a protection diode is connected in parallel with  $C_{\text{BLANK\_A}}$  (C89), note that the terminal capacitance of the protection diode affects  $t_{\text{BLANK}}$ .

$C_{\text{BLANK\_A}}$  (C89) and  $R_{\text{DESAT\_A}}$  (R85 + R86) also affect the SiC MOSFET module  $V_{\text{DS}}$  at DESAT detection and the noise immunity of the DESAT\_A pin (CR filter constant), so adjust them carefully. Depending on the actual operating conditions, parasitic inductance ( $L_s$ ) in the wiring may generate a large surge voltage when current is interrupted. If this exceeds the rated voltage of a component, damage may occur. Connecting a snubber circuit close to the SiC MOSFET module is effective in reducing surge voltage caused by  $L_s$ . Thoroughly verify DESAT detection operation on the actual equipment.

### UVLO Function (Under Voltage Lockout)

Figure 4.10 shows the UVLO circuit. It monitors the secondary-side positive supply voltage ( $V_{P\_20\_A}$  -  $V_{0\_VE\_A}$ ) and stops operation when the voltage falls below the UVLO operating threshold  $V_{UVLOP\_A}$ . Normal operation resumes when the positive supply voltage exceeds  $V_{UVLOP\_A}$ . This function prevents current from flowing between the drain and source of the SiC MOSFET module when the gate voltage is insufficient, helping prevent damage due to overheating.

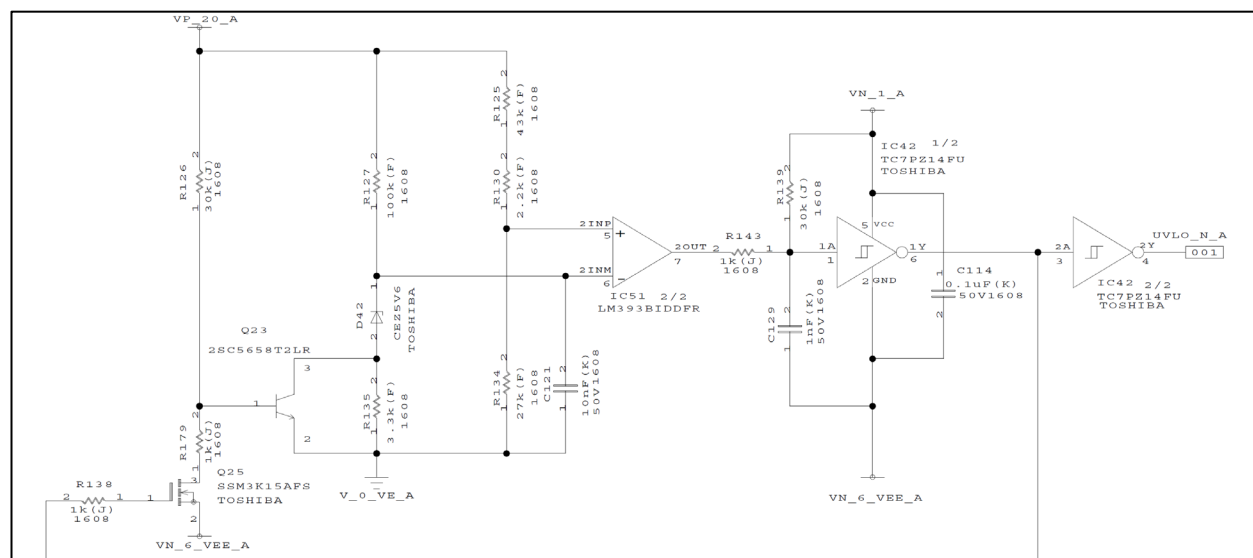


Figure 4.10 UVLO Detection Operation

### Power-On Reset Circuit

Figure 4.11 shows the power-on reset circuit. After the DESAT function operates, an FLT signal is output and the gate is locked so that it cannot be turned on. To release the lock, the power-on reset circuit must be operated by restarting the power supply.

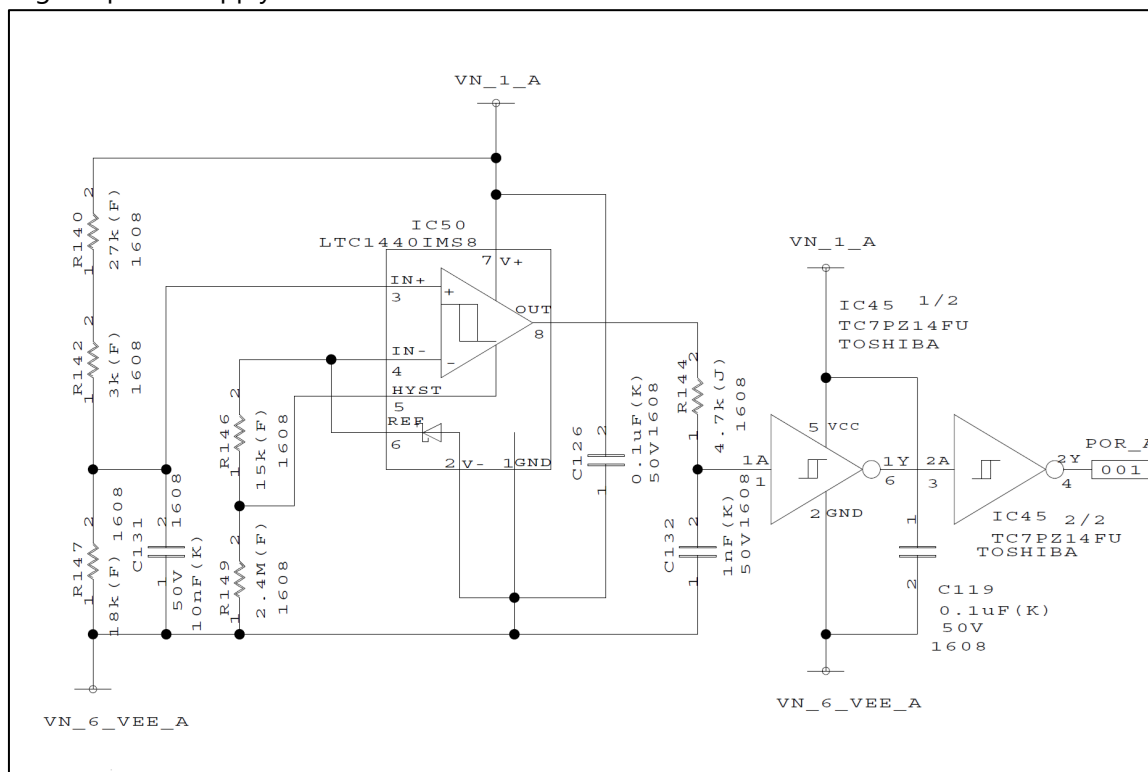
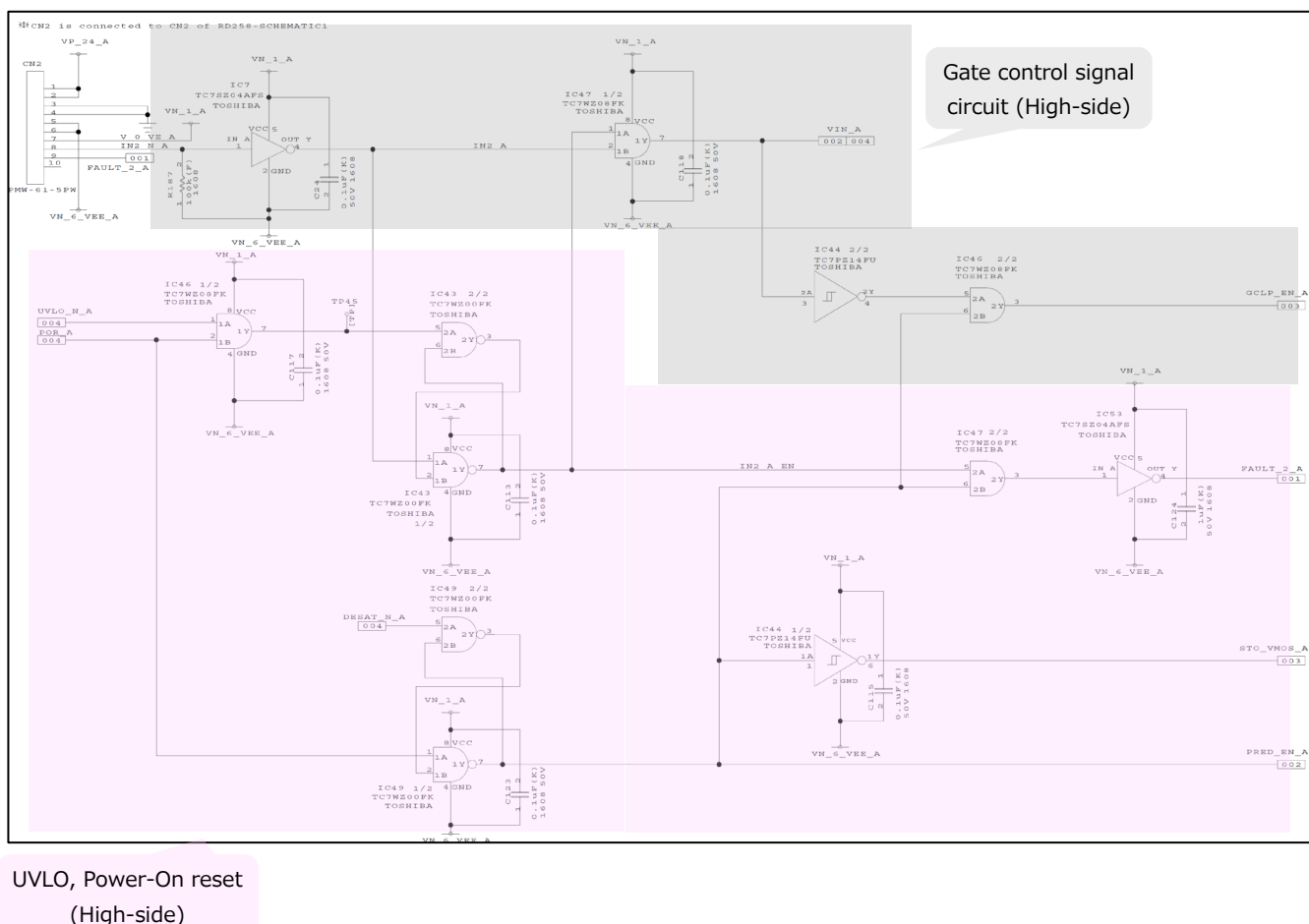


Figure 4.11 Power-On Reset Circuit



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