eFuse IC TCKE1401NM Application Note

Description

The TCKE1401NM is a 75 V high input voltage single input-single output eFuse IC. It can be used as a reusable fuse, and includes protection features like adjustable overcurrent limit, adjustable undervoltage lockout and adjustable overvoltage protection by external resistor, short circuit protection, adjustable slew rate control by an external capacitance and thermal shutdown. With low ON resistance of 44.5 mΩ (Typ.) and high output-current capability of up to 6.0 A characteristics, this device is suitable for protecting the power supply circuit of fan line, storage power supply circuit and Industrial power supply applications, etc. This device is available in a small package VQFN24D (4.0 mm (Typ.) x 4.0 mm (Typ.)).

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1. Introduction

Fuses and poly switches (resettable fuses or poly fuses) are widely used as safety components to prevent overheating, fire, and other hazards in various electronic devices. Both are protective devices that use the Joule heating generated when a current exceeding the rated value flows. In this document, these devices are referred to as conventional fuses.

Glass-tube fuses and chip fuses interrupt current by melting an internal metal element. Poly switches limit current through a rapid increase in resistance caused by the thermal expansion of a conductive polymer. In this way, conventional fuses protect circuits and prevent damage to equipment.

However, conventional fuses have several disadvantages. Their operating current has low accuracy, and their cutoff current varies widely. Protection is also delayed because these devices rely on Joule heating.

In addition, fuses that melt a metal element are irreversibly destroyed once they operate, so the fuse itself must be replaced.

As shown in Figure 1.1, an eFuse IC (electronic fuse) uses a MOSFET to interrupt current and overcomes these disadvantages of conventional fuses. An eFuse IC can be used in the same way as a conventional fuse. Because it is an IC, it can also provide various protection functions in addition to overcurrent protection.

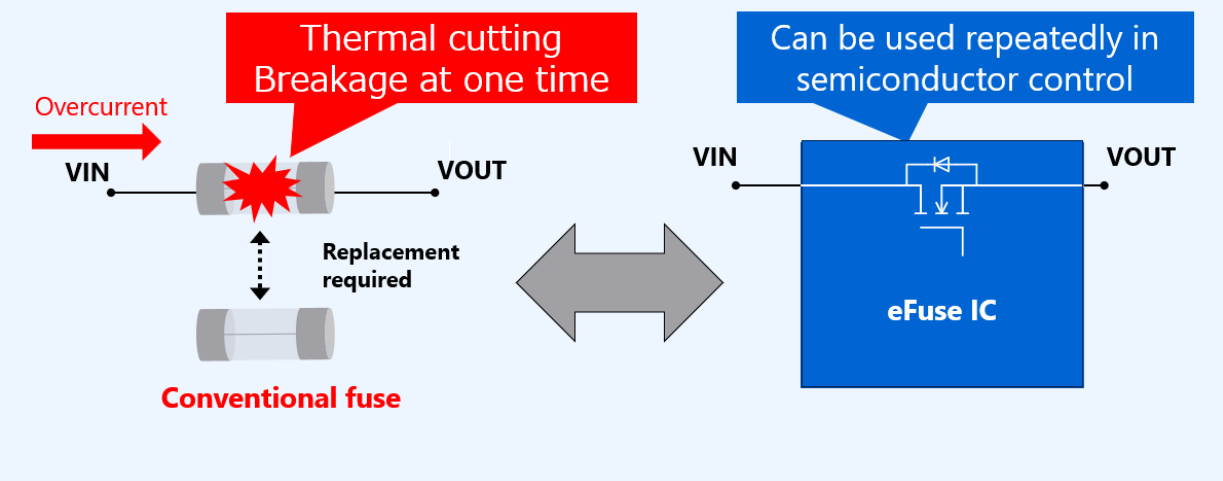


Figure 1.1 Difference between conventional fuses and eFuse IC

This document describes the main characteristics, operation, usage, and application of the TCKE1401NM, which incorporates various protections, including Over Current protection (OCP), Short Circuit Protection (SCP), Overvoltage protection (OVP), Undervoltage lockout (UVLO), and Thermal Shutdown (TSD), as well as an Inrush current limit function, FLAG function (Note 1), Power Good (PGOOD) (Note 2), and output current monitor function (Note 3). In addition, this document describes the reverse input polarity protection and always-on reverse current blocking functions using an external MOSFET, as well as how to set the thresholds for some of the protections.

Note 1: FLAG function : Outputs a signal to notify an external circuit when an abnormal condition is detected.
Note 2: Power Good function : Outputs a signal to notify an external circuit when the output voltage reaches the specified level.
Note 3: Output current monitor function : Outputs a small current proportional to the output current. The current can be monitored as a voltage using an external resistor.

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2. What is an eFuse IC?

2.1. How to use the eFuse IC

An eFuse IC uses a semiconductor switch to interrupt current, a task that conventional fuses perform by melting a metal element. When it detects an overcurrent exceeding the set value, it controls the internal MOSFET to limit or interrupt the current. Figure 2.1 shows a block diagram of an eFuse IC used to supply power to a PMIC (Power Management IC).



Figure 2.1 Example of eFuse IC usage and main function

In this example, an eFuse IC is inserted in the power line of the PMIC instead of a conventional fuse. When an overcurrent flows due to a fault in the PMIC itself or in the downstream circuits, the eFuse IC limits or interrupts the current to protect the circuits, helping to prevent the equipment from emitting smoke or catching fire.

2.2. Benefits of using eFuse IC

- **Reduction of maintenance costs and time by eliminating the need for replacement**

An eFuse IC interrupts the current by turning off its internal MOSFET. Unlike a conventional fuse, which irreversibly blows when an overcurrent condition occurs, an eFuse IC is not destroyed by a single overcurrent event. Normal operation can be restored by turning the MOSFET on again, allowing current to flow. Since the eFuse IC can be used repeatedly without requiring replacement, it helps reduce the cost and time required for repair and maintenance.

- **Robust protection through high-accuracy overcurrent detection**

Conventional fuses interrupt current by melting or thermal expansion, making it difficult to precisely determine the current level at which interruption occurs. Therefore, a rated current with a certain margin from the expected load current must be selected, which may result in insufficient protection. In contrast, an eFuse IC monitors current during operation, enabling highly accurate overcurrent protection. The TCKE1401NM also provides adjustable overcurrent protection, allowing the protection level to be set according to system requirements.

- **Improved reliability through fast protection response**

With a conventional fuse, there is a time delay between the occurrence of an overcurrent condition and current interruption because it takes time for the temperature generated by Joule heating to reach the melting point of the fuse material. During this period, the overcurrent continues to flow. In contrast, an eFuse IC can turn off its internal switch and interrupt the current almost immediately after detecting an overcurrent condition. This significantly reduces the duration of overcurrent flow, thereby reducing damage to equipment and improving long-term reliability.

- **Lower cost and smaller size through integration of multiple functions in a single package**

An eFuse IC integrates various functions into a single package. In addition to overcurrent and short-circuit protection, it can provide functions unavailable with a conventional fuse alone, such as overvoltage protection, inrush current limiting (slew rate control), and thermal protection. Compared with implementations using discrete components and multiple ICs, this integration reduces component count, assembly steps, and board area, contributing to lower system cost and smaller size.

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3. Pin configuration and internal block diagram of the TCKE1401NM

3.1. Pin assignment of the TCKE1401NM

Figure 3.1 shows the pin assignment of the TCKE1401NM. The pins serve various roles, such as power input/output, protection setting, operation control, and status notification. For details on the function of each pin, refer to the pin descriptions in Table 3.1 below.

(Note 4)

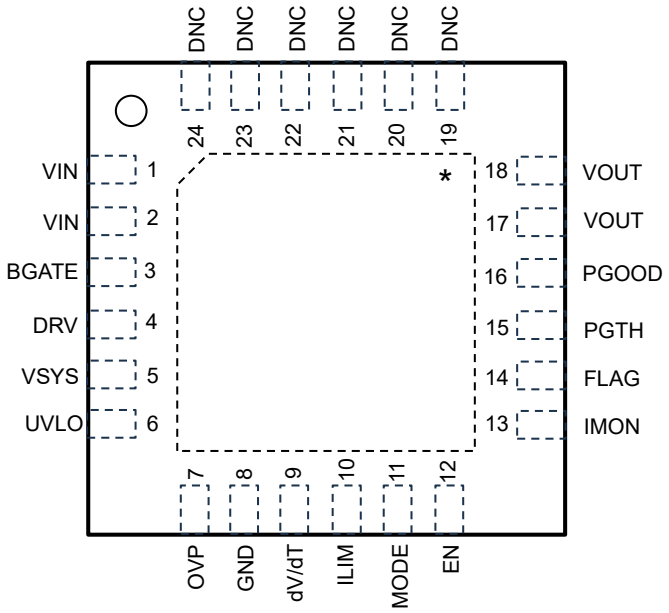


Figure 3.1 Pin assignments

Note 4: Center electrode must be connected to GND or Open

3.2. Pin description of the TCKE1401NM

Table 3.1 lists the pin functions of the TCKE1401NM.

Table 3.1 Pin description

Pin name	Type (Note 5)	Description
VIN	P	Power input. Input to the power switch.
VSYS	P	Supply input. Input to the supply voltage for the device. When using the external blocking Nch MOSFET, refer to Figure 5.14 and connect the VSYS pin to the source of the MOSFET. If the MOSFET is not used, short VSYS pin and VIN pin.
BGATE	O	Gate drive output pin for the external blocking Nch MOSFET (Q1). When using the MOSFET, refer to Figure 5.14 and connect this pin to the gate of the MOSFET. If the MOSFET is not used, leave this pin open.
DRV	O	Gate drive output pin for the external Fast pull-down Nch MOSFET (Q2). When using the MOSFET, refer to Figure 5.14 and connect this pin to the gate of the MOSFET. If the MOSFET is not used, leave this pin open.
UVLO	I	Undervoltage lockout (UVLO) input pin. This pin has an adjustable threshold by using external resistors. When this pin voltage falls below the threshold, the internal MOSFET turns off and the FLAG pin outputs at low level. This pin must not be left open. For operation using the internal UVLO threshold, connect this pin directly to GND
OVP	I	Overvoltage protection (OVP) input pin. This pin has an adjustable threshold by using external resistors. When this pin voltage exceeds the threshold, the internal MOSFET turns off and the FLAG pin outputs at low level. This pin must not be left open. For operation using the internal OVP threshold, connect this pin directly to GND.
dV/dT	I/O	Sets the output rise time. The output slew rate can be adjusted by connecting a capacitor between the dV/dT pin and GND.
ILIM	I/O	Sets the output current limit (I_{LIM}) for the overcurrent protection. I_{LIM} can be adjusted by connecting a resistor between the ILIM pin and GND.
MODE	I	Mode selection pin for auto-retry or latch-off fault response. Refer to Table 5.10.
EN	I	Enable input pin. If external control is not used, this pin can be left open. In this case, this pin is internally pulled up. To reset the device that has latched off due to a fault condition, cycle this pin (drive it low and then high).
IMON	O	Current monitor output pin. When using the current monitor, connect a resistor between IMON pin and GND. If the current monitor function is not used, this pin can be left open except V_{SYS} < 9 V condition
FLAG	O	FLAG open-drain output Pin. FLAG pin outputs at low level when a fault is detected. If this pin is not used, connect to GND or leave this pin open.
PGTH	I	PGOOD threshold input. PGTH pin must not be left open
PGOOD	O	PGOOD open-drain output pin. Active-high. When V_{PGTH} exceeds the V_{PGTHR} threshold, this pin outputs at high level, indicating that the output voltage is at a valid level. When V_{PGTH} falls below the V_{PGTHF} threshold, this pin outputs at low level, indicating that the output voltage has not reached a valid level. If this pin is not used, connect to GND or leave this pin open.
VOUT	P	Output pin. Output of the power switch.
DNC	-	Do Not Connect pin other than GND. Connect DNC to GND or leave this pin open.

Note 5: I = Input, O = Output, I/O = Input and Output, P = Power

3.3. Block diagram of the TCKE1401NM

Figure 3.2 shows the block diagram of the TCKE1401NM.

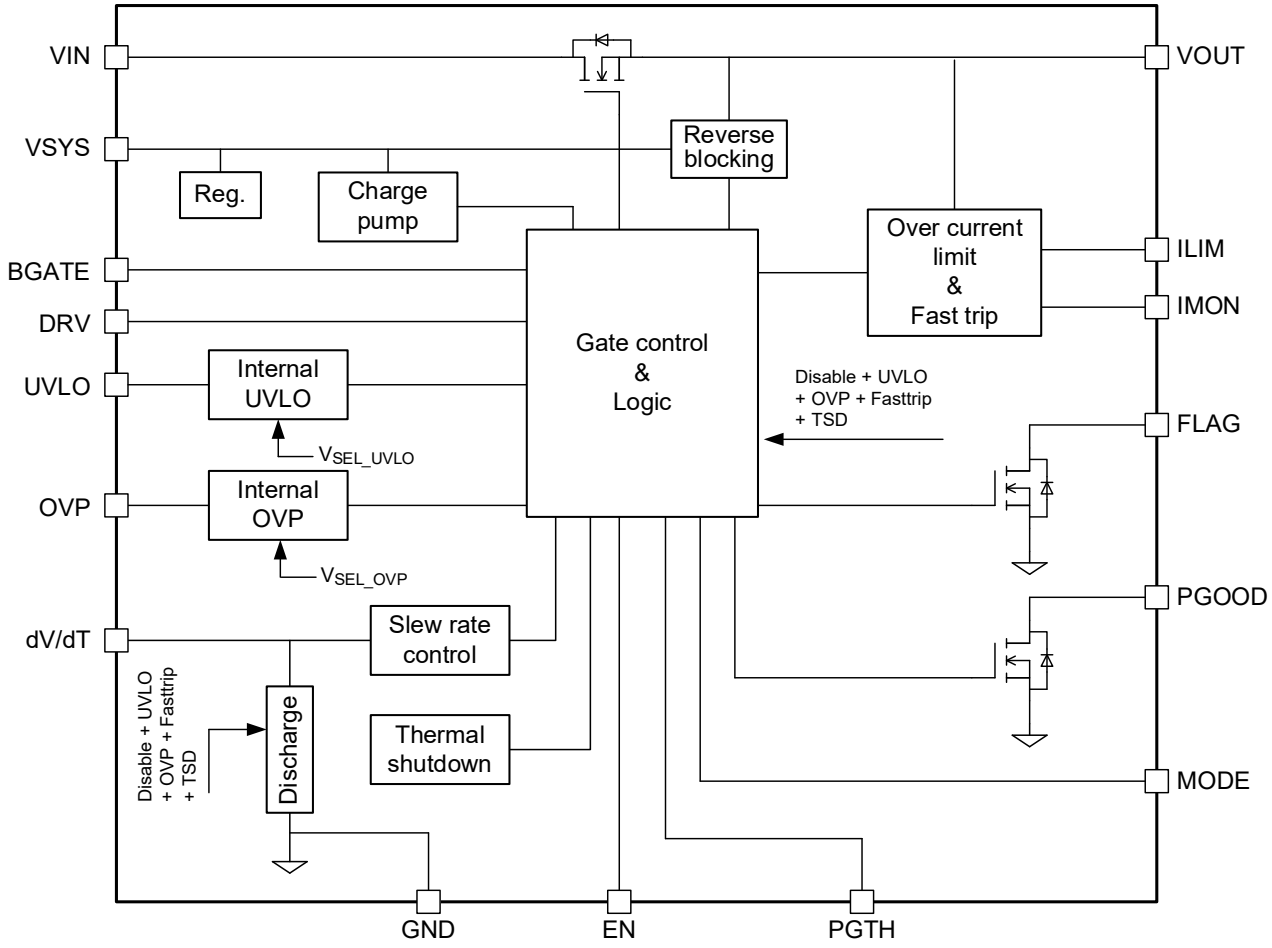


Figure 3.2 Block diagram

4. Built-in functions of the TCKE1401NM

The TCKE1401NM incorporates multiple functions, as listed in Table 4.1.

Table 4.1 Built-in Functions of the TCKE1401NM

Function	Supported / Not Supported	Adjustable setting
Overcurrent protection (OCP)	Supported	Yes
Short-circuit protection (SCP)	Supported	Yes (Note 6)
Overvoltage protection (OVP)	Supported	Yes
Undervoltage lockout (UVLO)	Supported	Yes
Thermal shutdown (TSD)	Supported	—
Slew rate control	Supported	Yes
Input reverse polarity protection / reverse current blocking	Supported (Note 7)	—
FLAG output	Supported	—
Power Good (PGOOD)	Supported	Yes (Note 8)
Output current monitoring	Supported	—
Output discharge	Not Supported	—

Note 6: Determined by the OCP setting. The SCP function has two thresholds. $I_{FASTTRIP}$, which is adjustable as I_{LIM} ×2.0 (Typ.), and I_{SCP}, which is internally fixed at 45 A (Typ.)
Note 7: An external MOSFET is required to use the input reverse polarity protection and reverse current blocking function.
Note 8: The PGOOD threshold can be set using voltage divider resistors connected between the V_{OUT} pin, the PGTH pin, and GND.

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5. Circuit description of the TCKE1401NM

5.1. Inrush current reduction

When the output turns on, an inrush current flows to charge the load capacitance. If this inrush current is too large, it may activate the OCP circuit and prevent the device from starting up, or it may cause an overshoot in the output voltage. This function limits the inrush current by controlling the slew rate of the output voltage during its rise, enabling stable startup.

Figure 5.1 shows the rise of the output voltage (V_{OUT}) and the inrush current when EN rises, and Figure 5.2 shows them when V_{IN} rises.

V_{IN} = 48 V, R_{ILIM} = 3 kΩ, R_{LOAD} = 48 Ω,
$C_{dV/dT}$ = 0.01 μF, T_a = 25°C

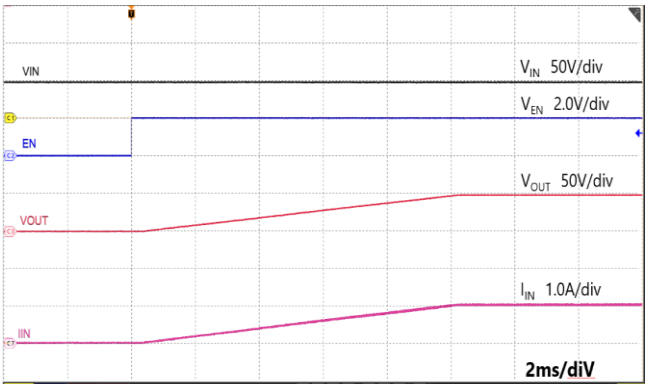


Figure 5.1 EN rising waveform

V_{IN} = 48 V, R_{ILIM} = 3 kΩ, R_{LOAD} = 48 Ω,
$C_{dV/dT}$ = 0.01 μF, T_a = 25°C

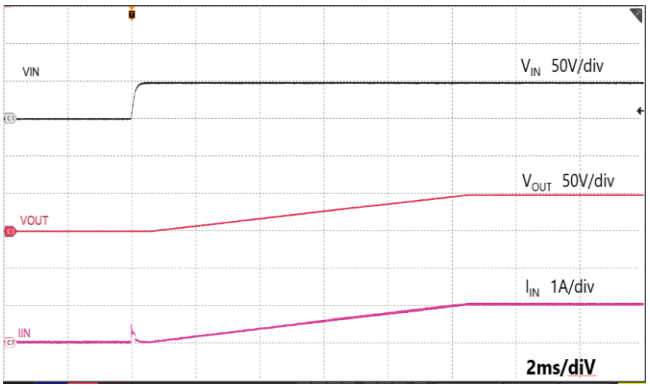


Figure 5.2 V_{IN} rising waveform

The slew rate is set by an external capacitor connected between the dV/dT pin and GND, allowing the rise time to be adjusted to the application. The inrush current can be calculated using formulas 1 and 2.

$$\text{Formula 1 :} \quad I\,(A) = C\,\frac{dV}{dT} \geq I_{INRUSH} = C_{OUT}\,\frac{V_{IN}}{t_{dV/dT}}$$

$$\text{Formula 2 :} \quad t_{dV/dT}\,(s) = 20.8 \times 10^{3} \times V_{IN} \times C_{dV/dT}$$

I_{INRUSH} : Inrush current (A)
C_{OUT} : Output capacitance (F)
V_{IN} : Input voltage (V)
$t_{dV/dT}$: V_{OUT} rise time (0% to 100%) (s)
$C_{dV/dT}$: External capacitance at the dV/dT pin (F)

Figure 5.3 shows the $t_{dV/dT}$ as a function of $C_{dV/dT}$.

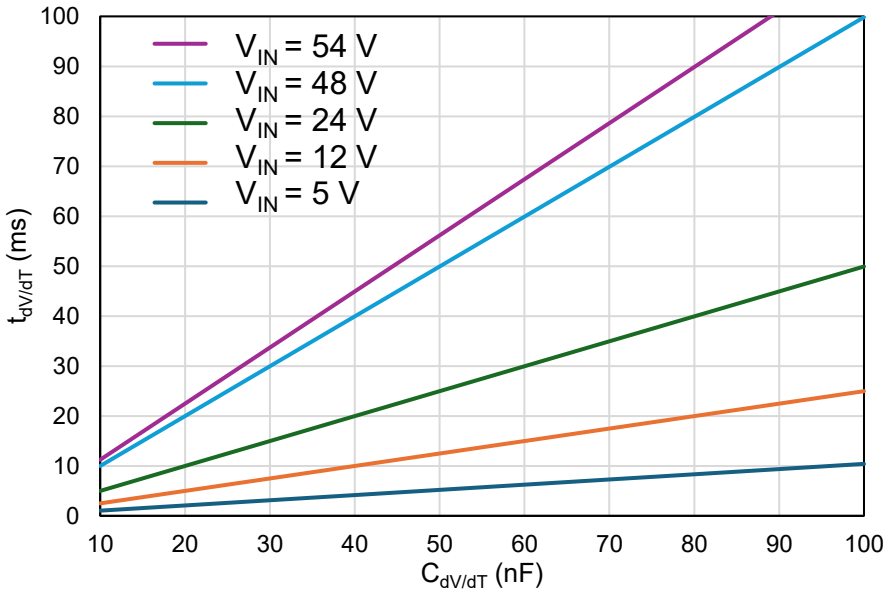


Figure 5.3 $t_{dV/dT}$ - $C_{dV/dT}$

5.2. Operation of the Power Good (PGOOD) and V_{OUT} sensing (PGTH)

The Power Good (PGOOD) function notifies an external circuit that the output voltage has reached the specified level. The PGOOD threshold can be set using voltage divider resistors connected between the VOUT pin, the PGTH pin, and GND.

Figure 5.4 shows the PGTH peripheral circuit of the TCKE1401NM.

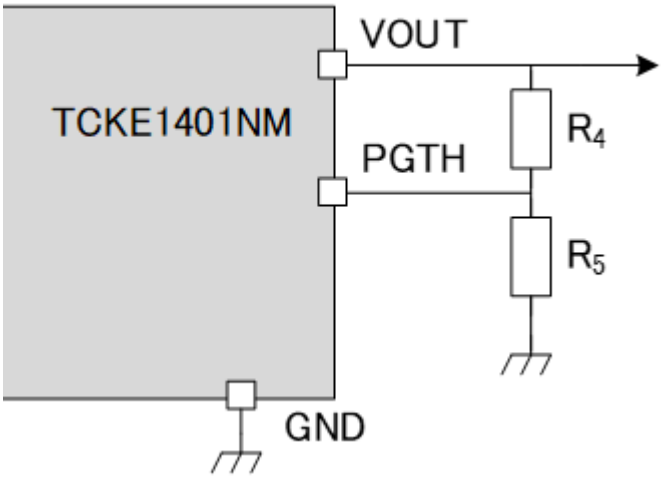


Figure 5.4 PGTH peripheral circuit

The PGTH pin is the input pin for Power Good detection. When the PGTH pin voltage exceeds the input threshold voltage, the PGOOD pin outputs high. When VOUT drops due to protection or other causes and the PGTH pin voltage falls below the input threshold voltage, the PGOOD pin outputs low (Table 5.1). Based on Figure 5.4, the PGTH pin voltage is expressed by formula 3.

Formula 3 :

$$V_{PGTH}\,(V) = V_{OUT} \times \frac{R5}{R4+R5}$$

Table 5.1 PGOOD output status and operation of each protection

Protective Function (Note 9)		IC Operation	PGOOD Output
Normal Operation		Normal Operation	High
Thermal Shutdown	$T_j > T_{SD}$	Shutdown	Low
Undervoltage Protection	$V_{UVLO} < V_{UVLOF}$ $V_{SYS} < V_{SYS_UVLO}$ (Note 10)	Shutdown	Low
Overvoltage Protection	$V_{OVP} > V_{OVPR}$ $V_{SYS} > V_{SYS_OVP}$ (Note 11)	Shutdown	Low
Over Current Protection (during t_{CL_PLIM})	$I_{LIM} < I_{OUT} < I_{FASTTRIP}$	I_{OUT} Current Limit	High / Low (Note 12)
Over Current Protection (after t_{CL_PLIM})	$I_{LIM} < I_{OUT} < I_{FASTTRIP}$	Shutdown	Low
Reverse Current Protection (Note 13)	$V_{OUT} - V_{SYS} \geqq 10$ mV	External MOSFET (Q1) OFF	High
Reverse connection (Note 13)	$V_{SYS} > -80$V, $V_{OUT} > -0.3$ V, $V_{SYS} - V_{OUT} \geqq -85$ V (Note 14)	Keeping OFF status	Low

Note 9: Unless otherwise specified, 4.7 V $\leqq V_{SYS} = V_{IN} \leqq$ 75 V.
Note 10: When the UVLO pin is connected to GND, it enters internal UVLO mode.
Note 11: When the OVP pin is connected to GND, it enters internal OVP mode.
Note 12: If the PGTH pin voltage is V_{PGTHF} or higher, PGOOD output is high; if less than V_{PGTHF}, PGOOD output is low.
Note 13: For details on the reverse current prevention function and reverse input connection prevention function, please refer to section 5.5.
Note 14: Voltage application is a condition for a 10 ms pulse.

Like the PGOOD function, the FLAG function notifies an external circuit of the IC status. However, the FLAG function uses a detection circuit independent of the PGOOD function. Therefore, the PGOOD output does not affect the FLAG output. For details on the FLAG function, refer to section 5.9.

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Figure 5.5 is a timing chart showing an example of the PGOOD function and PGTH input operation. When the output turns on and the PGTH pin voltage (V_{PGTH}) exceeds the PGOOD rising threshold (V_{PGTHR}), the PGOOD pin outputs high. On the other hand, when V_{PGTH} falls below the PGOOD falling threshold (V_{PGTHF}), the PGOOD pin outputs low. In addition, a deglitch time is applied to the PGOOD output (t_{PGOODR} when V_{PGTH} rises and t_{PGOODF} when V_{PGTH} falls).

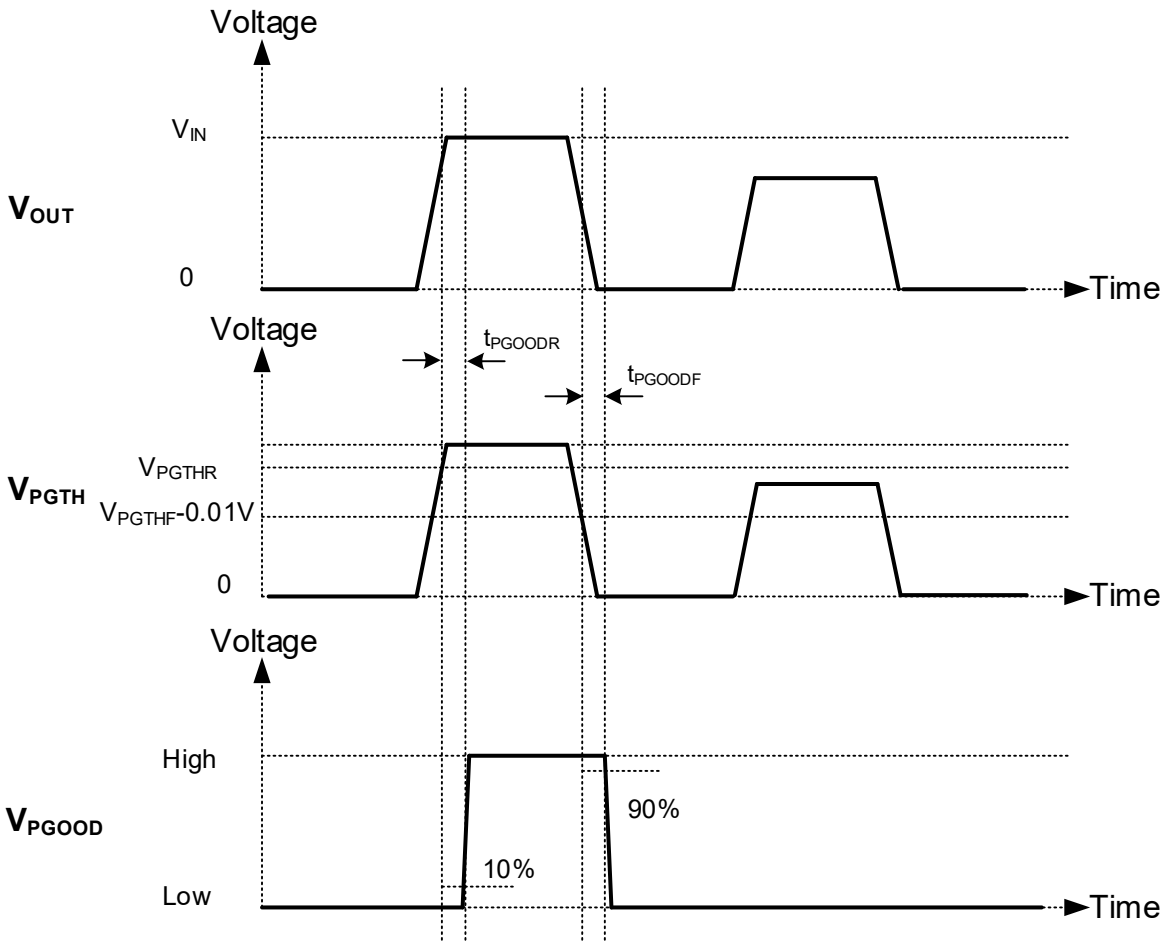


Figure 5.5 Example of PGOOD function and PGTH input operation

The PGOOD pin is open-drain output and therefore requires an external pull-up resistor. In addition, PGTH can be used to set the UVLO threshold of a downstream circuit, and PGOOD output can be used for enable/disable control of a downstream circuit. When the device recovers from a fault condition detected by OVP, UVLO, or other protection features, it starts up in either fast recovery mode or slew rate control mode (dV/dT mode), depending on the state of V_{PGTH}. For details, refer to Section 5.3 and 5.4.

If V_{PGTH} is below V_{PGTHF} when the device recovers from a fault condition, it starts up in dV/dT mode. In this mode, the slew rate is determined by the external capacitor connected to the dV/dT pin. Fast recovery mode can also be disabled by connecting the PGTH pin to GND. In this case, the PGOOD outputs low.

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5.3. Undervoltage lockout (UVLO)

The undervoltage lockout (UVLO) prevents downstream circuits from operating below their minimum operating voltage when the input voltage (V_{IN}) drops, helping prevent system malfunctions. When the UVLO pin voltage falls below V_{UVLOF}, the output turns off, and the FLAG pin outputs low after 0.33 µs (Typ.). The UVLO hysteresis is 70 mV (Typ.). To set the UVLO threshold, connect voltage divider resistors between the VIN pin, the UVLO pin and GND, as shown in the peripheral circuit diagram.

Figure 5.6 shows the UVLO peripheral circuit of the TCKE1401NM, and Figure 5.7 shows an example of UVLO detection.

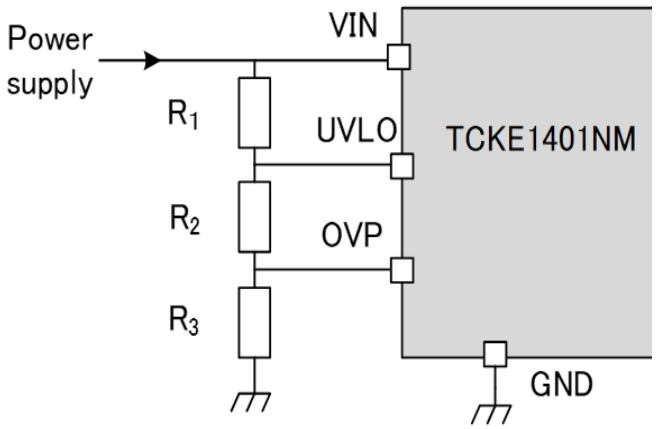


Figure 5.6 UVLO peripheral circuit

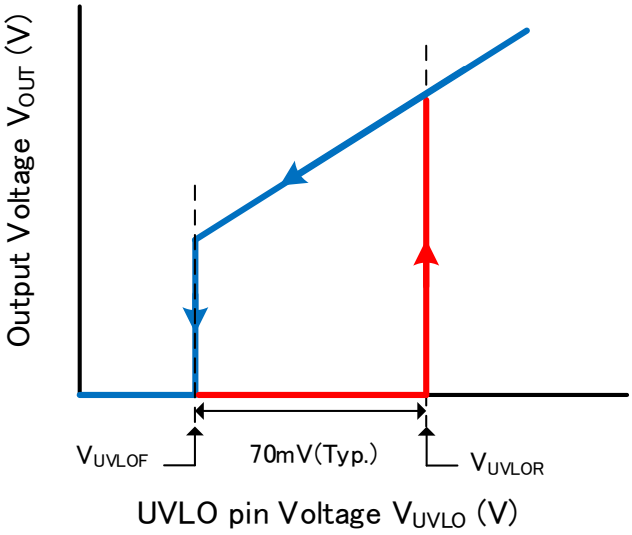


Figure 5.7 Example of UVLO detection

The TCKE1401NM also features an internal UVLO mode with a fixed threshold (V_{SYS_UVLO} (falling)) of 14.84 V (Typ.) and a hysteresis of 980 mV (Typ.). Figure 5.8 shows an example of internal UVLO mode detection.

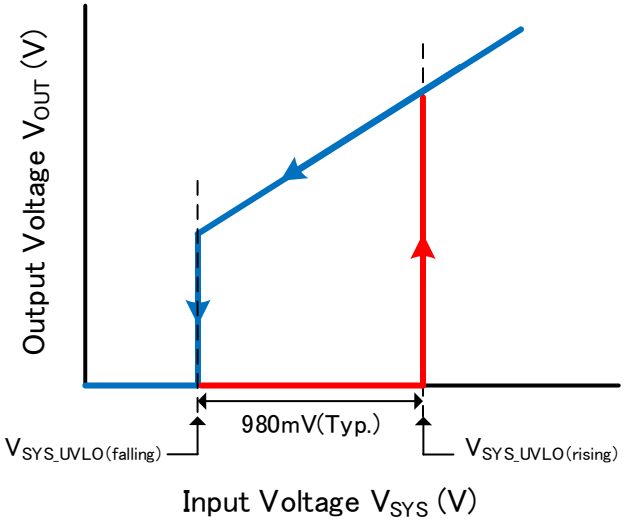


Figure 5.8 Example of internal UVLO detection

To use this mode, short the UVLO pin to GND. If UVLO is not used, the UVLO pin can be connected to the VSYS pin. In this case, design the circuit with careful attention to the absolute maximum rating of the UVLO pin (-0.3 V). Do not leave the UVLO pin open. When using input reverse polarity protection, connect a resistor of 300 kΩ or more between the UVLO pin and the VSYS pin.

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The UVLO threshold for the circuit in Figure 5.6 can be set using formulas 4 and 5 below.

$$\text{Formula 4 :} \quad V_{IN_UVLOF} = \frac{R_1 + R_2 + R_3}{R_2 + R_3} \times V_{UVLOF}$$

$$\text{Formula 5 :} \quad V_{IN_UVLOR} = \frac{R_1 + R_2 + R_3}{R_2 + R_3} \times V_{UVLOR}$$

V_{IN_UVLOF} : Input voltage at UVLO falling threshold
V_{UVLOF} : 1.12 V (Typ.)
V_{IN_UVLOR} : Input voltage at UVLO rising threshold
V_{UVLOR} : 1.19 V (Typ.)
R_1, R_2, R_3 : Divider resistors

Table 5.2 UVLO DC characteristics (as stated in the datasheet)

Characteristics	Symbol	Test condition	T_a = 25°C			T_a = -40 to 125°C		Unit
			Min	Typ.	Max	Min	Max	
Fixed V_{SYS} undervoltage lockout (UVLO) threshold	V_{SYS_UVLO}	V_{SYS} rising, V_{UVLO} = 0 V	—	15.82	—	14.61	23.62	V
		V_{SYS} falling, V_{UVLO} = 0 V	—	14.84	—	13.45	22.23	V
Undervoltage lockout threshold	V_{UVLOR}	Rising	—	1.19	—	1.142	1.224	V
	V_{UVLOF}	Falling	—	1.12	—	1.039	1.15	V
Internal UVLO select threshold	V_{SEL_UVLO}		—	213	—	153.2	272.8	mV

Table 5.3 UVLO AC characteristics (as stated in the datasheet)

Characteristics	Symbol	Test condition	T_a = -40 to 125°C			Unit
			Min	Typ.	Max	
UVLO switch turn on delay	UVLO_t_{on}	UVLO = H (100 mV above V_{UVLOR}) to V_{OUT} = 100 mV with V_{PGTH} < V_{PGTHF}, $C_{dV/dT}$ ≥ 10 nF, [$C_{dV/dT}$ in nF]	—	220 + 14.5 × $C_{dV/dT}$	—	µs
UVLO switch turn on delay (fast)	UVLO_t_{on_fast}	UVLO = H (100 mV above V_{UVLOR}) to MOSFET ON with V_{PGTH} > V_{PGTHF}	—	195	410	µs
UVLO switch turnoff delay	UVLO_t_{off}	UVLO = L (20 mV below V_{UVLOF}) to FLAG = L	—	0.33	3	µs
UVLO to fault de-assertion delay	UVLO_t_{FLAG}	UVLO = H to FLAG = H delay	382	580	772	µs

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Figure 5.9 is a timing chart showing an example of UVLO operation. When the device recovers from UVLO, it starts up in either fast recovery mode or dV/dT mode, depending on the state of V_{PGTH}. This makes it possible to distinguish between a fault condition and a transient event and to control the startup timing appropriately.

If V_{PGTH} is above V_{PGTHF} when the device recovers from a fault condition, it starts up in fast recovery mode after UVLO_t_{ON_fast}, regardless of the $C_{dV/dT}$ value. Fast recovery mode is enabled approximately 500 µs (Typ.) after the output slew rate control is completed. If V_{PGTH} is below V_{PGTHF}, the device starts up in dV/dT mode. In this mode, the slew rate is set by the external capacitor connected to the dV/dT pin. In addition, fast recovery mode can be disabled by connecting the PGTH pin to GND.

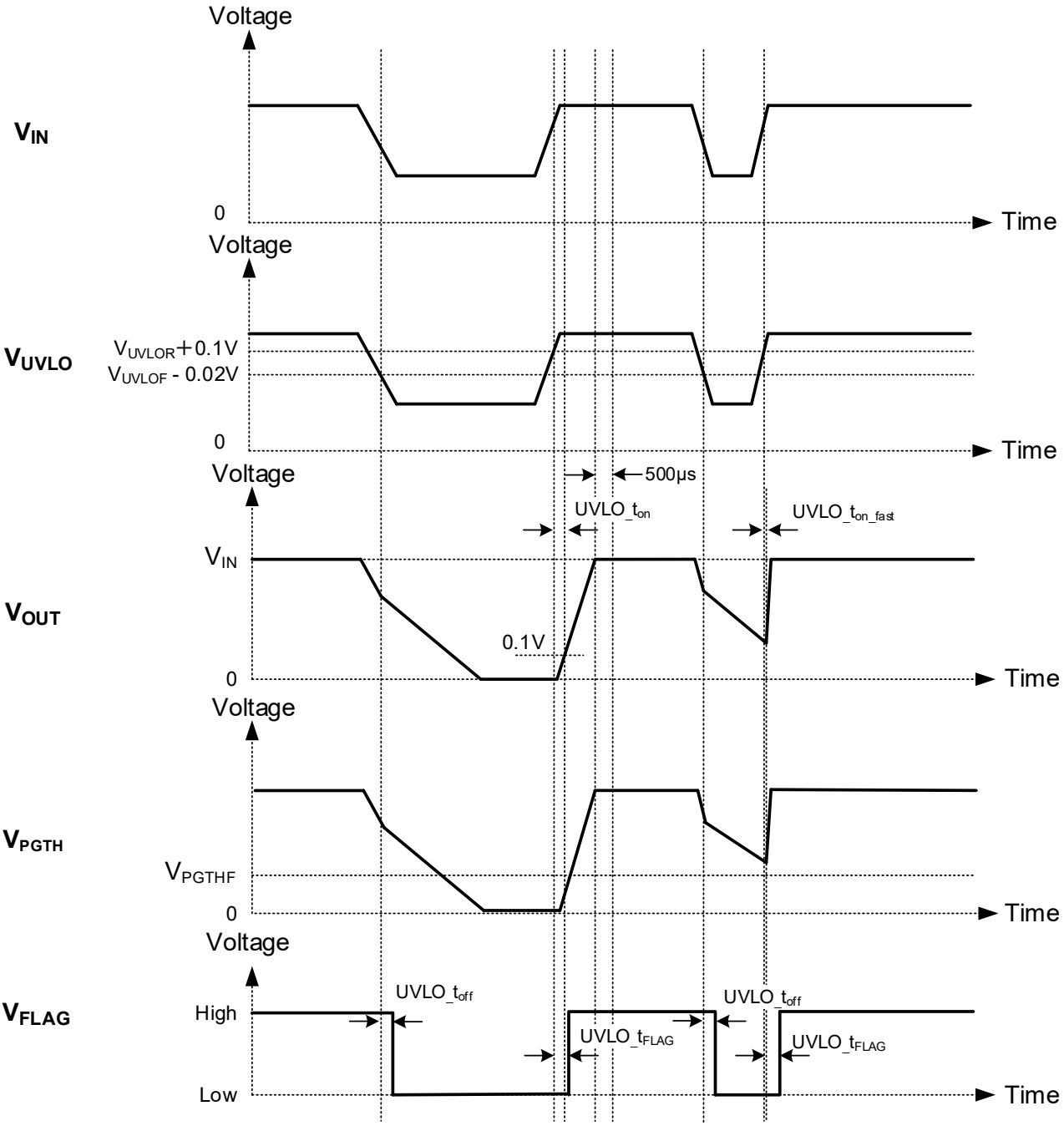


Figure 5.9 Example of UVLO operation

For an example of resistor value setting when using this function with OVP (section 5.4), refer to the application circuit example in section 6.3.

5.4. Overvoltage protection (OVP)

Overvoltage protection (OVP) turns off the output when the input voltage (V_{IN}) exceeds the set threshold, preventing an overvoltage from being applied to the load. When a voltage exceeding VOVPR is applied to the OVP pin, the output turns off to protect the load. To set the OVP threshold, connect voltage divider resistors between the VIN pin, the OVP pin, and GND, as shown in the peripheral circuit diagram.

Figure 5.10 shows the OVP peripheral circuit of the TCKE1401NM, and Figure 5.11 shows an example of OVP detection.

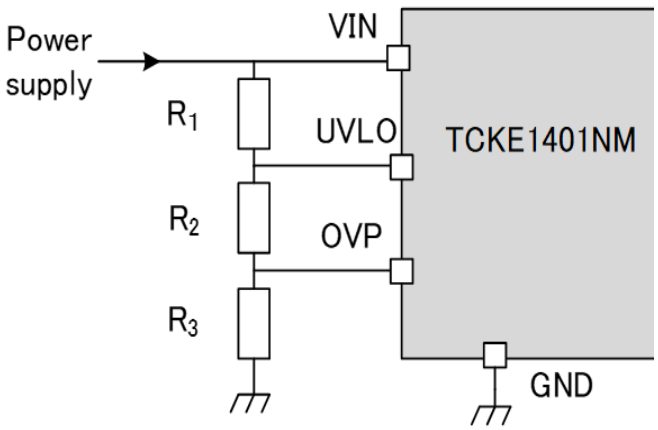


Figure 5.10 OVP peripheral circuit

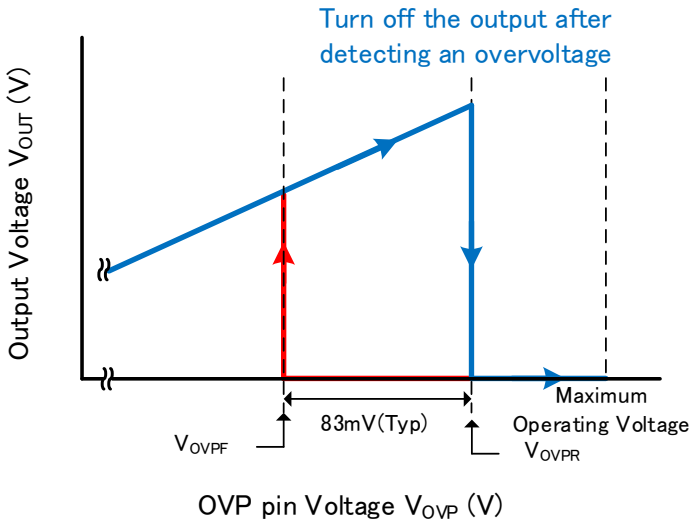


Figure 5.11 Example of OVP detection

The TCKE1401NM also features an internal OVP mode with a fixed threshold ($VSYS_{_OVP(rising)}$) of 35.72 V (Typ.) and a hysteresis of 380 mV (Typ.). Figure 5.12 shows an example of internal OVP mode detection.

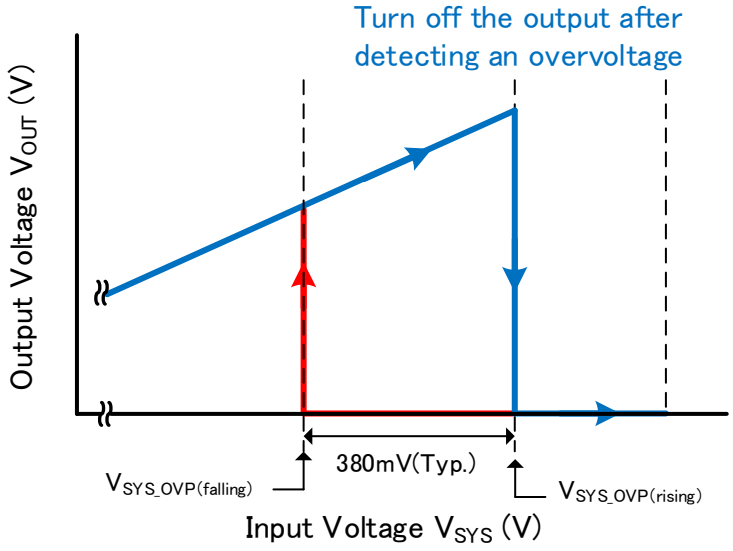


Figure 5.12 Example of internal OVP mode detection

To use this mode, connect the OVP pin to GND. Do not leave the OVP pin open.

The OVP threshold for the circuit in Figure 5.10 can be set using formulas 6 and 7 below.

$$\text{Formula 6 :} \quad V_{IN_OVPF} = \frac{R_1 + R_2 + R_3}{R_3} \times V_{OVPF}$$

$$\text{Formula 7 :} \quad V_{IN_OVPR} = \frac{R_1 + R_2 + R_3}{R_3} \times V_{OVPR}$$

V_{IN_OVPF} : Input voltage at OVP falling threshold
V_{OVPF} : 1.15 V (Typ.)
V_{IN_OVPR} : Input voltage at OVP rising threshold
V_{OVPR} : 1.233 V (Typ.)
R_1, R_2, R_3 : Divider resistors

Table 5.4 OVP DC characteristics (as stated in the datasheet)

Characteristics	Symbol	Test condition	T_a = 25°C			T_a = -40 to 125°C		Unit
			Min	Typ.	Max	Min	Max	
Fixed V_{SYS} overvoltage protection (OVP) threshold	V_{SYS_OVP}	V_{SYS} rising, V_{OVP} = 0 V	—	35.72	—	33.11	45.93	V
		V_{SYS} falling, V_{OVP} = 0 V	—	35.34	—	32.74	45.46	V
Overvoltage protection threshold	V_{OVPR}	Rising	—	1.233	—	1.18	1.298	V
	V_{OVPF}	Falling	—	1.15	—	1.09	1.187	V
Internal OVP select threshold	V_{SEL_OVP}		—	216	—	167	265	mV

Table 5.5 OVP AC characteristics (as stated in the datasheet)

Characteristics	Symbol	Test condition	T_a = -40 to 125°C			Unit
			Min	Typ.	Max	
OVP switch turn off delay	OVP_t_{off}	OVP = H (20 mV above V_{OVPR}) to FLAG = L	—	0.74	3	µs
OVP switch turn on delay (fast)	$OVP_t_{on_fast}$	OVP = L (100 mV below V_{OVPF}) to MOSFET ON with $V_{PGTH} > V_{PGTHF}$	—	165	374	µs
OVP switch disable delay	OVP_t_{on}	OVP = L (100 mV below V_{OVPF}) to MOSFET ON with $V_{PGTH} < V_{PGTHF}$, $C_{dV/dT} \geq 10$ nF, [$C_{dV/dT}$ in nF]	—	190 + 14.5 × $C_{dV/dT}$	—	µs

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Figure 5.13 shows a timing chart illustrating an example of OVP operation. When recovering from OVP, the device starts up in either fast recovery mode or dV/dT mode depending on the V_{PGTH} level. This allows the device to distinguish between a fault condition and a transient event and appropriately control the startup timing. When OVP is activated, the FLAG pin goes low after OVP_t_{off} (0.74 µs (Typ.)) and remains low until OVP is released.

If the V_{PGTH} level exceeds V_{PGTHF} when recovering from a fault condition, the device starts up in fast recovery mode after OVP_t_{ON_fast}, regardless of the CdV/dT value. Fast recovery mode becomes available approximately 500 µs (Typ.) after the output slew-rate control is completed. If the V_{PGTH} level falls below V_{PGTHF}, the device starts up in dV/dT mode. In this case, the slew rate is determined by the external capacitor connected to the dV/dT pin. Fast recovery mode can be disabled by connecting the PGTH pin to GND.

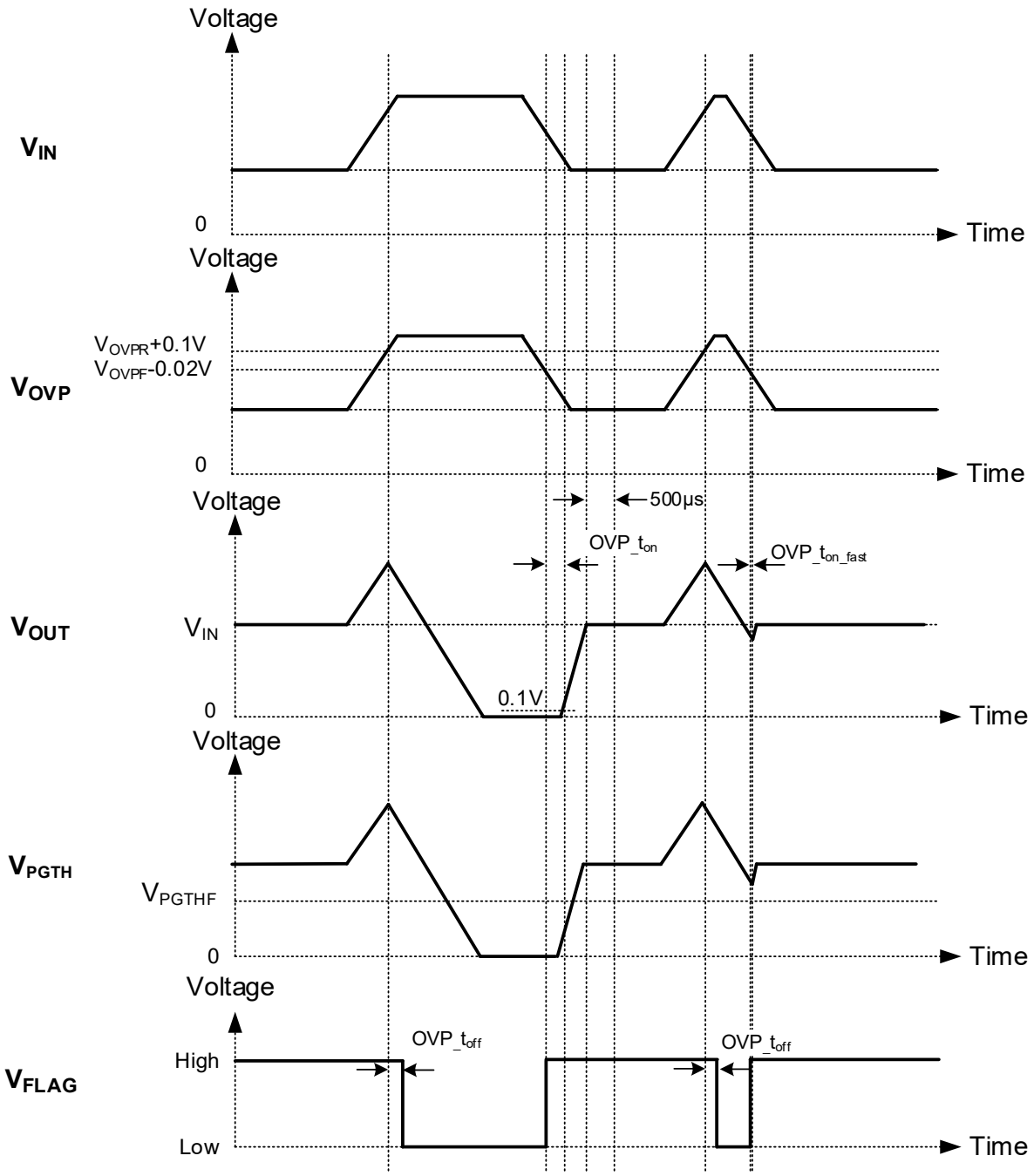


Figure 5.13 Example of OVP operation

For an example of resistor value settings when used in combination with the UVLO function described in Section 5.3, refer to the application circuit example in Section 6.3.

5.5. Input reverse polarity protection and reverse current blocking

The input reverse polarity protection function protects the eFuse IC and the load circuit when the input power supply is connected in reverse.
The reverse current blocking function protects the eFuse IC and the input power supply from reverse current that may occur when the output voltage becomes higher than the input voltage.
These functions are implemented using an external blocking N-channel MOSFET (Q1) and a fast pull-down N-channel MOSFET (Q2), as shown in Figure 5.14.
The BGATE pin outputs an internally boosted voltage of VIN + 10 V (Typ.). Therefore, when the input reverse polarity protection and reverse current blocking functions are not used, short the VSYS pin to the VIN pin, and leave the BGATE and DRV pins open, as shown in Figure 5.15.

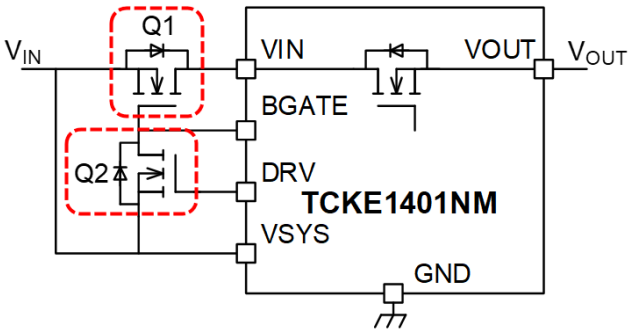


Figure 5.14 Circuit with reverse polarity protection and reverse current blocking

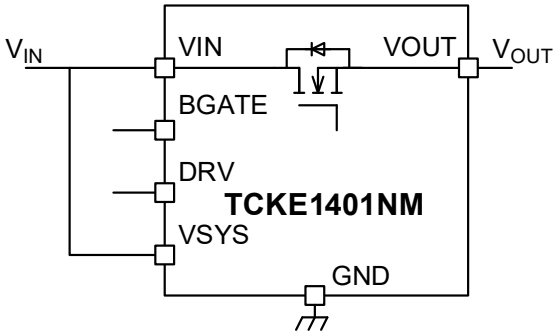


Figure 5.15 Circuit without reverse polarity protection and reverse current blocking

Q1 is connected back-to-back with the eFuse IC and functions as a switch for input reverse polarity protection and reverse current blocking. Q2 functions as a pull-down switch that rapidly discharges the gate charge of Q1, allowing Q1 to turn off quickly during protection operation.
During normal operation, Q1 is turned on by the gate drive voltage supplied from the BGATE pin.
For Q2, use an N-channel MOSFET with $V_{DSS} \geq 15$ V, a V_{GSS} rating of ±20 V, $C_{iss} < 50$ pF, and $V_{th} \leq 3$ V.
Select Q1 and Q2 by referring to the electrical characteristics of the BGATE and DRV pins.
In this application note, Toshiba TPN1200APL and T2N7002AK are used as recommended examples of external MOSFETs for Q1 and Q2, respectively. The key characteristics of TPN1200APL and T2N7002AK are shown in Table 5.6. For details, refer to the datasheet of each product.

Table 5.6 Key characteristics of TPN1200APL and T2N7002AK

Characteristics	Symbol	TPN1200APL	T2N7002AK
Drain-source voltage	V_{DSS}	100 V	60 V
Gate-source voltage	V_{GSS}	±20 V	±20 V
Drain current	I_D	40 A	200 mA
Drain-source on-resistance	$R_{DS(ON)}$	13.3 mΩ (Typ.) @V_{GS}= 4.5 V	3.2 Ω (Typ.) @V_{GS}= 4.5 V
Input capacitance	C_{iss}	1425 pF	11 pF

When using other MOSFETs, select devices with sufficient margin in the V_{DSS} and I_D ratings for the power supply voltage and load current, and with as low an on-resistance as possible.

- Parametric Search for Blocking Nch MOSFET (Q1)→ Click Here
- Parametric Search for Fast pull-down Nch MOSFET (Q2)→ Click Here

5.5.1. Input reverse polarity protection

When a reverse-polarity voltage is applied to the input pin, Q1 blocks the current path to the load to protect the eFuse IC and the load circuit.

Figure 5.16 shows the waveforms of the input reverse polarity protection operation.

V_{IN} = 0 V → -80 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, R_{LOAD} = OPEN, T_a = 25°C

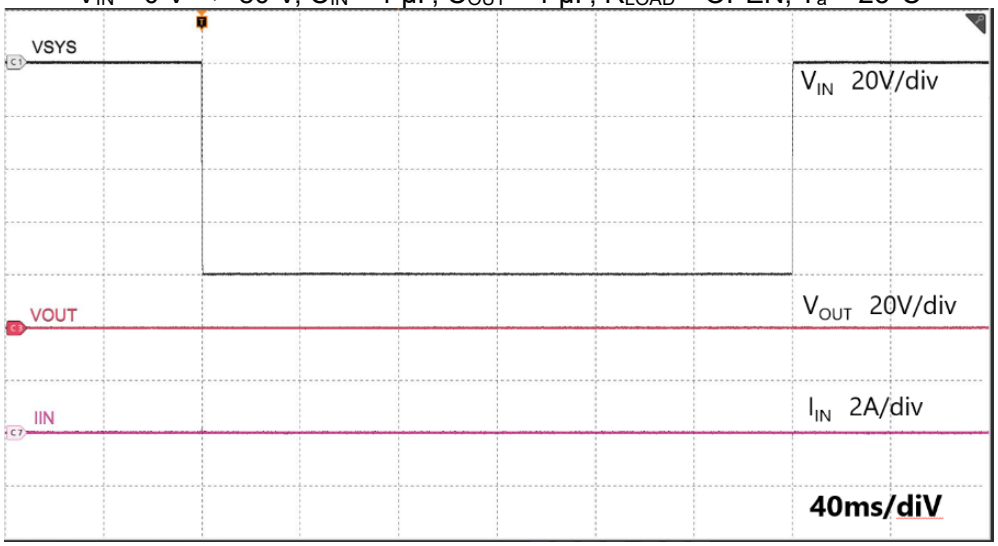


Figure 5.16 Input reverse polarity protection waveforms

5.5.2. Reverse current blocking

When V_{SYS} − V_{OUT} falls below the reverse current blocking voltage threshold (V_{RB}), a reverse current condition is detected. The DRV pin goes high to turn off Q1 and block reverse current to the input side.

In this case, the total time required to turn off Q1 is expressed as the reverse current blocking response time (t_{RCB_fast}) + t_{Driver}. t_{Driver} is calculated using formula 8 below.

Formula 8 :

$$t_{Driver} = -R_{DS(ON)(Q2)} \times C_{iss(Q1)} \times \ln \frac{V_{GTH(Q1)}}{V_{BGATE}}$$

$R_{DS(ON)(Q2)}$	:	On-resistance of Fast pull-down Nch MOSFET (Q2)
$C_{iss(Q1)}$	:	Q1 input capacitance
$V_{GTH(Q1)}$	:	Q1 gate threshold voltage
V_{BGATE}	:	10 V (Typ.)

Q1 turns on when V_{SYS} − V_{OUT} exceeds V_{RBR}. The reverse current blocking response time (t_{RCB}) becomes shorter as the difference between V_{SYS} and V_{OUT} increases.

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5.6. Overcurrent protection

The overcurrent protection (OCP) function reduces power consumption when an overcurrent condition occurs. This helps prevent degradation or damage to the IC and the load. When an overcurrent condition in which the output current exceeds the programmed current limit (I_{LIM}) is detected, the output current is limited to I_{LIM}. The response time from the detection of an overcurrent condition until the output current is limited to I_{LIM} is defined as t_{LIM}. The output voltage also decreases depending on the load condition.

In combination with the short-circuit protection function described later, the OCP function improves protection against overcurrent and short-circuit conditions and contributes to improved system safety. Figure 5.17 shows the relationship between the output voltage and output current of the TCKE1401NM during current limiting operation.

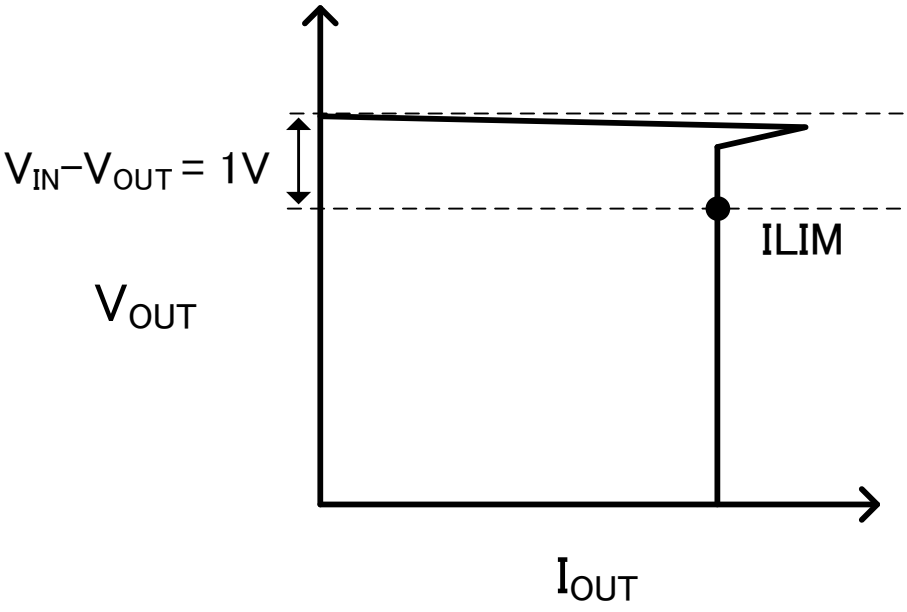


Figure 5.17 Output voltage vs Output current characteristic

During current limiting operation, the power dissipation is calculated as $(V_{IN} - V_{OUT}) \times I_{LIM}$, causing the temperature of the eFuse IC to rise. If the overcurrent condition continues and the IC temperature reaches the thermal shutdown threshold, the thermal shutdown (TSD) function is activated, and the output is turned off.

The current limiting state at I_{LIM} can be maintained for t_{CL_PLIM}, which is 160 ms (Typ.). If TSD is activated before t_{CL_PLIM} elapses, the output is turned off and the IC enters the shutdown state. Figure 5.18 shows the t_{LIM} waveform, and Figure 5.19 shows the t_{CL_PLIM} waveform.

V_{IN} = 48 V, R_{ILIM} = 30 kΩ, R_{LOAD} = 48 Ω, T_a = 25°C

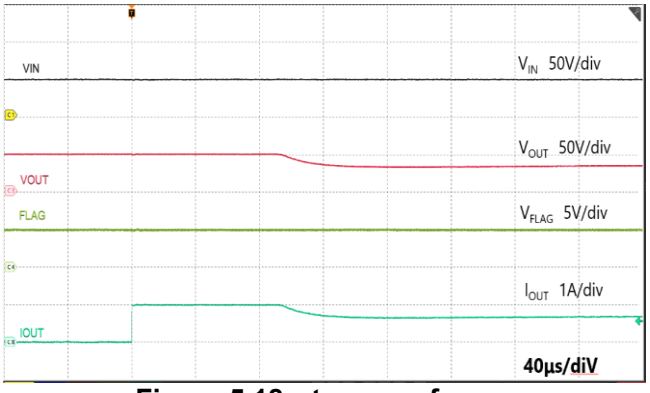


Figure 5.18 t_{LIM} waveform

V_{IN} = 48 V, R_{ILIM} = 30 kΩ, R_{LOAD} = 48 Ω, T_a = 25°C

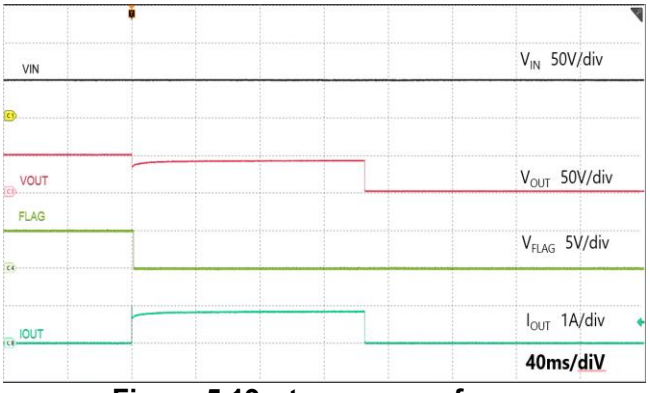


Figure 5.19 t_{CL_PLIM} waveform

5.6.1. Overcurrent protection in Auto-retry mode

Figure 5.20 shows a timing chart of an overcurrent protection operation example in Auto-retry mode. When the output is turned off after t_{CL_PLIM} elapses or by the TSD function described above, the auto-retry operation starts with a period of t_{TSD_retry} = 330 ms (Typ.). If the overcurrent condition has not been cleared after t_{TSD_retry}, the current limiting operation is performed again.

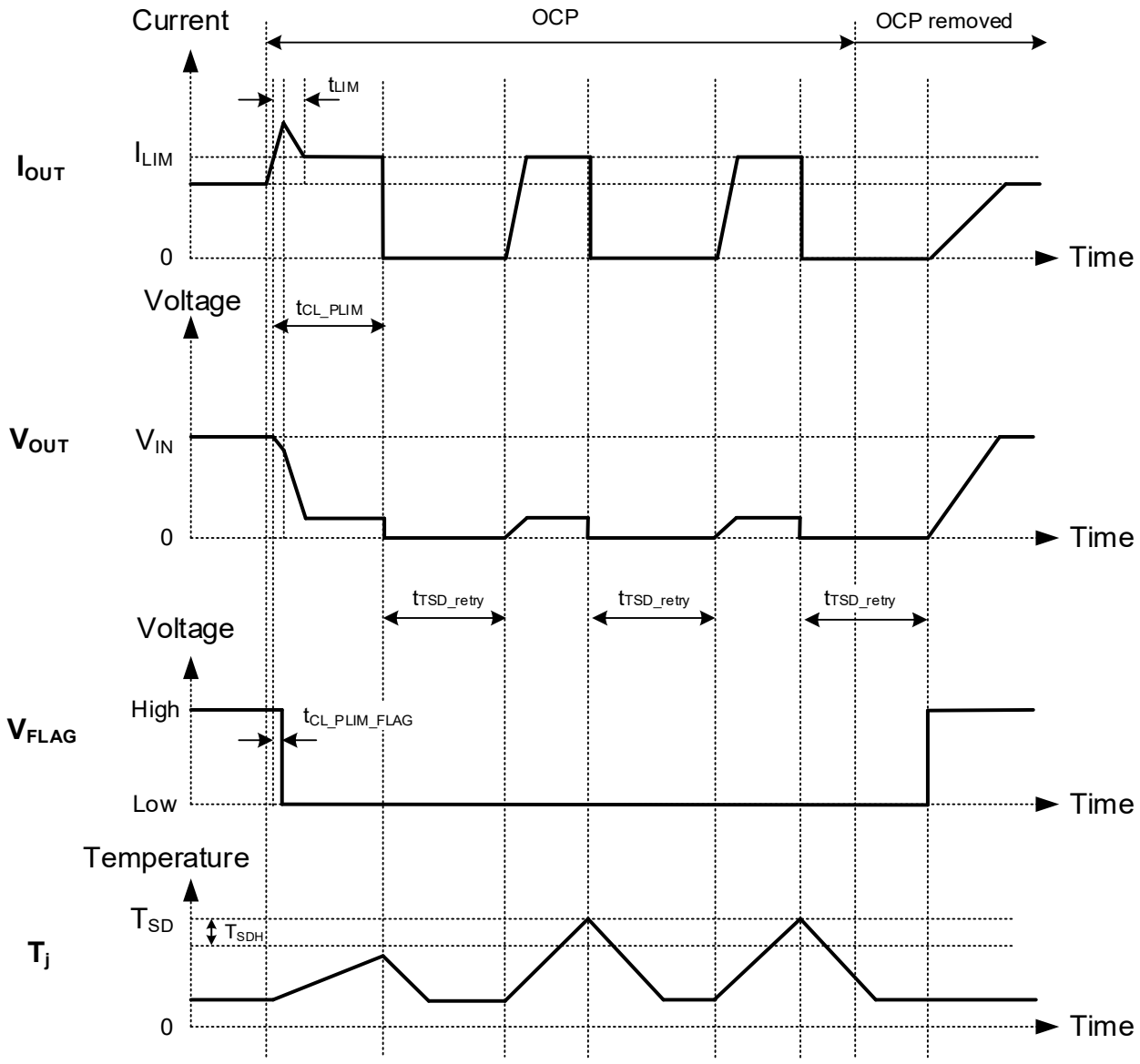


Figure 5.20 Example of OCP operation (Auto-retry mode)

5.6.2. Overcurrent protection in Latch-off mode

Figure 5.21 shows a timing chart of an overcurrent protection operation example in Latch-off mode. When the output is turned off due to an overcurrent condition, the protection state is latched and the device does not restart automatically. The device must be restarted by applying the control signal to the EN pin again or by setting the VSYS pin input voltage to 0 V once and then reapplying it. The protection state is maintained until the device is restarted.

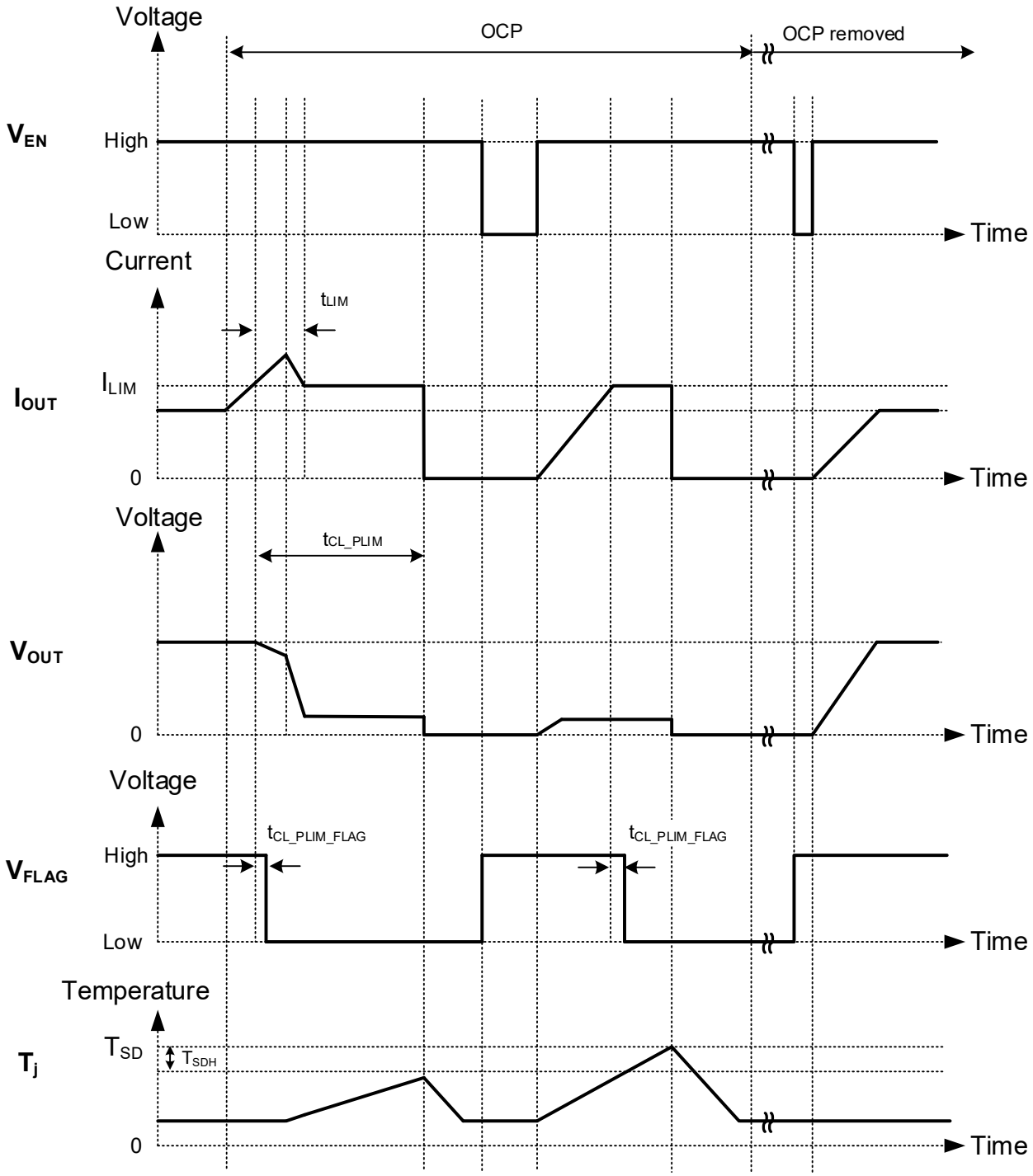


Figure 5.21 Example of OCP operation (Latch-off mode)

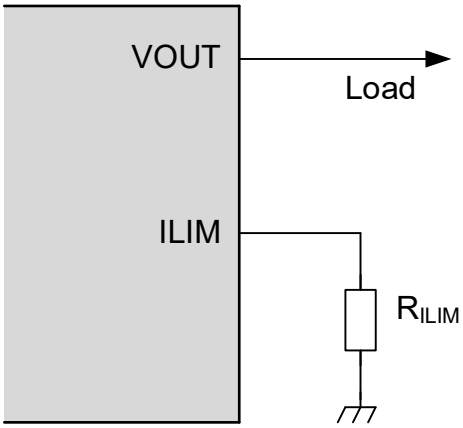
5.6.3. Setting the OCP protection circuit

The output current limit, I_{LIM}, of the TCKE1401NM is adjustable and can be set to an appropriate value for the application by selecting an appropriate external resistor (output current limit setting resistor R_{ILIM}) for the ILIM pin. I_{LIM} can be calculated using formula 9. The resistor value should be verified with the actual circuit. R_{ILIM} should be 3 kΩ or higher.

$$\text{Formula 9 :} \quad I_{LIM} = \frac{18.9}{R_{ILIM}} + 0.13$$

I_{LIM} : Overcurrent limit (A)
R_{ILIM} : Overcurrent limit setting resistor (kΩ)

Figure 5.22 shows the peripheral circuit of the ILIM pin. Figure 5.23 shows the relationship between the R_{ILIM} setting and the output current limit I_{LIM}.



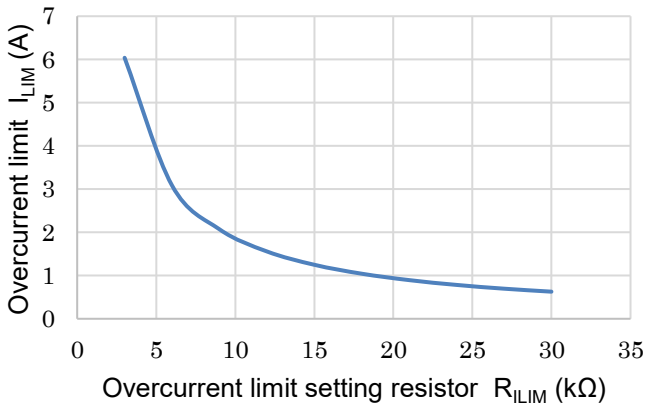


Figure 5.22 External circuit for the ILIM pin **Figure 5.23 Example of I_{LIM}–R_{ILIM} characteristics**

Table 5.7 Overcurrent protection (OCP) characteristics (as stated in the datasheet)

Characteristics	Symbol	Test condition		T_a = 25°C			T_a = -40 to 125°C		Unit
				Min	Typ.	Max	Min	Max	
Overcurrent limit (Note 15)	I_{LIM}	$V_{IN} - V_{OUT}$ = 1 V	R_{ILIM} = 30 kΩ	—	0.82	—	0.54	1.10	A
			R_{ILIM} = 9 kΩ	—	2.21	—	1.84	2.59	A
			R_{ILIM} = 4.02 kΩ	—	4.83	—	4.18	5.47	A
			R_{ILIM} = 3 kΩ	—	6.43	—	5.58	7.28	A

Note 15: This IMON pin can be left open when the IMON function is not used, except VSYS < 9 V (1 kΩ ≤ R_{IMON} ≤ 10 kΩ).

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5.7. Short circuit protection

The short-circuit protection function turns off the output when the power supply line or load is short-circuited due to an abnormal condition, preventing excessive current from flowing. The TCKE1401NM has a short-circuit protection circuit (Fast-Trip circuit). When the output current exceeds the short-circuit protection threshold current $I_{FASTTRIP}$ (I_{LIM} × 2.0 (Typ.)), a short-circuit condition is detected.

The short-circuit protection function operates when $I_{FASTTRIP} < I_{OUT} < I_{SCP}$ (45 A (Typ.)) and turns off the output within $t_{FASTTRIP}$ = 3 µs (Typ.). When the output current exceeds I_{SCP}, the SCP circuit detects the short-circuit condition within t_{SCP} = 1 µs (Typ.) and immediately turns off the output.

This function reduces the large current and IC power dissipation caused by a short circuit.

5.7.1. V_{OUT} short-circuit protection in Auto-retry mode

Figure 5.24 shows an example of the short-circuit protection operation in Auto-retry mode. When the VOUT pin is short-circuited and the short-circuit protection function is activated, the device restarts with soft-start operation. However, if the short-circuit condition remains, the overcurrent protection (OCP) function continues to limit the output current, causing the IC temperature to rise. When the thermal shutdown (TSD) function is activated due to the temperature rise, the device shuts down.

After a certain period, the device restarts. If the VOUT pin remains short-circuited, the output current is limited again. Therefore, the following cycle is repeated:

Current limiting → Temperature rise → Thermal shutdown protection → Shutdown → Temperature decrease → Restart → Current limiting

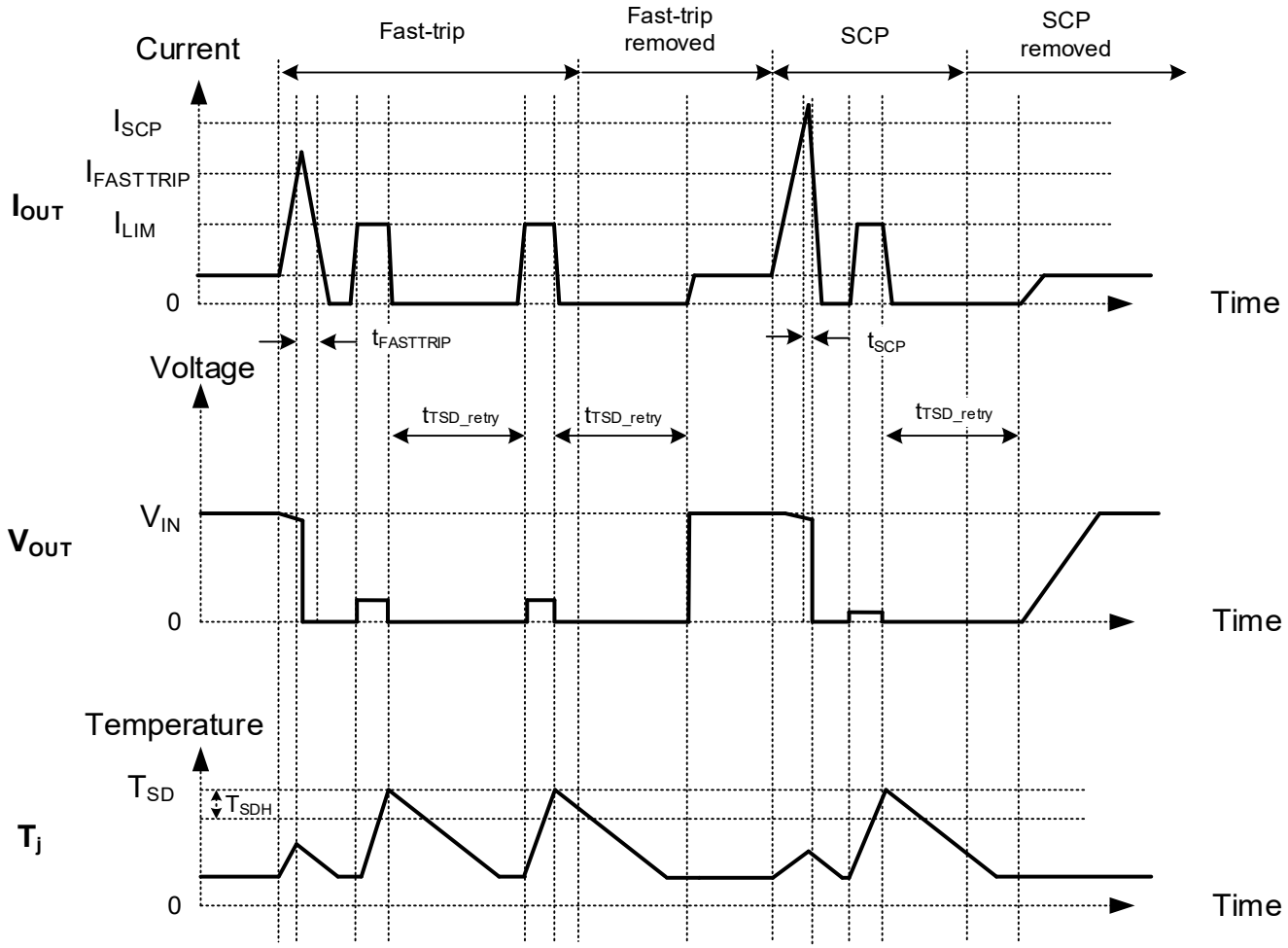


Figure 5.24 Example of short-circuit protection operation (Auto-retry mode)

5.7.2. V_{OUT} short-circuit protection in Latch-off mode

Figure 5.25 shows a timing chart of a short-circuit protection operation example in Latch-off mode. When the VOUT pin is short-circuited and the output current reaches the short-circuit protection threshold current $I_{FASTTRIP}$, the device detects a short-circuit condition and turns off the output. The device then restarts with soft-start operation. However, if the short-circuit condition remains, the overcurrent protection (OCP) function continues to limit the output current, causing the IC temperature to rise. When the thermal shutdown (TSD) function is activated due to the temperature rise, the device shuts down.
Unlike in Auto-retry mode, the protection state is latched and the device does not restart automatically. The device must be restarted by applying the control signal to the EN pin again or by setting the V_{IN} input voltage to 0 V once and then applying it again. The protection state is maintained until the device is restarted.

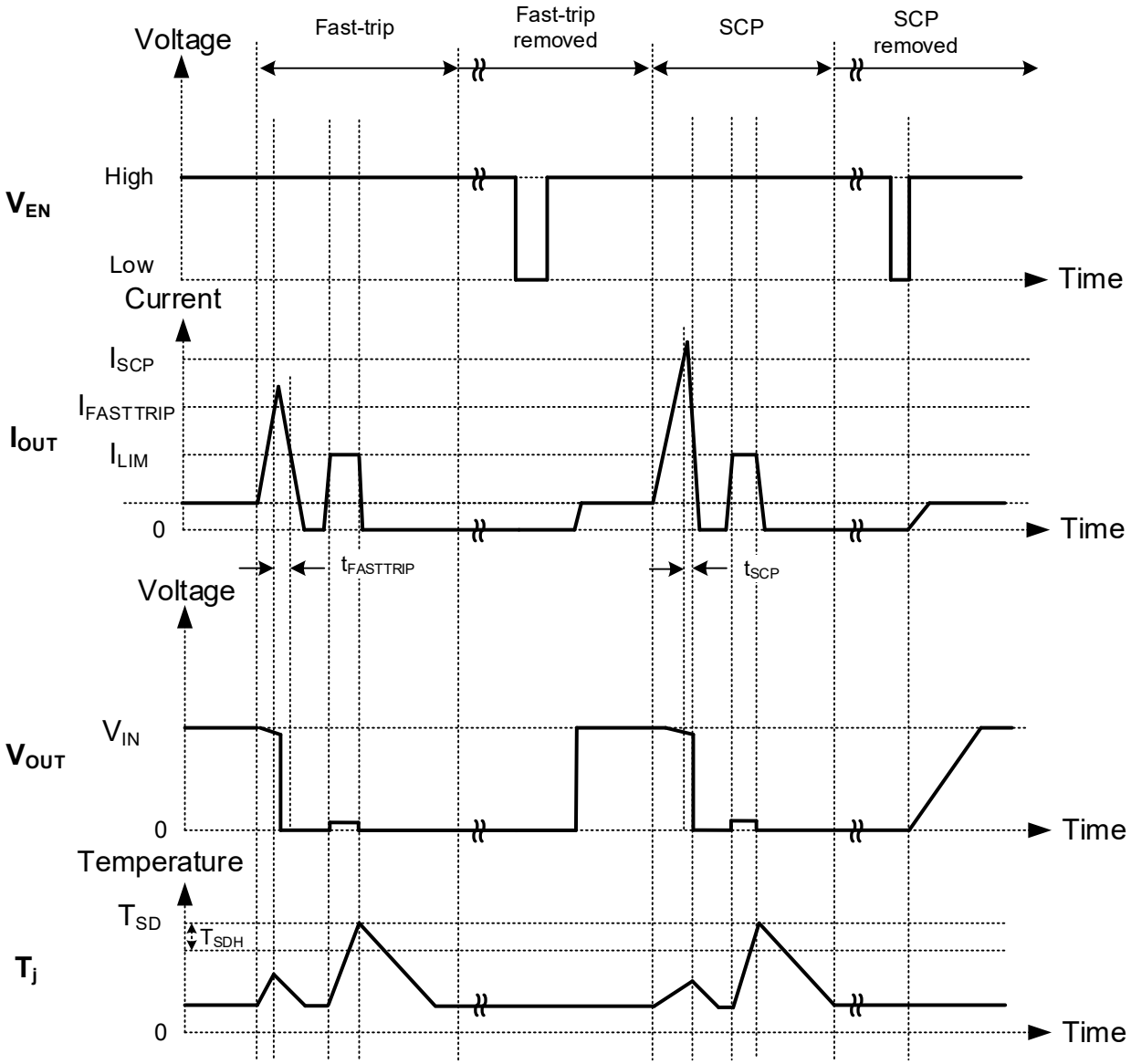


Figure 5.25 Example of short-circuit protection operation (Latch-off mode)

5.8. Output current monitor (IMON)

The current source at the IMON pin is proportional to the current flowing from V_{IN} to V_{OUT}. This current is converted to a voltage by the resistor R_{IMON} connected between the IMON pin and GND. The maximum current monitor voltage (V_{IMON} max) is limited to 4 V when 9 V ≤ VSYS = VIN, or 2 V when VSYS = VIN < 9 V. Set R_{IMON} using formula 10 so that V_{IMON} max is not exceeded.

Do not connect a capacitor to the IMON pin because it reduces the response of the current monitor. When VSYS is 9 V or higher and the output current monitor is not used, the IMON pin can be left open.

Formula10 : $$V_{IMON} = [I_{OUT} \times G_{IMON}] \times R_{IMON}$$

G_{IMON} : I_{MON}/I_{OUT} gain (27.9 μA/A (Typ.))

I_{OUT} : VOUT pin Output Current (A)

5.9. Fault response (FLAG)

The FLAG pin outputs a low level when the device detects fault conditions such as undervoltage lockout, overvoltage protection, overcurrent protection, reverse current blocking, an ILIM pin short, and thermal shutdown. An internal deglitch circuit is used to prevent false detection. The FLAG pin is an open-drain output. Connect an external pull-up resistor to the FLAG pin, as shown in Figure 5.26.

When the FLAG pin is not used, it can be left open or connected to GND.

Select the pull-up resistor considering the maximum sink current of the FLAG pin. Check the operation with the actual circuit and select an appropriate resistor value.

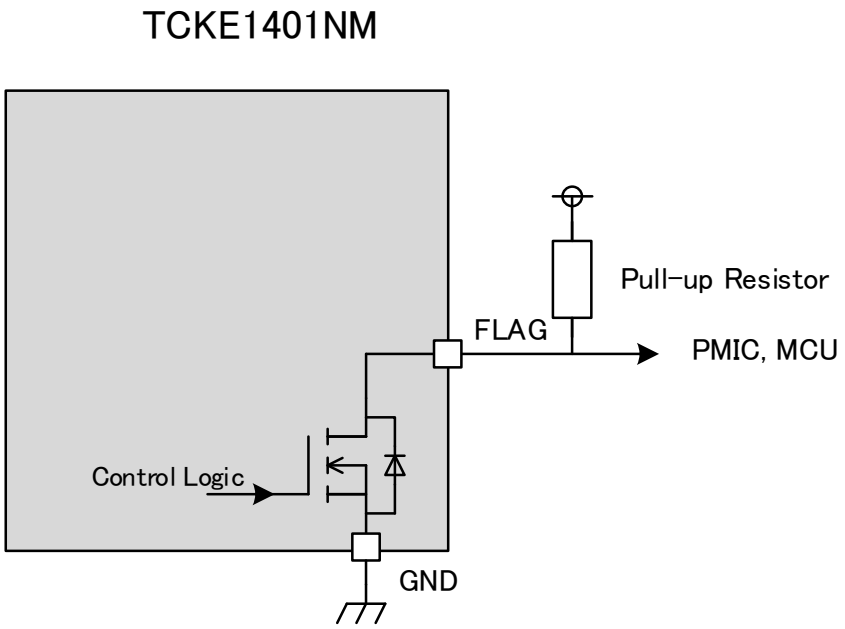


Figure 5.26 FLAG pin equivalent circuit

Table 5.8 Target functions and operations of FLAG output

Protective Function (Note 9)		IC Operation	FLAG Output
Normal Operation		Normal Operation	High
Thermal Shutdown	$T_j > T_{SD}$	Shutdown	Low
Undervoltage Protection	$V_{UVLO} < V_{UVLOF}$ $V_{SYS} < V_{SYS_UVLO}$ (Note 10)	Shutdown	Low
Overvoltage Protection	$V_{OVP} > V_{OVPR}$ $V_{SYS} > V_{SYS_OVP}$ (Note 11)	Shutdown	Low
Over Current Protection	$I_{LIM} < I_{OUT} < I_{FASTTRIP}$ $t_{CL_PLIM_FLAG} < t_{CL_PLIM}$	I_{OUT} Current Limit	Low
Reverse Current Protection (Note 13)	$V_{OUT} - V_{SYS} \geqq 10$ mV	External MOSFET (Q1) OFF	Low
Reverse connection (Note 13)	$V_{SYS} > -80$ V, $V_{OUT} > -0.3$ V, $V_{SYS} - V_{OUT} \geqq -85$ V (Note 14)	Maintaining OFF status	Indefinite

Note 9: Unless otherwise specified, the condition is 4.7 V ≦ V_{SYS} = VIN ≦ 75 V.
Note 10: When the UVLO pin is connected to GND, it enters internal UVLO mode.
Note 11: When the OVP pin is connected to GND, it enters internal OVP mode.
Note 13: For details on the reverse current prevention function and reverse input connection prevention function, please refer to section 5.5.
Note 14: Voltage application is a condition for a 10 ms pulse.

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5.10. VSYS, VIN and GND pins

The VSYS pin supplies power to the internal control circuit. Connect a capacitor between the VSYS pin and GND to provide a stable power supply. When using the input reverse polarity protection and reverse current blocking functions, connect external MOSFETs Q1 and Q2.

5.11. Thermal shutdown (TSD)

The thermal shutdown (TSD) function stops the IC operation when the junction temperature (Tj) of the eFuse IC exceeds the set value due to continuous high current. After TSD is activated, the device either remains in Latch-off mode or starts auto-retry at intervals of t_{TSD_retry} = 330 ms (Typ.) after T_j falls below 165°C (Typ.), depending on the recovery mode shown in Table 5.10.

5.11.1. Thermal shutdown in Auto-retry mode

After the device enters the shutdown state due to thermal shutdown, it restarts after 330 ms (Typ.).
The thermal shutdown (TSD) function protects the IC by turning off the output when the junction temperature rises to the thermal shutdown threshold temperature T_{SD} (165°C (Typ.)) or higher due to IC power consumption caused by continuous high output current or an output short circuit. When TSD is activated in the TCKE1401NM, the output is turned off and the FLAG pin output changes from high to low. The thermal shutdown and recovery temperatures have hysteresis (T_{SDH}).

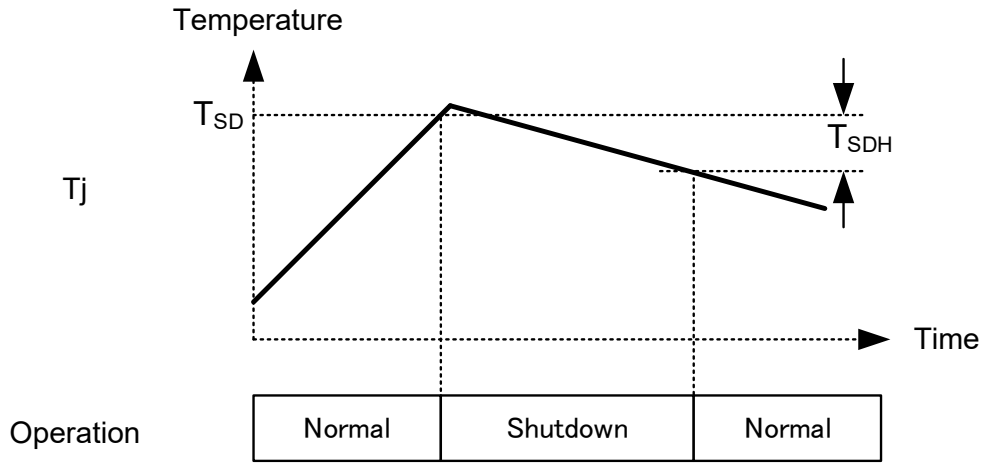


Figure 5.27 Thermal shutdown timing chart

5.11.2. Thermal shutdown in Latch-off mode

After the thermal shutdown (TSD) function is activated and the device enters the shutdown state, the device must be restarted by applying the control signal to the EN pin again or by setting the input voltage VIN to 0 V and then applying it again. The protection state is maintained until the device is restarted.

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5.11.3. Operating principle of the thermal shutdown circuit

Detection of junction temperature is performed by comparing V_{TSD}, which is produced by dividing the reference voltage V_{REF} with R_A and R_B, with the forward voltage of the diode. As shown in Figure 5.28, V_{REF} shows little change with temperature.

When the TCKE1401NM is operating normally, the forward voltage of the diode is higher than V_{TSD}. The forward voltage of the diode has a temperature coefficient of approximately –2 mV/°C. When the junction temperature rises and the forward voltage drops below V_{TSD}, the comparator switches and turns off the output of the TCKE1401NM. At the same time, the FLAG pin output changes from high to low.

Table 5.9 Thermal Shutdown T_{SD} Characteristics (as stated in the datasheet)

Characteristics	Symbol	Test condition	T_a = 25°C	T_a = -40 to 125°C			Unit
			Typ.	Min	Typ.	Max	
Thermal shutdown threshold	T_{SD}	T_j	165	-	-	-	°C
Thermal shutdown hysteresis	T_{SDH}	T_j	20	—	-	-	°C
Retry delay in TSD	t_{TSD_retry}	MODE = GND	-	230	330	430	ms

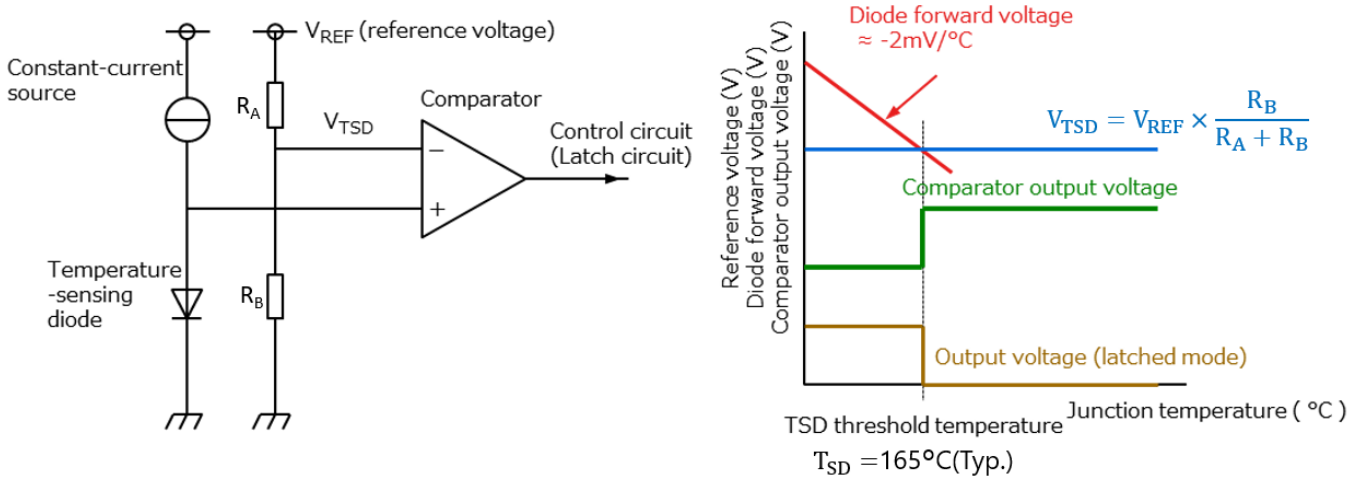


Figure 5.28 Thermal shutdown circuit and operating principle

5.12. EN pin

The EN pin can be used to control the TCKE1401NM with an external control signal, as shown in Figure 5.29. The EN pin can also be left open. When the EN pin is left open, it is internally pulled up to a high level.

When using an external control signal, the ON/OFF threshold voltages of the EN pin have hysteresis. Set the high level of the control signal to 2.0 V or higher and the low level to 0.8 V or lower.

The EN pin of the TCKE1401NM also has a window comparator, as shown in Figure 5.30. The window comparator has two threshold voltages, V_{REF_P} and V_{REF_N}. Therefore, even when an unstable control signal with chattering or ringing is applied, a stable output can be obtained as shown in Figure 5.31 (b). With a normal inverter that has only one threshold voltage, the output may not operate correctly, as shown in Figure 5.31 (a).

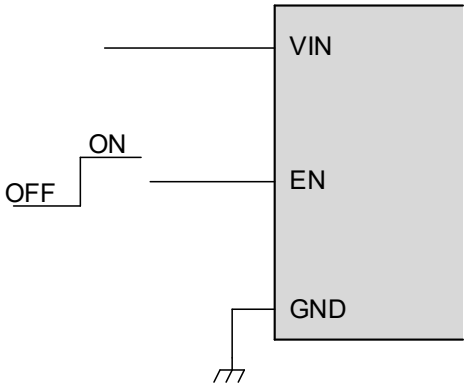


Figure 5.29 Example of EN terminal connection (external control)

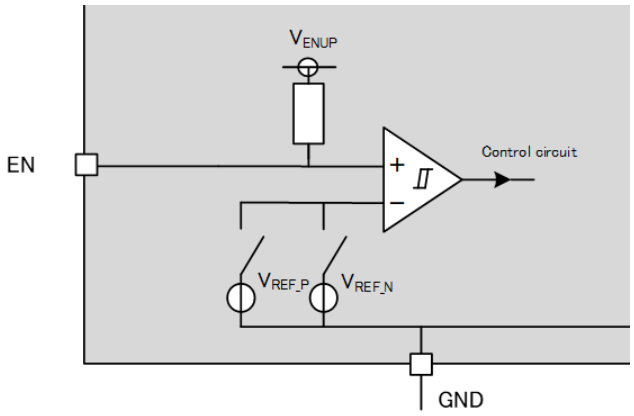


Figure 5.30 EN Terminal Equivalent Circuit

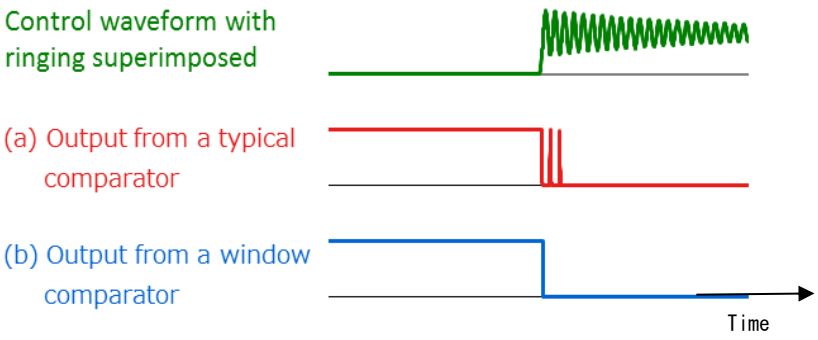


Figure 5.31 Operation of standard comparator and window comparator

5.13. Mode pin setting

The device can change the fault response depending on the MODE pin state. Refer to Table 5.10 for the MODE pin state.

Table 5.10 Fault response setting

MODE pin state	Fault response
Open	After the abnormal state, the eFuse IC will latch off. To restart the eFuse IC, either apply the EN pin again, set the VSYS pin input voltage to 0 V once and then apply again, or lower the UVLO pin voltage below V_{UVLOF} and recover from UVLO state.
Shorted to GND	Auto-retry mode with t_{TSD_retry}.

6. Application example of TCKE1401NM

6.1. TCKE1401NM application examples

The following sections show some application examples of the TCKE1401NM.

- **Server Power supplies**

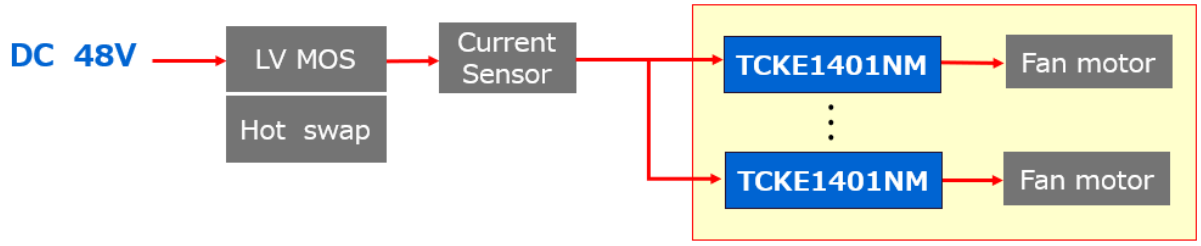


Figure 6.1 Application to server power supplies

- **Power tools**



Figure 6.2 Application to power tools

- **Commercial printers**

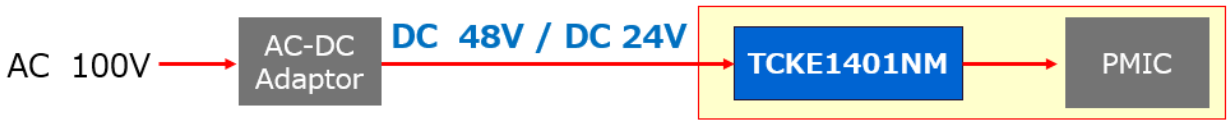


Figure 6.3 Application to commercial printers

6.2. TCKE1401NM peripheral circuit example

Figure 6.4 shows a peripheral circuit example of the TCKE1401NM. Connect the power supply to the VIN and VSYS pins. During normal operation, almost the same voltage as the VIN pin voltage is output from the VOUT pin through the MOSFET.

When the current drops rapidly due to short-circuit protection or overcurrent protection, a high spike voltage may occur due to the inductance of the wiring connected to the input and output pins of the eFuse IC. This spike voltage may damage the eFuse IC. In this case, a positive spike voltage occurs on the input side and a negative spike voltage occurs on the output side.

When designing the board, keep the wiring on the input and output sides of the eFuse IC as short as possible. Also, make the GND area as large as possible to reduce the impedance.

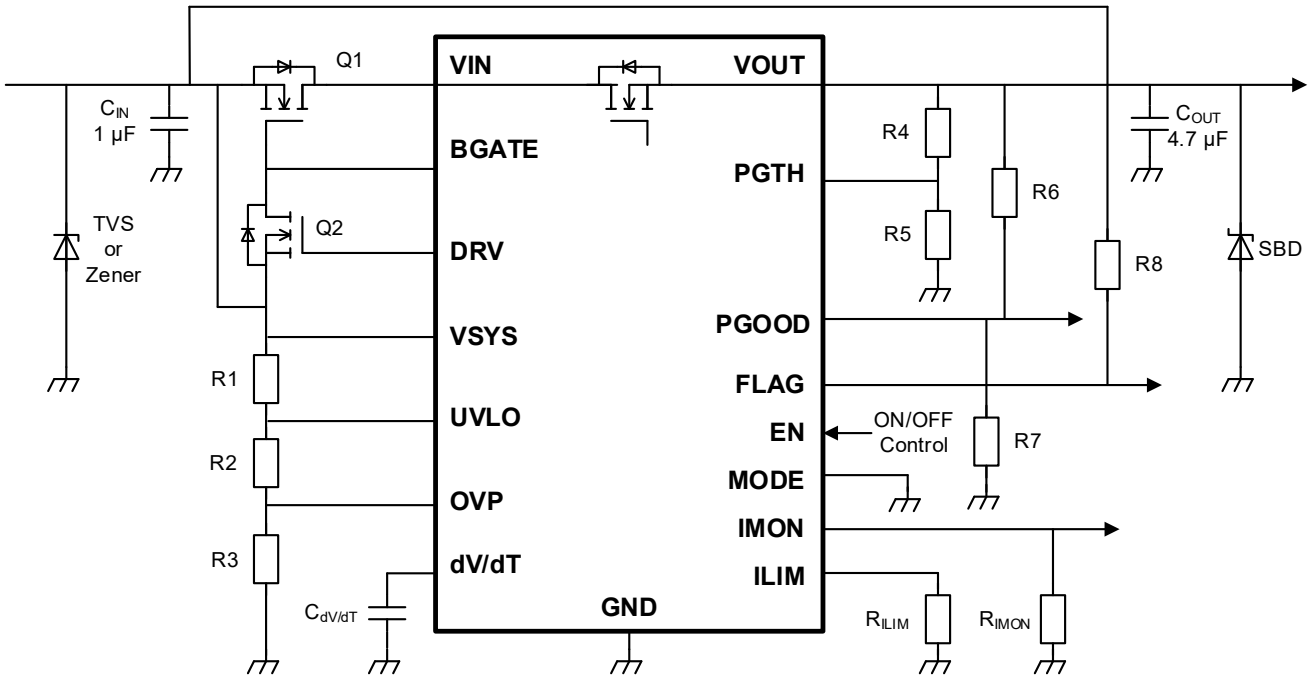


Figure 6.4 TCKE1401NM peripheral circuit example

Table 6.1 Functions of peripheral circuit components

Symbol	Description
C_{IN}	Input capacitor
C_{OUT}	Output capacitor
$C_{dV/dT}$	Slew rate adjustment capacitor
Q1, Q2	MOSFETs for always-on reverse current blocking and input reverse polarity protection
R1, R2, R3	Resistors for setting the overvoltage protection and undervoltage lockout thresholds
R4, R5	Resistors for setting the Power Good threshold
R6, R7	Pull-up / Voltage divider resistors for the Power Good (PGOOD)
R8	FLAG pin pull-up resistor
R_{ILIM}	Output current limit setting resistor
R_{IMON}	Current monitor resistor

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CIN functions to suppress the peak value against the positive spike voltage generated by the inputs. A CIN of at least 0.1 µF is recommended for this device, but the appropriate capacitor value should be determined based on operation on the actual PCB board. The peak value V_{SPIKE} of the spike voltage and the capacitance value of the CIN have the following relationship. It can be understood that the spike voltage can be reduced by increasing the C_{IN}, and it is determined by formula 11.

$$\text{Formula 11 :} \quad V_{SPIKE} = V_{IN} + I_{OUT} \times \sqrt{\frac{L_{IN}}{C_{IN}}}$$

V_{SPIKE}	:	Peak value of generated spike voltage (V)
V_{IN}	:	Input voltage during normal operation (V)
I_{OUT}	:	Output current (A)
L_{IN}	:	Effective inductance of input terminal (H)
C_{IN}	:	Input capacitor capacitance (F)

If VIN is high, VOUT is also high, and the current change during short-circuit or overcurrent protection is large, causing unstable operation due to unstable VIN and VOUT and possibly leading to IC destruction. If transient voltages exceeding the absolute maximum ratings are applied to the VIN pin, connect a TVS diode (ESD protection diode) or a Zener diode between the input pins and GND. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS or a Zener diode can help to absorb the excessive energy dump and prevent the device from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.

For negative spike voltages generated on the output side, such as during short-circuit protection operation, connect an SBD (Schottky barrier diode) between the output pin and GND. This will prevent the output potential from dropping significantly below GND.

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6.3. TCKE1401NM application circuit examples

This section introduces application circuit design examples for 24 V and 48 V power supply systems based on the peripheral circuits described above. The examples include resistor values for each setting pin and threshold values for the protection functions.

Figure 6.5 shows a reference circuit for a 24 V line using reverse polarity protection and reverse current blocking.

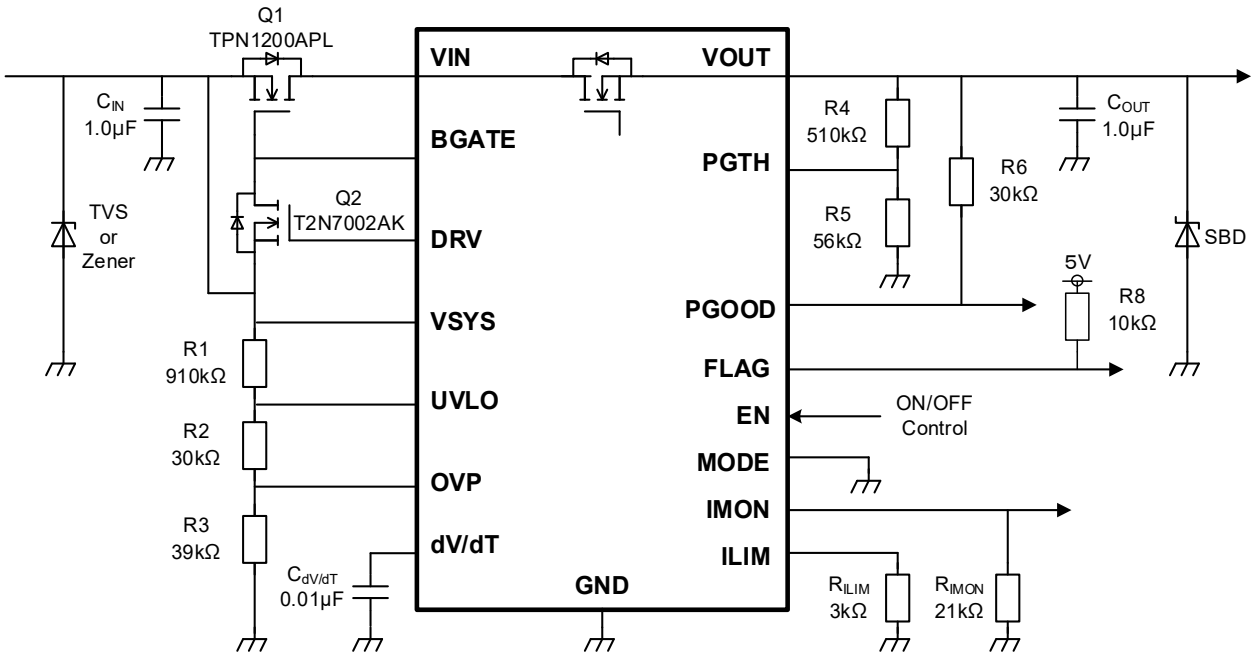


Figure 6.5 24 V reference circuit with reverse polarity and reverse current protection

Table 6.2 shows the calculated threshold values and operating times based on the external resistor and capacitor values shown in Figure 6.5. The calculated results are reference values based on the typical values of each electrical characteristic.

Table 6.2 Calculated values for the reference circuit in Figure 6.5

Setting item	Calculated result (Typ.) (Note 16)
UVLO detection voltage	15.9 V
UVLO release voltage	16.9 V
OVP detection voltage	31.0 V
OVP release voltage	28.9 V
PGOOD detection voltage	11.8 V
PGOOD release voltage	11.2 V
Overcurrent limit (I_{LIM})	6.43 A
V_{OUT} rise time (10% to 90%) (t_r)	3.99 ms

Note 16: The calculated values in this table are based on the typical values in the datasheet. The actual threshold values and operating times may vary depending on the electrical characteristics of the IC and the tolerance of the external components.

Figure 6.6 shows a reference circuit for a 48 V line without reverse polarity protection and reverse current blocking.

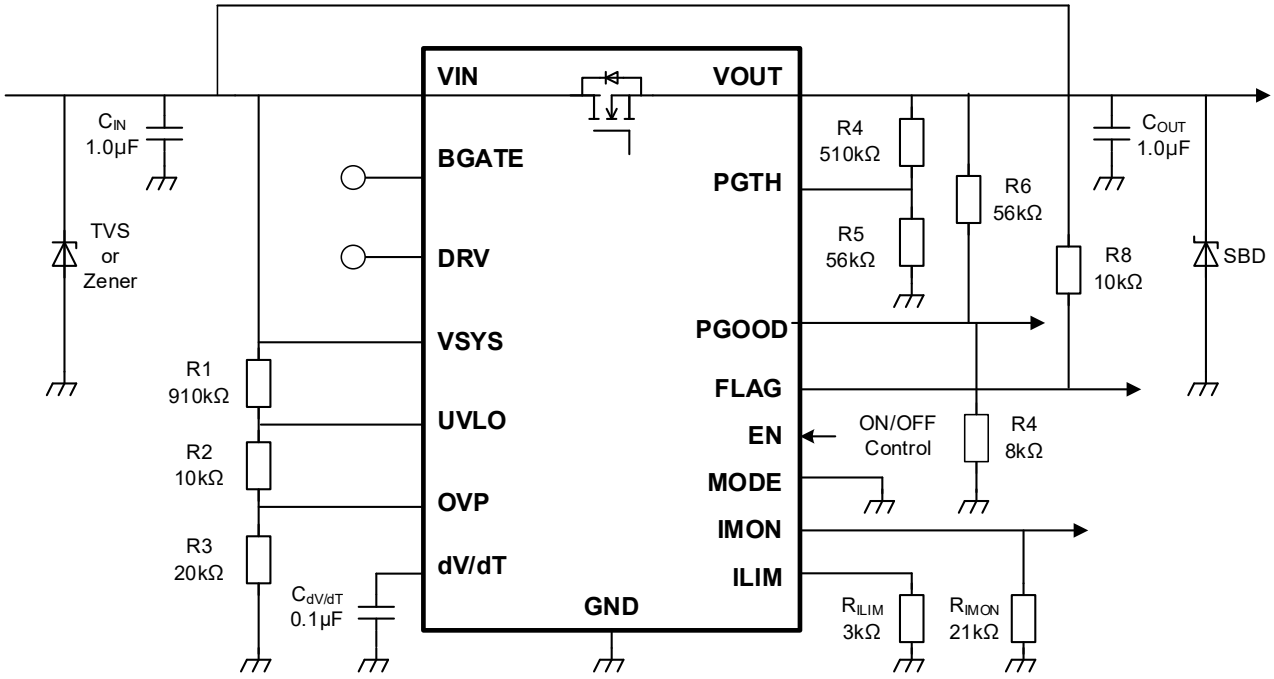


Figure 6.6 48 V reference circuit without reverse polarity and reverse current protection

Table 6.3 shows the calculated threshold values and operating times based on the external resistor and capacitor values shown in Figure 6.6. The calculated results are reference values based on the typical values of each electrical characteristic.

Table 6.3 Calculated values for the reference circuit in Figure 6.6

Setting item	Calculated result (Typ.) (Note 16)
UVLO detection voltage	35.1 V
UVLO release voltage	37.3 V
OVP detection voltage	58.0 V
OVP release voltage	54.0 V
PGOOD detection voltage	11.8 V
PGOOD release voltage	11.2 V
Overcurrent limit (ILIM)	6.43 A
VOUT rise time (10% to 90%) (tr)	39.9 ms

Note 16: The calculated values in this table are based on the typical values in the datasheet. The actual threshold values and operating times may vary depending on the electrical characteristics of the IC and the tolerance of the external components.

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7. Attention in use

(1) **Absolute maximum ratings**

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.

(2) **Input/ Output capacitors**

Ceramic capacitors can be used with the IC, however some type capacitors may have very large temperature dependence. Please consider usage environment conditions carefully to select the capacitors.

(3) **Mounting**

The long distance between IC and C_{OUT} might affect phase assurance by impedance in wire and inductor. For stable power supply, C_{OUT} needs to mount near IC as much as possible. Also, VIN and GND patterns need to be large and make the wire impedance small as possible.

(4) **VSYS pin**

The VSYS pin is the power supply pin for the device's internal circuit. To prevent unexpected behavior, we recommend designing the system so that a stable power supply is provided to this pin, taking into consideration C_{IN}, C_{OUT}, and impedance.

(5) **Maximum permissible loss and output current**

Please have enough design margin for expected maximum permissible loss and output current. And under consideration of surrounding temperature, input voltage etc., we recommend proper dissipation ratings for maximum permissible loss and output current; in general, maximum dissipation rating is 70 to 80 %.

(6) **Protection circuit**

Overcurrent protection, overvoltage protection and thermal shutdown function are designed in this device, but these are not intended to constantly ensure the suppression of this device within operation limits. Depending on the condition during actual usage, it could affect the electrical characteristic specification and reliability.

When using these products, please read through and understand the concept of dissipation for absolute maximum ratings from the above-mentioned or our 'Semiconductor Reliability Handbook'. Then use these products under absolute maximum ratings in any condition. Furthermore, Toshiba recommend inserting failsafe system into the design.

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8. Conclusion

This document has described how to use the TCKE1401NM and its protection functions. The TCKE1401NM can protect the IC and equipment from various abnormal conditions, including not only overcurrent but also overvoltage, overtemperature, and reverse current. It also provides useful functions such as inrush current limiting and protection against improper operation at low input voltages. These functions help improve the reliability of electronic equipment.

We hope that this document will help you make effective use of the TCKE1401NM to improve equipment performance, reduce size, and lower total costs.

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