Application Example of 3-Phase constant current control SRC

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1. Purpose and Objective of This Document

• Target Products and Functions

TB9M003FG and TB9M030FG (hereinafter referred to as “the ICs”), members of the SmartMCD™ series of SoCs integrating a microcontroller and motor driver, feature slew rate control (SRC) based on three-phase constant-current control.

SRC controls the gate current (hereinafter referred to as “Ig”) during MOSFET turn-on, allowing adjustment of d(Vds)/dt, which represents the slew rate (SR) of the drain-source voltage (hereinafter referred to as “Vds”). This enables the balance between electromagnetic noise and switching loss to be adjusted according to system requirements.

• Content of This Document

In addition to the basic concept of SRC, this document describes the parameter adjustment procedure for the three-phase constant-current SRC (hereinafter referred to as “3-Phase SRC”) implemented in the ICs, along with practical adjustment examples using actual waveforms.

• Considerations for Application

This document provides an example of how to adjust the balance between electromagnetic noise and switching loss while observing actual waveforms. The appropriate d(Vds)/dt varies depending on the system specifications, operating conditions, MOSFETs used, and other factors. Therefore, determine the final parameter settings through evaluation on the actual system.
We hope this document will serve as a useful reference for system design using 3-Phase SRC.

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2. Overview and Basic Concept of 3-Phase SRC

2.1. Overview of 3-Phase SRC

To achieve precise motor control, the MOSFETs need to be switched at an appropriate speed. However, increasing the MOSFET switching speed causes steeper changes in the drain-source voltage and drain current (hereinafter referred to as “Id”) during turn-on and turn-off, which may increase electromagnetic noise and lead to interference with peripheral circuits or malfunctions. SRC addresses this issue by enabling adjustment of the balance between electromagnetic noise and switching loss.

Direct evaluation of electromagnetic noise is not straightforward. Therefore, in this document, d(Vds)/dt, which correlates with electromagnetic noise and can be readily observed in waveforms, is used as an evaluation metric.

In general, there are two types of SRC: open-loop SRC and closed-loop SRC. With open-loop SRC, the gate current must be set to achieve the target d(Vds)/dt. In contrast, with closed-loop SRC, Ig is automatically adjusted to achieve the target d(Vds)/dt. SRC adjusts the MOSFET switching speed by controlling Ig and adjusts the balance between electromagnetic noise and switching loss by controlling d(Vds)/dt. As a secondary effect, SRC also helps suppress self-turn-on caused by d(Vds)/dt and voltage spikes caused by reverse-recovery current.

The ICs support constant-current drive as well as variable-current drive using open-loop SRC. The variable-current drive of the ICs uses three-phase constant-current SRC, which divides the switching period into three phases and allows Ig to be set individually for each phase. The definition of each phase is described in Section 3.1.

In Phase 1 and Phase 3, which have a relatively small contribution to electromagnetic noise, Ig is set to a large value to switch the MOSFET quickly and reduce switching loss. In contrast, in Phase 2, where Vds changes significantly and the contribution to electromagnetic noise is relatively large, Ig is set to a small value to reduce d(Vds)/dt and suppress electromagnetic noise.

In this document, SR is defined as |d(Vds)/dt| during the period in which Vds decreases from 90% to 10% of its total change. Adjust each 3-Phase SRC parameter so that d(Vds)/dt meets the system requirements.

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2.2. Effects of 3-Phase SRC

◆ **Balancing Electromagnetic Noise and Switching Loss by Adjusting d(Vds)/dt**

As a representative example, Figure 2.1 shows timing charts of constant-current drive and 3-Phase SRC during MOSFET turn-on. A conceptual diagram of the instantaneous switching loss is also shown at the bottom of the figure.

With constant-current drive, Ig remains constant throughout the switching period. In contrast, with 3-Phase SRC, Ig can be switched stepwise as the switching operation progresses. In the period where Vds changes significantly (Phase 2), Ig is set to a small value to reduce d(Vds)/dt and suppress electromagnetic noise caused by d(Vds)/dt. In contrast, in the periods where the change in Vds is small and the contribution to electromagnetic noise is relatively small (Phase 1 and Phase 3), Ig is set to a large value to shorten the duration of each phase and suppress an increase in switching loss.

Note that actual electromagnetic noise and switching loss are affected not only by d(Vds)/dt but also by factors such as d(Id)/dt, MOSFET characteristics, and PCB layout. The instantaneous loss waveforms shown in Figure 2.1 are conceptual representations intended to illustrate the trend in switching loss associated with 3-Phase SRC.

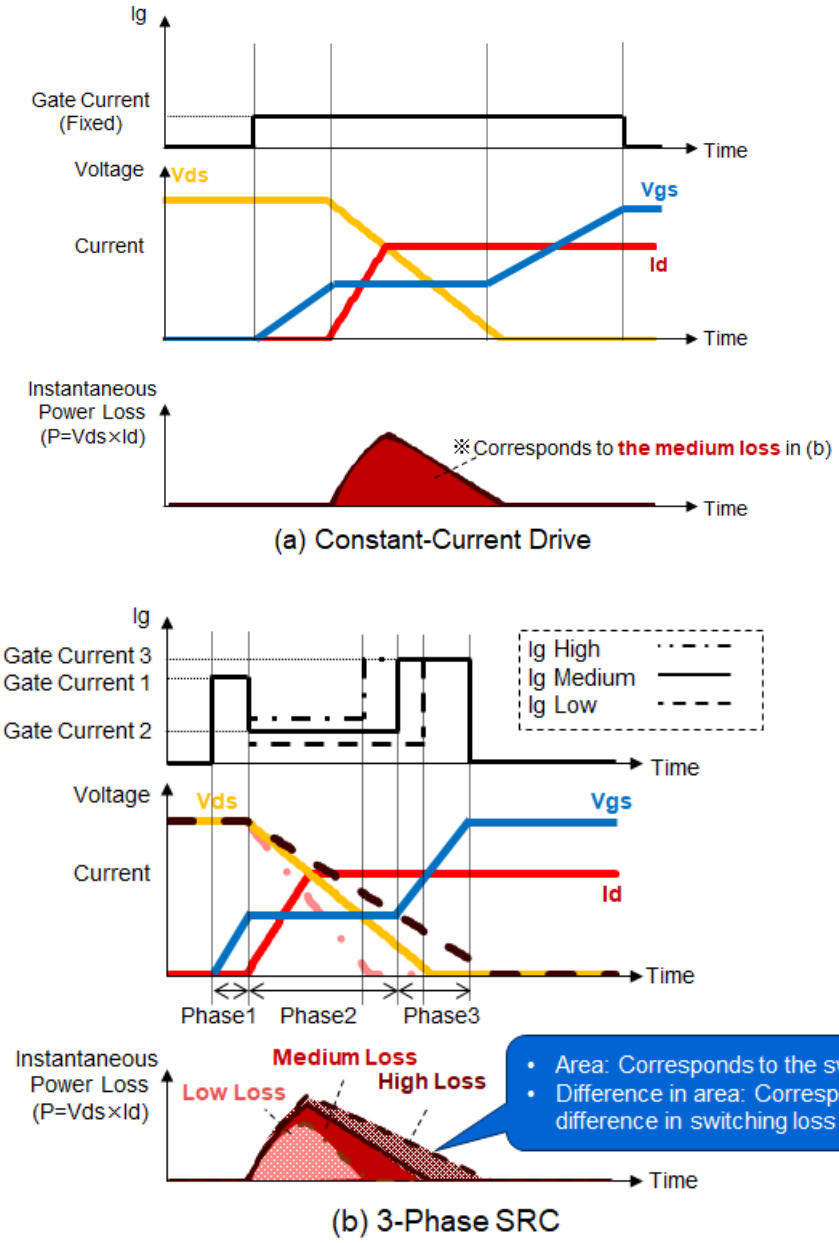


Figure 2.1 Constant-Current and 3-Phase SRC Drive Timing Chart

3. Guidelines for Adjusting 3-Phase SRC Parameters

3.1. Overview of 3-Phase SRC Parameter Adjustment

This section describes the guidelines for adjusting 3-Phase SRC parameters.
Figure 3.1 shows the SRC drive circuit, and Figure 3.2 illustrates the concept of each phase. Table 3.1 lists the 3-Phase SRC parameters of the ICs. Refer to Figure 3.2 and Table 3.1 for the definition of each phase.

As described in Chapter 2, the 3-Phase SRC of the ICs allows Ig to be set individually for each of Phases 1 through 3. Adjust each parameter while observing the waveforms to achieve the target d(Vds)/dt.

Even with the same SRC settings, the actual d(Vds)/dt varies depending on operating conditions, such as the battery voltage (Vbat) and temperature, as well as MOSFET characteristics. Therefore, set each parameter with sufficient design margin so that electromagnetic noise and switching loss meet the system requirements, considering variations in operating conditions and MOSFET characteristics.

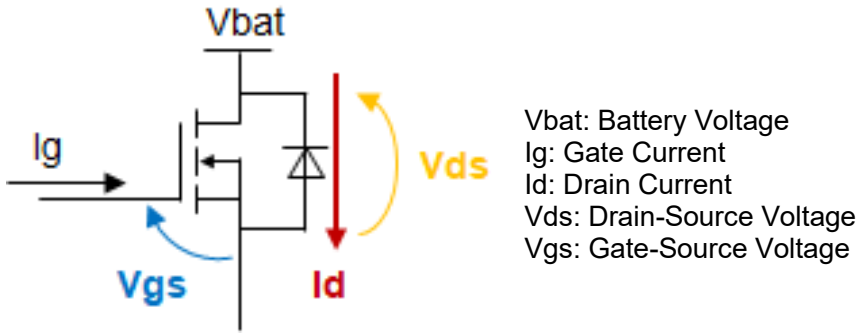


Figure 3.1 SRC Drive Circuit

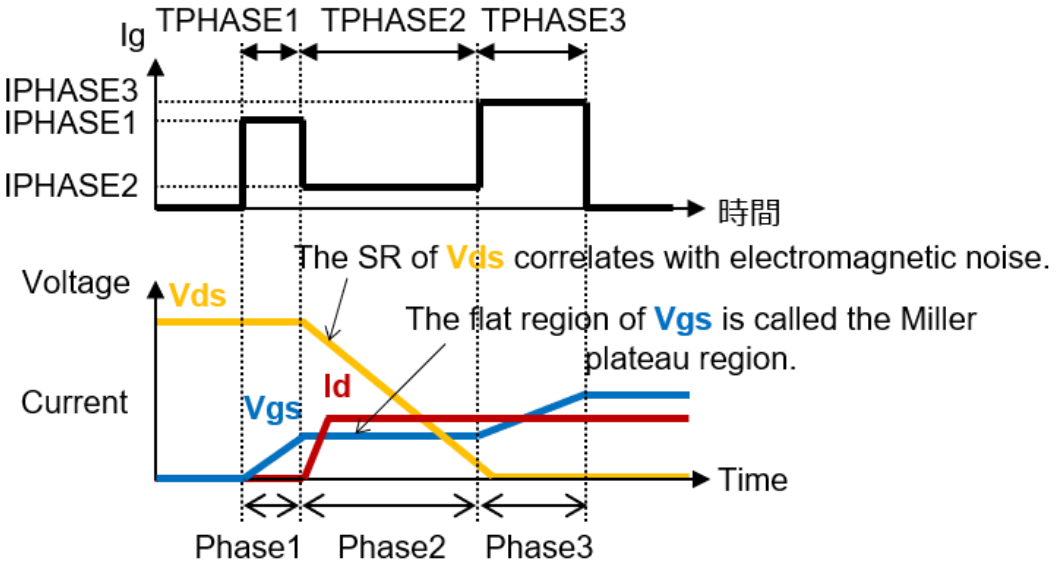


Figure 3.2 Phase Definition in 3-Phase SRC

Table 3.1 3-Phase SRC Setting Parameters

Phase of SRC	Explanation	Parameter (Note)	Remark
Phase1 (pre-charge)	The region where Vgs rises and reaches approximately the threshold voltage (Vth) (Low contribution to noise)	TPHASE1	・ Sets the duration of Phase 1. ・ Set so that the operation transitions to Phase 2 just before the MOSFET reaches the Miller plateau region. ・ If the setting is too short, the operation may transition to Phase 2 before Ig sufficiently reaches the set value. ・ Common to the high side and low side.
		IPHASE1	・ Sets Ig for Phase 1. ・ Set Ig to a high value to reduce switching time and switching loss, after confirming its impact on electromagnetic noise. In this document, Ig is set to the maximum value of 120 mA. ・ Common to the high side and low side.
Phase2 (charge)	The region where Vds mainly changes (High contribution to noise)	TPHASE2	・ Sets the duration of Phase 2. ・ Set considering the target d(Vds)/dt and operating conditions such as Vbat. ・ If the setting is too short, the operation may transition to Phase 3 before the Vds transition is completed. ・ Common to the high side and low side.
		IPHASE2H	・ Sets the high-side Ig for Phase 2. ・ Reducing Ig lowers d(Vds)/dt and suppresses electromagnetic noise. This is a key parameter for balancing electromagnetic noise and switching loss.
		IPHASE2L	・ Sets the low-side Ig for Phase 2. ・ Reducing Ig lowers d(Vds)/dt and suppresses electromagnetic noise but tends to increase switching loss.
Phaes3 (post-charge)	The region where Vgs rises to the final drive voltage after the Vds transition is completed (Low contribution to noise)	-	・ Ig for Phase 3 is automatically determined as the sum of the Ig settings for Phases 1 and 2. ・ A high Ig allows the MOSFET to quickly transition to the on-state, suppressing an increase in switching loss.

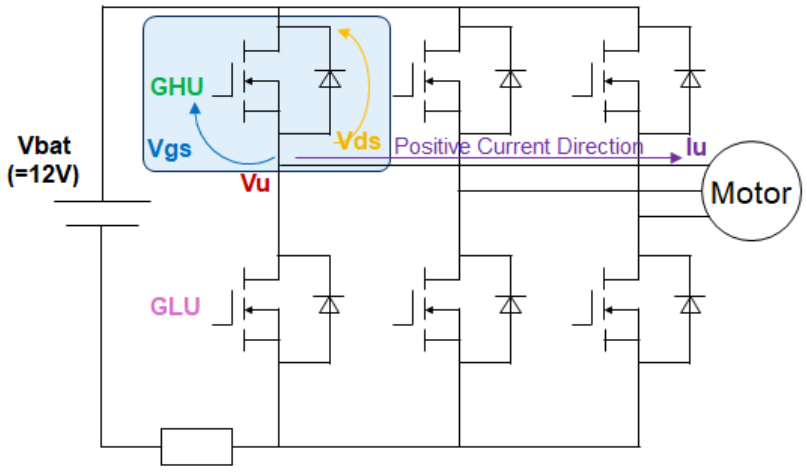
Note:
[MCSSDRVPTSR] register : TPHASE1, TPHASE2 (time parameters)
[PREDRVSRCR] register : IPHASE1, IPHASE2H, IPHASE2L (current parameters)

3.2. Evaluation Method for 3-Phase SRC

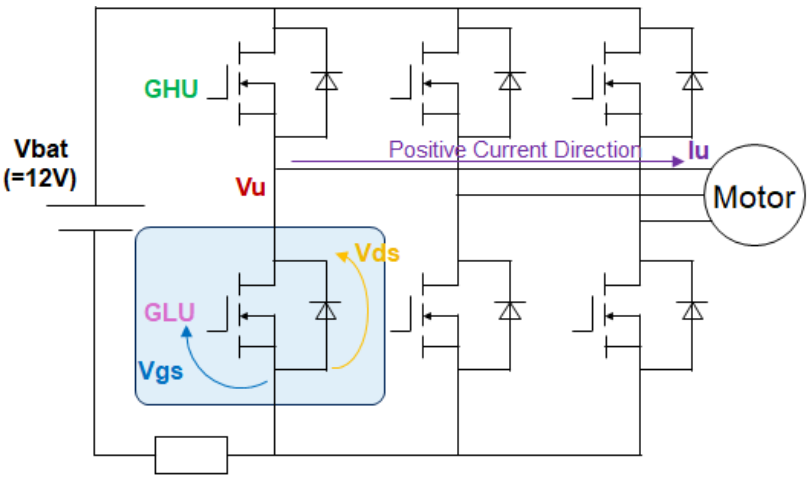
Figure 3.3 shows the waveform measurement setup for 3-Phase SRC.
Due to limitations of the measurement setup, the high-side and low-side waveforms are measured separately, as shown in Figure 3.3. In this evaluation, the waveforms associated with the U-phase are measured.

To verify that the 3-Phase SRC parameter settings differ depending on the MOSFET gate charge (Qg), two MOSFETs with different Qg values are used for the evaluation. Chapter 4 describes the waveforms obtained from parameter adjustment examples using each MOSFET.

(1) Qg = 76 nC (TK100S04N1L)
(2) Qg = 39 nC (TK65S04N1L)



(a) High side MOSFET Measurement



(b) Low side MOSFET Measurement

Figure 3.3 3-Phase SRC Waveform Measurement Example

4. 3-Phase SRC Parameter Adjustment Examples

4.1. Adjustment Procedure

Figure 4.1 shows the flowchart for adjusting the 3-Phase SRC parameters. Since d(Vds)/dt is mainly affected by the Phase 2 parameter settings, this section focuses primarily on Phase 2. Set each parameter to achieve the target d(Vds)/dt, considering the MOSFET characteristics described in Chapter 3.

Chapter 4 describes the phase transition timing required for 3-Phase SRC to function effectively and how to adjust it. Adjust TPHASE1 while observing the Vds waveform. Set IPHASE1 to 120 mA, which is the maximum setting.

Guidelines for Phase 1 Adjustment

- TPHASE1: Set TPHASE1 so that the transition to Phase 2 occurs just before the MOSFET reaches the Miller plateau region.
- IPHASE1: Set IPHASE1 to as large a value as possible within the range that allows stable MOSFET turn-on. (In this document, IPHASE1 is set to the maximum setting of 120 mA.)

Guidelines for Phase 2 Adjustment

- TPHASE2: Set TPHASE2 to sufficiently cover the entire period during which Vds changes.
- IPHASE2H: Adjust IPHASE2H while observing the overshoot and ringing in the Vds waveform of the high-side MOSFET.
- IPHASE2L: Adjust IPHASE2L while observing the overshoot and ringing in the Vds waveform of the low-side MOSFET.

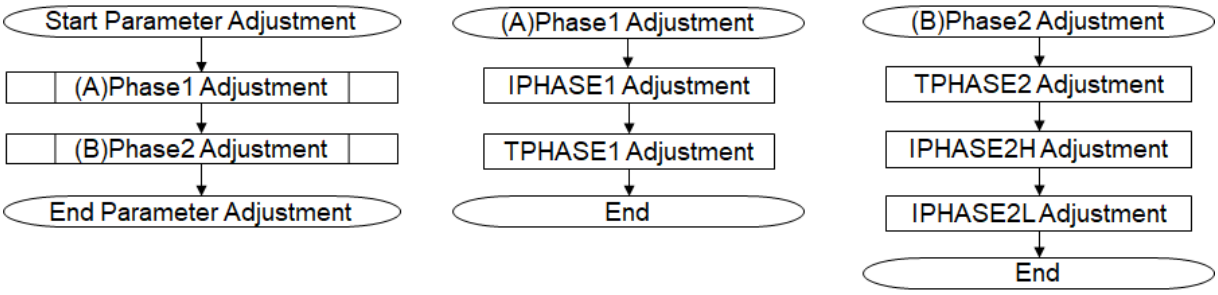
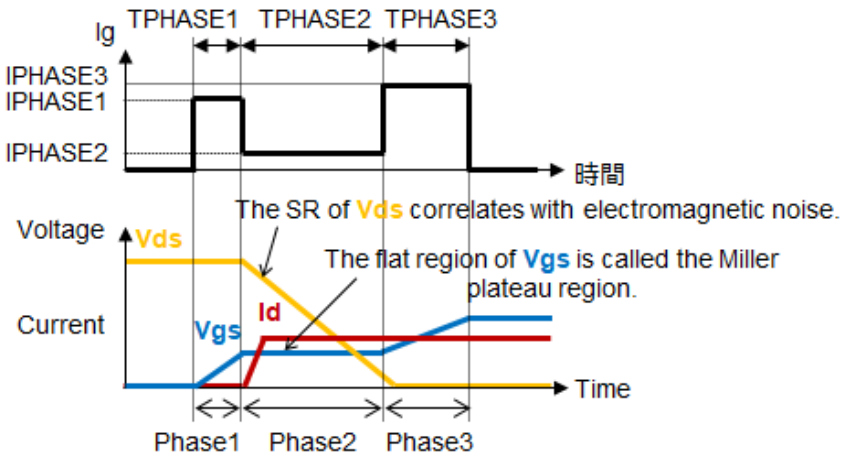


Figure 4.1 3-Phase SRC Adjustment Flow



Shown in Chapter 3 (Figure 3.2, Concept of Phases in 3-Phase SRC)

4.2. (A) Waveform Example of Phase 1 Adjustment (Qg = 76 nC, TK100S04N1L)

First, in step (A), set TPHASE1, which is a Phase 1 parameter. At this point, also set the Phase 2 parameters provisionally. Note that the gate output on-time may vary depending on the TPHASE2 setting.
Figure 4.2 shows an example of Phase 1 parameter adjustment.
If TPHASE1 is too large, Phase 1 may continue even after Vds starts to change, and sufficient time for control in Phase 2 may not be ensured. In contrast, if TPHASE1 is too small, the transition to Phase 2 may occur before Vds starts to change, and the Phase 2 settings may not be fully effective. Adjust TPHASE1 while observing the Vds waveform so that Phase 1 ends just before Vds starts to change.

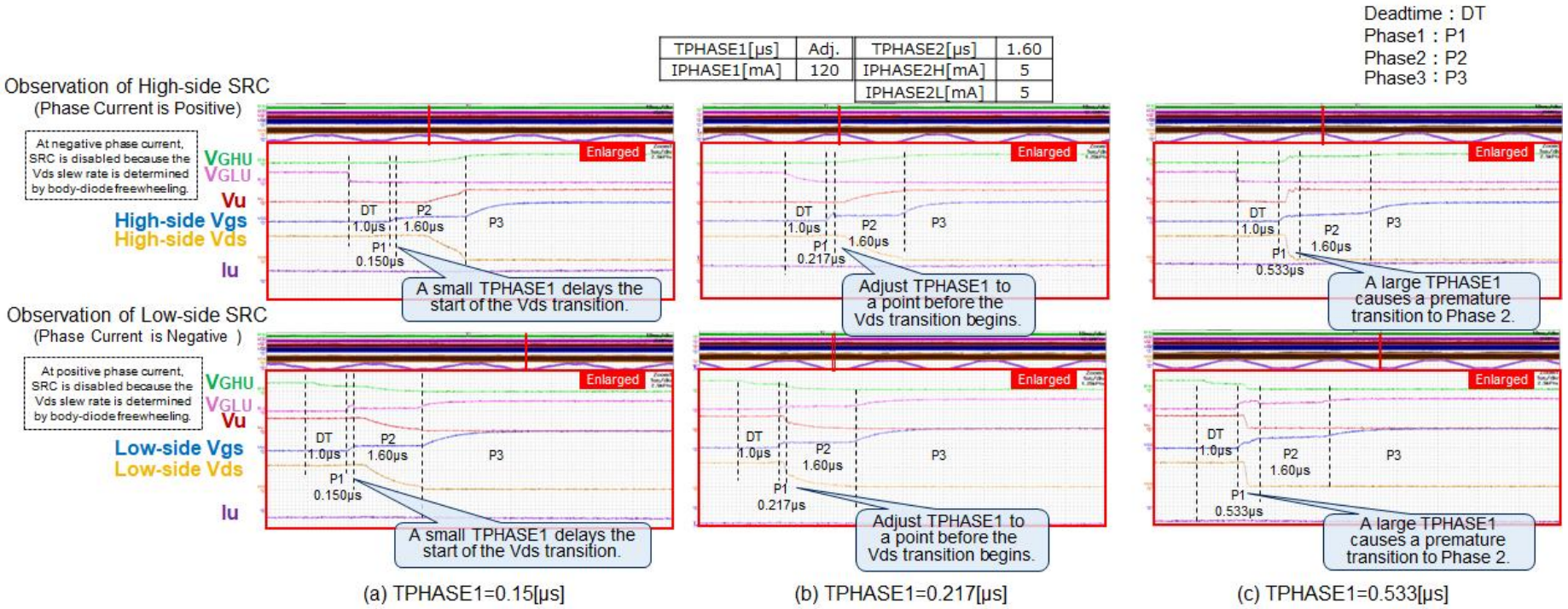


Figure 4.2 Phase 1 Parameter Adjustment Example

4.3. (B) Waveform Example of Phase 2 Adjustment (Qg = 76 nC, TK100S04N1L)

Next, in step (B), set the Phase 2 parameters TPHASE2, IPHASE2H, and IPHASE2L. Set TPHASE2 to sufficiently cover the entire period during which Vds changes. As a guideline for the initial setting, use the following equation:

TPHASE2 ≈ Vbat / |d(Vds)/dt|

Figure 4.3 shows examples of Phase 2 parameter adjustment under three conditions with different target d(Vds)/dt values. IPHASE2H mainly affects d(Vds)/dt of the high-side MOSFET, and IPHASE2L mainly affects d(Vds)/dt of the low-side MOSFET. Adjust each parameter while observing the corresponding Vds waveform to achieve the target d(Vds)/dt.
Note: The parameter settings shown in this chapter do not consider variations in individual MOSFET characteristics or operating conditions and are adjusted for the MOSFETs and evaluation conditions used in this evaluation.

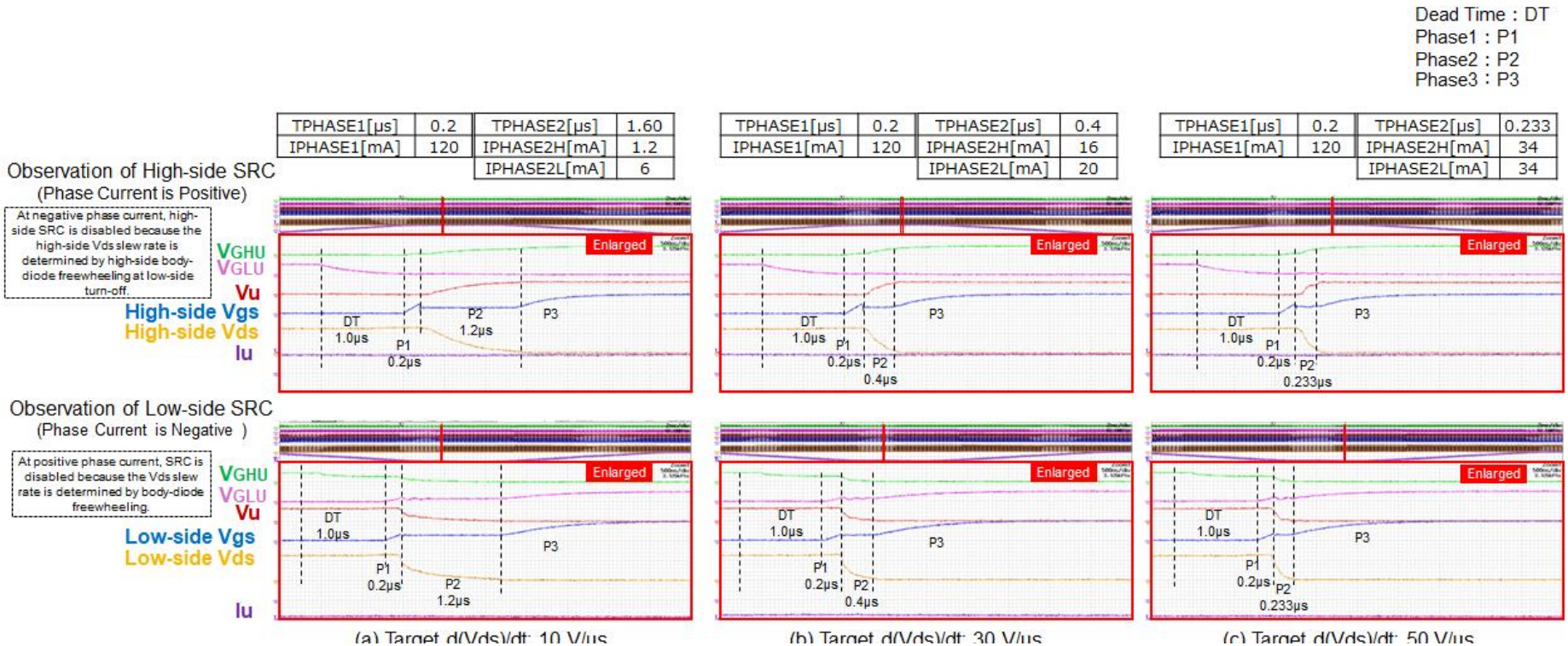


Figure 4.3 Phase 2 Parameter Adjustment Example

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4.4. Waveform Example of Adjustment for a MOSFET with Low Qg (Qg = 39 nC, TK65S04N1L)

This section provides an adjustment example using a MOSFET with a lower Qg than the MOSFET used in Section 4.3. Note that the target d(Vds)/dt is set to the same value as in Section 4.3. Figure 4.4 shows the adjustment results.

Note: In this adjustment example, priority is given to achieving comparable d(Vds)/dt values for the high-side and low-side MOSFETs. Therefore, the Vds of the low-side MOSFET starts to change around the transition timing to Phase 2.

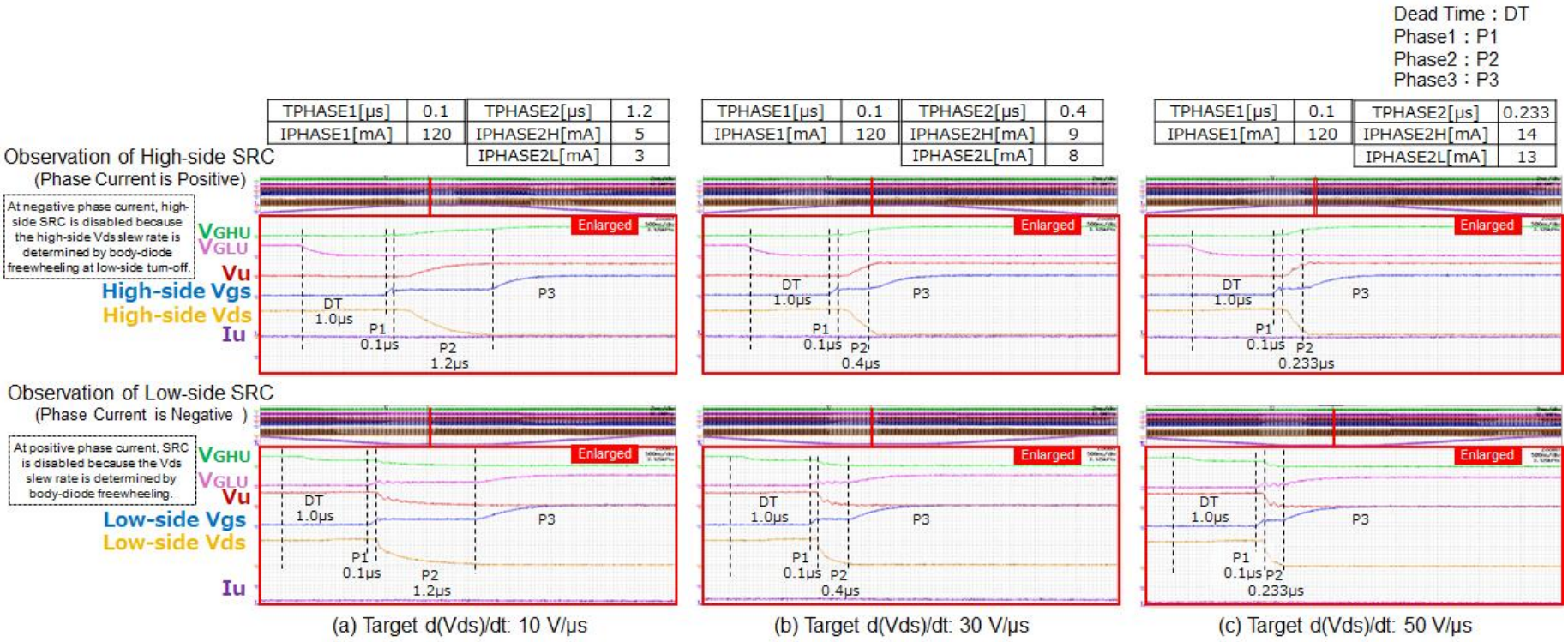

Figure 4.4 Parameter Adjustment Example for a Low-Qg MOSFET

Notes on Contents

1. **Block Diagrams**
   Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. **Equivalent Circuits**
   The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

IC Usage Considerations

Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.
Exceeding the Absolute Maximum Ratings may cause destruction, damage, or degradation of the device, and may result in injury due to rupture or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure.
The IC may be destroyed due to operation beyond the Absolute Maximum Ratings, incorrect wiring, or abnormal pulse noise induced from wiring or loads. As a result, a large current may continue to flow through the IC, potentially leading to smoke generation or fire. Therefore, it is necessary to properly design protective measures, including fuse rating, blowing time, and circuit insertion location, assuming the possibility of large current inflow or outflow caused by IC failure, in order to minimize the impact of such failures.

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Points to Remember on Handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the operating conditions and application, the overcurrent protection circuit may not operate correctly, or the IC may be damaged before the overcurrent protection circuit becomes active, for example, when the Absolute Maximum Ratings are exceeded.

In addition, if an overcurrent continues to flow for an extended period after the protection circuit has operated, the IC may be damaged due to heat generation or other factors, depending on the operating conditions and application.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. After the protection circuit has operated, promptly eliminate the condition causing excessive heat generation.

When the Absolute Maximum Ratings are exceeded, depending on the operating conditions and application, the thermal shutdown circuit may not operate properly, or the IC may be damaged before the thermal shutdown circuit is activated.

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