TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HCT74AP, TC74HCT74AF

Dual D-Type Flip Flop with Preset and Clear

The TC74HCT74A is a high speed CMOS D FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

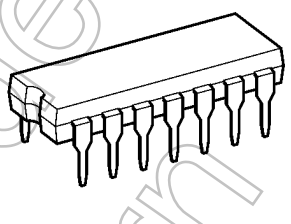
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL , NMOS and CMOS output voltage levels.

The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CLOCK pulse.

$\overline{\text{CLEAR}}$ and $\overline{\text{PRESET}}$ are independent of the CLOCK and are accomplished by setting the applopriate input to an "L" level.

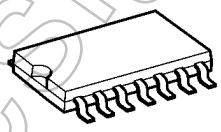
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TC74HCT74AP



DIP14-P-300-2.54

TC74HCT74AF



SOP14-P-300-1.27A

Weight

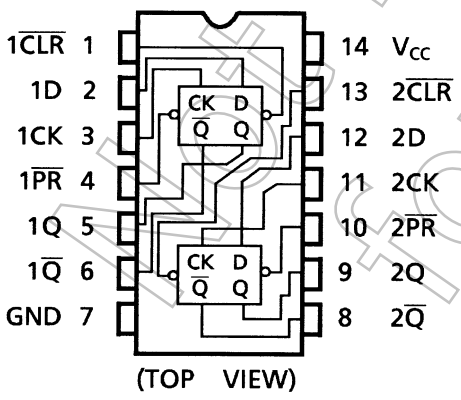
DIP14-P-300-2.54 : 0.96 g (typ.)

SOP14-P-300-1.27A : 0.18 g (typ.)

Features

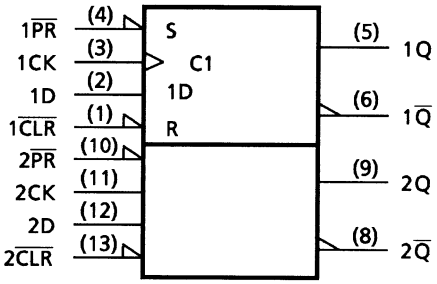
- High speed: f_{max} = 53 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 2 μA (max) at Ta = 25°C
- Compatible with TTL outputs: V_{IH} = 2 V (min)
  V_{IL} = 0.8 V (max)
- Wide interfacing ability: LSTTL, NMOS, CMOS
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 4 mA (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Pin and function compatible with 74LS74

Pin Assignment



Start of commercial production
1988-11

IEC Logic Symbol

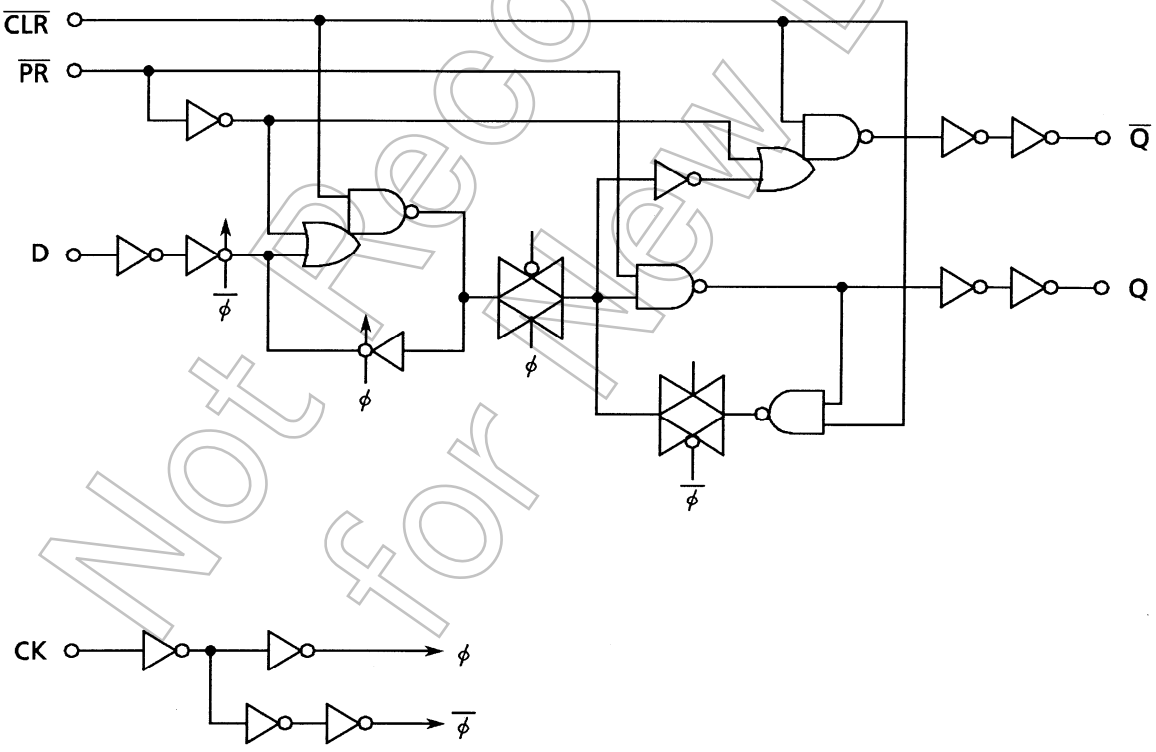


Truth Table

Inputs				Outputs		Function
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q_n	$\overline{Q}_n$	No Change

X: Don't care

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 500	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
High-level input voltage	V_{IH}	—	4.5 to 5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V_{IL}	—	4.5 to 5.5	—	—	0.8	—	0.8	V
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5	4.4	4.5	—	4.4	—	V
		V_{IN} = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5	4.18	4.31	—	4.13	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5	—	0.0	0.1	—	0.1	V
		V_{IN} = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND	5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND	5.5	—	—	2.0	—	20.0	μA
	I_C	Per input: V_{IN} = 0.5 V or 2.4 V Other input: V_{CC} or GND	5.5	—	—	2.0	—	2.9	mA

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = −40 to 85°C	Unit
			V_{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (CK)	$t_{W(L)}$	—	4.5	—	15	19	ns
	$t_{W(H)}$		5.5	—	14	17	
Minimum pulse width ($\overline{CLR}$, $\overline{PR}$)	$t_{W(L)}$	—	4.5	—	15	19	ns
			5.5	—	14	17	
Minimum set-up time	t_s	—	4.5	—	15	19	ns
			5.5	—	14	17	
Minimum hold time	t_h	—	4.5	—	0	0	ns
			5.5	—	0	0	
Minimum removal time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}	—	4.5	—	5	5	ns
			5.5	—	5	5	
Clock frequency	f	—	4.5	—	27	22	MHz
			5.5	—	30	24	

AC Characteristics ($C_L = 15$ pF, $V_{CC} = 5$ V, Ta = 25°C, input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH} t_{THL}	—	—	6	12	ns
Propagation delay time (CK-Q, $\overline{Q}$)	t_{pLH} t_{pHL}	—	—	17	28	ns
Propagation delay time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)	t_{pLH} t_{pHL}	—	—	15	25	ns
Maximum clock frequency	f_{max}	—	29	53	—	MHz

AC Characteristics ($C_L = 50$ pF, input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH} t_{THL}	—	4.5	—	8	15	—	19	ns
			5.5	—	7	13	—	16	
Propagation delay time (CK-Q, $\overline{Q}$)	t_{pLH} t_{pHL}	—	4.5	—	21	33	—	41	ns
			5.5	—	19	30	—	37	
Propagation delay time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)	t_{pLH} t_{pHL}	—	4.5	—	18	30	—	38	ns
			5.5	—	15	27	—	35	
Maximum clock frequency	f_{max}	—	4.5	27	48	—	22	—	MHz
			5.5	30	53	—	24	—	
Input capacitance	C_{IN}	—		—	5	10	—	10	pF
Power dissipation capacitance	C_{PD}	(Note)		—	32	—	—	—	pF

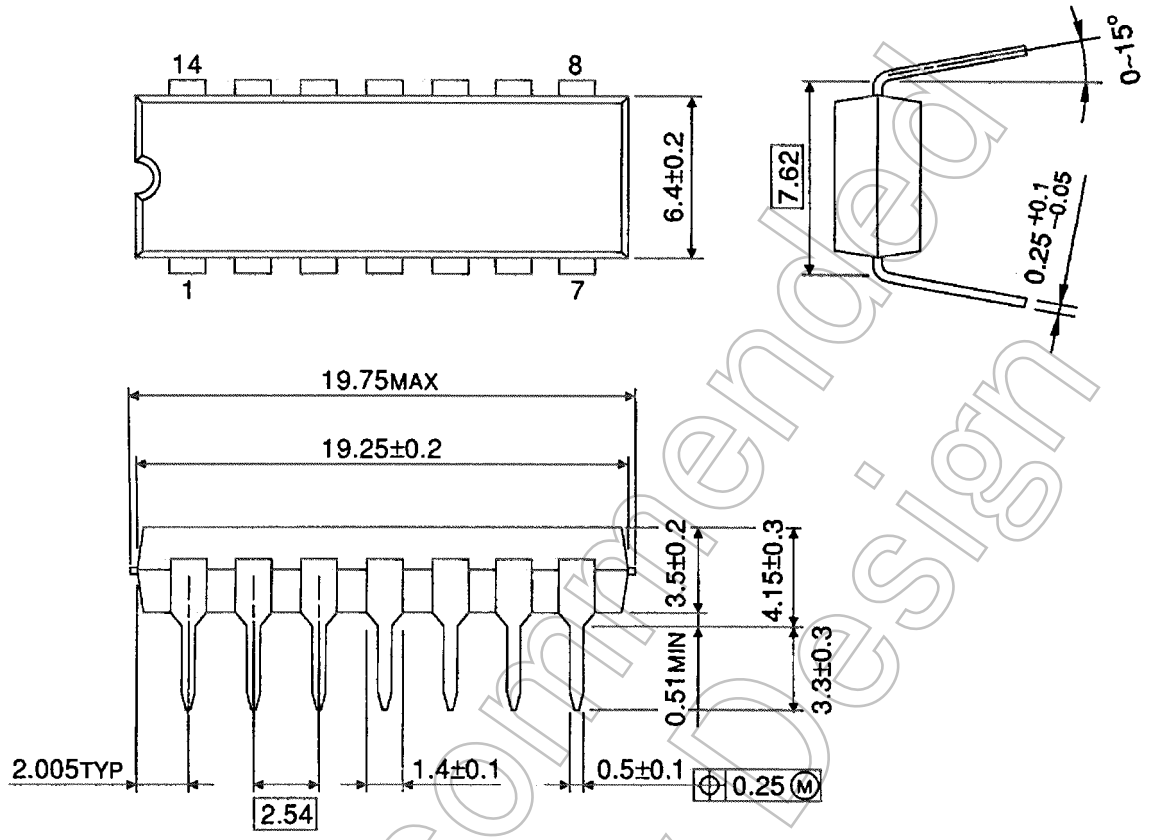
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

I_{CC} (opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per F/F)

Package Dimensions

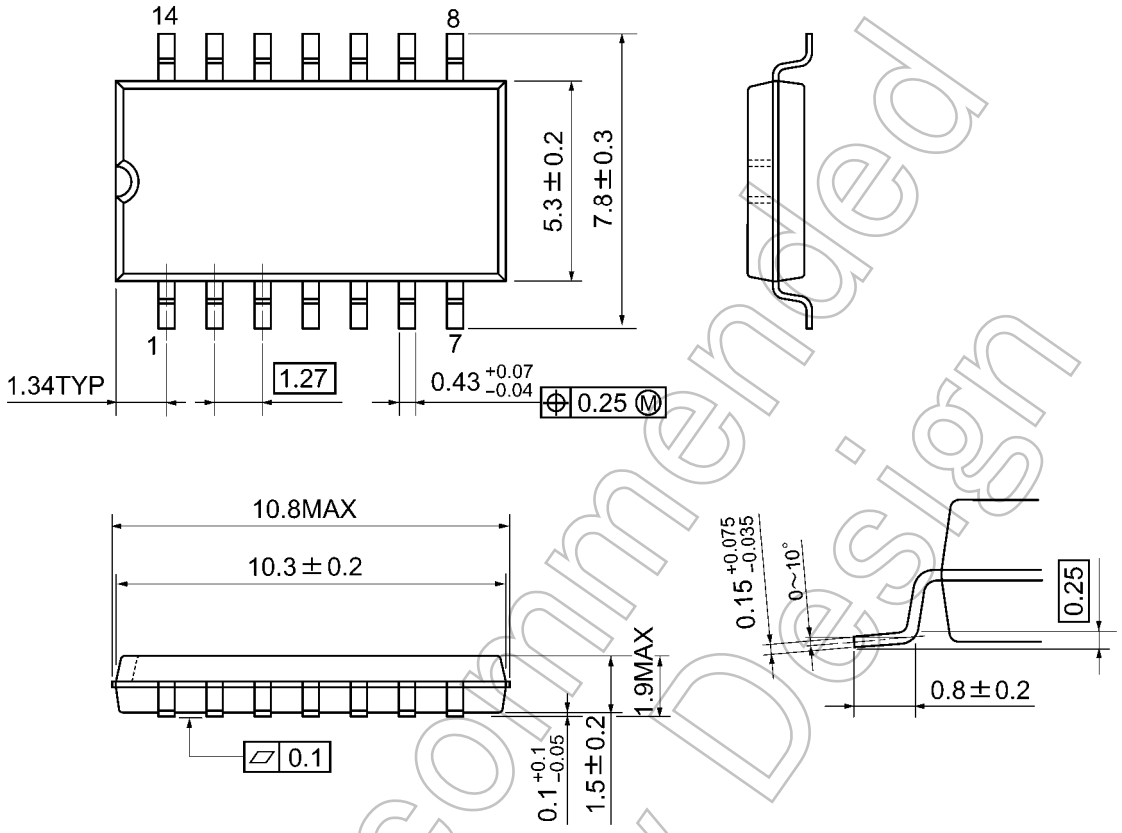
DIP14-P-300-2.54 Unit : mm



Weight: 0.96 g (typ.)

Package Dimensions

SOP14-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

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