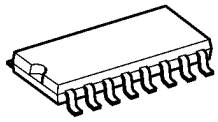
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHC174F, TC74VHC174FK

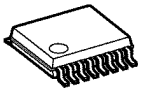
Hex D-Type Flip Flop with Clear

TC74VHC174F



SOP16-P-300-1.27A

TC74VHC174FK



VSSOP16-P-0030-0.50

Weight
SOP16-P-300-1.27A : 0.18 g (typ.)
VSSOP16-P-0030-0.50 : 0.02 g (typ.)

The TC74VHC174 is an advanced high speed CMOS HEX D-TYPE FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Information signals applied to D inputs are transferred to the Q output on the positive going edge of the clock pulse.

When the $\overline{CLR}$ input is held low, the Q output are in the low logic level independent of the other inputs.

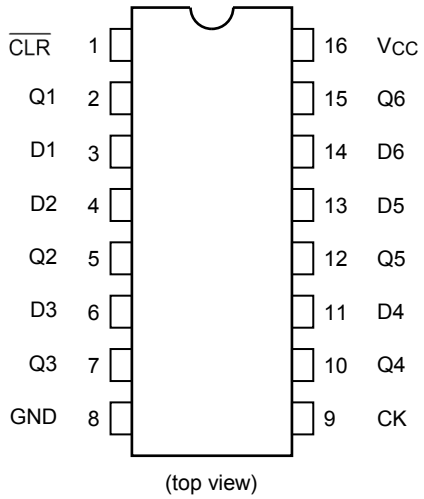
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High speed: f_{max} = 175 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: $V_{CC\ (opr)}$ = 2 to 5.5 V
- Low noise: V_{OLP} = 0.8 V (max)
- Pin and function compatible with 74ALS174

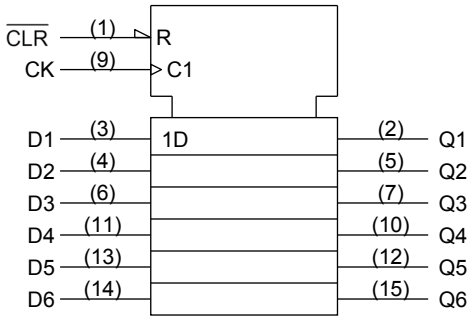
Start of commercial production
1991-11

Pin Assignment



(top view)

IEC Logic Symbol

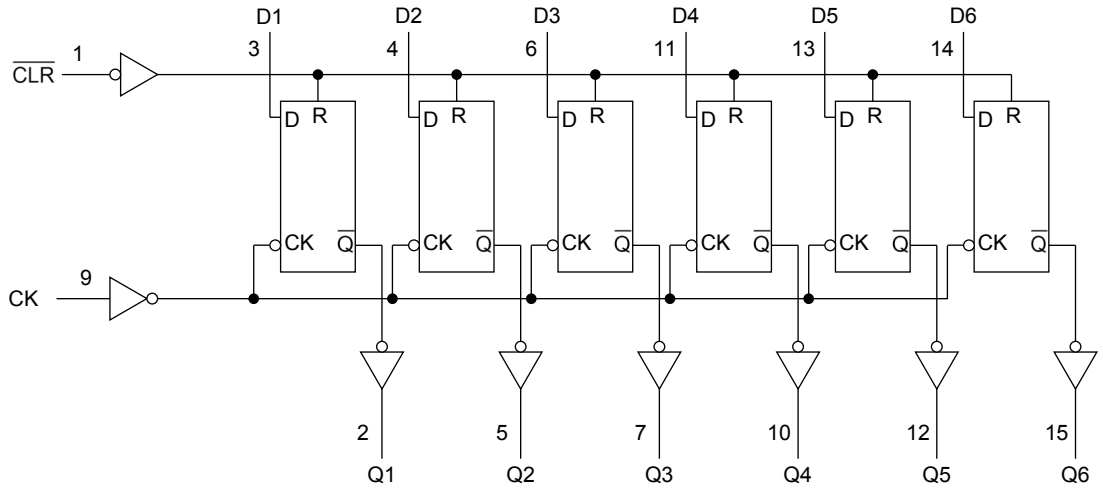


Truth Table

Inputs			Output	Function
$\overline{CLR}$	D	CK	Q	
L	X	X	L	Clear
H	L	↑	L	—
H	H	↑	H	—
H	X	↓	Qn	No Change

X: Don't care

System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to 7.0	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	−20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 (V_{CC} = 3.3 ± 0.3 V) 0 to 20 (V_{CC} = 5 ± 0.5 V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—		2.0 3.0 to 5.5	1.50 V_{CC} × 0.7	— —	— —	1.50 V_{CC} × 0.7	— —	V
Low-level input voltage	V_{IL}	—		2.0 3.0 to 5.5	— —	— —	0.50 V_{CC} × 0.3	— —	0.50 V_{CC} × 0.3	V
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I_{OH} = −4 mA I_{OH} = −8 mA	3.0 4.5	2.58 3.94	— —	— —	2.48 3.80	— —	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 8 mA	3.0 4.5	— —	— —	0.36 0.36	— —	0.44 0.44	
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	μA

Timing Requirements (input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C Typ.	Ta = 25°C Limit	Ta = −40 to 85°C Limit	Unit
Minimum pulse width (CK)	$t_{w\,(L)}$ $t_{w\,(H)}$	—	3.3 ± 0.3 5.0 ± 0.5	— —	5.0 5.0	5.0 5.0	ns
Minimum pulse width ($\overline{CLR}$)	$t_{w\,(L)}$	—	3.3 ± 0.3 5.0 ± 0.5	— —	5.0 5.0	5.0 5.0	ns
Minimum set-up time	t_s	—	3.3 ± 0.3 5.0 ± 0.5	— —	5.0 4.5	6.0 4.5	ns
Minimum hold time	t_h	—	3.3 ± 0.3 5.0 ± 0.5	— —	0.0 0.5	0.0 0.5	ns
Minimum removal time ($\overline{CLR}$)	t_{rem}	—	3.3 ± 0.3 5.0 ± 0.5	— —	3.0 2.5	3.0 2.5	ns

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	7.2	11.0	1.0	13.0	ns
				50	—	9.7	14.5	1.0	16.5	
			5.0 ± 0.5	15	—	4.9	7.2	1.0	8.5	
				50	—	6.4	9.2	1.0	10.5	
Propagation delay time ($\overline{CLR}$ -Q)	t_{pHL}	—	3.3 ± 0.3	15	—	7.4	11.4	1.0	13.5	ns
				50	—	9.9	14.9	1.0	17.0	
			5.0 ± 0.5	15	—	5.1	7.6	1.0	9.0	
				50	—	6.6	9.6	1.0	11.0	
Maximum clock frequency	f_{max}	—	3.3 ± 0.3	15	95	150	—	80	—	MHz
				50	55	85	—	50	—	
			5.0 ± 0.5	15	130	175	—	110	—	
				50	90	120	—	80	—	
Output to output skew	t_{osLH} t_{osHL}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns
			5.5 ± 0.5	50	—	—	1.0	—	1.0	
Input capacitance	C_{IN}	—			—	4	10	—	10	pF
Power dissipation capacitance	C_{PD}	(Note 2)			—	29	—	—	—	pF

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|,\ t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per F/F)}$$

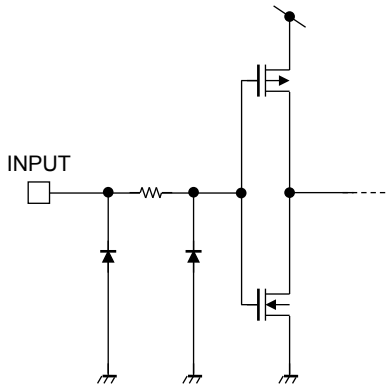
And the total C_{PD} when n pcs. of flip flop operate can be gained by the following equation:

$$C_{PD}\ (\text{total}) = 19 + 10 \cdot n$$

Noise Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Unit
			V_{CC} (V)	Typ.	Max	
Quiet output maximum dynamic V_{OL}	V_{OLP}	C_L = 50 pF	5.0	0.4	0.8	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	C_L = 50 pF	5.0	−0.4	−0.8	V
Minimum high level dynamic input voltage	V_{IHD}	C_L = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage	V_{ILD}	C_L = 50 pF	5.0	—	1.5	V

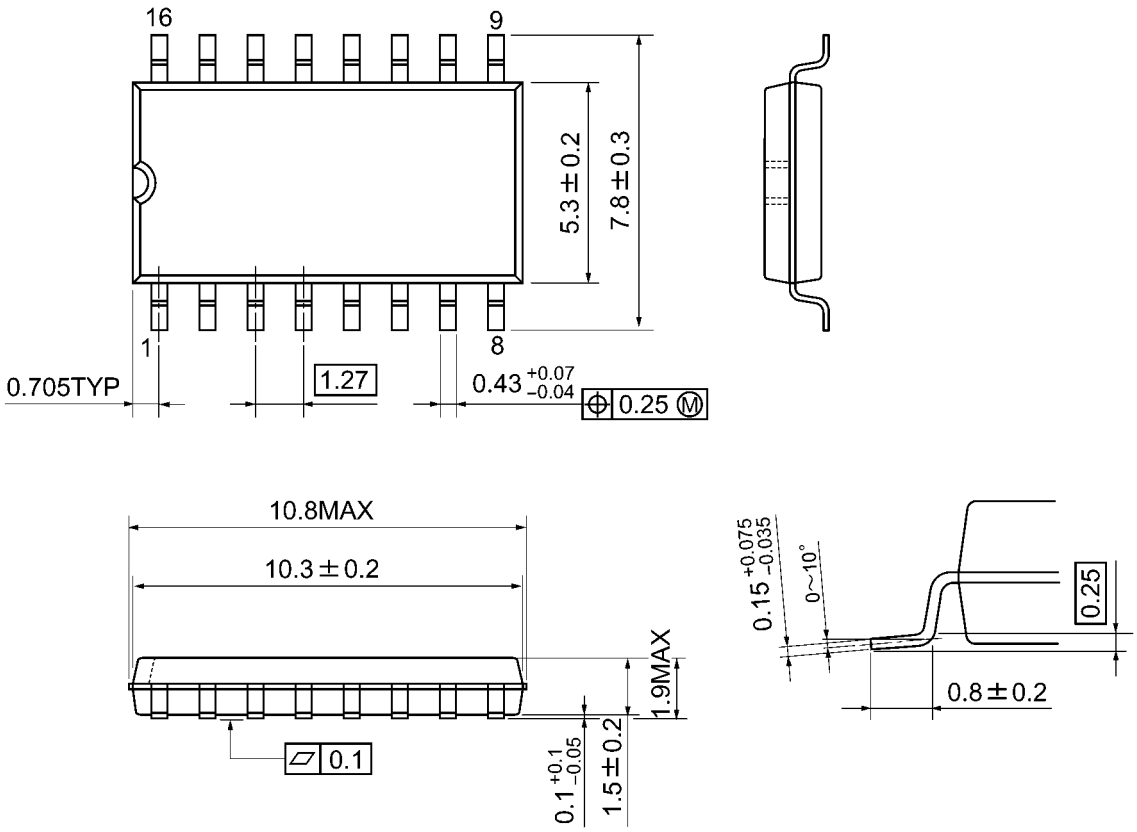
Input Equivalent Circuit



Package Dimensions

SOP16-P-300-1.27A

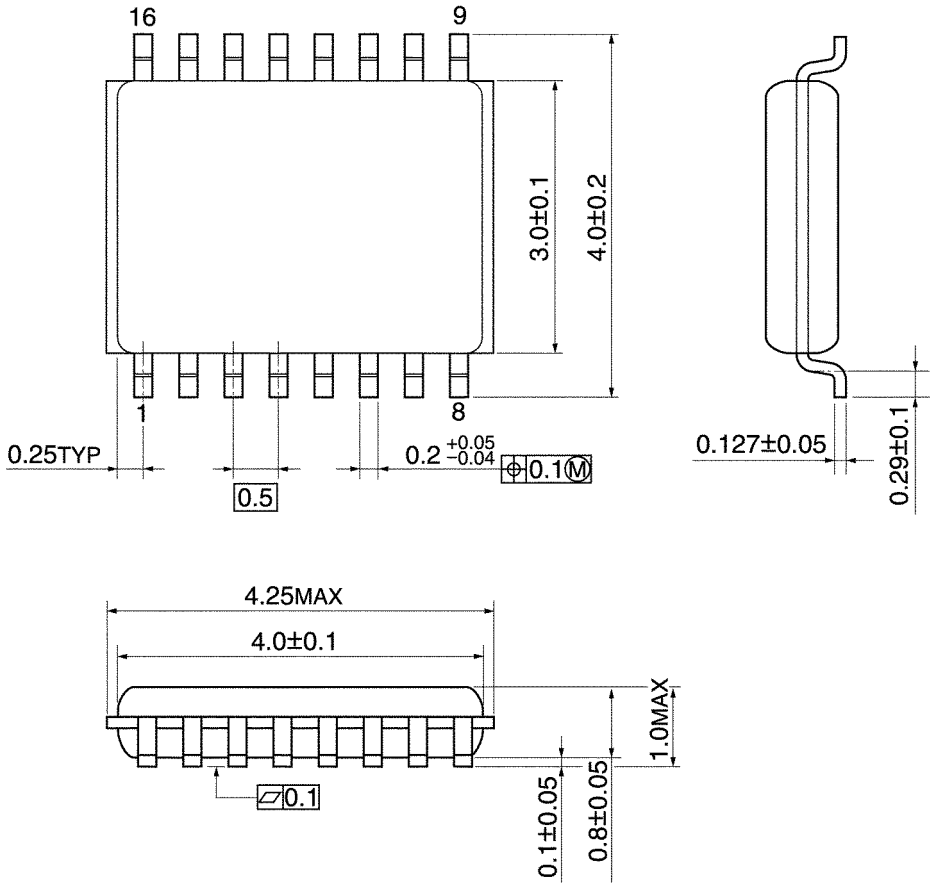
Unit: mm



Weight: 0.18 g (typ.)

Package Dimensions

VSSOP16-P-0030-0.50 Unit: mm



Weight: 0.02 g (typ.)

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