

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHCT574AF, TC74VHCT574AFK

Octal D-Type Flip-Flop with 3-State Output

The TC74VHCT574A is an advanced high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This 8-bit D-type flip-flop is controlled by a clock input (CK) and an output enable input (\overline{OE}).

When the \overline{OE} input is high, the eight outputs are in a high impedance state.

The input voltage are compatible with TTL output voltage.

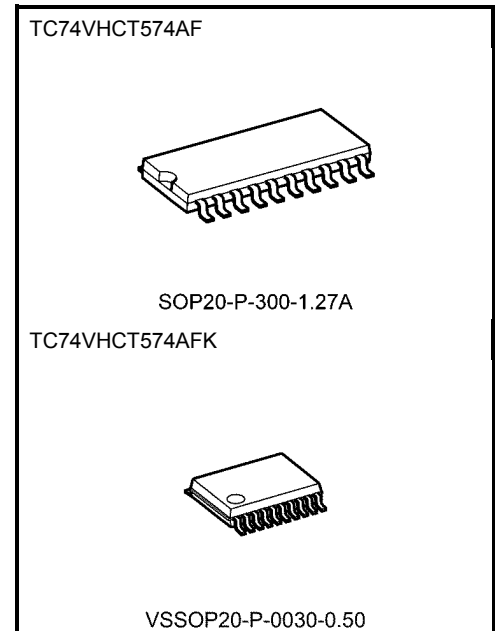
This device may be used as a level converter for interfacing 3.3 V to 5 V system.

Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output (Note) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.

Note: Output in off-state

Features

- High speed: $f_{max} = 140$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 4$ μ A (max) at $T_a = 25^\circ\text{C}$
- Compatible with TTL inputs: $V_{IL} = 0.8$ V (max)
 $V_{IH} = 2.0$ V (min)
- Power down protection is provided on all inputs and outputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Low noise: $V_{OLP} = 1.5$ V (max)
- Pin and function compatible with the 74 series (74AC/HC/F/ALS/LS etc.) 574 type.

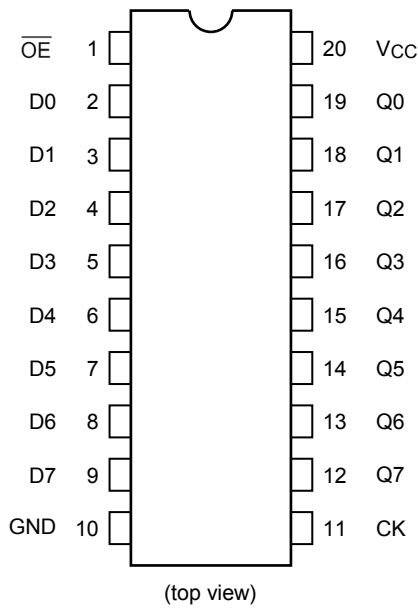


Weight

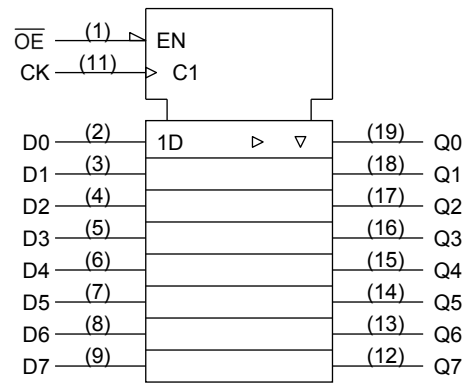
SOP20-P-300-1.27A:	0.22 g (typ.)
VSSOP20-P-0030-0.50:	0.03 g (typ.)

Start of commercial production
1995-12

Pin Assignment



IEC Logic Symbol



Truth Table

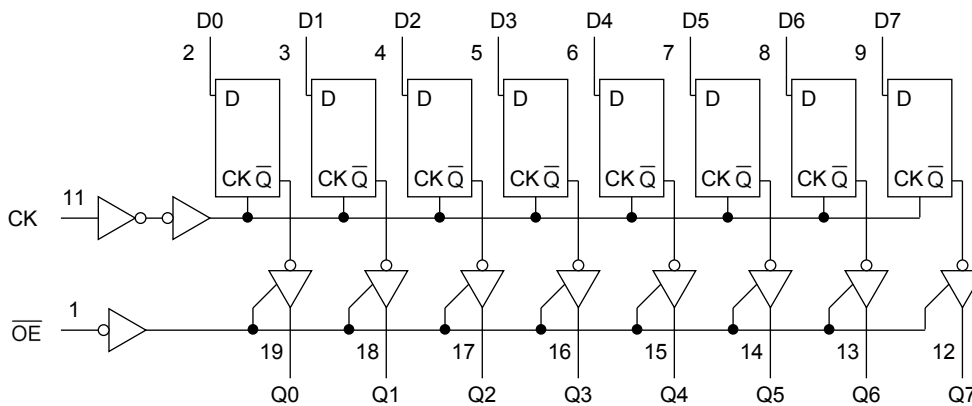
Inputs			Output
\overline{OE}	CK	D	
H	X	X	Z
L	\downarrow	X	Q_n
L	\uparrow	L	L
L	\uparrow	H	H

X: Don't care

Z: High impedance

Q_n : No change

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	-0.5 to 7.0	V
DC input voltage	V _{IN}	-0.5 to 7.0	V
DC output voltage	V _{OUT}	-0.5 to 7.0 (Note 2)	V
		-0.5 to V _{CC} + 0.5 (Note 3)	
Input diode current	I _{IK}	-20	mA
Output diode current	I _{OK}	±20 (Note 4)	mA
DC output current	I _{OUT}	±25	mA
DC V _{CC} /ground current	I _{CC}	±75	mA
Power dissipation	P _D	180	mW
Storage temperature	T _{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Output in off-state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: V_{OUT} < GND, V_{OUT} > V_{CC}

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	4.5 to 5.5	V
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to 5.5 (Note 2)	V
		0 to V _{CC} (Note 3)	
Operating temperature	T _{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 20	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Note 2: V_{CC} = 0 V

Note 3: High or low state

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				VCC (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V _{IH}	—		4.5 to 5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V _{IL}	—		4.5 to 5.5	—	—	0.8	—	0.8	V
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	4.5	4.40	4.50	—	4.40	—	V
			I _{OH} = -8 mA	4.5	3.94	—	—	3.80	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	4.5	—	0.0	0.10	—	0.10	V
			I _{OL} = 8 mA	4.5	—	—	0.36	—	0.44	
3-state output off-state current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	—	—	±0.25	—	±2.50	μA
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	4.0	—	40.0	μA
	I _{CCCT}	Per input: V _{IN} = 3.4 V Other input: V _{CC} or GND		5.5	—	—	1.35	—	1.50	mA
Output leakage current (Power-OFF)	I _{OPD}	V _{OUT} = 5.5 V		0	—	—	+0.5	—	+5.0	μA

Timing Requirements (input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C	Unit	
				VCC (V)	Typ.	Limit		Limit
Minimum pulse width (CK)	t _w (H)	—		5.0 ± 0.5	—	6.5	8.5	ns
	t _w (L)							
Minimum set-up time	t _s	—		5.0 ± 0.5	—	2.5	2.5	ns
Minimum hold time	t _h	—		5.0 ± 0.5	—	2.5	2.5	ns

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
		VCC (V)	CL (pF)	Min	Typ.	Max	Min	Max		
Propagation delay time (CK-Q)	t_{pLH}	—	5.0 ± 0.5	15	—	4.1	9.4	1.0	10.5	ns
	t_{pHL}			50	—	5.6	10.4	1.0	11.5	
3-state output enable time	t_{pZL}	RL = 1 kΩ	5.0 ± 0.5	15	—	6.5	10.2	1.0	11.5	ns
	t_{pZH}			50	—	7.3	11.2	1.0	12.5	
3-state output disable time	t_{pLZ} t_{pHZ}	RL = 1 kΩ	5.0 ± 0.5	50	—	7.0	11.2	1.0	12.0	ns
Maximum clock frequency	f_{max}	—	5.0 ± 0.5	15	90	140	—	80	—	MHz
				50	85	130	—	75	—	
Output to output skew	t_{osLH} t_{osHL}	(Note 1)	5.0 ± 0.5	50	—	—	1.0	—	1.0	ns
Input capacitance	CIN	—		—	4	10	—	10	pF	
Output capacitance	COUT	—		—	9	—	—	—	pF	
Power dissipation capacitance	CPD	(Note 2)		—	25	—	—	—	pF	

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = CPD \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per F/F)}$$

And the total CPD when n pcs. of latch operate can be gained by the following equation:

$$CPD \text{ (total)} = 14 + 11 \cdot n$$

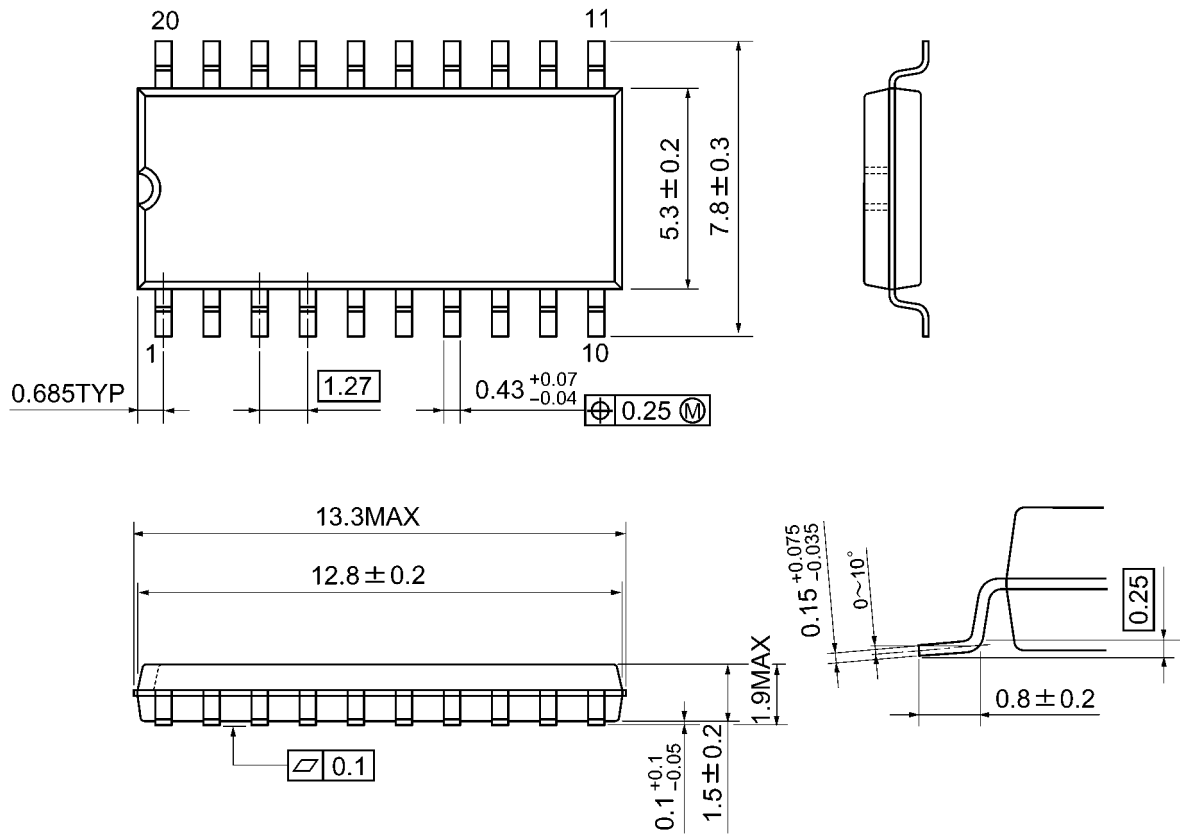
Noise Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			VCC (V)	Typ.	Limit	
Quiet output maximum dynamic VOL	VOLP	CL = 50 pF	5.0	1.1	1.5	V
Quiet output minimum dynamic VOL	VOLV	CL = 50 pF	5.0	-1.1	-1.5	V
Minimum high level dynamic input voltage	VIHD	CL = 50 pF	5.0	—	2.0	V
Maximum low level dynamic input voltage	VILD	CL = 50 pF	5.0	—	0.8	V

Package Dimensions

SOP20-P-300-1.27A

Unit: mm

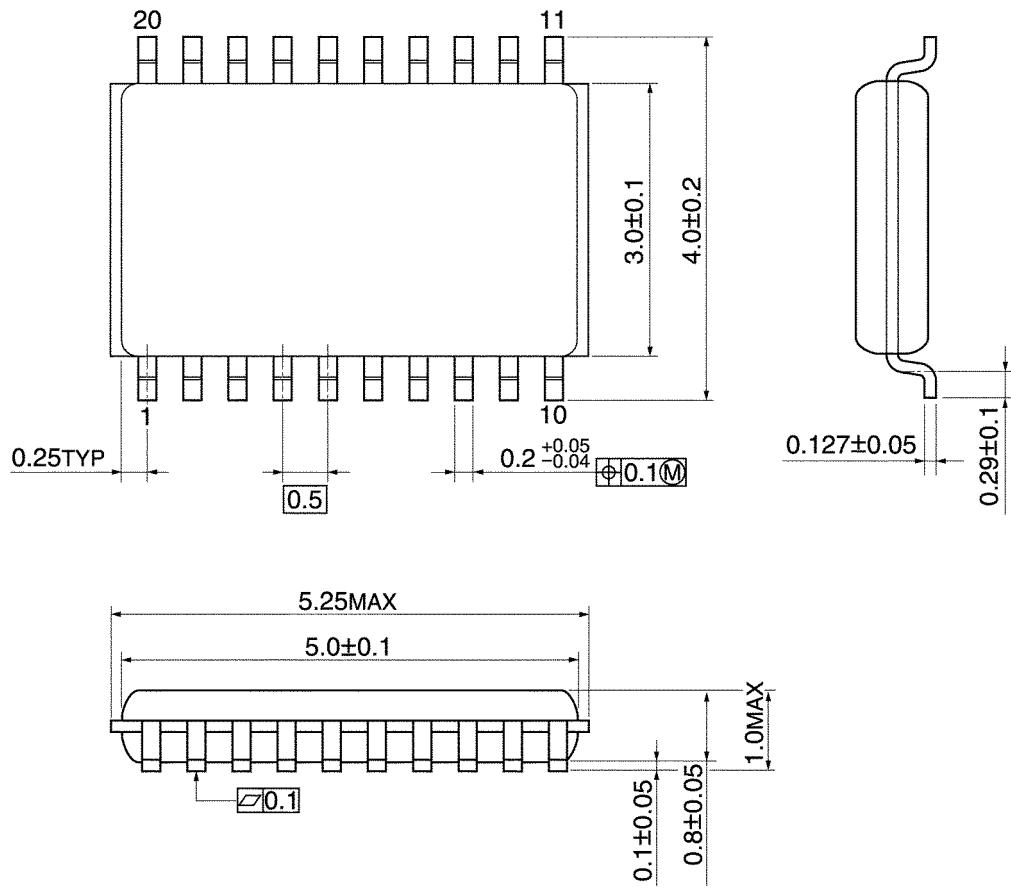


Weight: 0.22 g (typ.)

Package Dimensions

VSSOP20-P-0030-0.50

Unit: mm



Weight: 0.03 g (typ.)

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